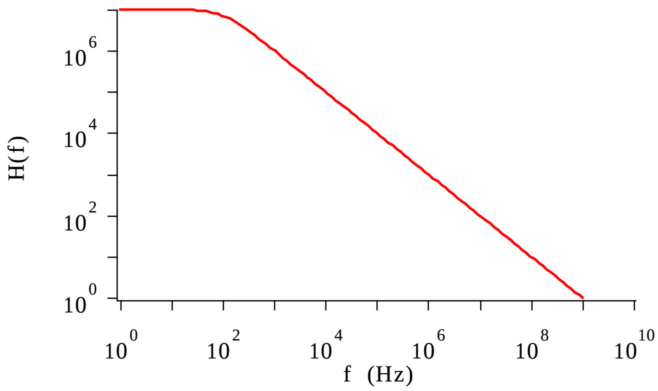
Instrumentation Problem Sheet 4 Answers

(1) The amplifier behaves like a low pass filter with a DC gain of 10^7. So the transfer function at high frequencies can be written

$$G(\omega) = 10^7/(1 + \omega^2\tau^2)^{1/2} \approx 10^7/\omega\tau$$



The pole at f = 100Hz gives τ = 200π rad/s so $G(\omega) = 1$ at 10^9 Hz, which is the Gain-Bandwidth product, GBW.

This is also easily solved graphically, as shown in the figure.

(2) Draw a Bode plot similar to the one for the previous problem. It should intersect the frequency axis at 10^7Hz, since the high frequency behaviour is

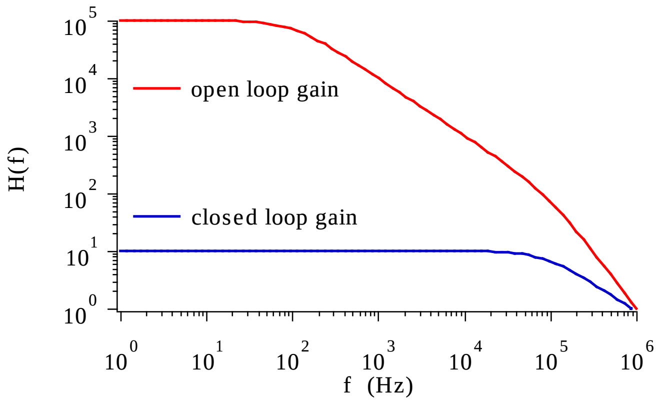
$$G(f) = G(0)f_0/f \quad \text{where } f_0 = 100 \text{ Hz}$$

Now add the second pole at 100kHz. The gain here is 10^2 or 40dB. From this point, the gain drops as

$$G(f) = G(0)f_0f_1/f^2 \quad \text{where } f_1 = 100\text{kHz}$$

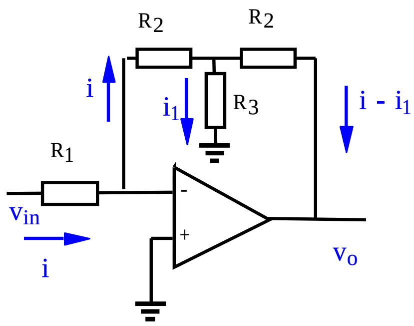
So the GBW is 1MHz, where the phase shift will be 180°, and we don't want oscillations by causing positive feedback by introducing more phase shift at lower frequencies.
To ensure stability the gain of the circuit should reduce to 1 at, or before, the unity gain frequency. This can be achieved with a capacitor which gives a closed circuit gain of

$$G_{closed} = 1 + Z/R_1 = 1 + [R_2/R_1(1 + j\omega\tau)] \text{ with } \tau = R_2C$$



ie the gain resistor R_2 is effectively shorted out at high frequency, killing the gain. The form is just like the low pass filter as we expect. A capacitor of about 20pF would safely do this without reducing the gain too much at lower frequencies.

It's worth noting that this is the sort of calculation one should be making suitable approximations, eg a quick sketch of the Bode plot should be enough to estimate the capacitor value. One could even guess (but not wildly!) a trial value and reach the final choice by a putting numbers in for a few values. I made some approximations. The closed loop gain is $G_{closed} = G_{open}/(1+G_{open}.\alpha) = (1/G_{open}+\alpha)^{-1} \approx 1/\alpha$ for $G_{open} \gg 1$, where $\alpha = R_1/(R_1+Z)$.



(3) To solve this you need to put in the currents flowing in the elements of the feedback loop, as shown.

Since $v_+ = v_- = 0$

$-v_0 = iR_2 + (i-i_1)R_2$

and $0 = iR_2 + i_1R_3$

$-v_0 = iR_2[2 + R_2/R_3]$

so $R_{effective} = R_2[2 + R_2/R_3]$ for the feedback loop

or $G = R_{effective}/R_1$

It's one way of making a very large resistor from smaller value components.

(4) $v_- = (v_1 - v_{out})R_f/(R_1+R_f) + v_{out}$ and $v_+ = v_2R_3/(R_2+R_3)$

Since $v_+ = v_-$, with some algebra

$$v_{out} = v_2(R_3/R_1)[(R_1+R_f)/(R_2+R_3)] - v_1(R_f/R_1)$$

If $R_1 = R_2$ and $R_f = R_3$ $\quad v_{out} = (R_f/R_1)(v_2 - v_1)$

Suppose the input signals are $v_1 = u_1 + v_{CM}$ and $v_2 = u_2 + v_{CM}$ where v_{CM} is the common mode, then

$$v_{out} = (R_f/R_1)(u_2 - u_1)$$

ie, amplifying only the differential (normal mode) signal. For the non-matched case, when $u_2 = u_1 = 0$,

$$v_{out} = (v_{CM}/R_1)[R_3(R_1+R_f)/(R_2+R_3) - R_f]$$

To calculate the accuracy rigorously involves a lot of algebra. It should be done like an error calculation since all the resistors are involved. However, sufficient precision is obtained by using the differential gain;

$$x = R_f/R_1$$

and

$$\sigma^2(x) = [\sigma^2(R_f)(\partial x/\partial R_f)^2 + \sigma^2(R_1)(\partial x/\partial R_1)^2]$$

so

$$\sigma^2(x)/x^2 = \sigma^2(R)[(1/R_f)^2 + (1/R_1)^2]$$

The differential gain involves two resistor networks so should be multiplied by √2.

(5) The closed loop response of a current sensitive amplifier is

$$v_{out} = [-A/(A+1)]i_{in}R_f$$

and $v_{in} = [1/(A+1)]i_{in}R_f$ so $Z_{in} = R_f/(A+1) \approx R_f/A$

At high frequencies the closed loop gain rolls off like a low pass filter leading to

$A(\omega) = \omega_h/j\omega$ where ω_h is the GBW (unity gain frequency) (The DC gain is not needed unless the pole frequency is calculated.)

Thus $Z_{in} = \approx j\omega R_f/\omega_h = j\omega L_{eff}$ with $L_{eff} = R_f/\omega_h$

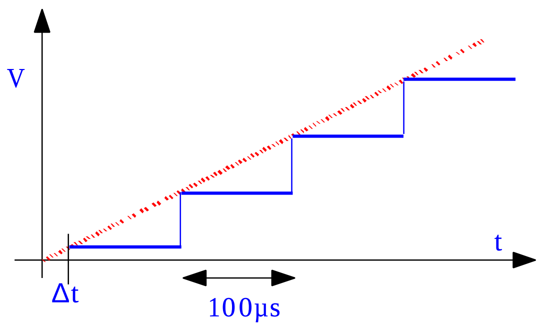
For the values given $L_{eff} = 10^6/(2\pi 10^7) = 1/20\pi$ H $\approx$ 16mH

With a capacitive load at the input, we have an LC circuit, which is a natural resonator at a frequency of $\omega = (LC)^{-1/2}$. In this case, this resonant frequency will be about 126kHz. This could be a problem for some high speed applications, so some care should be taken, perhaps decreasing R_f, or limiting the range of loads.

(6) This is an emitter follower voltage buffer. It is best to start with the DC conditions:
$V_{BE} \approx 0.7V$ so V_{out} = -0.7V is the DC level at the output. Thus the emitter current must be 4.3V/4.3kΩ = 1mA. The dynamic resistance of the base-emitter junction is $r_e = (kT/qI_C) \approx 25\Omega$ at room temperature. This is small compared to R_E. To estimate the input impedance we should know the current gain (β) of the transistor. Without access to a data sheet for the transistor, this is not known, but a reasonable estimate is to assume β ~ 100. In this case the input impedance of the circuit is $\beta(R_E+r_e) \sim 400k\Omega$. Since this is so high, we can see that the exact value of β is not crucial; for a voltage buffer, the input impedance should be large in comparison with the driving output impedance.

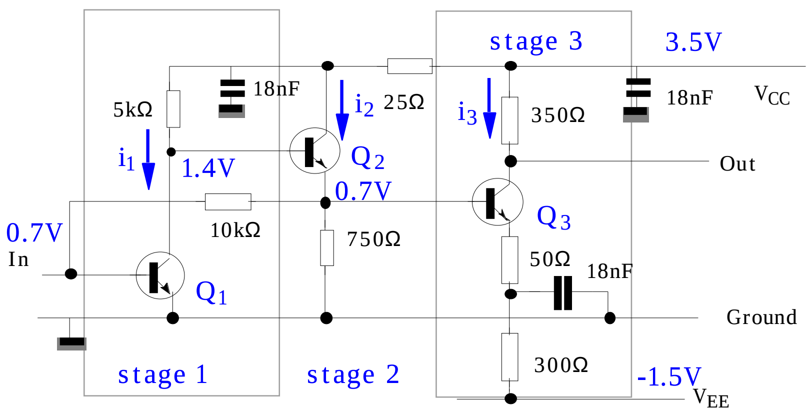
(7) $V_- = V_+$ so $V_- = V_{ref}$
$V_- = V_{out}R_2/(R_1+R_2)$
so $V_{out} = V_{ref}(1+R_1/R_2)$
The output voltage is limited by the transistor. The base voltage must always exceed the emitter voltage by about 0.7V. The base voltage should not rise above the collector voltage, so $V_{max} \approx V_S - 0.7V$.

(8) The sample and hold will convert the linearly rising ramp into a staircase waveform. The ON-resistance of the FET and the capacitor form a low pass filter with a time constant of 0.5μs. This has a 10-90% rise time of 2.2RC = 1.1μs, so the 2μs ON-time gives sufficient time for the output to follow the input, with a delay Δt = 2μs and the leading edge of the steps will have low pass filter shape. To be really accurate the input voltage should be convoluted with the filter.



In practical situations, one should choose R and C to ensure RC << time during which the signal varies significantly so that these effects are minimised.

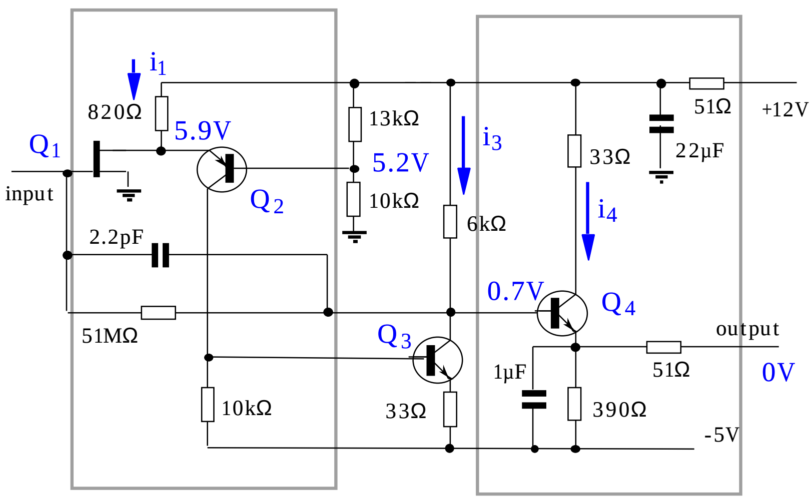
(9) The feedback resistor is 10kΩ, connecting the input to the emitter of Q_2. The voltage gain stages are stages 1 and 3, while stage 2 is a voltage buffer (emitter follower).



To calculate the input impedance we need to calculate the biasing of the different stages:
Stage 1. The base of Q_1 is 0.7V above the emitter, which is at 0V.
Stage 2: In equilibrium conditions, the emitter of Q_2 and base of Q_1 are at the same voltage, ie the feedback resistor carries almost no current, since it is only required to provide a negligible base current to Q_1. The emitter of Q_2 is also at 0.7V.
Stage 1: Thus the collector of Q_1 is at 1.4V, which defines i_1 = (3.5V-1.4V)/5kΩ = 0.4mA. This in turn defines the base-emitter resistance r_e ≈ 25Ω/0.4mA = 60Ω. The voltage gain of the input stage is (R_C/r_e) = 5000/60 = 84 (inverting).
Stage 2: The current in stage 2 is 0.7V/750Ω ≈ 1mA and we can estimate an input impedance of ~75kΩ. The voltage gain = 1.
Stages 1 and 2 provide voltage gain and a driving buffer. Overall, this is a voltage amplifier resembling an op-amp in current sensitive mode. So the input impedance is given by $R_{in} = R_{feedback}$/Open loop gain = 10kΩ/84 ≈ 120Ω.

The odd point about the final stage is that it is another voltage amplifier, rather than a buffer. But what is the gain? The emitter resistance is 50Ω + 300Ω = 350Ω, to be compared with the 350Ω collector resistance, but the 18nF capacitor plays an important role at high frequencies by effectively shorting out the 300Ω. It does not matter that the connection is to the –1.5V line, since to AC signals all DC levels are equivalent. Thus, for the fast pulses for which the amplifier was designed, the gain of this stage is 350/50 = 7. However, the unusual feature is that the gain is provided with modest driving capacity since the output impedance is dominated by the 350Ω collector resistor. The probable reason is that if three stages had been used there would have been a high risk of instability, since three stages with their associated capacitance and phase shifts have good chance of generating positive feedback.
Although the input current is small, typically ~i_1/100 ≈ 4µA, this is significant compared to the DC currents drawn by detectors with which this amplifier may be used. As we'll see later, this makes the amplifier most suitable for processing fast signals, ie with short time constants.

(10) The time constant is defined by the feedback network, which connects the collector of Q_3 to the input. Thus τ = 50MΩx2.2pF ≈ 110µs. The sensitivity is defined by (Q_{in}/C_f) ≈ 0.45V/pC.



The impulse response is simply $v_{out} = -(Q_{in}/C_f)\exp(-t/\tau)$

Typically this amplifier would be followed with a bandpass filter with a much smaller time constant, eg ~ few μs, so the amplitude from the preamplifier will not decay much in this time.

The important difference between this amplifier and the previous one is the presence of the FET, instead of a bipolar transistor, at the input. This means the input current is very small. Since this is a noise source (as we'll see later) this amplifier is suited for low noise measurements with bandpass filter time constants in the several μs range.

The output impedance is defined by the output stage which is an emitter follower and is therefore small. 51Ω is inserted to ensure an approximate 50Ω impedance for coaxial cable matching.

Q_3 is a voltage amplifier stage with a gain of $6000/(33 + r_e)$

Q_1 and Q_2 provide the initial gain, of $g_m(Q_1)$.10kΩ. If g_m is 10mS, then the voltage gain from these two stages is 100.

The base voltage of Q_2 is set by a resistor divider, at 5.2V, so the emitter voltage is approximately 0.7V higher, ie 5.9V. The current shared between Q_1 and Q_2 can now be calculated as (12-5.9)V/0.82kΩ ≈ 7.4mA. This is not enough to allow us to calculate the current in Q_2 but an upper limit can be set by assuming the collector voltage is as high as the base voltage. If so the collector current ≈ 10V/10kΩ ≈ 1mA. As expected, most of the current will flow in Q_1, maximising g_m. The actual current will be set by the characteristics of the input FET.

The current in Q_3 can be calculated as $i_3 = (12 - 0.7)/6\text{k}\Omega \approx 2\text{mA}$, so $r_e \approx 13\Omega$ and we can calculate the gain in Q_3 as 6000/45 ≈ 130. The overall voltage gain of the amplifier is thus approximately 13000 or 82dB.

The final stage draws a current which can be calculated from the emitter biasing, of $i_4 = 5\text{V}/0.39\text{k}\Omega \approx 13\text{mA}$.

The overall power consumption is then

$$P \approx 6.4\text{mA} \times 12\text{V} + (1\text{mA} + 2\text{mA} + 13\text{mA}) \times 17\text{V} = 350\text{mW}.$$

(11) This is best done by considering the Fourier transforms of the responses of the different stages, ie the transfer functions. The charge integrator is an amplifier with a capacitor C_f in the feedback loop, so it has a transfer function $H_1 = 1/j\omega C_f$. The differentiator (high pass filter) has a transfer function $H_2 = j\omega\tau/(1+j\omega\tau)$. Thus the overall response is the product, which is

$$H(\omega) = (\tau/C_f)/(1+j\omega\tau).$$

This is simply the transfer function of a falling exponential, with time constant τ. This should not be a surprise, since the integrator turns the current impulse into a voltage step, so we have calculated the well known step response of a high pass filter.

If we now add another differentiator the filter has a response

$$H(\omega) = (\tau_1\tau_2/C_f)[j\omega/(1+j\omega\tau_1)(1+j\omega\tau_2)]$$

This can most easily be simplified by expressing it as a sum of partial fractions, ie

$$H(\omega) = (\tau_1\tau_2/C_f)[A/(1+j\omega\tau_1)+B/(1+j\omega\tau_2)]$$

with a bit of algebra this becomes

$$H(\omega) = [\tau_1\tau_2/(\tau_2-\tau_1)C_f][1/(1+j\omega\tau_1) - 1/(1+j\omega\tau_2)]$$

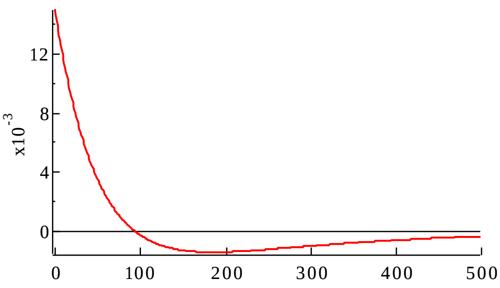
so

$$h(t) = [1/(\tau_2-\tau_1)C_f][\tau_2\exp(-t/\tau_1) - \tau_1\exp(-t/\tau_2)]$$

which has a zero at

$$t_0 = \tau_1\tau_2\ln(\tau_1/\tau_2)/(\tau_1-\tau_2)$$

The plot shows an example using τ_1 = 200 and τ_2 = 50.
This kind of pulse occurs when a charge sensitive amplifier with a long decay time constant is followed by a differentiating filter to shorten the pulse shape. A pole zero cancellation is required to eliminate the baseline undershoot.



Because the high pass filter means the signal has to pass through a capacitor, the area under the baseline is the same as the area above the baseline. It is easy to show that the minimum of the pulse occurs at

$$t = 2t_0 = 2\tau_1\tau_2 \ln(\tau_1/\tau_2)/(\tau_1-\tau_2)$$

The relative amplitude of the undershoot involves some lengthy algebra but in the case where $\tau_1 \gg \tau_2$ it can be approximated to $\tau_1 \exp(-t_0/\tau_2)/(\tau_1-\tau_2)$

(12) The previous problem shows that, without the resistor R_p, the pulse shape at the output is defined by a transfer function which gives an undershoot. The purpose of R_p is to cancel a pole in the transfer function, to restore a pure exponential decay.
The transfer function of the input stage alone is

$$H(\omega) = v_{out}/i_{in} = -Z_f = -R_f/(1+j\omega\tau_f) \quad \text{with } \tau_f = R_fC_f$$

This produces a pulse shape from a delta input with charge Q of

$$h(t) = -(Q/C_f)\exp(-t/\tau_f)$$

When combined with the high pass filter, this becomes

$$H(\omega) = -R_fR/[(1+j\omega\tau_f)(R+Z)] \quad \text{where } Z = R_p/(1+j\omega\tau_p) \text{ with } \tau_p = R_pC$$

Thus

$$H(\omega) = -R_fR(1+j\omega\tau_p)/[(1+j\omega\tau_f)(R+R_p+j\omega R\tau_p)]$$

by choosing $\tau_p = \tau_f$, ie $R_p = R_fC_f/C$, the pole from the first stage is cancelled leaving an overall transfer function of

$$H(\omega) = -R_f[R/(R+R_p)]/(1+j\omega\tau) \quad \text{with } \tau = R_XC$$

R_X is the parallel resistance of R_p and R, ie $R_X = RR_p/(R+R_p)$

so the final pulse shape is

$$h(t) = -(Q/C_f)[R/(R+R_p)]\exp(-t/\tau)$$

(11) From the results of the previous problem, $\tau_f = R_fC_f$ = 10µs so R_p = 45kΩ and R_X = 9.5kΩ. The decay time constant $\tau = R_XC$ = 2.1µs. C_2 defines the integration time of the final stage, and should give the same time constant, so C_2= 20pF.
The output stage has a low output impedance so the 47Ω resistance would ensure the amplifier output is well matched to drive a 50Ω coaxial cable which is frequently used without suffering from reflections.