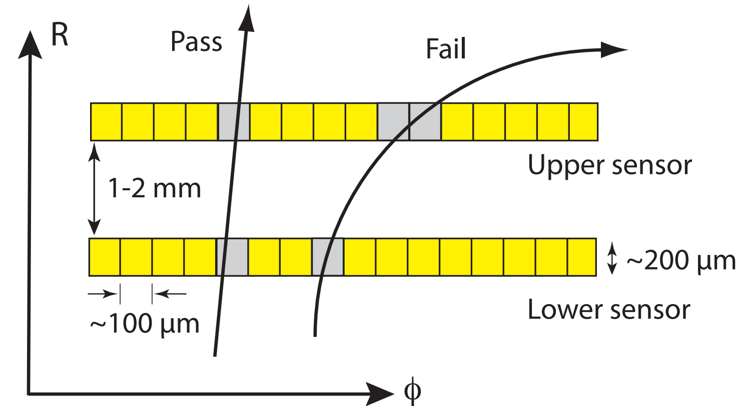
Motives and design of future CMS tracker

- Tracker replacement essential for Run 4 (post-2025)
  - because of radiation damage and high pileup
    - LS3 - 30 months 2023-2025
- Trigger must be substantially upgraded to handle high pileup
  - -> $\mathcal{L}_{inst}$ ~ 5 x 10^{34} $cm^{-2}s^{-1}$ (levelled) => $\langle N_{ev} \rangle$ ~ 140 – 200
- Calorimeter issues
  - isolation of $e/\gamma/\tau$ degraded by pile-up from $\pi^0\gamma$s and hadrons
  - many more jets, which overlap
- Muon system issues
  - increased combinatorial fakes, enhanced by multiple scattering
- To control much higher rate of L1 triggers only significant new data comes from tracker

Silicon tracker with trigger-stub capability

- ~15000 modules transmitting
  - p_T-stubs to L1 trigger @ 40 MHz
  - full hit data to HLT @ 0.5-1 MHz



Outer Tracker

r [mm]

z [mm]

η

0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0 3.2 4.0

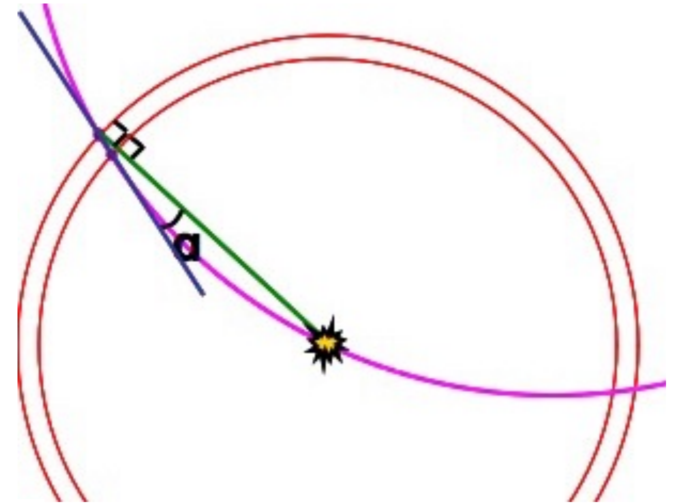
0 200 400 600 800 1000 1200

0 500 1000 1500 2000 2500

Pixel Detector

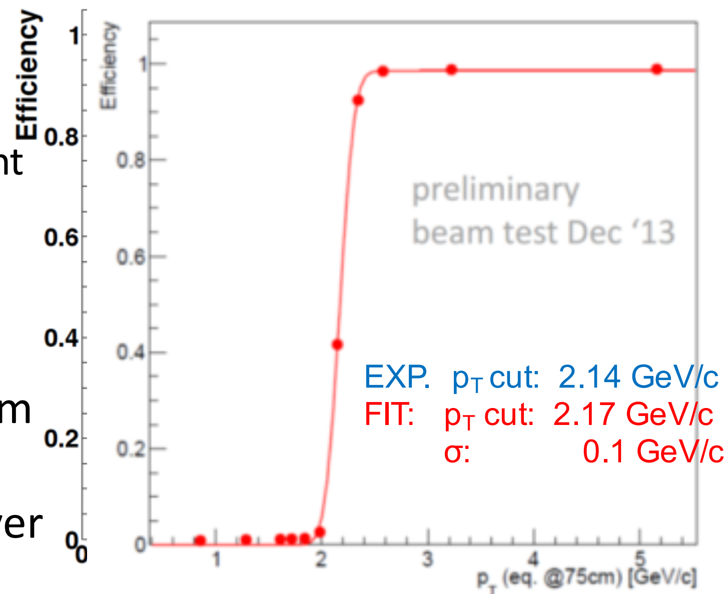
Stacked-tracker principle

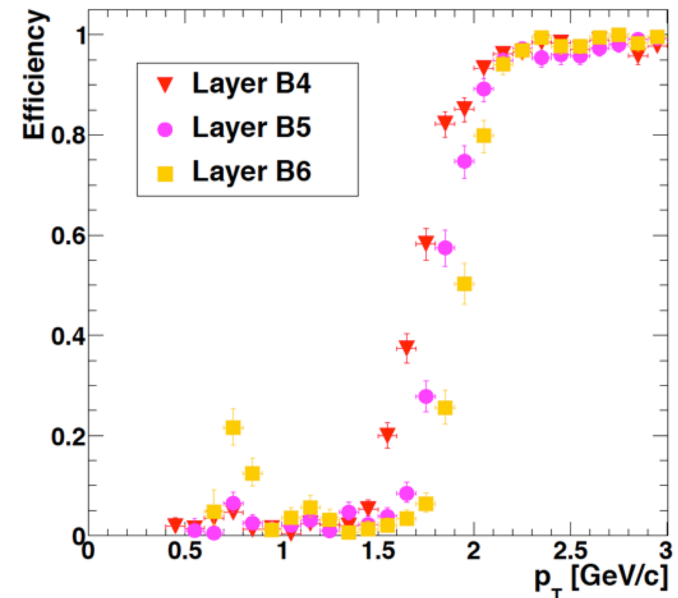
- Compare pattern of hits in contiguous sensor elements in closely spaced layers
  - p_T cut set by angle of track in layer
  - primarily depends on layer separation
    - but increasing separation worsens fake combinations
  - details depend on
    - pitch
    - thickness
    - charge sharing
    - track impact point
    - …



data from 2013 beam test

assumes r=75cm layer

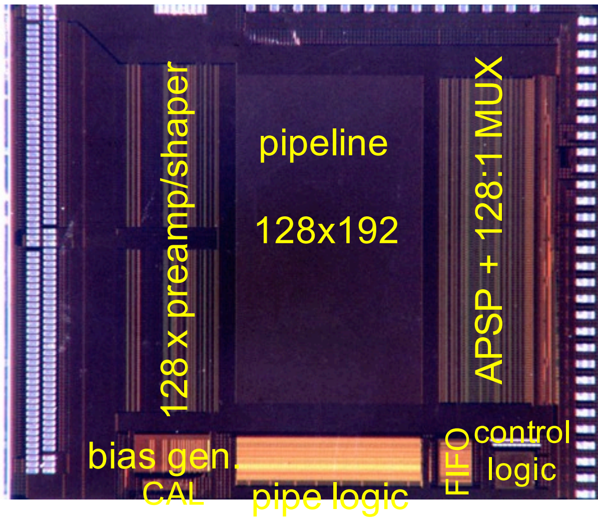




RAL TD-Imperial

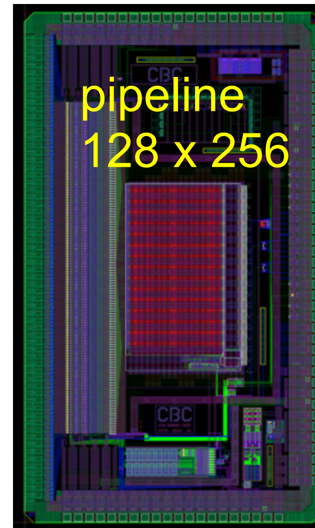
CMS Tracker ASIC evolution

- 1999: APV25 0.25µm
  - 7 mm x 8mm (128 chan)



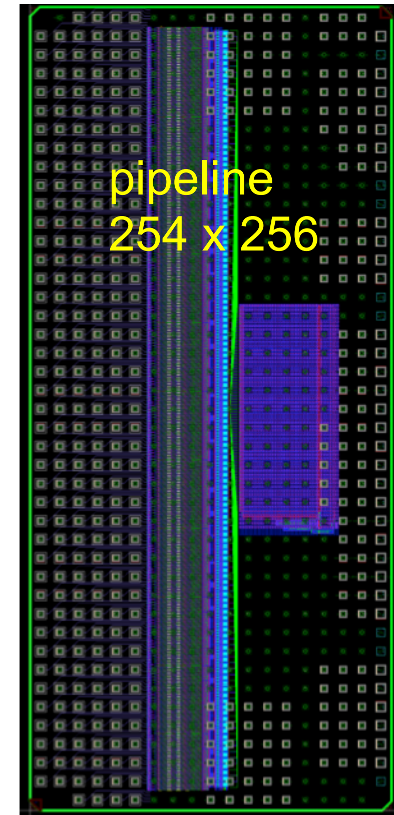
analogue data
~4 µs latency

2011: CBC 0.13µm
7mm x 4mm (128 chan)



binary data,
6.4 µs latency
wire-bondable

2013: CBC2 0.13µm
11mm x 5mm (254 chan)



bump-bondable,
cluster & correlation logic

2015: CBC3 (final – in layout)
up to 12.8 µs latency
(512 bx)

PS and 2S Modules

PS modules: Macro Pixel + Strip

Macro Pixel: 1.5 mm × 100 μm DC coupled
Strip: 2.4 cm × 100 μm AC coupled
Module area: ~5 × 10 cm^2
Power: ~6-8 W

DC/DC converter
10-12V lines: lower current, lower material

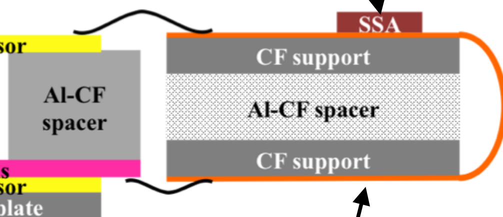
Low-power GigaBit Transceiver
current under development

Concentrator IC (CIC)
FE chip data sparsification

Silicon strip sensor

Short Strip ASIC (SSA)

Macro-Pixel ASIC (MPA)



Flexible hybrid

Silicon pixel sensor

2S modules: Strip + Strip

Strip: 5 cm × 90 μm AC coupled (both sides)
Module area: ~10 × 10 cm^2
Power: ~4-5 W

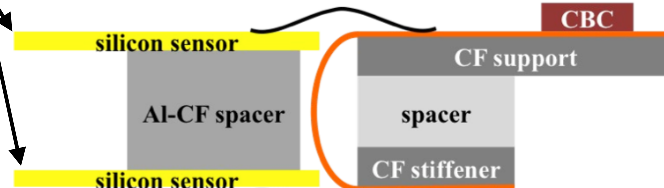
Concentrator IC (CIC)
FE chip data sparsification

DC/DC converter
10-12V lines: lower current, lower material

Low-power GigaBit Transceiver
current under development

CMS Binary Chip (CBC)

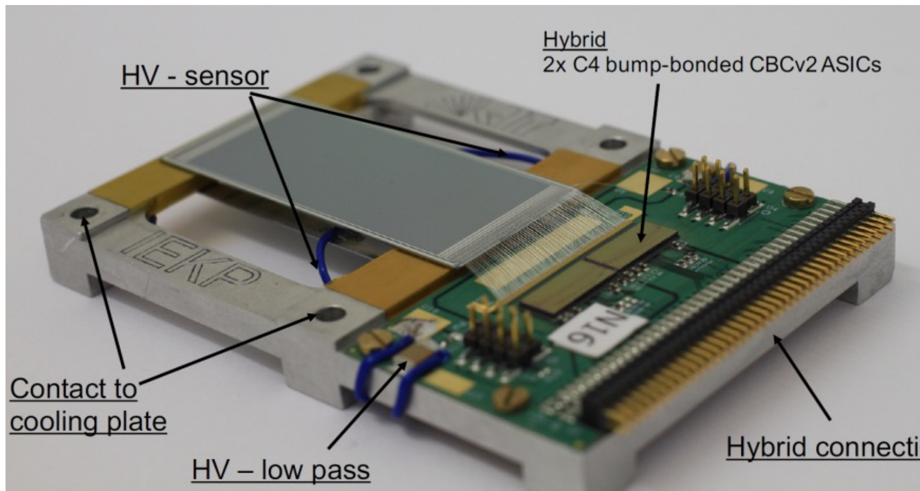
Silicon strip sensors

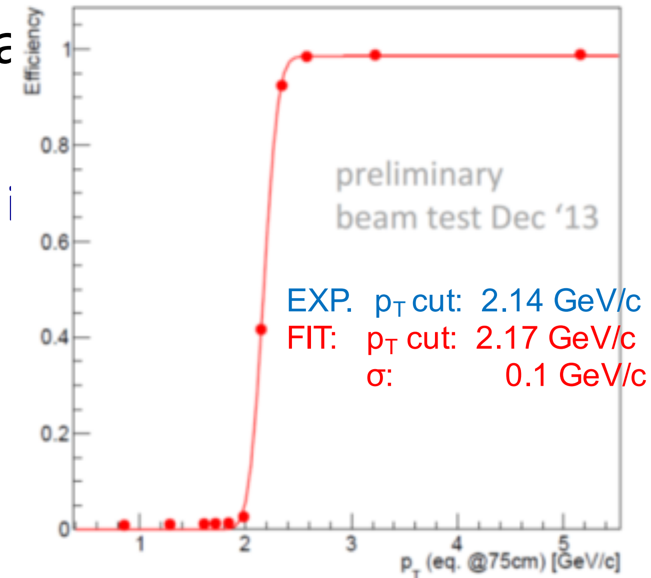


Flexible hybrid

Module status

- 2S-modules furthest advanced – several bea
  - Dec 2013: DESY test beam
  - June 2015: mini-module with irradiated sensors i
  - Nov 2015: first full-size module in H6 test beam





reconstructed p_T cut of r=75cm layer