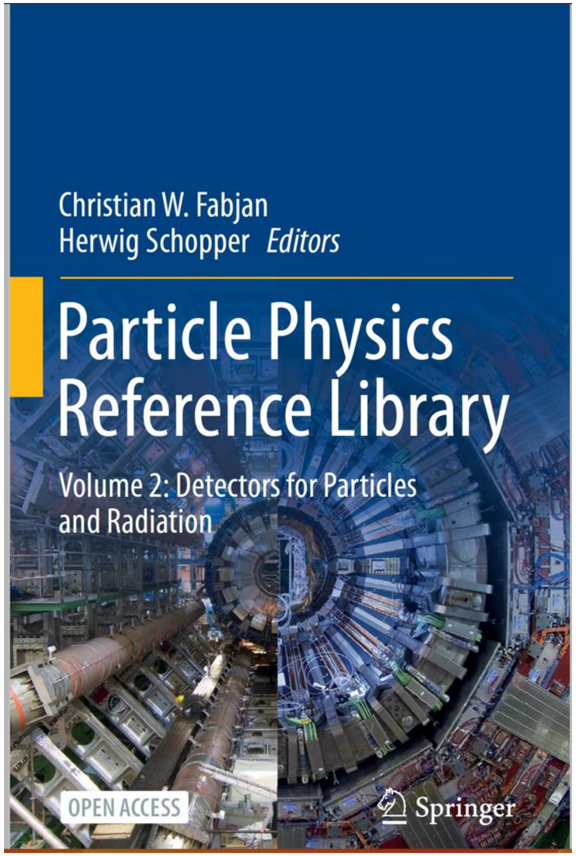
Reference material

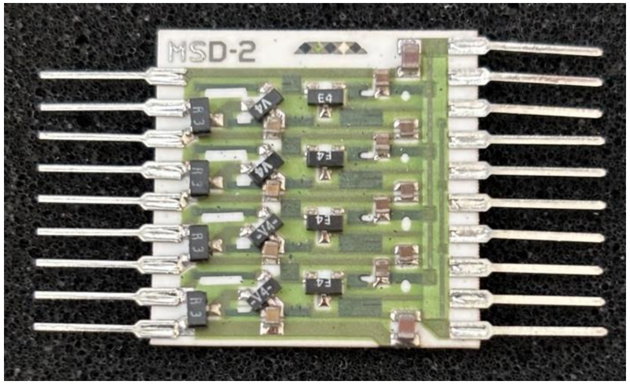
- Strongly recommended open access book https://doi.org/10.1007/978-3-030-35318-6

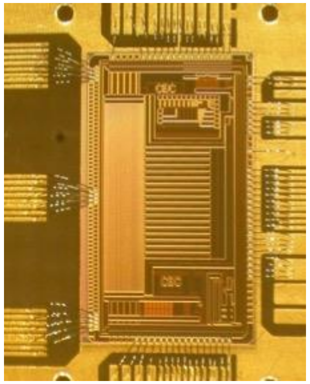


Contents

vii

viii Contents





A brief history of electronics for particle physics

selected from some recent conference talks

Geoff Hall

For more details and references see

“The evolution of particle physics electronics”

JINST_103P_1025 has been published as: 2025_JINST_20_C12006
https://doi.org/10.1088/1748-0221/20/12/C12006

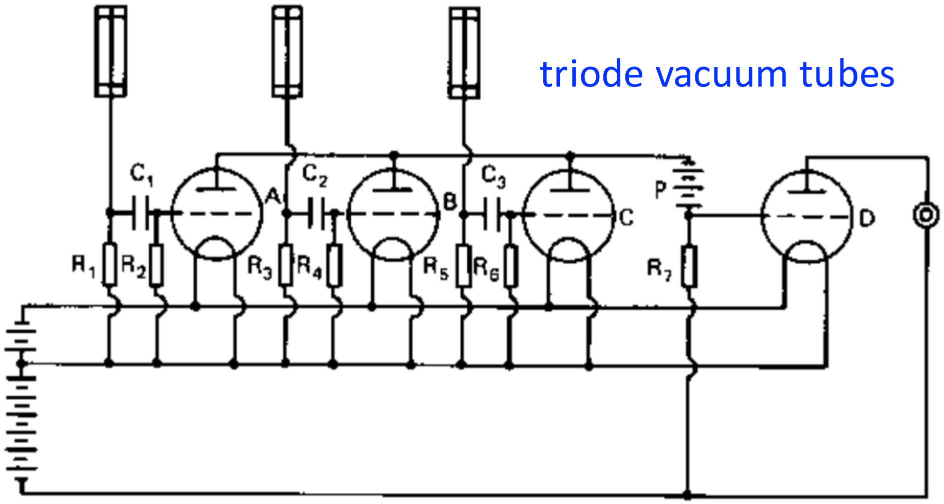
My involvement

- SLAC: triggered rapid-cycling bubble chamber 1975-1982
  - – the charm era, but only our final experiment observed charm ~1981
    - γp –> charm : < 100 events from ~2M triggered photos
    - triggered on tracks using NOVA mini-computer, algorithm in assembler code (2ms)
    - various hardware projects, including Cerenkov counters with PM readout

- NA14’: first UK project to use silicon detectors, started ~1981: γp –> charm
  - – Our first silicon microstrips manufactured by Micron Semiconductor
    - initially very basic design, based on MOS process devised by J Kemmer
  - – UK contribution to NA14’ cancelled before telescope operated!
    - but experiment continued
  - – I became involved with many silicon detector projects, leading to SSC & LHC preparations
    - radiation damage studies, initially of silicon, then FE electronics
  - – CMS since 1992 – in many activities

Pre-CERN

- Bruno Rossi was **the** pioneer
  - coincidence circuit (1930) triggering using Geiger counters and valves
    - Quickly adopted, e.g. Blackett & Occhialini (1932) triggered cloud chamber in a magnetic field to observe the positron (but scooped by Anderson to publish)



triode vacuum tubes

"The consequent variation of the anode current was detected acoustically by a telephone."

Rossi's coincidence circuit, the first fast electronic coincidence circuit of the parallel type, became essential in cosmic-ray research. It allowed the simultaneous registration of electrical pulses from any number of Geiger-Müller counters and had a resolving time of 10 -3 second, an order of magnitude faster than Walther Bothe's

- earlier triggers not electronic

Bothe and Geiger defined a coincidence using electrometers recorded on fast photographic film - when both counters showed a signal within a 1 ms interval

Some subsequent developments

- Electronic counter – Wyn-Williams (1931)
  - to record numbers of events with "mechanical counting meter" (octal)
- Schmitt trigger (1937) - comparator with hysteresis
  - threshold crossing circuit using valves -> 1-bit A-D conversion
- TDC – invented by Rossi (1940) but kept secret during the war years
- ADC – Wilkinson (1949)
  - A stable 99-channel pulse amplitude analyser for slow counting

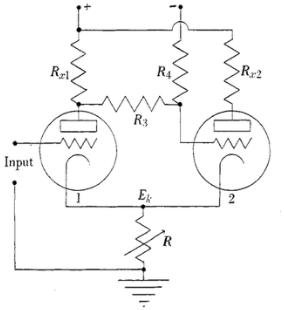
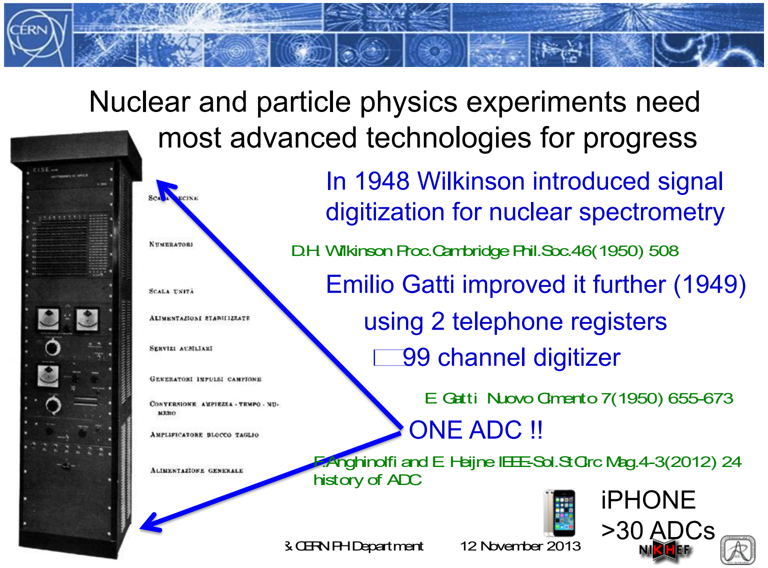


Fig. 1. Thermionic trigger circuit

- All vacuum tube (valve) based
  - shrinkage began…

from E. Heijne EPS Workshop 2013



Nuclear and particle physics experiments need most advanced technologies for progress

In 1948 Wilkinson introduced signal digitization for nuclear spectrometry

D.H Wilkinson Proc.Cambridge Phil.Soc.46(1950) 508

Emilio Gatti improved it further (1949)

using 2 telephone registers

□99 channel digitizer

E Gatti Nuovo Cimento 7(1950) 655-673

ONE ADC !!

F.Anghinolfi and E Heijne IEEE-Sol.St.Circ Mag.4-3(2012) 24 history of ADC

iPHONE
>30 ADCs

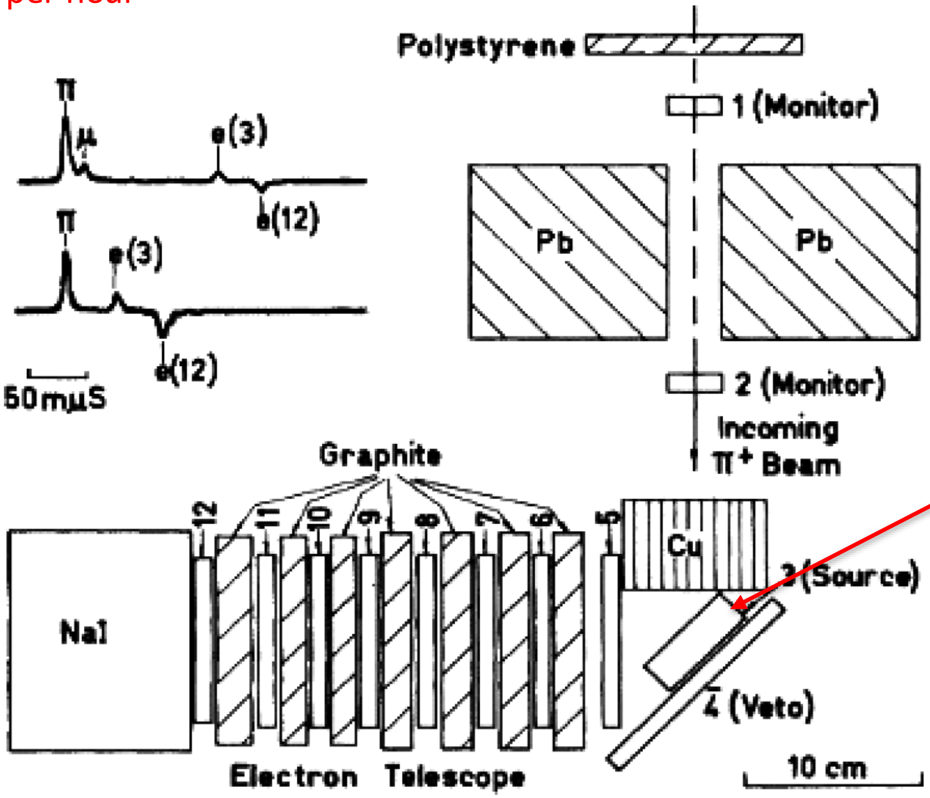
& CERN PH Department 12 November 2013

Early CERN

- Fidecaro et al. Discovery of $\pi \rightarrow e\nu$ decay 1958

events recorded on fast oscilloscope – few per hour – photographically

need to distinguish from $\pi \rightarrow \mu \rightarrow e$



π^+ stopped in active target – plastic scintillator + PM – opened ~150 ns gate for oscilloscope

"positron detection efficiency… Monte Carlo program … at CERN when the first *electronic computer* [my emphasis] (British-made Ferranti-Mercury…) was installed"

Fig. 3. Layout of the SC experiment[29] together with typical $\pi^+ \rightarrow \mu^+ \rightarrow e^+$ and $\pi^+ \rightarrow e^+$ signals, as recorded on a fast oscilloscope (the time scale unit, "milli-micro-second" (mμs) is called "nanosecond" (ns) today). Counter 3 is the active target where incident π^+ mesons stop. The NaI counter information was not used in the final analysis.

electronics?

$\pi \rightarrow e\nu$ experiment electronics

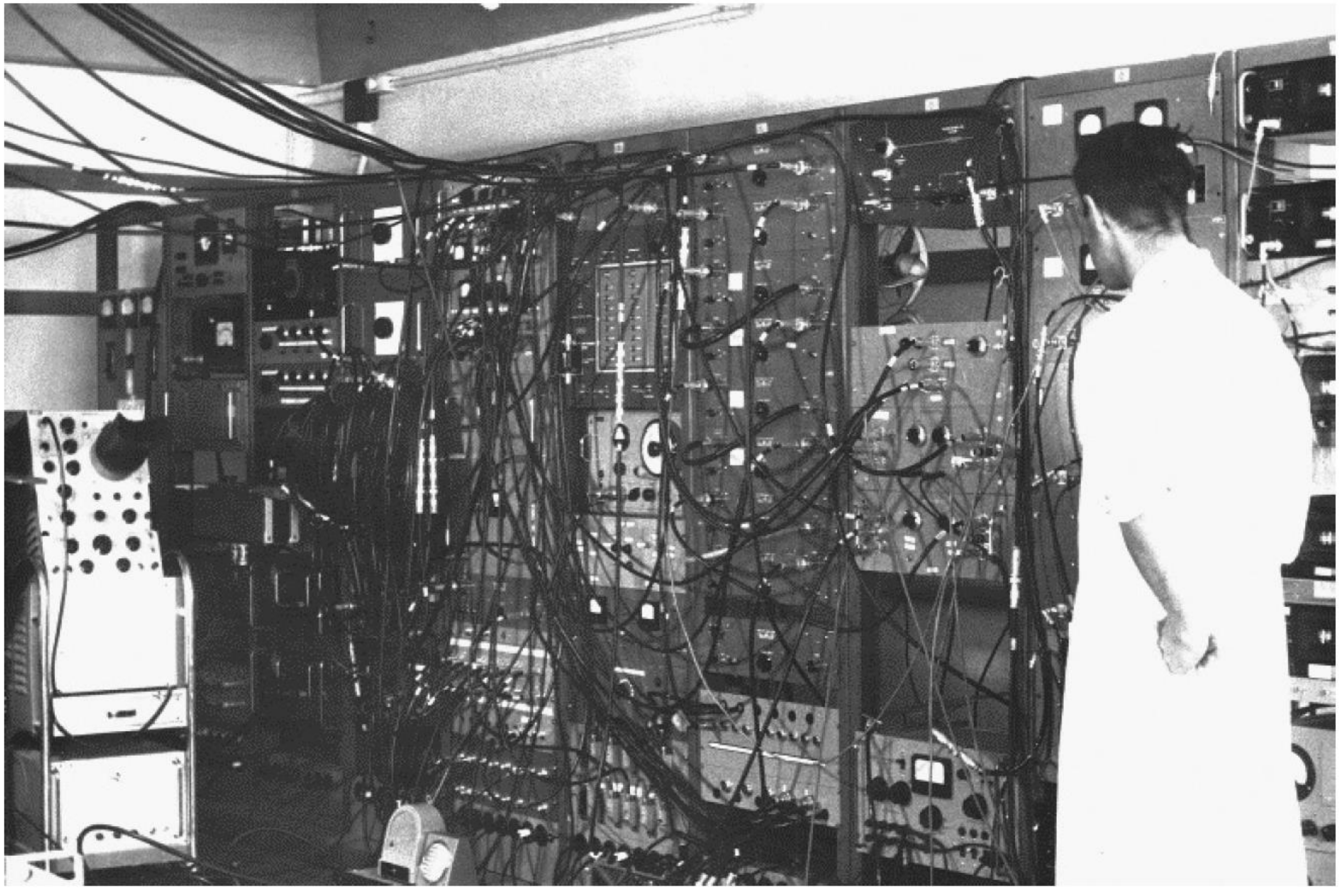


Fig. 6. The main electronic racks in the counting room of the SC experiment.[29]

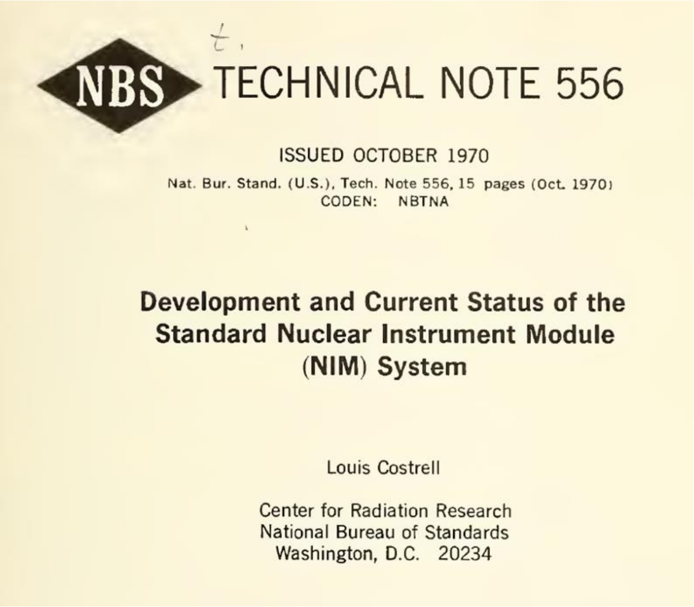
Not so different from today?

NIM (Nuclear Instrumentation Module) era

By the 1950's it was realized that most all nuclear instrumentation utilized several, common, basic building blocks with only a single or couple of application specific items for each different measurement scheme or system.

The idea came to a number of people that the basic building blocks could be provided in portable, removable modules common to a single cage or rack which would itself have a built in power supply to supply 4 commonly used DC and the standard line AC voltages on a bussed together group of standard amp plugs. The cage and attached power supply would itself fit into a standard 19" rack for laboratory use. The standardized modules could then just slide into the rack on rails and the rear mounted power plugs couple into the modules. The modules could then be linked up in logical order via front or back BNC jacks and cables to make any instrument desired. Neat, huh?

with the invention of the bipolar transistor, more shrinkage began



t,

NBS TECHNICAL NOTE 556

ISSUED OCTOBER 1970

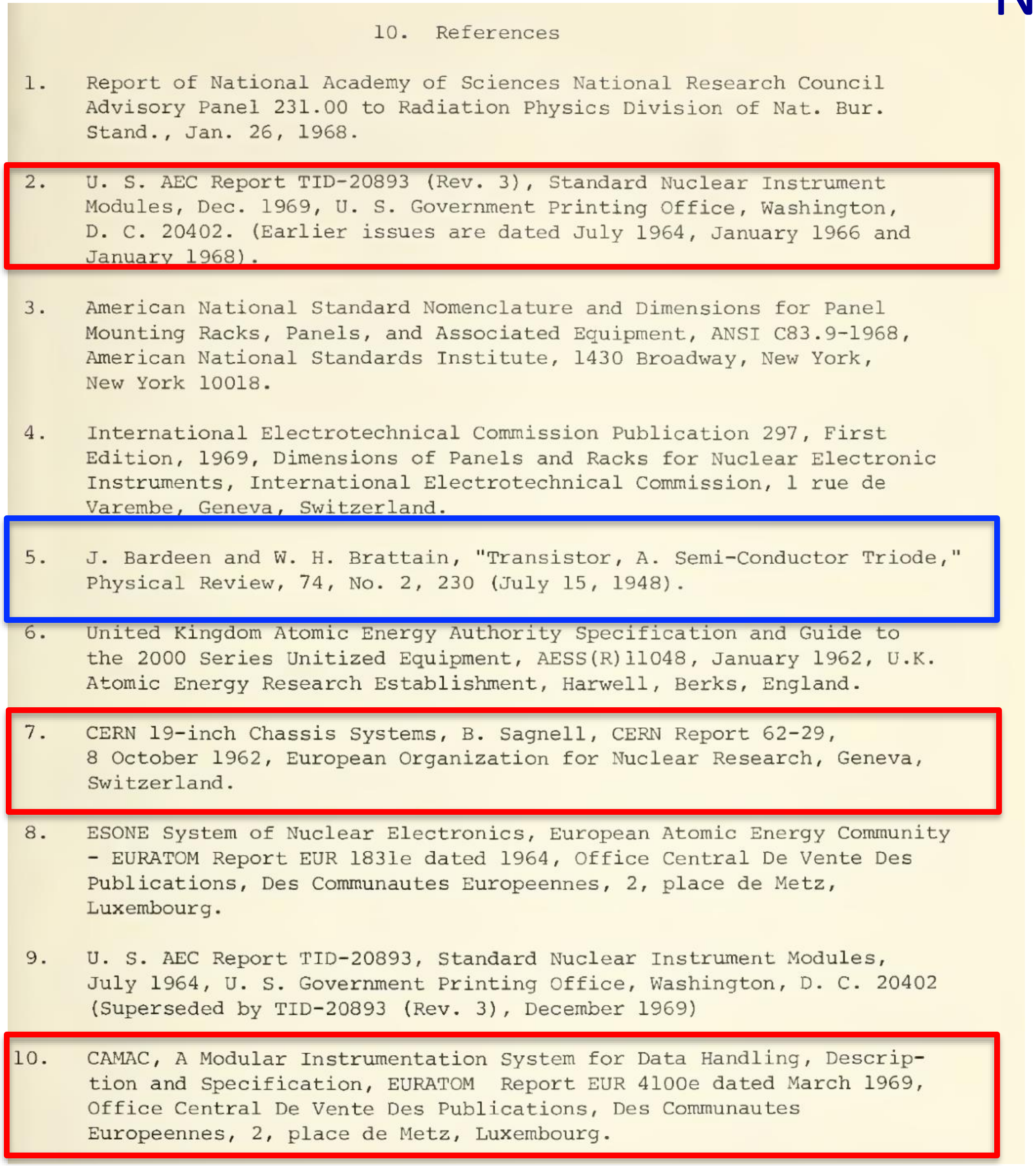
Nat. Bur. Stand. (U.S.), Tech. Note 556, 15 pages (Oct. 1970)
CODEN: NBTNA

Development and Current Status of the Standard Nuclear Instrument Module (NIM) System

Louis Costrell

Center for Radiation Research
National Bureau of Standards
Washington, D.C. 20234

NIM and miniaturisation



10. References

1. Report of National Academy of Sciences National Research Council Advisory Panel 231.00 to Radiation Physics Division of Nat. Bur. Stand., Jan. 26, 1968.

2. U. S. AEC Report TID-20893 (Rev. 3), Standard Nuclear Instrument Modules, Dec. 1969, U. S. Government Printing Office, Washington, D. C. 20402. (Earlier issues are dated July 1964, January 1966 and January 1968).

3. American National Standard Nomenclature and Dimensions for Panel Mounting Racks, Panels, and Associated Equipment, ANSI C83.9-1968, American National Standards Institute, 1430 Broadway, New York, New York 10018.

4. International Electrotechnical Commission Publication 297, First Edition, 1969, Dimensions of Panels and Racks for Nuclear Electronic Instruments, International Electrotechnical Commission, 1 rue de Varembe, Geneva, Switzerland.

5. J. Bardeen and W. H. Brattain, "Transistor, A. Semi-Conductor Triode," Physical Review, 74, No. 2, 230 (July 15, 1948).

6. United Kingdom Atomic Energy Authority Specification and Guide to the 2000 Series Unitized Equipment, AESS(R)11048, January 1962, U.K. Atomic Energy Research Establishment, Harwell, Berks, England.

7. CERN 19-inch Chassis Systems, B. Sagnell, CERN Report 62-29, 8 October 1962, European Organization for Nuclear Research, Geneva, Switzerland.

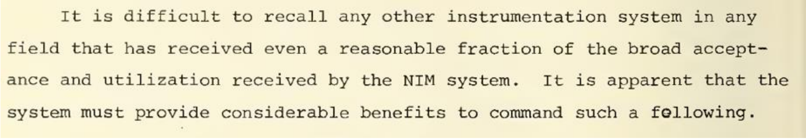
8. ESONE System of Nuclear Electronics, European Atomic Energy Community - EURATOM Report EUR 1831e dated 1964, Office Central De Vente Des Publications, Des Communautes Europeennes, 2, place de Metz, Luxembourg.

9. U. S. AEC Report TID-20893, Standard Nuclear Instrument Modules, July 1964, U. S. Government Printing Office, Washington, D. C. 20402 (Superseded by TID-20893 (Rev. 3), December 1969)

10. CAMAC, A Modular Instrumentation System for Data Handling, Description and Specification, EURATOM Report EUR 4100e dated March 1969, Office Central De Vente Des Publications, Des Communautes Europeennes, 2, place de Metz, Luxembourg.

"Though transistors are extremely small compared to vacuum tubes and consume far less power, transistorized instruments that emerged in the 1950 's were nonetheless constructed in a manner quite similar to that of their vacuum tube predecessors. Thus the ***instruments utilized 19-inch front panels*** *and contained their own dc power supplies operated from the ac line. It rapidly became apparent that such construction was quite uneconomical and inefficient, that* ***a number of transistorized instruments in modular form could be accommodated in the space occupied by a single 19-inch panel****, and that a single dc power supply…"*

Popular too…



It is difficult to recall any other instrumentation system in any field that has received even a reasonable fraction of the broad acceptance and utilization received by the NIM system. It is apparent that the system must provide considerable benefits to command such a following.

As seen in 1980

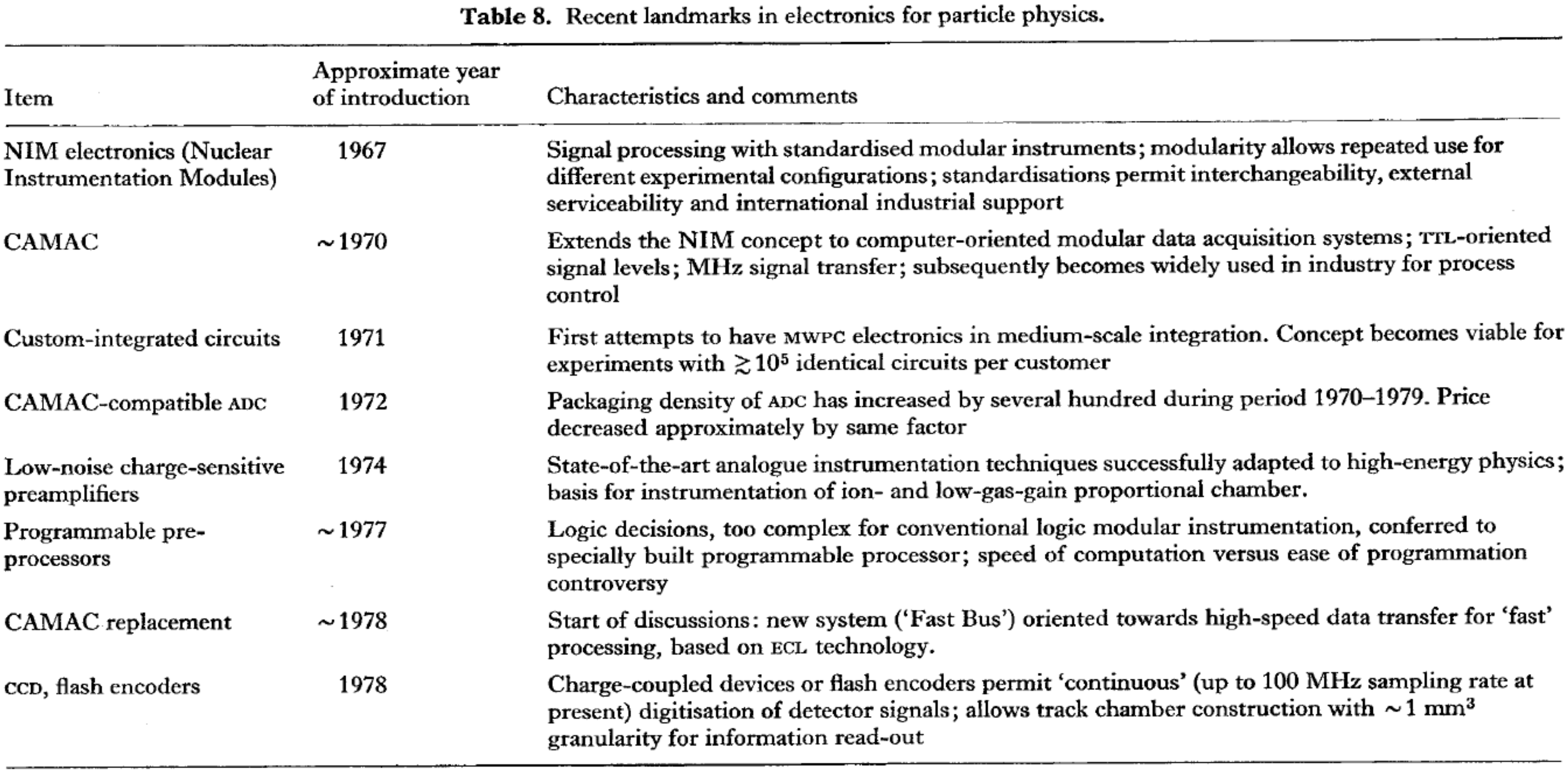


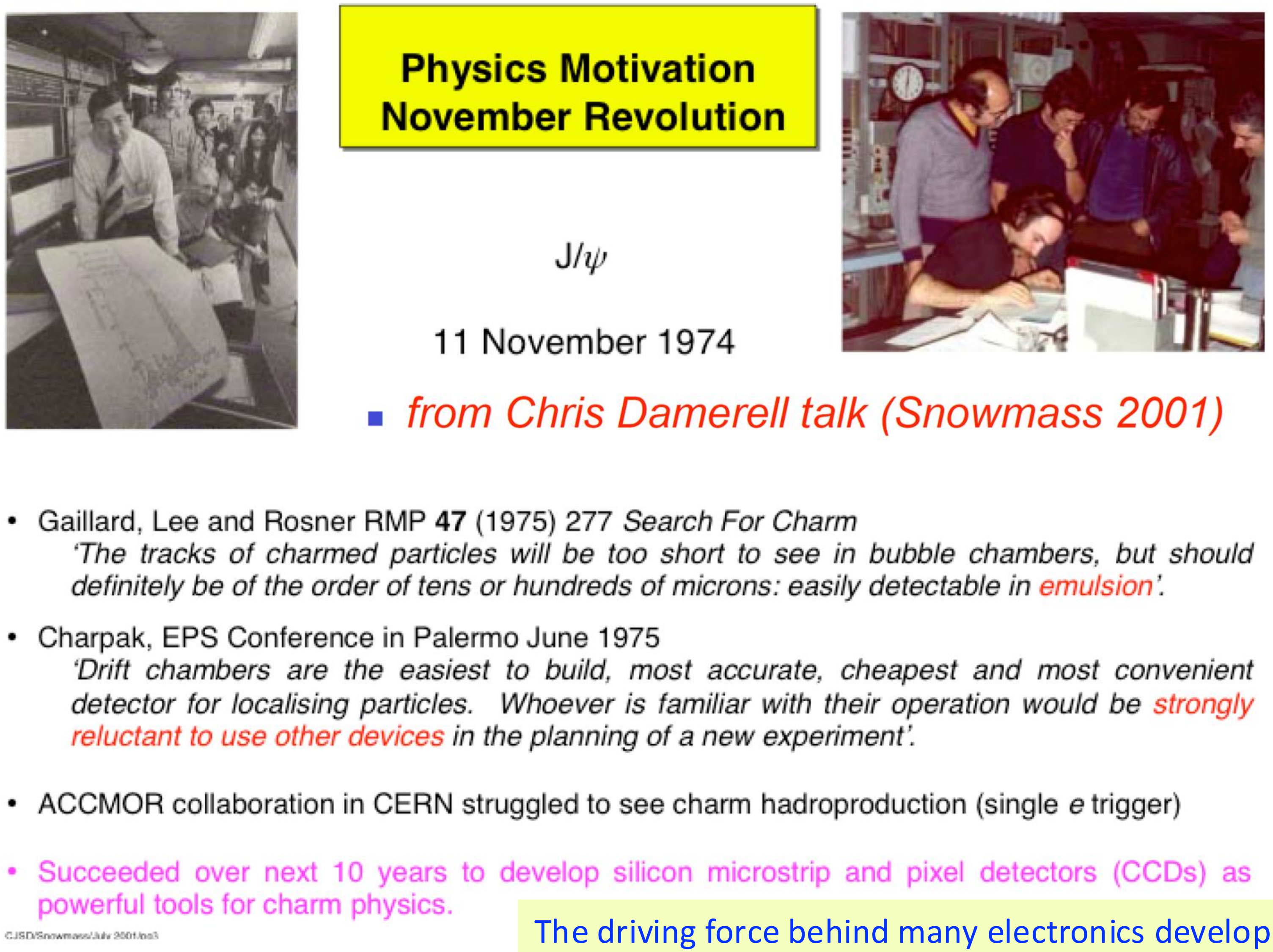
Table 8. Recent landmarks in electronics for particle physics.

Item	Approximate year of introduction	Characteristics and comments
NIM electronics (Nuclear Instrumentation Modules)	1967	Signal processing with standardised modular instruments; modularity allows repeated use for different experimental configurations; standardisations permit interchangeability, external serviceability and international industrial support
CAMAC	~1970	Extends the NIM concept to computer-oriented modular data acquisition systems; TTL-oriented signal levels; MHz signal transfer; subsequently becomes widely used in industry for process control
Custom-integrated circuits	1971	First attempts to have MWPC electronics in medium-scale integration. Concept becomes viable for experiments with $\gtrsim 10^5$ identical circuits per customer
CAMAC-compatible ADC	1972	Packaging density of ADC has increased by several hundred during period 1970–1979. Price decreased approximately by same factor
Low-noise charge-sensitive preamplifiers	1974	State-of-the-art analogue instrumentation techniques successfully adapted to high-energy physics; basis for instrumentation of ion- and low-gas-gain proportional chamber.
Programmable pre-processors	~1977	Logic decisions, too complex for conventional logic modular instrumentation, conferred to specially built programmable processor; speed of computation versus ease of programmation controversy
CAMAC replacement	~1978	Start of discussions: new system ('Fast Bus') oriented towards high-speed data transfer for 'fast' processing, based on ECL technology.
CCD, flash encoders	1978	Charge-coupled devices or flash encoders permit 'continuous' (up to 100 MHz sampling rate at present) digitisation of detector signals; allows track chamber construction with ~1 mm^3 granularity for information read-out

"Particle detectors" C W Fabjan and H G Fischer 1980 Rep. Prog. Phys. 43 1003

- Report dominated by gaseous detectors, but also Cerenkov, TR and hadronic and EM calorimetry. Electronics is discussed under detector systems.
- What happened next?

In fact, it had already happened!



Physics Motivation
November Revolution

J/ψ

11 November 1974

- *from Chris Damerell talk (Snowmass 2001)*

- Gaillard, Lee and Rosner RMP **47** (1975) 277 *Search For Charm*
  'The tracks of charmed particles will be too short to see in bubble chambers, but should definitely be of the order of tens or hundreds of microns: easily detectable in emulsion'.
- Charpak, EPS Conference in Palermo June 1975
  'Drift chambers are the easiest to build, most accurate, cheapest and most convenient detector for localising particles. Whoever is familiar with their operation would be strongly reluctant to use other devices in the planning of a new experiment'.
- ACCMOR collaboration in CERN struggled to see charm hadroproduction (single *e* trigger)
- Succeeded over next 10 years to develop silicon microstrip and pixel detectors (CCDs) as powerful tools for charm physics.

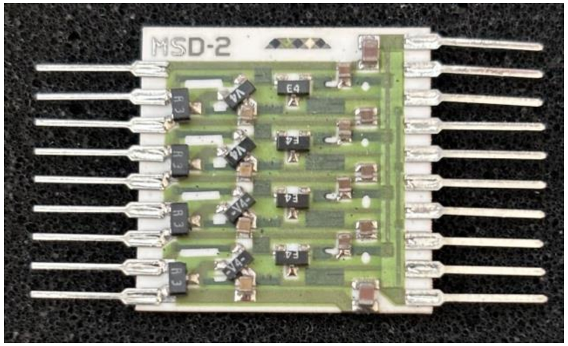
CJSD/Snowmass/July 2001/ps3

The driving force behind many electronics developments since the mid-1980s. Would it have happened anyway?

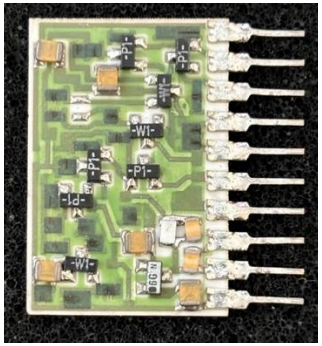
1980s custom integrated circuits

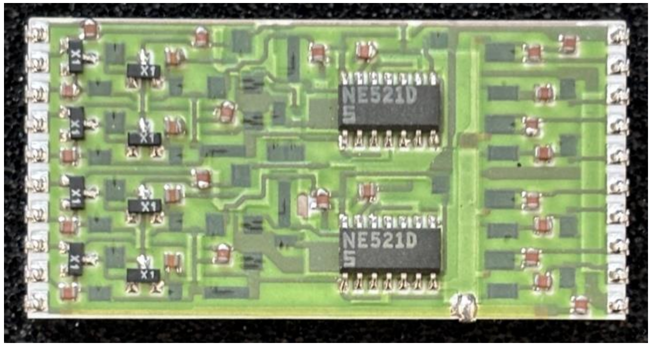
- Hybrid thick film ceramic circuits
  - from LABEN (1958-2004) *LABoratori Elettronici e Nucleari*
    - merged into Alcatel Alenia Space

Quad bipolar preamplifier



Single channel JFET-bipolar preamplifier



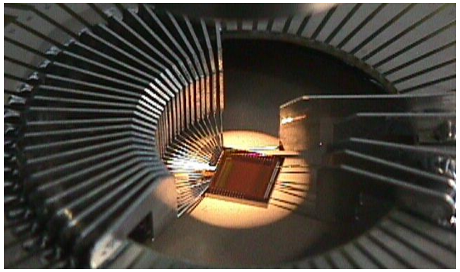


Quad bipolar-IC comparator shaper discriminator

Pitch of pins = 0.1 inch

Not small enough for colliding beam experiments!

The ASIC era



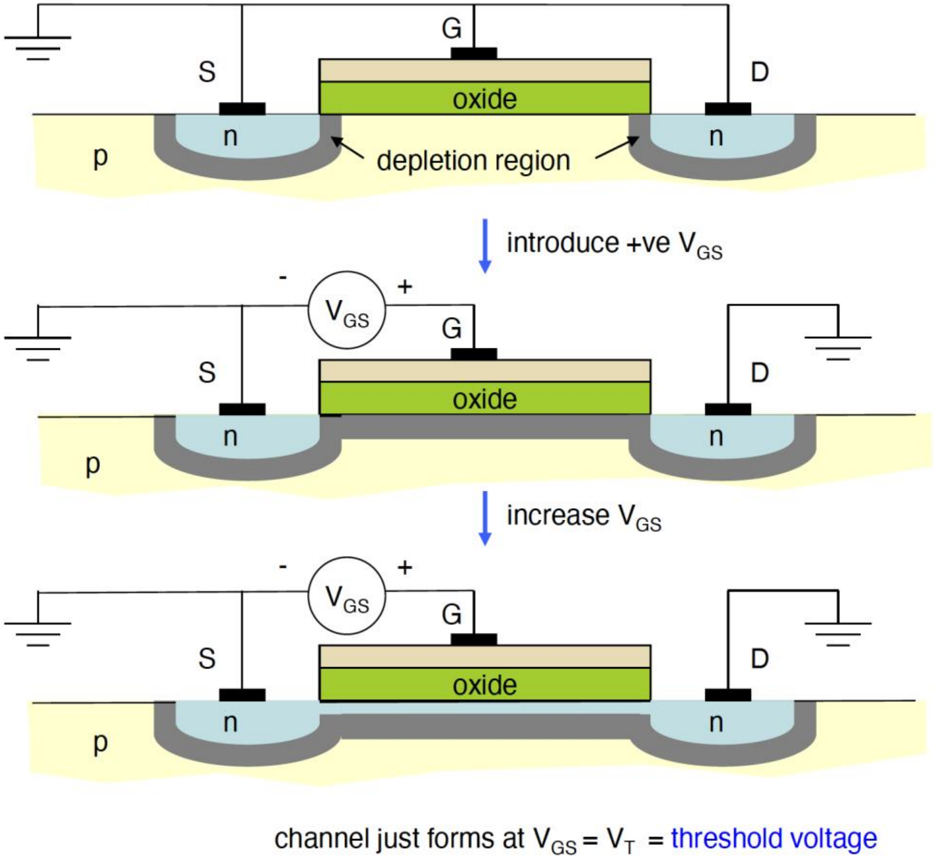
- Application Specific Integrated Circuit
  - customised electronic circuit for a well-defined requirement
  - generally manufactured in **CMOS**

- Pros of ASICs
  - **can be optimised** for demanding requirements: size, power, functions, performance,…
  - **miniature** – large numbers of channels
  - very **dependable manufacturing quality with low unit cost** on large scale
  - **radiation hardness** now understood, and can be excellent in commercial processes
- Cons of ASICs
  - **Big development investment** required in both time and cost
  - **Unchangeable** once complete, unless a lot of flexibility built-in (adds complexity)
  - **Substantial design and evaluation** requiring specialist skills (industry pays well!)

- Well matched – and essential! - to the later LHC era

MOSFETs – in principle and practice

- Transistor is simple device: layout and behaviour, especially digital
  - but also many good analogue properties, if needed



channel just forms at $V_{GS} = V_T$ = threshold voltage

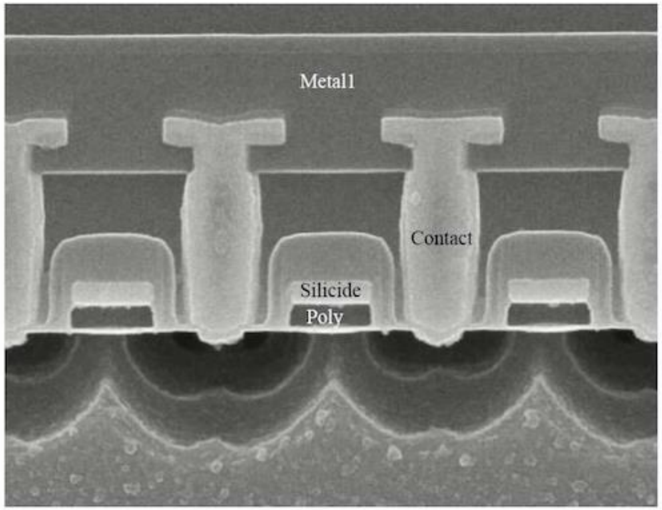


Figure 5.22 SEM image of the cross-section of three MOSFETs.

1990s: many investigations of noise vs power, radiation tolerance in multiple processes

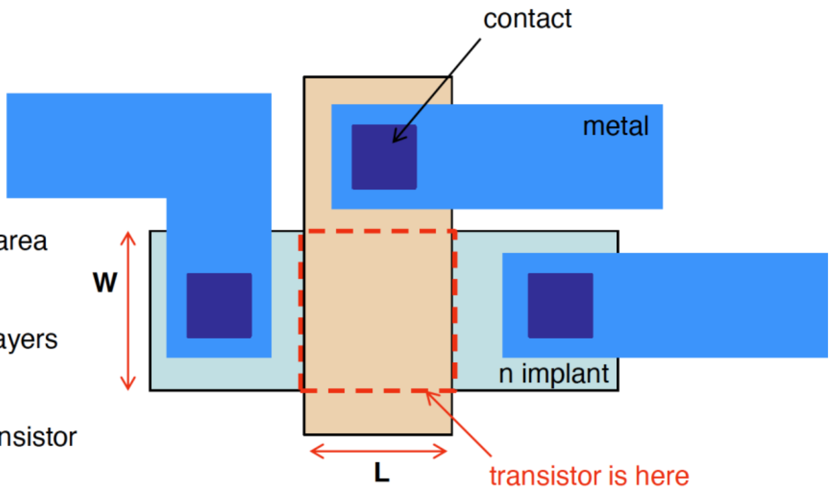
MOSFET design

designer draws the masks

NMOS transistor is formed where gate area crosses n implanted area

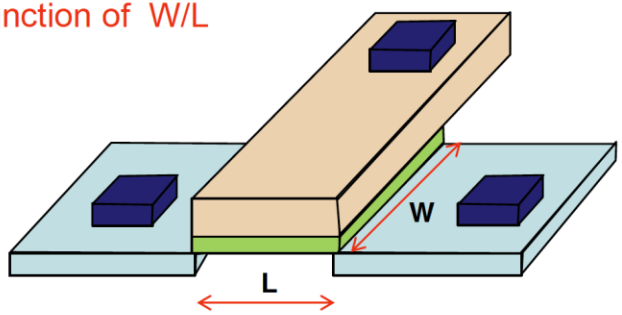
contact regions are defined and metal layers used for connections

only the width **W** and length **L** of the transistor are under the designer's control



transconductance is a rather simple function of W/L

In practice today, sophisticated computerised design software is used to lay out transistors often with libraries of frequently used circuits



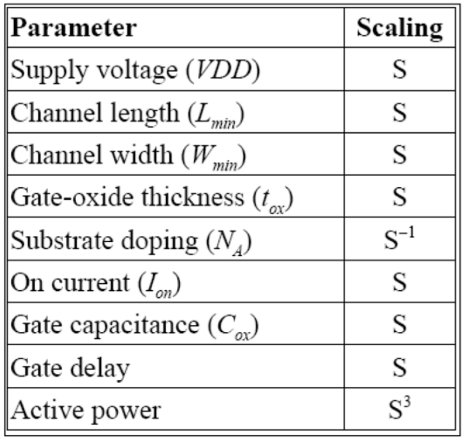
plus a lot of complex simulation tools and checking to validate designs

It really was like this around 1985! Our engineers were learning this new technology.

Circuit properties mainly scale with feature size

L, W, t_{ox}, V =>
L/S, W/S, t_{ox}/S, V/S

Table 6.3 CMOS scaling relationships.

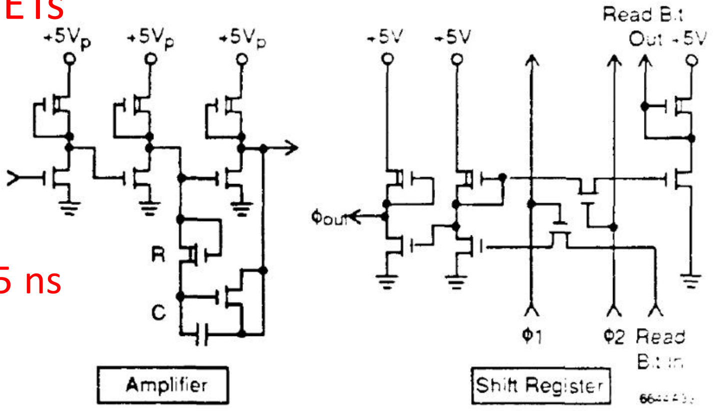


Parameter	Scaling
Supply voltage (VDD)	S
Channel length (L_{min})	S
Channel width (W_{min})	S
Gate-oxide thickness (t_{ox})	S
Substrate doping (N_A)	S^{-1}
On current (I_{on})	S
Gate capacitance (C_{ox})	S
Gate delay	S
Active power	S^3

A very brief history

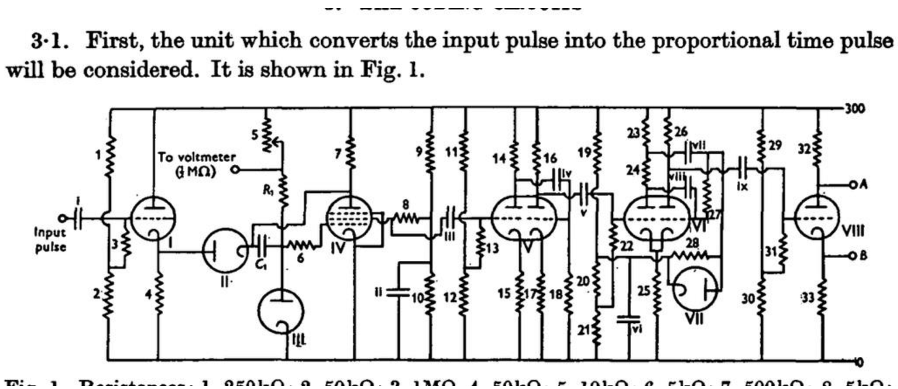
- 1984 - first HEP ASIC: Microplex at SLAC (California!) Mark-II silicon vertex detector
  - NMOS only : 128 channel - amplifier, Sample-Hold, DCS processing, multiplexing.
    - 34 mm^2 , 5µm university lab process, **14 mW/ch**. **Pioneers** learned from first principles!
- Late 1980s: MX3, MX7, CAMEX64 - LEP silicon vertex detectors
  - Commercial CMOS, initially ~3µm and later 1.5µm => 1-2 mW/channel
    - Amplifiers: integrators with switched capacitor filters. Switching noise injected during the amplifier reset subtracted due to its very reproducible behaviour. $t_{rise} \approx 400$ ns, $t_{int} \approx 1.8$ µs
- 1988: SVX ASIC for CDF (& L3) – memory & sparsification
  - amplifier, comparator, multiplexer, nearest neighbour logic, pedestal subtraction
    - 128 channels in 3 µm CMOS $t_{int} \approx 200$ ns, $t_{sample} \approx 0.5$ µs
- 1990: Amplex for UA2 Si pads - feedback resistors using FETs
  - 16 channel 3µm CMOS, precise control of non-linear R
    - more conventional RC filters implemented: $\tau_{peak} = 0.75$ µs
- Early 1990s – LHC developments began
  - originally 66 MHz beam crossing rate, later 40 MHz => $\tau \approx 25$ ns
    - almost x 10^6! - from 120 Hz at Mark-II in a decade
    - but 1-2 µm processes

Part of the Microplex circuit



The low noise era

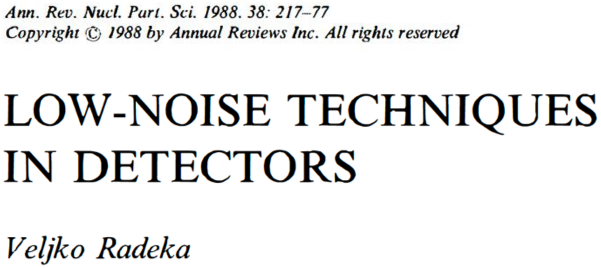
- We owe a lot to the early nuclear physicists and engineers
  - e.g. the design of the Wilkinson ADC, based on valve circuits, is far from simple



3·1. First, the unit which converts the input pulse into the proportional time pulse will be considered. It is shown in Fig. 1.

- Most of the literature on signal processing originates in the 1960s
  - e.g. Radeka, Goulding, Gatti, Manfredi, Kandiah,…

In my case, also:

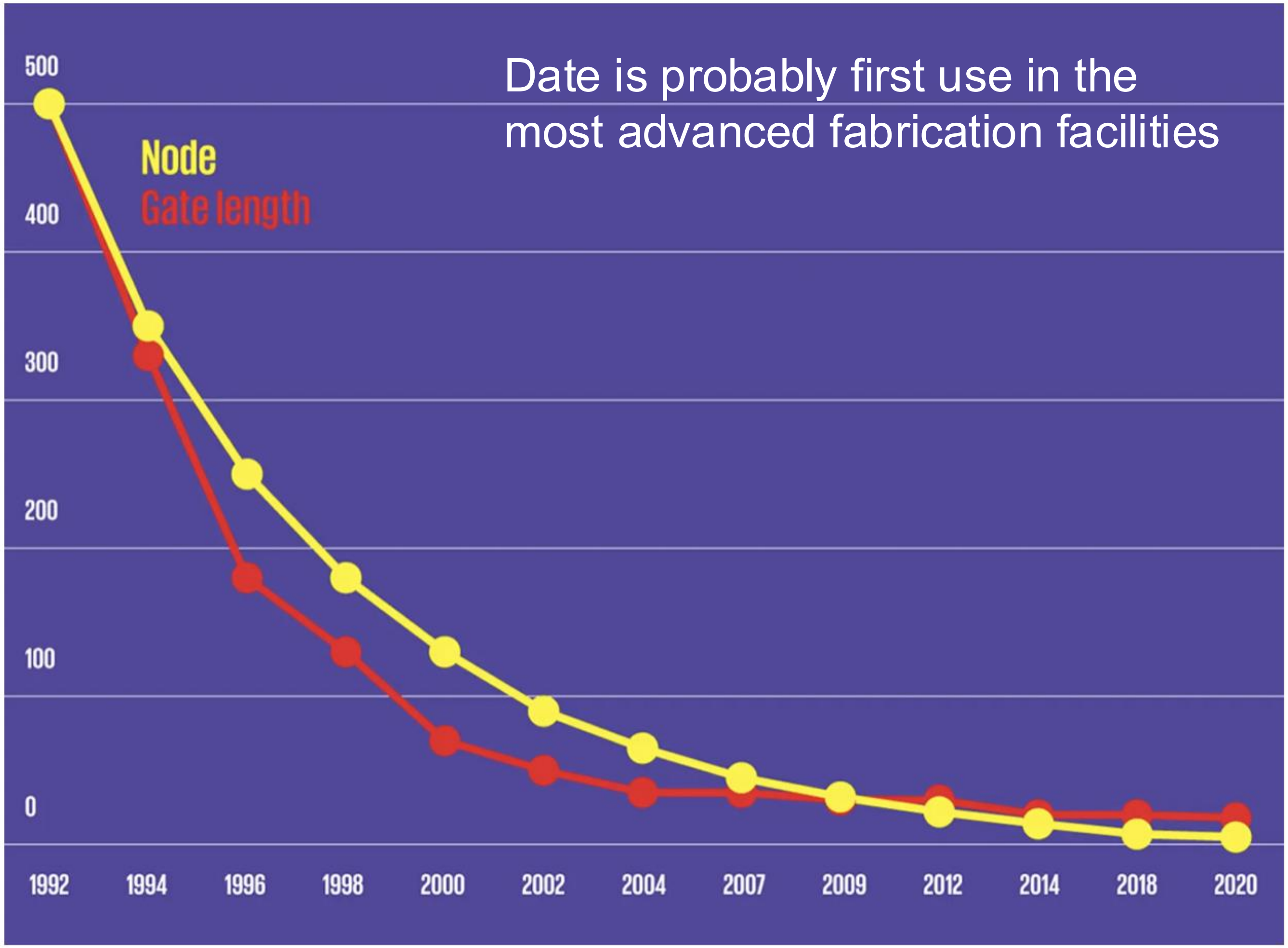


Ann. Rev. Nucl. Part. Sci. 1988. 38: 217–77
Copyright © 1988 by Annual Reviews Inc. All rights reserved

LOW-NOISE TECHNIQUES
IN DETECTORS

Veljko Radeka

ASIC technology progress



Date is probably first use in the most advanced fabrication facilities

SOURCES: STANFORD NANOELECTRONICS LAB, WIKICHIP, IEEE INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2020

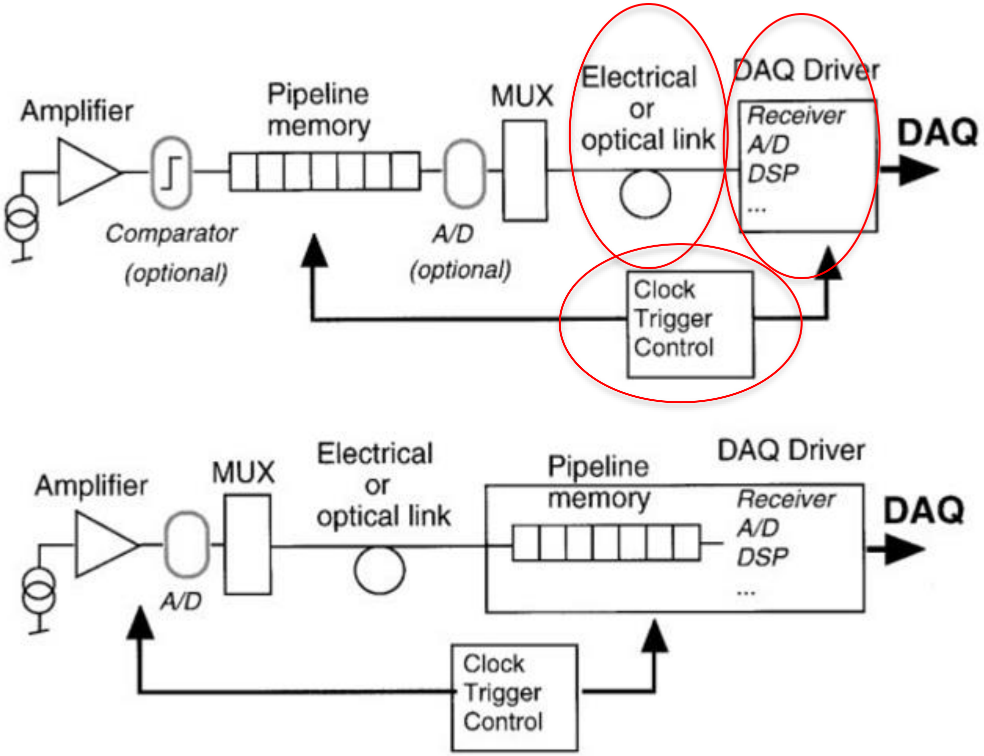
- In 1998 we were designing the APV25 for CMS in 0.25 µm
  - finalised 2000/2001
- We started designing the CBC chip in 2010, in 130 nm
  - "completed" CBC3.1 in 2018/2019
- Today HEP is designing in 65 nm
  - Some are testing the water with 28 nm
- Note the lag to HEP

LHC era

- Developments initially driven mainly by trackers and ECALs
  - Amplifiers, data conversion and FE storage, data transfer, ….
  - Clock and control, Trigger

- Many possible design choices, e.g.:
  - analogue/digital/binary
  - performance
  - commercial or custom
  - radiation tolerance
  - power, cost, risk …

- ASICs came first but other things were essential too, especially
  - optoelectronics
  - trigger processors
  - computer technology evolution



a couple of possible variants

How did we get to where we are today?

- Sponsored R&D (US SSC detector R&D 1988, CERN DRDC 1990)
  - essential because SSC/LHC detectors were unbuildable
  - **serendipity**: mass commercial electronics era -> internet age
    - 1980s-1990s: RISC processors, PCs, Apple desktops, WWW, modems, mobile phones, laptops,…
  - all were driving greater miniaturisation
    - many "invisible" components, like connectors, packaging, batteries…

- Integrated circuit electronics
  - emergence of **accessible ASIC processes**, and design tools
  - significant investment in **training** of new generation of engineers as designers

Several crucial areas - **commercially driven** - not by HEP

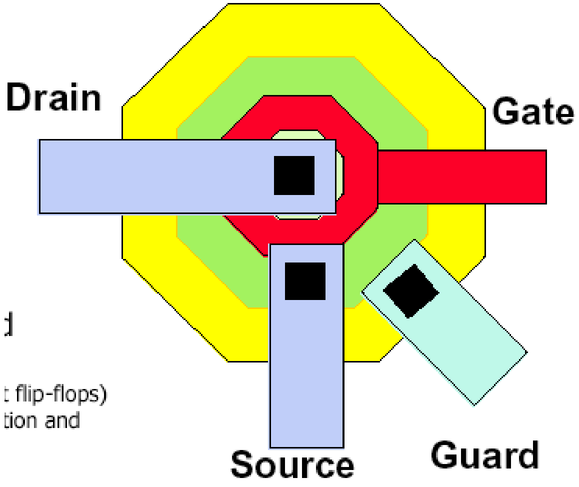
Example: CMS silicon µstrip tracker ASICs

- Began in 1991 in RD20 DRDC project
  - series of prototype chips in supposed rad-hard 1.2 µm technology, 32- then 128-channel
  - by 1997: APV6 might have been a candidate for final system
    - many irradiation studies of single transistors (noise) and chip performance
  - Along the way, some important innovations
    - programming chip parameters via serial command interface (I2C) using software control
    - **hugely beneficial in accelerating** chip configuration and evaluation
    - simple signal processing on chip

- Bad luck in September 1997
  - Foundry move of 1.2 µm process **reduced** radiation tolerance (marginal anyway)
- Followed by good luck
  - Unexpected **positive** CERN results on 0.25 µm radiation tolerance
- In 1998 switched to "standard commercial" process
  - how was that possible?

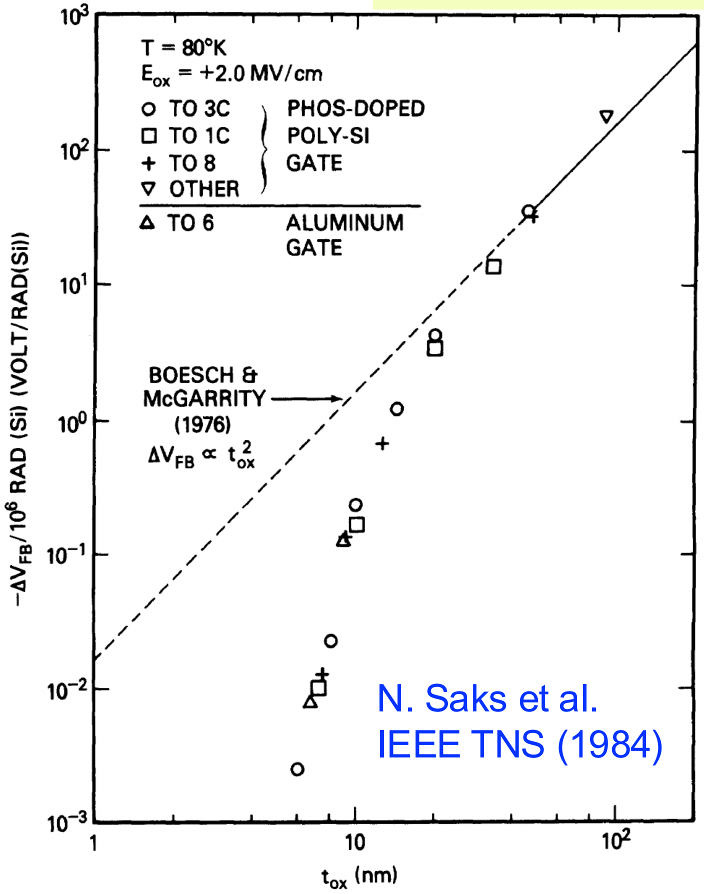
Radiation behaviour of commercial CMOS

- Evidence of radiation tolerance in mid-1980s, improving with thinner oxides
  - tunnelling of carriers reduces trapped oxide charge
  - but confusing results from commercial chip evaluations
- negative effects attributed to leakage paths around NMOS transistors
  - *cured in CERN 1997 with enclosed gate geometry*



This was a **hugely important** breakthrough

ΔV_{FB}/Mrad vs t_{ox}

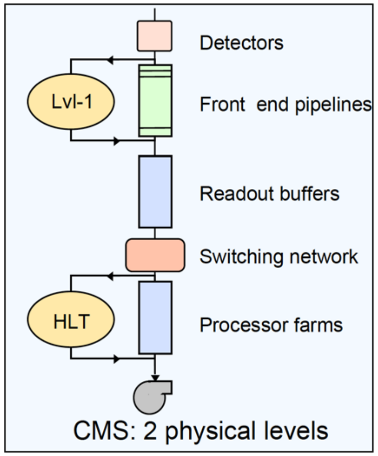


N. Saks et al.
IEEE TNS (1984)

Other important technologies

- Two other crucial technologies evolved rapidly during the LHC preparations
  - exploiting the ASIC revolution

- **Optoelectronics** – i.e. fibre optic links
  - almost non-existent in 1990
  - now 25 Gbps links, and infrastructure, are commonplace
  - immense benefits in power, material, lack of noise transfer



- **Programmable digital logic**
  - 1980s – board-based logic assembled from arrays of digital chips
  - **FPGAs** evolved to (probably) allow all(?) trigger logic and flexible DAQ

- No totally free lunch though
  - challenges of power, cooling, connectivity, specialist skills,…

Opto-electronics

- B. Leskovar (1990) SSC workshop
  - *Optical data transmission at the SSC* IEEE Trans.Nucl.Sci. 37 (1990) 271-287
    - extremely detailed discussion, including radiation hardness issues
- Many DRDC projects started in 1991, including RD12 & RD23
  - RD12 proposed optical distribution of TTC signals at the LHC
    - commercial parts using 1300 nm lasers and SM fibres, but not radiation hard
  - RD23 proposed optoelectronic modulators for data transmission **inside** the experiments
    - technologies: $LiNbO_3$ and Multi Quantum Well reflective modulators
- $LiNbO_3$ well established but several drawbacks
  - bulky, polarisation maintenance, cost
- MQW attractive but more speculative
  - very reliant on commercial device progress
- Other technologies became accessible
  - Fabry-Perot edge emitters, VCSELs
  - both successfully deployed in CMS & ATLAS

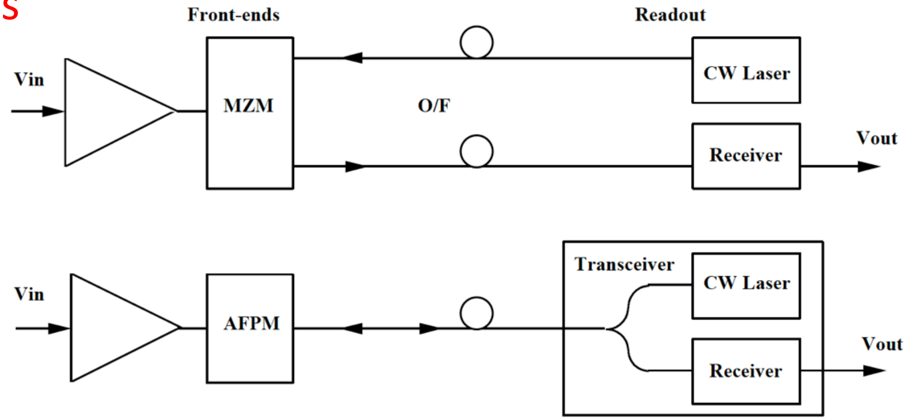
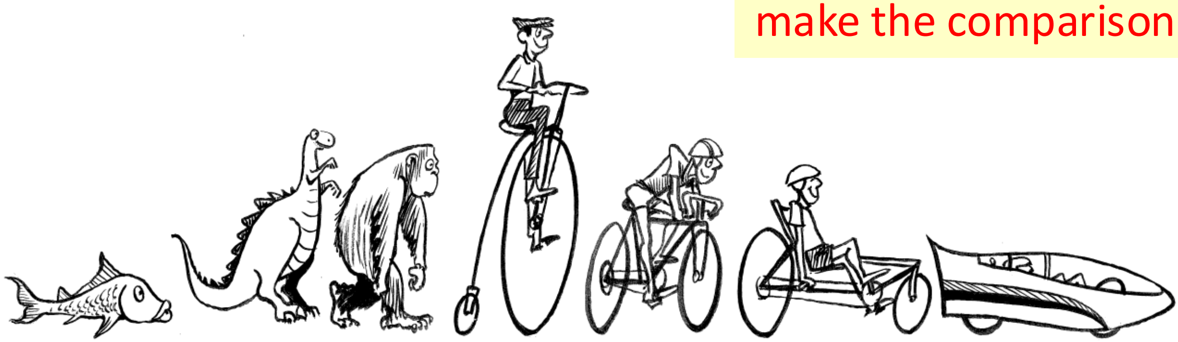


Fig. 3.1 - Optical links with transmission/reflection intensity modulators

Importance of optoelectronics

- Advantages of optical data transfer
  - (much) reduced material in cables
  - lower power (probably by a big factor)
  - (much lower) risk of excess noise and (likely greatly) improved signal integrity
  - higher (total) bandwidth
  - standardisation – a big step forward
    - e.g. CMS used the same technology for tracker (40 MHz analogue) and ECAL (800 Mbps)

fortunately we did not have to make the comparisons in practice



Digital processing & FPGAs

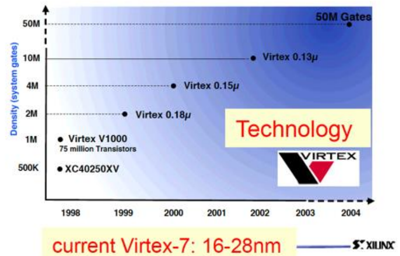
- 1980s: board based processors
  - COTS: various processor technologies: RISC, transputers, microprocessors, ….
  - custom: assemble arrays of digital chips to implement required logic

- 1990s: technology evolution
  - commercial switches, networks, fast links, traffic management, ever faster computers,..
    - but not sufficient for first level triggers:
  - Programmable chips materialised
    - Field Programmable Gate Arrays

- 2010+:
  - huge progress with FPGAs
    - speed, BW, connectivity, flexibility,…
  - feasible that most L1 triggers could be FPGA-based
    - but many practical issues of cooling, optical connectivity, board design, programming, complexity, …

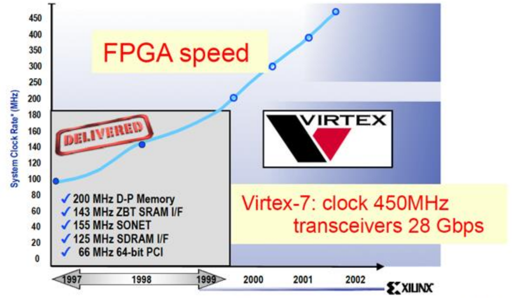
P Alfke (Xilinx Corp)

The view in 1999



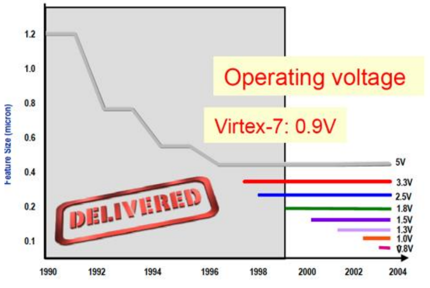
Technology

current Virtex-7: 16-28nm



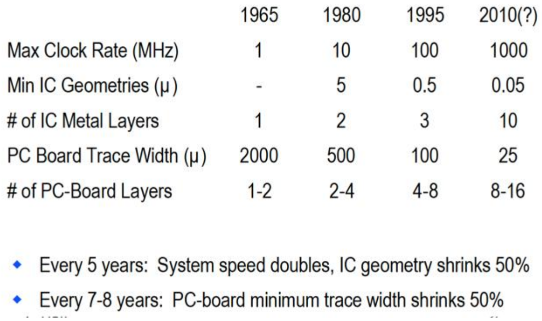
FPGA speed

Virtex-7: clock 450MHz
transceivers 28 Gbps



Operating voltage

Virtex-7: 0.9V



	1965	1980	1995	2010(?)
Max Clock Rate (MHz)	1	10	100	1000
Min IC Geometries (µ)	-	5	0.5	0.05
# of IC Metal Layers	1	2	3	10
PC Board Trace Width (µ)	2000	500	100	25
# of PC-Board Layers	1-2	2-4	4-8	8-16

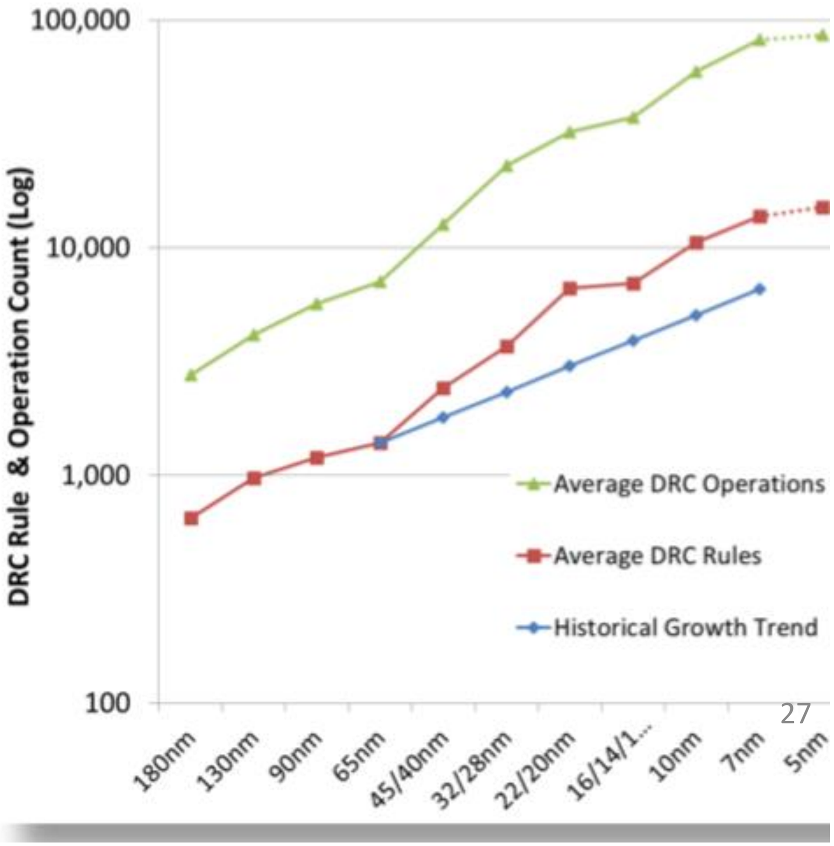
- Every 5 years: System speed doubles, IC geometry shrinks 50%
- Every 7-8 years: PC-board minimum trace width shrinks 50%

How to succeed in this world?

- Today’s designs are remarkably successful
  - Quality of design tools
  - Quality of manufacture
  - Experienced designers
  - Comprehensive simulations
  - Prototyping
  - Careful evaluation (eventually in situ)

  - Financial investment!

Evolution of ASIC design rules



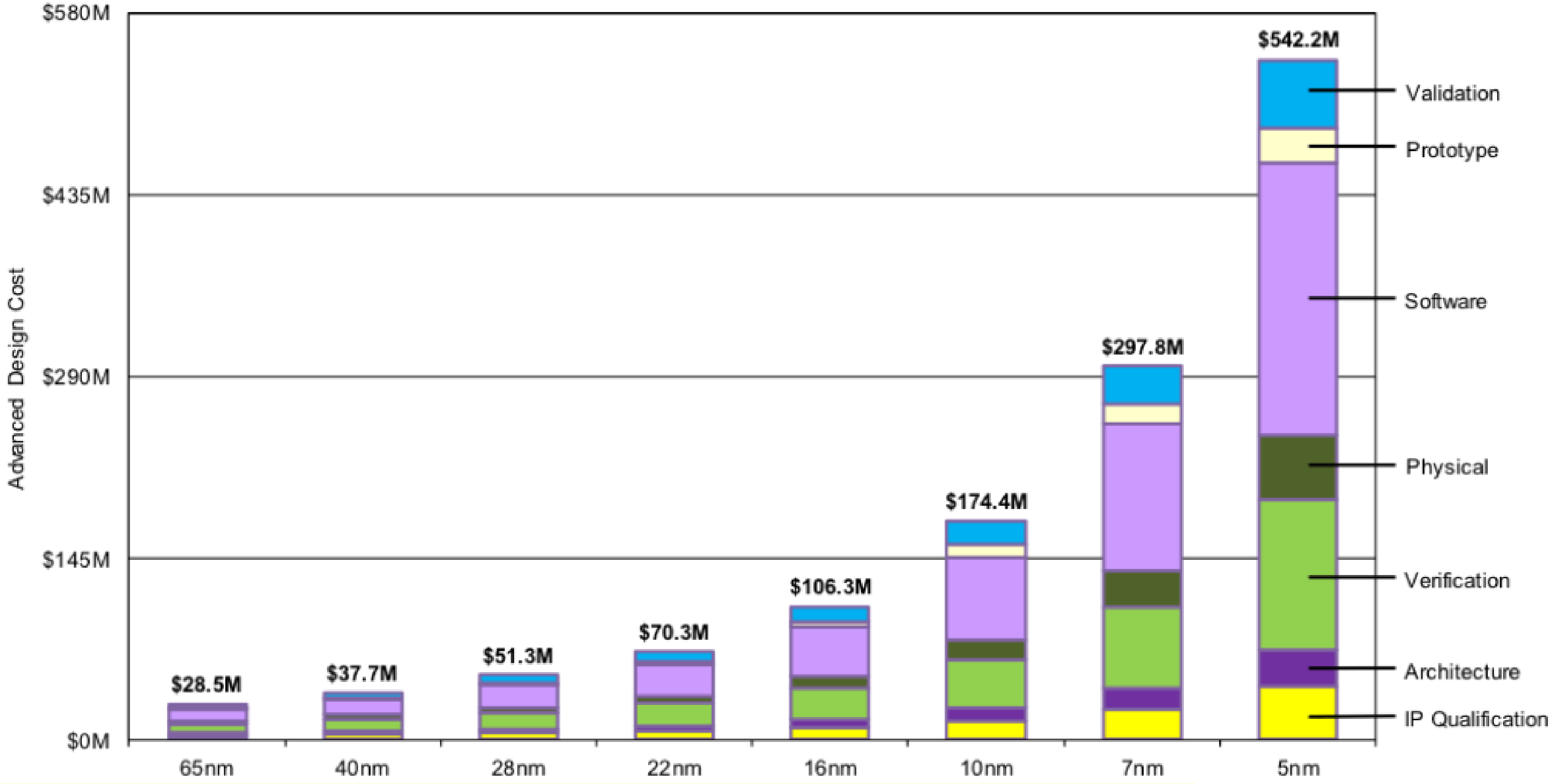
Another price to be paid =>

NB log scale

Costs cannot be ignored

- Not just financial

Design costs vs ASIC technology node



This probably applies everywhere in our electronics – industry too

From: Semiconductor Engineering

Some conclusions

- Our electronics has changed dramatically in CERN's lifetime
  - but the objectives (e.g. triggering, position, time and energy measurement) remain

- The LHC fortuitously coincided with the internet era
  - explosion of relevant technology development – high volume, low unit cost
    - much of it accessible to small users, such as HEP
  - **it is arguable that the biggest changes in detector technology were in electronics**
    - it has enabled implementation of increasingly complex functionality

- BUT greater complexity = longer development times and more resources
  - higher risk and less flexibility for small projects
  - How to manage this for the next generation?

- Not to be forgotten
  - electronics is commercially driven
  - and cannot be assumed to align with science

"When examining these new contracts, gentlemen, please note that in Paragraph 48 the word 'golden' has been replaced by 'plywood' and 'parachute' is now 'toboggan.'"

CartoonStock.com