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Single Event Upset rates in the CBC in CMS

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ABSTRACT

The CMS Binary Chip (CBC) is a front-end ASIC to be used by the CMS tracker following its upgrade for High Luminosity LHC operation. It will instrument special silicon microstrip detectors to identify high transverse momentum particles in real time so tracking data can be used in the L1 trigger. The CBC should be robust against Single Event Upsets (SEUs). SEU rates have been measured in a series of tests in a 62 MeV proton beam. Each version of the chip has increased the digital circuitry, and hence the SEU susceptibility, and has also been subject to design improvements which affect SEU tolerance. The relevant design features are explained and SEU measurements reported. The expected SEU rates at the HL-LHC are estimated.

1. Introduction

A single event upset (SEU) arises from a significant localised ionisation energy deposit in a digital circuit. At the LHC, this mostly results from knock-on silicon atoms generated by ionising particles or neutrons, which is described in more detail in [1]. SEUs are observed as a bit-flip in a register caused when the ionisation charge is sufficient to change its state. Depending on detailed circuit design, multiple simultaneous bit-flips may be possible. Few previous studies have reported SEU rates in front-end ASICs for the LHC (see e.g.[2–4]) although this will be increasingly important for operation at the High Luminosity LHC (HL-LHC).

The CBC ASICs have been manufactured in a 130 nm CMOS technology incorporating SEU-tolerant designs. The first version, CBC1, contained an amplifier, comparator and pipeline memory for each channel and multiplexed data output, but subsequent versions (denoted CBC2, CBC3.0 and CBC3.1) were developed to provide data to track-finding processors and the Level-1 trigger, using 2S pT-modules [5], hence with cluster-finding and stub processing logic. (A stub is a pair of clusters in the two layers of sensors in the pT-module, consistent with a short track vector of interest.) Each version of the CBC increased the digital circuitry, with the largest change between CBC2 and CBC3.0, thus potentially increasing overall SEU susceptibility.

The CBC is not expected to be totally immune to SEUs. Therefore evaluation of each chip has been carried out in a proton beam. Results of the tests are summarised here. A more detailed account is in preparation [6]. Typically, with an exposure of a couple of working days, the number of SEUs observed is small so results are limited by statistics. The impact of an SEU depends on its location in the CBC; most registers store values which have very limited consequences should they change. A few values, affecting the chip globally, might be more important for operation. SEUs which affect hit data in the pipeline should be unimportant. However, once an SEU has corrupted a register, it will remain so until a chip reset is issued, or the register is rewritten.

2. SEU measurements at Louvain

Average SEU cross sections for LHC secondary particle spectra in CMS are similar to those from 60–200 MeV protons [1] so tests were carried out in the Light Ion Irradiation Facility (LiF) at UC Louvain in a 62 MeV beam of protons from a cyclotron [7]. The tests were done with the maximum available intensity, $\sim 2 \times 10^8\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, measured with a precision of 5% [8], which is considerably higher than the flux expected in the LHC. SEU rates at HL-LHC can be inferred simply by scaling proportionately from the LiF measured rates. Each test had a duration of 12 to 16 h and CBCs in the beam received a radiation dose of 1–2 Mrad. The total dose behaviour of the CBC3 has been studied [9] and the consequences are insignificant at HL-LHC dose rates. At accelerated doses, an increase in power consumption, which does not affect operation, is observed. Because of this, care was taken to avoid possible bias under different SEU test conditions. The beam conditions for each test are summarised in Table 1.

For the tests, a CBC was wire-bonded on a small board connected to a support board to buffer and drive signals to and from the backend electronics. For the CBC2, these electronics were in a nearby control room connected by 5 m of twisted pair cable. For the CBC3.0 and CBC3.1, the backend electronics were closer, in the beam area behind a lead block, to shorten the cable for 320 MHz clock signals. In the CBC2 test, just one chip was placed in the beam. For the CBC3.0, one

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Table 1
Beam parameters and exposure conditions.

	CBC2	CBC3.0	CBC3.1
Proton energy [MeV]	62	62	62
Flux [10^8 $cm^{-2}s^{-1}$]	2.5	2.3	2.0
Flux relative to HL-LHC	×73.5	×67.6	×58.8
Beam exposure time [h]	12	14.6	(3×)15.6
Total fluence [10^{13} cm^{-2}]	1.1	1.2	1.1
CBC radiation dose [Mrad]	1.5	1.6	1.5

Table 2
Most relevant CBC parameters.

	CBC2	CBC3.0/3.1
Channels	254	254
Pipeline length	256	512
Storage buffer depth	32	32
I^2C registers	307	330/338
Data storage (memory) cells	73,536	138,592
Readout speed [MHz]	40	320
Data frame readout time [μs]	6.65	0.95

chip was placed in the beam and another outside it as a control, in case of background simulating an SEU. In the CBC3.1 test, three chips were placed in the beam, to increase statistics, and one outside. The data acquisition system was based on the GLIB board [10] for the CBC2 and the FC7 [11] for CBC3.0 and CBC3.1.

3. SEU sensitivity of the CBC

The design of the CBC is summarised in [12]. The CBC1 was not subjected to an SEU test. Later versions, starting with the CBC2, included logic for stub-finding [13–16] but the CBC2 did not transmit stub data off-chip at the full HL-LHC rate. This was done in the CBC3 [17,18] which, following CBC2 studies, included modifications to improve SEU robustness. The CBC3.1 had minor changes to finalise the chip for HL-LHC operation; some aimed to further reduce SEU sensitivity.

The chip has 254 front-end channels with amplifier and comparator and reads out microstrips from two sensors, with alternate CBC channels connected to either upper or lower sensor [15]. In this way, hit patterns in the two layers can identify those compatible with a higher transverse momentum track candidate ($p_T \gtrsim 2$ GeV/c). The comparator outputs follow two separate data paths; in one data are stored in a pipeline memory buffer. When a L1 trigger is received, hit data are loaded into a 32-bit deep readout buffer before being read out serially, at 40 Mbps in the CBC2, and at 320 Mbps in the CBC3. A second path identifies and transmits stubs using several stages of combinatorial logic. This runs at the LHC clock rate so track data from every beam crossing can be used in the CMS L1 trigger [19].

Digital logic controls the pipeline, and I^2C registers store values to program operating parameters in the chip. Binary hit values are stored in the pipeline until they are read out after the trigger latency period, which is up to 6.4 μs (CBC2) or 12.8 μs (CBC3). CBC parameters are summarised in Table 2. Possible types of error in the CBC are bit-flips in pipeline cells, pipeline logic upsets, and bit-flips in I^2C registers.

Bit-flips in pipeline cells should be unimportant as memory cells are overwritten every 25 ns clock cycle, so every cell in the CBC3 pipeline is refreshed once every 12.8 μs. SEUs can be detected by storing data at the start of a test with a high comparator threshold so that a logic 0 is written into all cells of the pipeline. Then later, if a logic 1 is detected, it must be due to a bit-flip in the pipeline cell. It was also done by initialising cells to logic 1 and checking for a logic 0.

Pipeline control logic upsets are detected by an error bit in the header of each data frame sent by the CBC. There are counters for the read and write pointers. The difference between their values corresponds to the trigger latency which is stored in an I^2C register. Any of the three values could be affected by an SEU. If the difference between the read and write pointer values differs from the I^2C latency register value, the error bit is set. The error will persist until the three values are reset.

For I^2C registers, bit-flips are detected by comparing the read value with the written value. Although there are more than 300 8-bit I^2C registers, 254 of them tune individual channel offsets so the impact of an SEU is very minor. Some control registers which define analogue circuit parameters globally or which influence hit detection and stub identification might have a bigger impact on operational efficiency. No error which disables the CBC has been detected.

The pipeline logic was designed using Whitaker cells [20], in which case SEU events can only corrupt the cell state while writing at a clock edge, which lasts for much less than 1 ns.

A majority voting scheme was implemented for the I^2C registers in the CBC2, where each bit is triplicated and stored. An SEU then has to occur in at least two cells to flip the state of the bit. An I^2C refresh signal was also implemented which could set a bit to the majority of the three relevant cells. If a refresh is issued sufficiently often, it should be rare that more than one cell of the three has changed state. However, in the CBC3, the majority voting logic was replaced by Whitaker cells.

To compute rates in the HL-LHC environment, it is necessary to know the particle flux where the CBCs will be located. This is explained in the tracker upgrade TDR [5]. The maximum total ionising dose in the Outer Tracker, in the vicinity of 2S-modules, is computed to be 9 Mrad for 3000 fb^{-1} of integrated luminosity. Assuming this is delivered over 10 years with an operational year of 10^7 s entirely by minimum ionising particles (MIPs), it corresponds to a maximum flux of 3.4×10^6 $cm^{-2}s^{-1}$. The statistical uncertainties were estimated to be less than 8% [5].

4. Method of SEU testing

The method was essentially the same for all tests, but detailed procedures were slightly adapted to differences in the CBC versions or the readout system.

Once the CBC receives a fast reset, the logic and error bit are reset, and the write counter starts to increment. The trigger pointer starts after the latency period. The CBC writes binary hit data to the pipeline address at the write pointer value. The CBC reads out data from the location of the read pointer, which is the trigger counter value when it receives the trigger signal.

The pipeline logic was tested by checking the error bit in the data frame header. A trigger was sent multiple times after a fast reset to accumulate statistics.

The pipeline and readout buffer cells were checked together with the pipeline logic. Triggers were sent periodically so that only data for a single event was present in the readout buffer.

The contents of the I^2C registers define the number of cells with logic 0 and 1. Offset values could be chosen to populate 0s and 1s in roughly equal numbers. However, control registers were configured for normal operation in all tests, which meant that arbitrarily chosen values of register settings could not be used. All registers were periodically checked at few s intervals.

5. SEU results from the CBC2

The test took place over two days in 2014. No SEUs were observed in the pipeline logic in an interval of 1.2×10^4 s, which corresponds to 8.8×10^5 s, or about 10 days, at HL-LHC. With a confidence level of 99%, this corresponds to a Poisson upper limit of 0.019 SEU $CBC^{-1}h^{-1}$.

In total, 78 bit-flips were observed in I^2C registers. Of those, 21 were $0\rightarrow1$ and 57 were $1\rightarrow0$ bit-flips. There were a few examples of multiple bit-flips; 14 registers were affected in this way. The results are summarised in Table 3. In runs 6, 8, 9A the I^2C refresh mechanism was studied. However, statistics limited comparisons between those runs, whose interest was limited in view of the change from majority voting logic to Whitaker cells. Run 9B was simply to verify that no bit-flips were observed without beam.

Table 3
Summary of CBC2 bit-flips in I^{2}C registers. N^c is the number of 10 min periods used for each run.

Run	Beam	Number of bit-flips				
	state	0→1	1→0	Total	N^c	Total/N^c
4	On	5	11	16	7	2.29 ± 0.57
6	On	1	5	6	7	0.86 ± 0.35
8	On	6	4	10	6	1.67 ± 0.53
9A	On	5	21	26	4	6.50 ± 1.27
9B	Off	0	0	0	3	0.00 ± 0.00
12	On	4	16	20	6	3.33 ± 0.74
Total		21	57	78		

Table 4
Summary of CBC3.0 bit-flips in I^{2}C registers. The setting type refers to the values in offset registers.

Setting type	Duration	Number of bit-flips		
	[h]	Total	0 → 1	1 → 0
A (all 0xff)	4.64	14	0	14
B (all 0x00)	1.62	2	1	1
C (all 0x0f)	2.80	4	0	4
D (0x80/0x7f)	2.91	5	0	5
Total	11.97	25	1	24

Using data from Run 4 and 12 in Table 3, a total of 36 registers experienced a bit-flip in 130 min exposure. Data from other runs was ignored, because of uncertainties in the efficiency of the refresh mechanism. Scaling to the HL-LHC would lead to an SEU event rate of approximately 0.22 CBC^{-1}h^{-1}.

As there were no bit-flips in the pipeline control logic it was decided that Whitaker cells should be adopted for I^{2}C registers in the next design iteration.

6. SEU results from the CBC3.0

The test carried out in 2017 dedicated 12.4 h to measure the SEU rates. However, a wrong procedure for most of the data taking resulted in a fast reset being sent just before the L1 trigger for 11 h so only 1.4 h could be used to estimate the SEU rate in the pipeline logic. No errors were observed in 5040 s, which corresponds to 3.4×10^5 s at HL-LHC. With a confidence level of 99%, this gives a Poisson upper limit of 0.049 SEU h^{-1}.

The 1.4 h of data taking could be used to estimate the error rate on hit data in the pipeline. In 5.1×10^6 triggers, no fake hits were detected.

The I^{2}C register tests were not affected by the wrong procedure. The results are given in Table 4. A total of 25 bit-flips were observed, all of them of single bits. Again 0→1 flips were significantly less frequent than 1→0.

The rate corresponds to 8.6×10^{-6} s^{-1} or 0.031 ± 0.006 CBC^{-1}h^{-1} in CMS. This is significantly lower than in the CBC2, as expected, but non-zero because there are still some SEU-sensitive nodes in the register circuitry. An SEU on a write node causes the storage cell to flip to the last write transaction on the bus. An SEU on the reset node causes the cell to flip to its default value.

7. SEU results from the CBC3.1

The CBC3.1 is the final version of the CBC, with a small number of minor changes from CBC3.0, of which the most relevant are explained below.

The I^{2}C registers for the CBC3 were designed so that the Whitaker cell for each bit employs its own set of standard inverters to buffer reset and write signals, and produce the inverse, to control both n- and p-type transistor switches in the circuit. The inverters have small node capacitances that make the circuit more susceptible to upset after an ionising charge. This was reasoned to be the cause of the single bit-flips observed in the CBC3. To counter this without major layout changes, it was shown by circuit simulations that by merging together all the reset lines, and likewise all the write lines, for every bit of the register, the effective capacitance of the sensitive nodes was multiplied eight times and required a greater charge deposit to cause an upset.

Table 5
The number of logic 0 and 1 in the 330 8-bit registers for the default settings of the CBC3.1 and for the configuration used in the test. Eight registers not checked are ignored.

	Number of logic 0	Number of logic 1
Default settings	2026	614
Test configuration	1234	1406

A consequence of this modification is that any particle depositing enough charge on either the reset or write line to a register will potentially cause all eight bits to upset. To increase further the capacitance, the size of the inverter cells was also increased as much as possible, leading to devices three times their original size. Simulations of the circuit using standard corner models for the technology showed the modified circuit to be resistant up to a deposited charge of 864 fC, over thirty times greater than for the unmodified circuit.

The CBC3.1 test was carried out in 2019. No pipeline logic errors were observed in 3662 s in the three exposed CBC3.1s. Combined with the results from the CBC3.0, this leads to a 99% confidence level Poisson upper limit of 0.017 SEU CBC^{-1}h^{-1}. This is slightly less than the limit established for the CBC2 but the memory is twice the size, with more extensive control logic.

A few errors in the pipeline memory were observed. Triggers were sent at 20 kHz with the latency between the write and read pointers set to 12.5 μs, which is almost the maximum value which will be allowed in CMS, checking for both 1→0 and 0→1 types of error. There were 74 unexpected values in the three CBCs observed in 7.32×10^7 triggers. Scaling to the HL-LHC flux in CMS leads to 2.2×10^{-11} fake hits per channel per trigger, to be compared with ~1%–2% occupancy.

A total of 15.4 h were dedicated to measuring the SEU rate in I^{2}C registers, which was where changes compared to the CBC3.0 were expected. In the entire test, the content of each register remained unchanged, and the 254 offset registers were all configured so that half of them took the value 0x80 and the other half 0x7f. In this way the offset was in both cases in the middle of the range but with 7 × 0 in one case and 7 × 1 in the other. While the numbers of logic 0 and 1 in the configuration used in the test were almost equal, the default values are dominated by 0, as shown in Table 5.

For the CBC3.0 test, the last written value to the I^{2}C register was always the same (0x41) but different values were used in the CBC3.1 exposures to study its influence. One register was written with the chosen value, e.g. 0x55, after all registers had been read to check their contents. Then, 0x55 stayed in the latch and if the write line of any register were to experience an SEU, that value would be written to the register.

Changes to 81 register values were observed, of which 38 altered a single bit. The three CBC3.1s appeared to behave similarly with 34, 23 and 24 SEUs observed in each. The multiple bit-flip behaviour was more complicated than originally expected and register changes were studied to seek any patterns which could explain it. As explained earlier for the CBC3.0, two types of correlation were expected: with the default value of the register setting, and the last written I^{2}C value.

It was found that the rate of bit-flips depended most strongly on the last written value. In particular, if the value was 0x00, the rate was significantly lower than when it was 0xff. Therefore, to improve statistics under those conditions, each I^{2}C register check, carried out at 2 s intervals, was followed by writing a register with either 0x00 and 0xff, toggling so that the last value alternated between 0x00 and 0xff, for 8.1 h. This method was adopted to avoid any risk of radiation effects from the accumulated dose biasing the result.

Table 6
Comparison of SEU rates in the CBC3.0 and CBC3.1 I^2C registers depending on the last written register value.

CBC version	Last written value	SEU rate at HL-LHC [$CBC^{-1}h^{-1}$]
CBC3.0	–	0.031 ± 0.006
CBC3.1	All used	0.090 ± 0.010
CBC3.1	0xff	0.168 ± 0.025
CBC3.1	0xc1	0.164 ± 0.041
CBC3.1	0x55	0.110 ± 0.030
CBC3.1	0x41	0.018 ± 0.012
CBC3.1	0x00	0.010 ± 0.006

For many of the flipped bits, the default and the last written value were the same, thus indistinguishable, but 72 events were consistent with bit-flips to the last written value, while 31 events were consistent with bit-flips to the default value. All of the four SEUs which were not consistent with either a flip to the default or last written value were single 1→0 bit-flips.

In total, 47 SEUs were observed in 4.76 h when the last written value was 0xff, while only 3 SEUs were observed in 5.00 h when the last value was 0x00, a ratio of 16.5, with a large statistical error because of the small number of 0x00 SEUs. Of the 3 events, 2 are single bit-flips while the third is an 8-bit transition from 0xff to 0x00.

The expected SEU rate in CMS at the HL-LHC can be calculated for different choices of the last written value, Table 6. By choosing a value of 0x00, it should be possible to operate in CMS with an SEU rate of 0.010 ± 0.006 $CBC^{-1}h^{-1}$.

8. Operation in CMS

Although SEUs in CMS at HL-LHC may be more troublesome than in the past, there is no specification for an acceptable rate, and SEU effects will in any case depend on the specific consequences for the affected ASIC and its location. The impact of SEUs may be most strongly felt on control functions, rather than on data corruption, which has been demonstrated by these measurements to be trivial for the CBC. An upset affecting the stored value of the latency or read or write counters would force that chip out of synchronisation and corrupt the data until the correct values have been restored. However, many chips would need to go out of sync before there is a noticeable effect on data quality, given the redundancy in the track finding, and the large number of tracks being measured in each interaction.

It is difficult to be guided by experience from the present tracker. SEUs were not explicitly monitored during data taking, except by counting the front-end ASICs which went out of sync during a run. However, this was difficult to correlate with luminosity, since global CMS resets were issued during data taking in response to unexpected conditions in a wide range of sub-systems which had not been foreseen.

In future, it seems wise to monitor the status of the registers on (all) the ASICs to keep a record of the rate of SEUs, and react if required. About twenty CBC registers have a global effect on the chip, and hence they could be checked regularly at a low rate. It would not be useful to continuously monitor the 254 threshold offset values, which affect only a single channel, but the pipeline logic could easily be monitored, e.g. at ∼1 Hz.

Checking the register contents requires an I^2C read transaction, which takes about 40 μs at the 1 MHz I^2C clock frequency. There are 7,680 2S-modules in CMS [5], each containing 16 CBC chips, so 122,880 CBCs in total. An upset rate of 0.01 SEU $CBC^{-1}h^{-1}$, monitoring 20 of the 338 registers, implies 0.02 registers s^{-1} in the entire system would require a reset. This can easily be accomplished by rewriting the value at a convenient moment in data taking, e.g. every few minutes.

9. Conclusions

SEU tests have been carried out on several versions of the CBC readout ASIC. In the final version, the CBC3.1, no pipeline logic error was observed in the equivalent of 11 days of continuous operation in CMS at the HL-LHC and gives a 99% Poisson upper limit of 0.017 SEU $CBC^{-1}h^{-1}$.

At the HL-LHC 2.2×10^{-11} fake hits per channel, for each triggered readout, are inferred from the measurements, compared with an expected occupancy of 1%–2%. Three SEU events were observed in I^2C registers in the equivalent of 903 h, or 38 days, of HL-LHC operation, providing the last value written to an I^2C register on the chip was set to be 0x00, which is a rate of 0.010 ± 0.006 $CBC^{-1}h^{-1}$.

SEU rates should be monitored in the experiment in future. Only a handful of I^2C registers have a significant effect on the chip. Checking their contents, and correcting when necessary, can be undertaken at a very low rate with no impact on data taking.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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