

CBC3 and CBC3.1 progress

- Imperial College London
Johan Borg, Kirika Uchida, Geoff Hall
- Rutherford Appleton Laboratory
Mark Prydderch

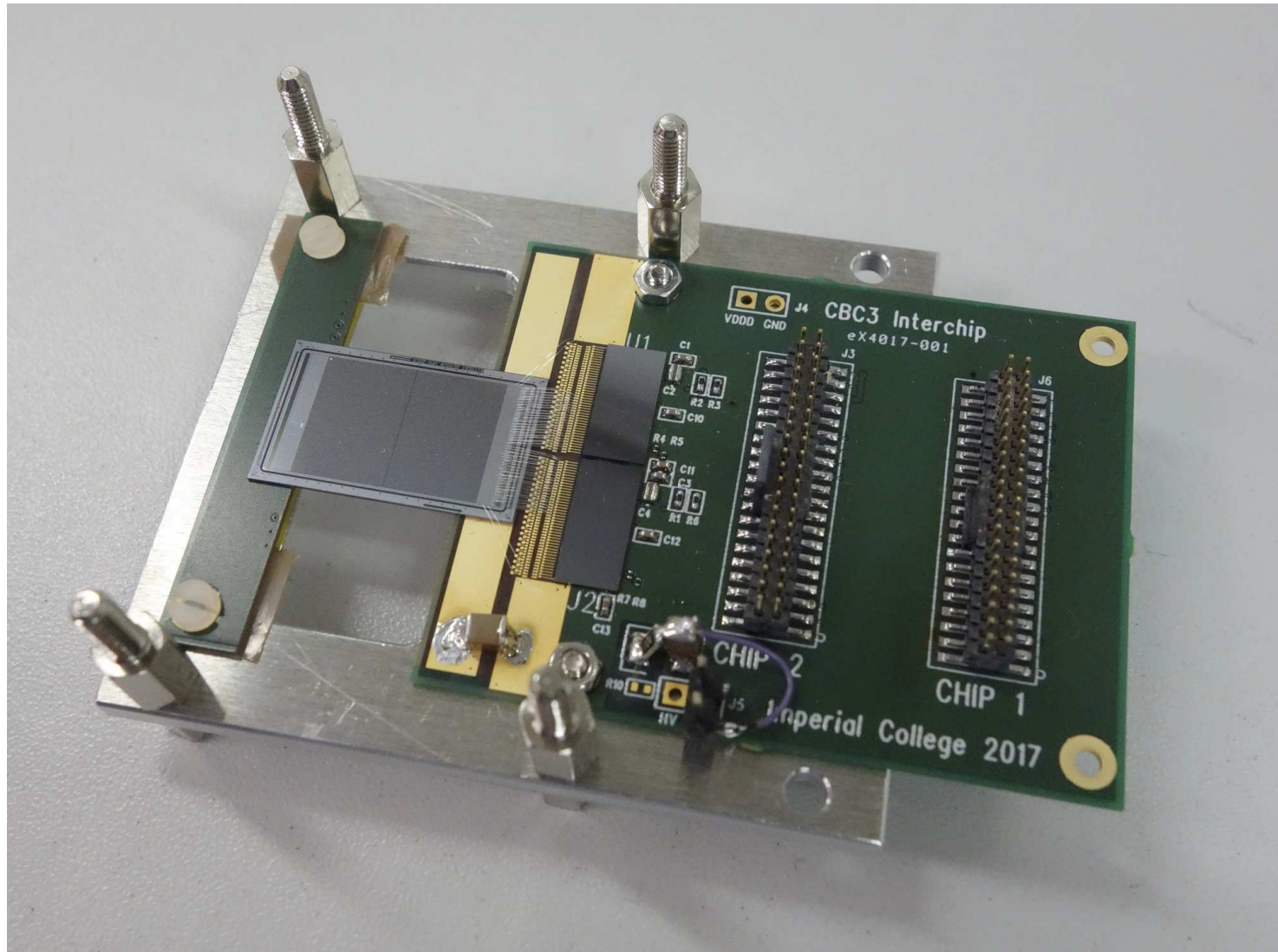
Documents

- 🔗 CBC3 documentation archive:
<http://www.hep.ph.ic.ac.uk/ASIC/>
- 🔗 Recommended CBC3 settings:
<http://www.hep.ph.ic.ac.uk/ASIC/cbc3/cbci2c/>

Progress

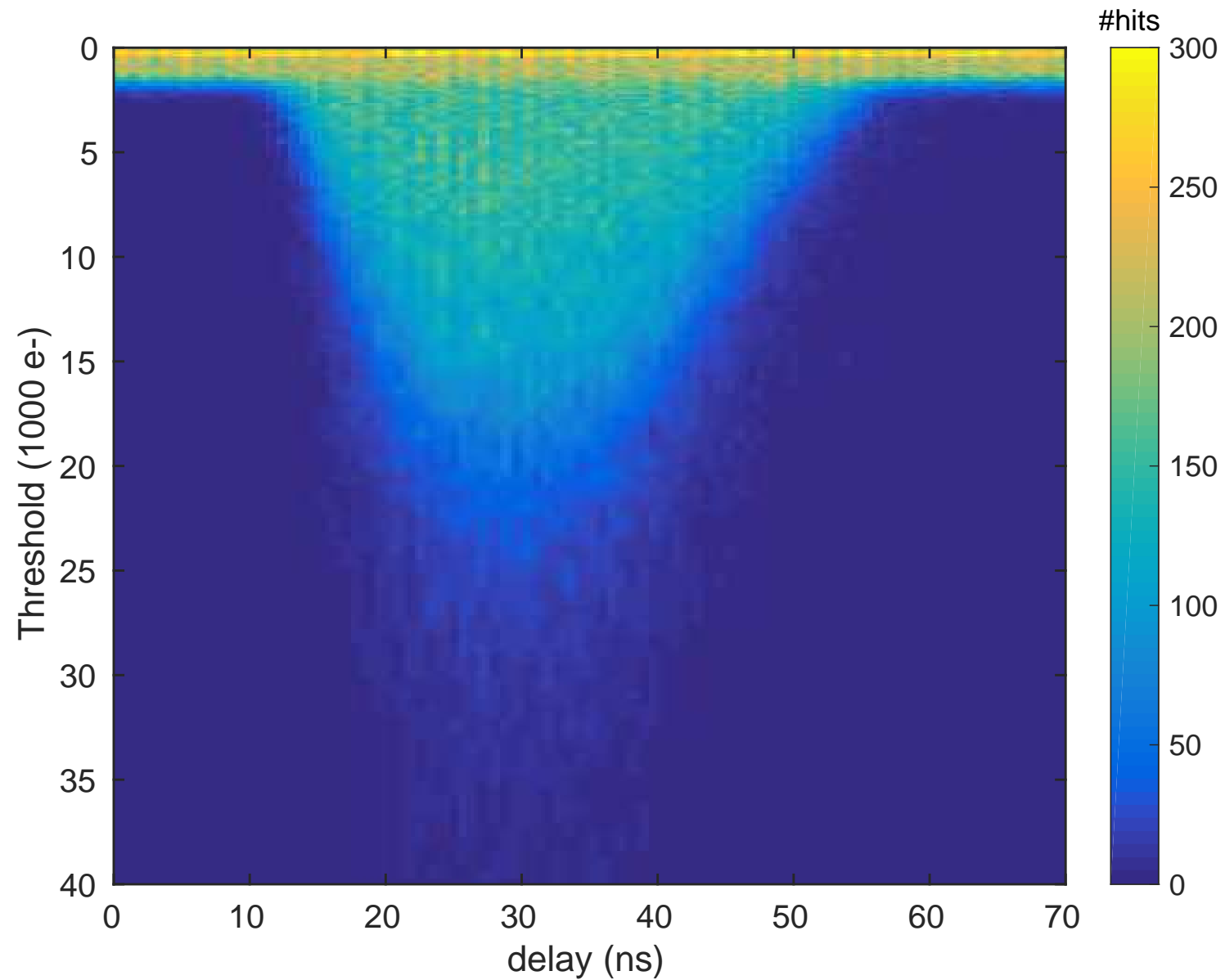
- Wafer testing using FC7s
 - Good progress
- CBC3.1
 - All planned changes except improved SEU tolerance of I2C registers implemented
 - Top level simulations running
 - Final design review in November
 - Submission for manufacturing planned for January 2018
- CBC3 on PCB modules
 - Less expensive, 3 week turnaround but reduced functionality (2/3rds of the channels) CBC3 modules using regular PCBs for misc. tests.
 - Assembled in-house using a BGA rework station
 - Initial beamtest of single-sensor module with Pions completed, Xe ion run commencing today

CBC3s on PCB module

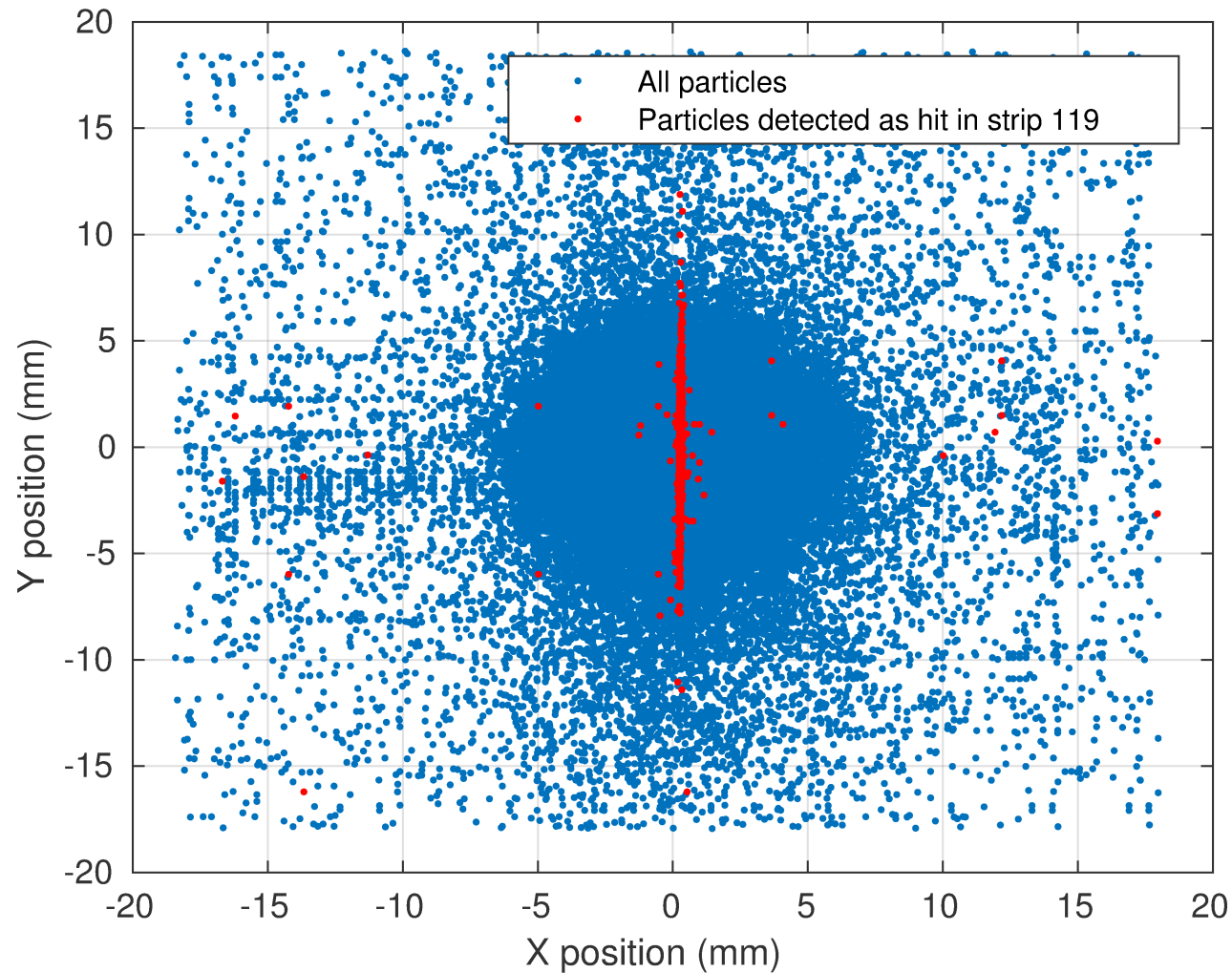


We are most grateful to Marko Dragicevic, Alex König and Marius Metzler for supplying sensors

Hits vs threshold and particle arrival time (sample mode)



Telescope integration



We are most grateful to the UA9 collaboration for the beam and telescope data