Signal I/O timing of CBC for CIC development

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Signal data with timing information

- To emulate CBC, fast signal sequences are created, sent to CBC, and data on 5 slvs lines are recorded real time.
- Sequencer and raw data buffer developed for wafer probing system is used.

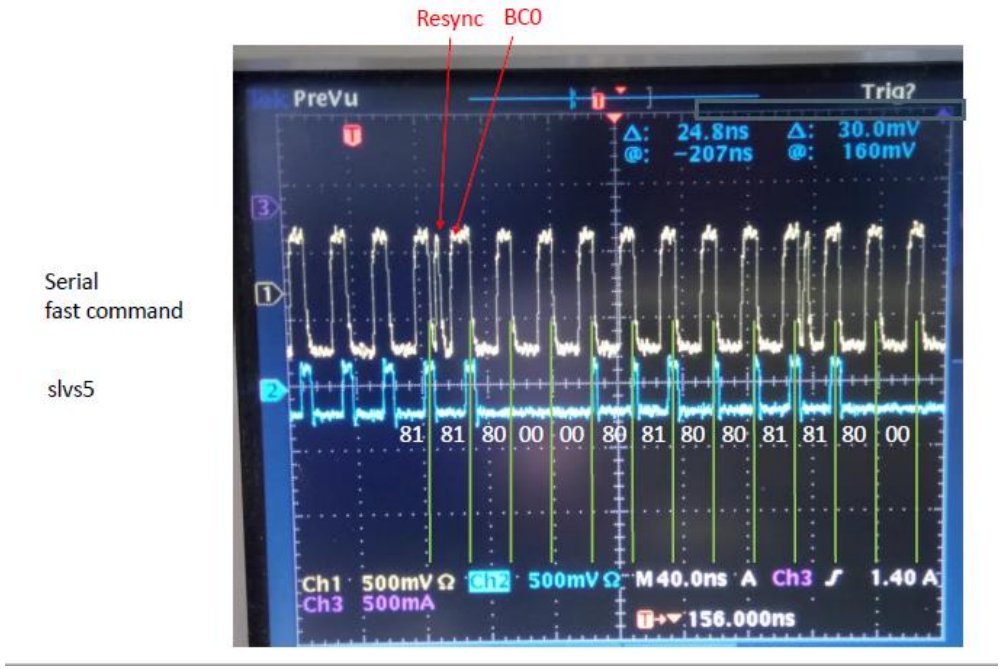
Data in text format

```
UNMASKED CHANNELS : 1   2  35  34 251 254
------------------
a0010200 #seq com. rdb recording trigger
a0011000 #seq com. fast reset
a0080000 #seq com. no signal for 8 BX
a0011000 #seq com. fast reset
e0000000
------------------
00000000 02 24 fc f0 81 00
00000001 02 24 fc f0 81 00
00000002 02 24 fc f0 81 00
00000003 02 24 fc f0 81 00
00000004 02 24 fc f0 81 00
00000005 02 24 fc f0 81 00 #fci : fast reset
00000006 00 00 c0 c0 80 00 #fci : no signal
00000007 00 00 00 00 00 00 #fci : no signal
00000008 00 00 00 00 00 00 #fci : no signal
00000009 00 00 00 00 80 00 #fci : no signal
0000000a 02 24 fc f0 81 00 #fci : no signal
0000000b 00 00 00 00 80 00 #fci : no signal
0000000c 00 00 00 00 80 00 #fci : no signal
0000000d 02 24 fc f0 81 00 #fci : no signal
0000000e 02 24 fc f0 81 00 #fci : fast reset
0000000f 00 00 c0 c0 80 00
00000010 00 00 00 00 00 00
00000011 00 00 00 00 00 00
00000012 00 00 00 00 80 00
00000013 02 24 fc f0 81 00
00000014 00 00 00 00 80 00
00000015 00 00 00 00 80 00
00000016 02 24 fc f0 81 00
00000017 02 24 fc f0 81 00
00000018 02 24 fc f0 81 00
00000019 02 24 fc f0 81 00
0000001a 02 24 fc f0 81 00
0000001b 02 24 fc f0 81 00
```

A command for sequencer / line in hex.
Each command is processed within a single 40MHz.
The 3 most significant bits (101) is for fast signal.
In this example, the second fast reset is sent at 9th BX after the first one.

Recorded raw data in hex.
Line number (BX index?), SLVS1, SLVS2, SLVS3, SLVS4, SLVS5, SLVS6 from the left to the right.
Rdb recording trigger start recording output of iserdes.

The comments show the fast command comes into CBC at the same time as the CBC output data in the same line comes out as shown in the picture.
There are little delays everywhere, so I decided just to check on the scope.



Another example

In this example, 1 stub is created with channel mask and test pulse. The single BX stub is observed. Trigger is sent after a proper latency and L1 raw data show the test pulse data.

```
Trigger is sent 11+2 clock cycle after the fast reset
I2C : Trigger latency  = 2
I2C : VCTH             = 590
I2C : Test pulse group = 1
-----------------
UNMASKED CHANNELS :   3(g1) 4(g1) 35(g1) 34(g0) 251(g5) 254(g6)
-----------------
a0010200 #seq com. rdb recording trigger
a0011001 #seq com. fast reset & orbit reset
a0070000 #seq com. no signal for 7 BX
a0010010 #seq com. test pulse request
a0040000 #seq com. no signal for 4 BX
a0010100 #seq com. trigger
e0000000
-----------------
00000000 00 00 00 00 80 00
00000001 00 00 00 00 80 00
00000002 00 00 00 00 80 00
00000003 00 00 00 00 80 00
00000004 00 00 00 00 80 00
00000005 00 00 00 00 80 00 #fci : fast reset & orbit reset
00000006 00 00 00 00 80 00 #fci : no signal
00000007 00 00 00 00 00 00 #fci : no signal
00000008 00 00 00 00 00 00 #fci : no signal
00000009 00 00 00 00 80 00 #fci : no signal
0000000a 00 00 00 00 80 00 #fci : no signal
0000000b 00 00 00 00 80 00 #fci : no signal
0000000c 00 00 00 00 80 00 #fci : no signal
0000000d 00 00 00 00 80 00 #fci : test pulse request
0000000e 00 00 00 00 80 00 #fci : no signal
0000000f 00 00 00 00 80 00 #fci : no signal
00000010 00 00 00 00 80 00 #fci : no signal, test pulse peak at comparator, 11 clock cycle after the fast reset, written at pipeline address 7
00000011 00 00 00 00 80 00 #fci : no signal
00000012 00 00 00 00 80 00 #fci : trigger <- 13 clock cycle after the fast reset.
00000013 00 00 00 00 80 00
00000014 00 00 00 00 80 00
00000015 00 00 00 00 80 00
00000016 04 00 00 00 80 00 #slvs1 : stub for the test pulse <- 6 clock cycle after the test pulse at comparator
00000017 00 00 00 00 80 00
00000018 00 00 00 00 80 00
00000019 00 00 00 00 80 00
0000001a 00 00 00 00 80 c0 #slvs6 : L1 Raw data starts
0000001b 00 00 00 00 80 38 #slvs6 : pipeline address = 7
0000001c 00 00 00 00 80 04 #slvs6 : level 1 counter = 1
0000001d 00 00 00 00 80 c0 #slvs6 : 3 & 4 channel hits
0000001e 00 00 00 00 80 00
0000001f 00 00 00 00 80 00
00000020 00 00 00 00 80 00 #slvs6 : no hit on channel 34, since this channel is in test pulse group 0.
00000021 00 00 00 00 80 80 #slvs6 : 35 channel hit
00000022 00 00 00 00 80 00
00000023 00 00 00 00 80 00
00000024 00 00 00 00 80 00
00000025 00 00 00 00 80 00
00000026 00 00 00 00 80 00
00000027 00 00 00 00 80 00
00000028 00 00 00 00 80 00
00000029 00 00 00 00 80 00
0000002a 00 00 00 00 80 00
0000002b 00 00 00 00 80 00
0000002c 00 00 00 00 80 00
```