CBC 3.1 status

Johan Borg, Mark Prydderch, Kirika Uchida

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CBC 3.1 manual

- New manual is uploaded at http://www.hep.ph.ic.ac.uk/ASIC/cbc3.1/CBC3p1_User_Manual_V1p3.pdf

  Changes
  - Clarification of the channel data order.
    (No additional information, but clear statement for no reordering is added.)
  - Section on ‘Further Reading’ added with list of publications.

  Please contact Mark Prydderch (mark.prydderch@stfc.ac.uk) for comments on the manual.

New CBC 3.1 wafer probe test system

Main changes

- Backend electronics : VME to µTCA (One FC7).
- Wafer probe station control, CBC test software including power supply and multimeter control are running on Linux machine.

Test menu

- Stuck bits test on all I2C registers,
- VDDD & VLDOI currents check,
- bandgap tuning, bandgap & chip ID fuse blowing,
- offset tuning, VCTH scan for pedestal & test pulse acquiring s-curves and gains,
- pipeline check, buffer ram check,
- channel masking check,
- check for stubs; addresses, cluster width discrimination, layer swap, pT window limits, pT window offsets,
- Hit detection and HIP suppression logic check,
- fast command interface delay function check,
- DLL test,
- sweep and measure bias voltages and currents,
- all AMUX parameter measurement.
- DVS (dynamic voltage screening) and EVS (enhanced voltage screening)
  <- has not been done. Might be implemented for the next test.

Performance

~ 40 sec / chip including moving wafer to the next chip. -> fast enough for production phase.
2 or 3 wafers / day, ~ half a year for 300 wafers.