CBC3 status report

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06.11.2018

Since 18th in September

CBC3.1

18.09
13 CBC3.1 wafers arrived.
Wafer testing for CBC3.1 started.

22.10
Some good dies came back to IC.
Single & two CBC modules are made.

21.09
Two wafers were shipped to RAL and sent to Novapack for dicing.

12.11-18.11
TID test

- No problem has been seen in the changes from CBC3.0 to CBC3.1. Some corrections and improvements are verified and summarized in Johan's slides, https://indico.cern.ch/event/752963/contributions/3186614/attachments/1740415/2816127/ote_oct18.pdf
- SEU test will be in early next year.

06.11
Today

CBC3.0

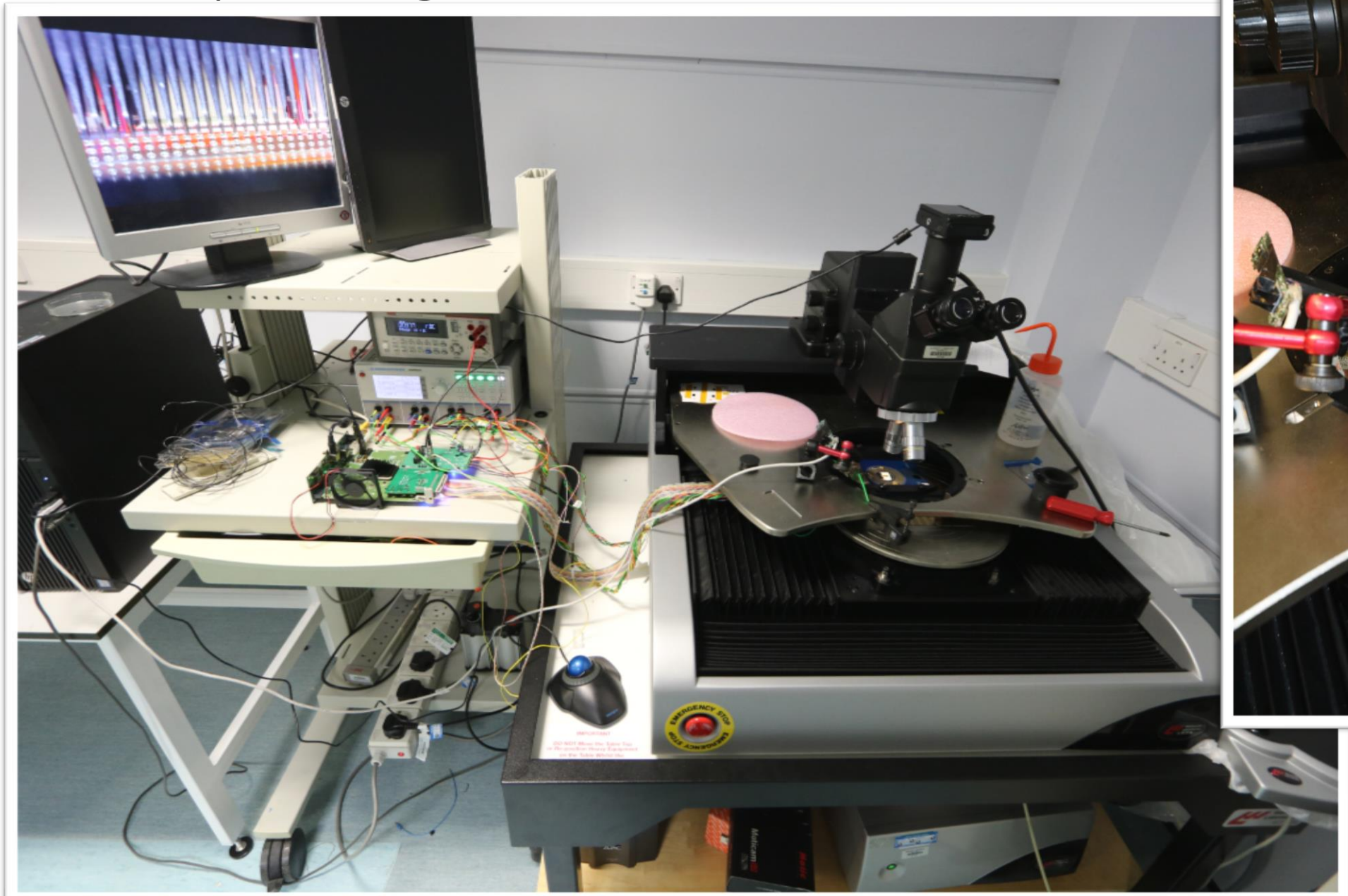
21.09
24 wafers arrived and wafer test started.

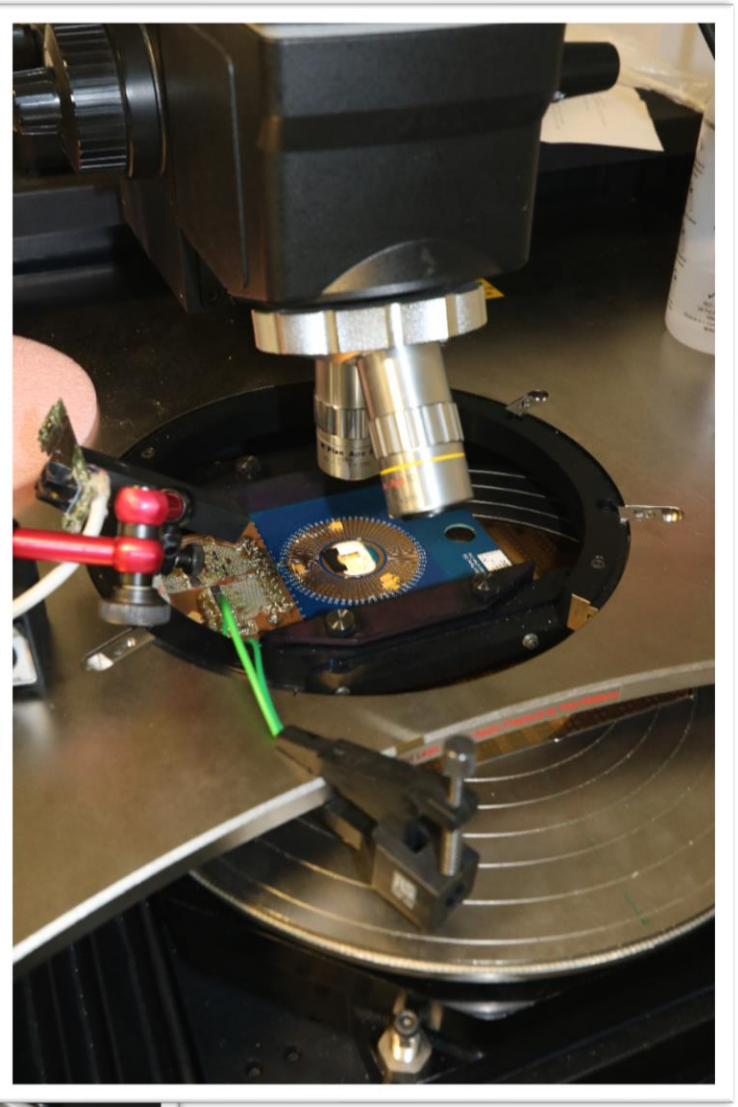
01.10
23 wafers were shipped to CERN.

- Post wafer testing analysis is still going on.

Wafer testing

Wafer probing station





Wafer test procedure

Default I2C main bias settings : default in wafer test.
Number of I2C r/w : ~ 60K < 2.4 sec between CBC & BE
Total testing time ~ 30 sec / chip
(The large contributions are indicated in purple brackets.)

Power on

- CBC reset, CBC I2C response check, Iserdes timing tuning for CBC output data on SLVS lines
- Stuck bit test on main bias setting I2C registers

Default I2C main bias settings

- Current check
- SLVS6 data check. (The header is searched for.)
- Stuck bit test on I2C registers; bend LUTs, channel offsets, channel mask, Nearest Neighbour hits

Main bias settings are chosen to give low currents

- Bandgap tuning, bandgap and chip ID register fuse blowing (2 sec)

Default I2C main bias settings with stub suppressed

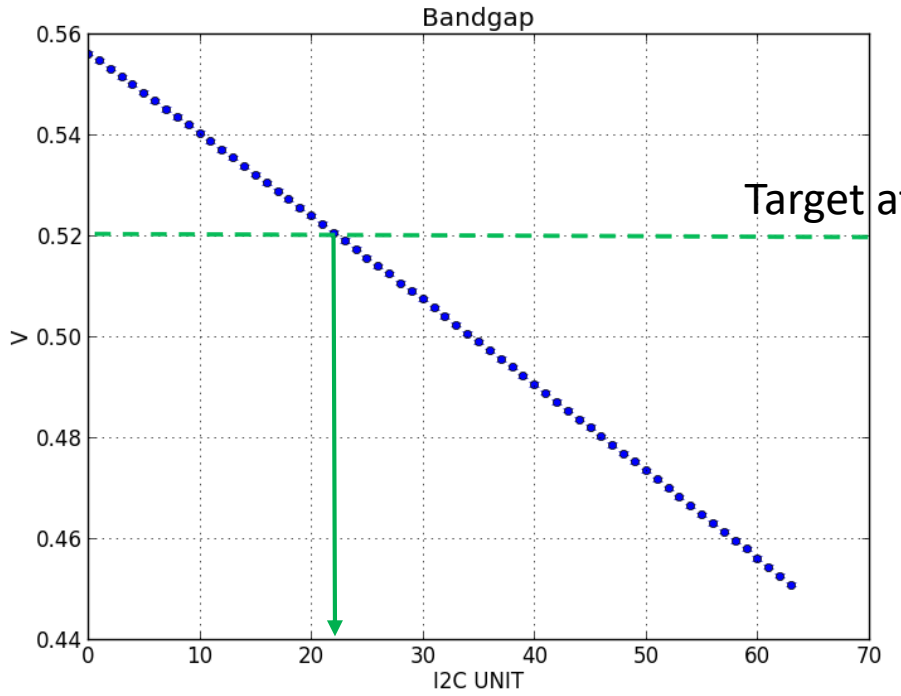
- Offsets and pedestal tuning. S-curve check for pedestal and test pulse, gain check. (10 sec)

Default I2C main bias settings and tuned offset values

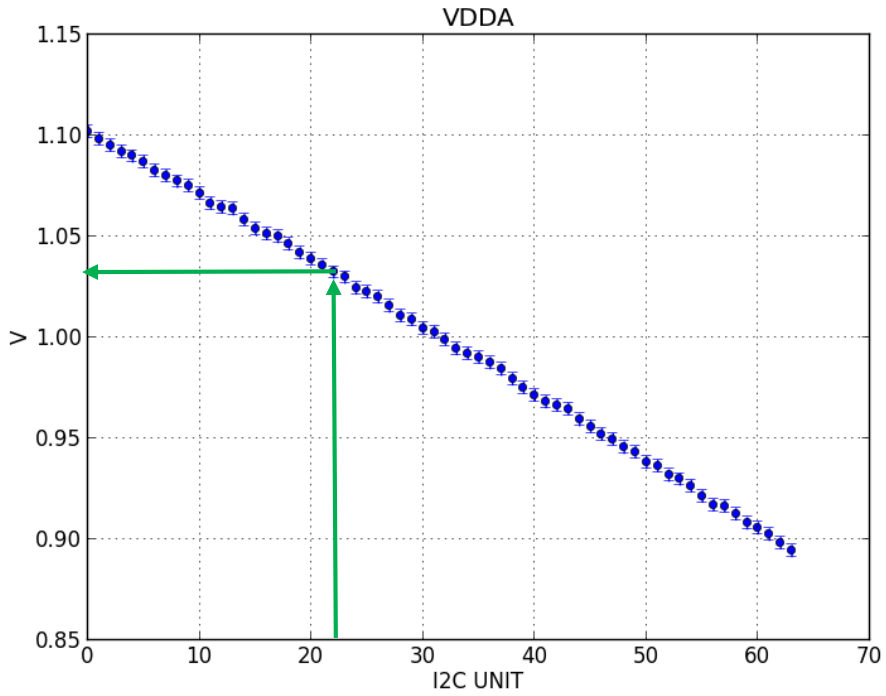
- Pipeline, buffer rams, channel mask, stubs, (2 sec)
- Hit detection and HIP suppression,
- FCI delay (to be changed to use edge selection),
- CLK40 DLL
- Sweep settings and measure the bias voltages and currents settings with VCTH = 0 (No hit is created. Except for VCTH scan) (7 sec)
- Measure all individual AMUX parameters (VCTH=400. No hit, 30.947 s) wait values have settled to 0.5% (6 sec)

Bandgap scan

- Bandgap voltage is read from AMUX output of CBC3.
- VDDA must be exactly twice of the bandgap, but there is a contact resistance with the needle and the pad on CBC in the probing environment.
  Measured VDDA is required to be +/- 10% from the expected optimal value.



Target at 0.52 V



The I2C setting value for the target bandgap is programmed into a set of 6 e-Fuses.

Offsets & pedestal tuning, pedestal & test pulse s-curve, gain check

- Offset tuning

  No valid value check is done.

- Pedestal & test pulse (60 [I2C unit] ~ 5 fC) S-curve check

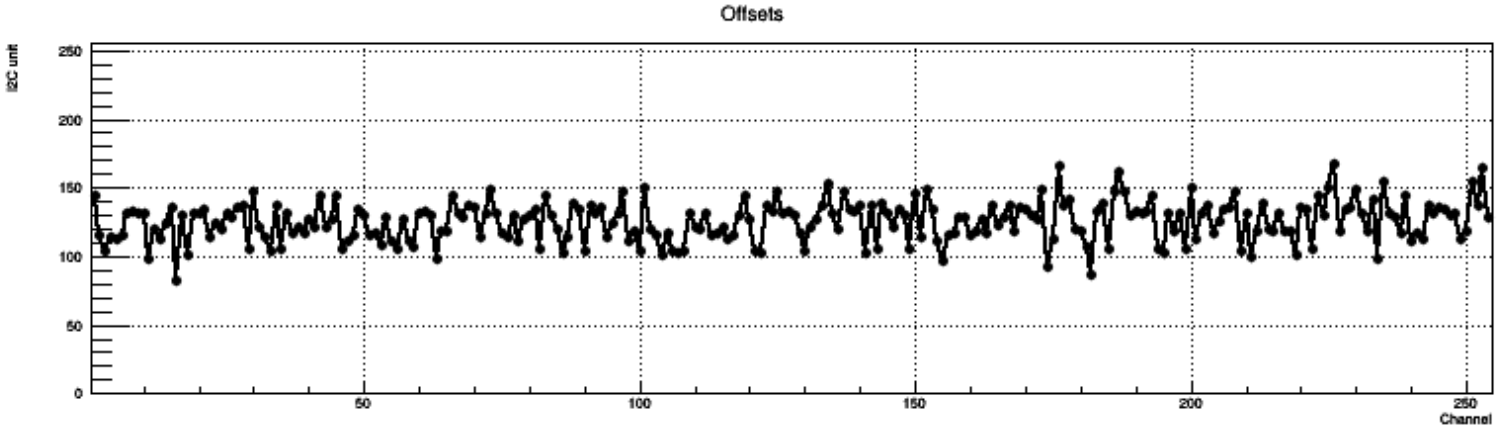
  S-curve fit must be successful.

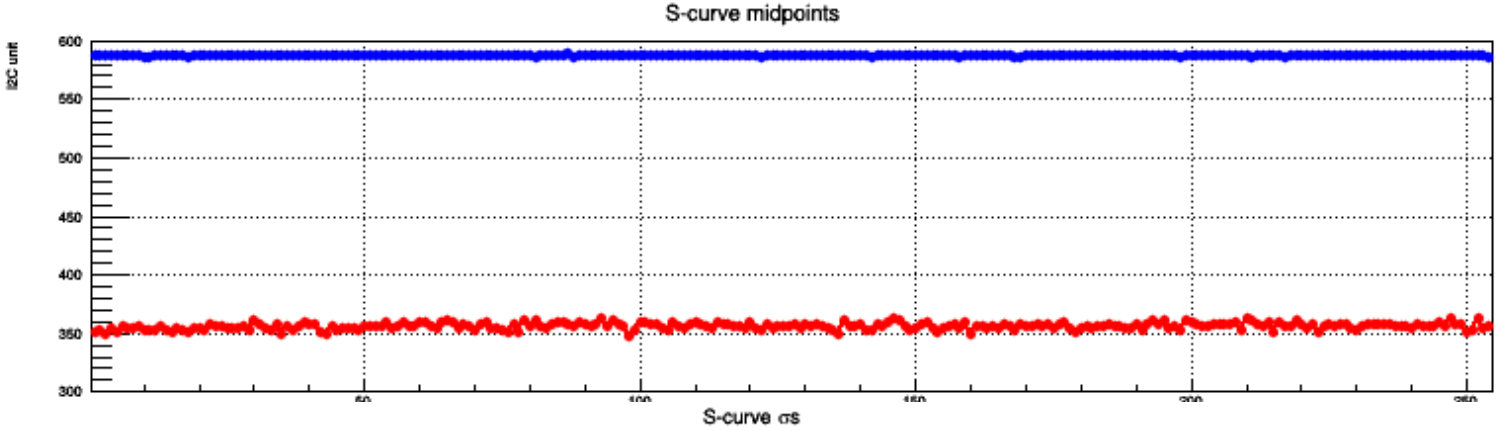
  No parameter check is done.

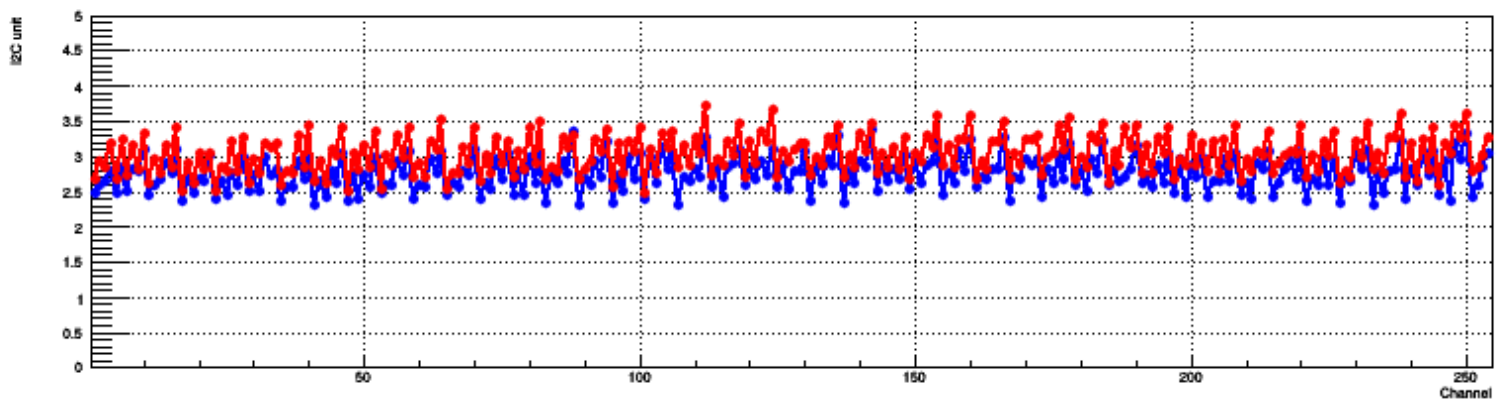
- Gain check

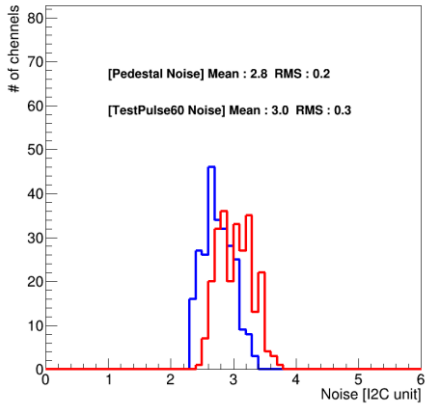
  Each channel’s gain to be < mean +/- 20 (~10%).

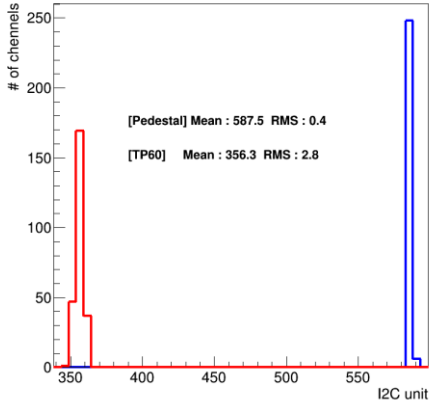
Offsets & pedestal tuning, pedestal & test pulse s-curve, gain check – good chip

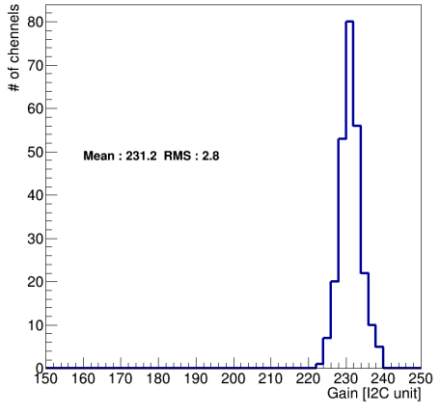










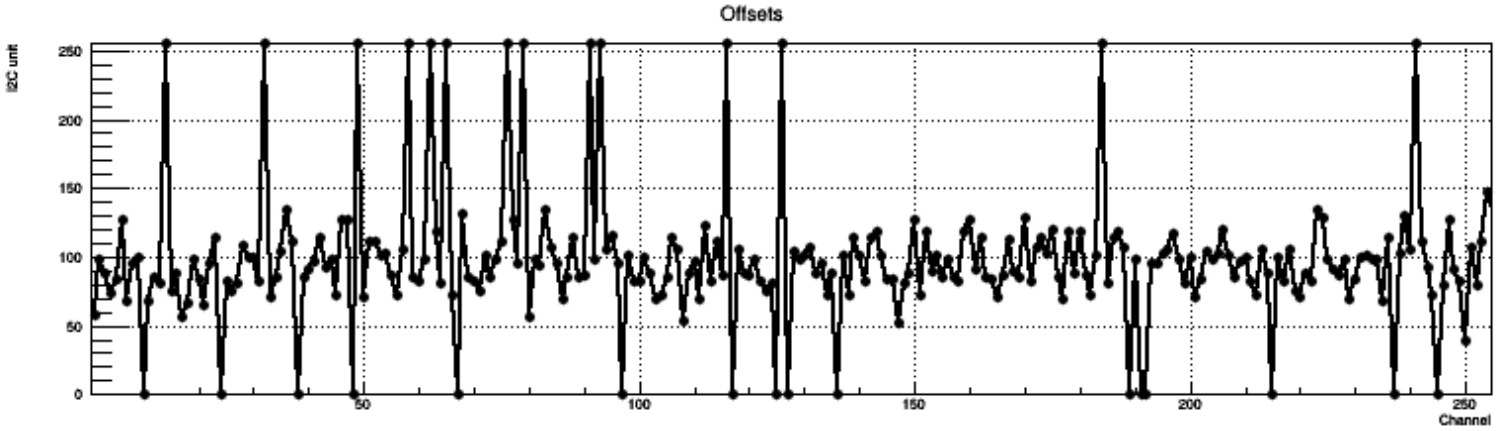


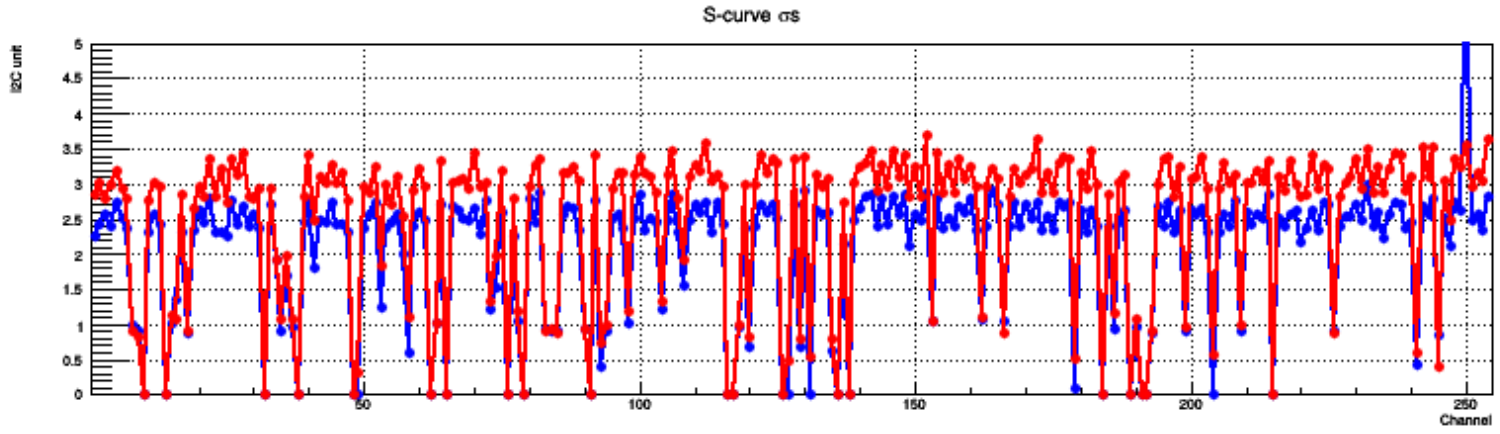
Test pulse ~5fC

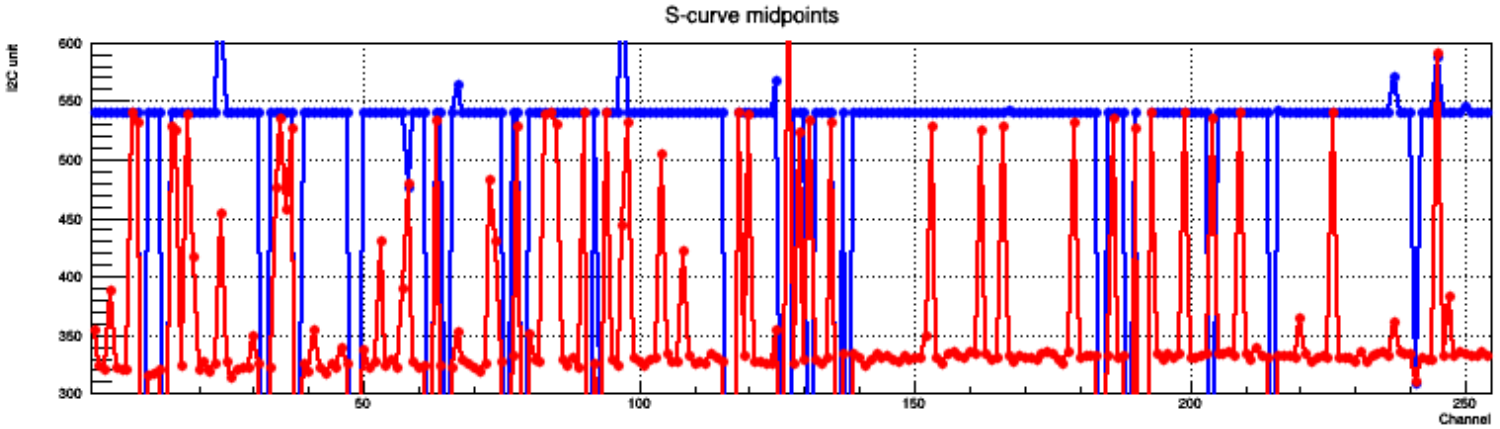
Requirements for all channels,

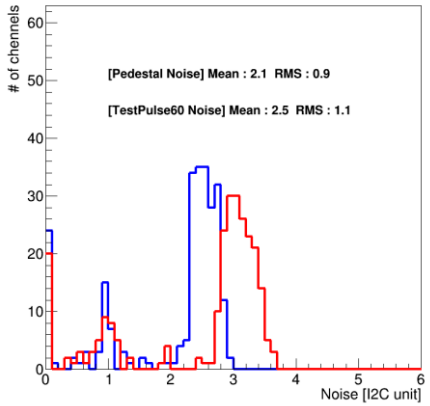
- ✓ S-curve fit should be successful,
- ✓ Gain must be < mean +/- 20 (~10%)

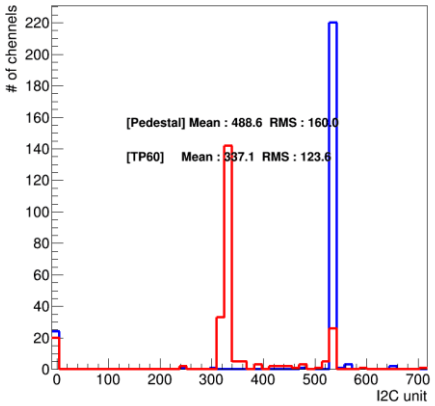
Offsets & pedestal tuning, pedestal & test pulse s-curve, gain check – bad chip

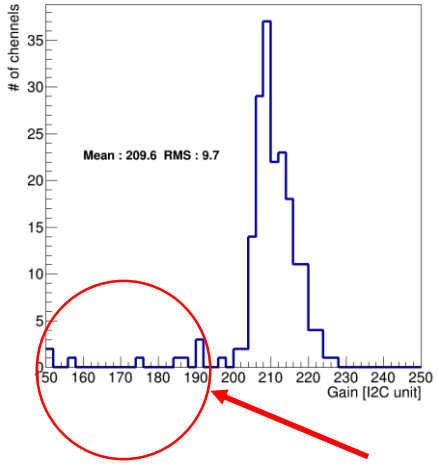












Test pulse ~5fC

This chip is rejected by these channels

Requirements for all channels,

- ✓ S-curve fit should be successful,
- ✓ Gain must be < mean +/- 20 (~10%)

This chip does not satisfy this requirement.

Pipeline and buffer check

- Pipeline

  Check all pipeline space. 512 set of channel hits, for both 0 & 1.

  Pipeline address can be controlled by the distance from fast reset to L1 trigger.

- Buffer

  32 consecutive triggers are sent so that data from all 32 buffers are checked.

  - Hit data & error bits(0) are checked with two sets of the 32 consecutive triggers for hit 0 & 1.
  - 512 pipeline addresses are created for all buffers, 32 x 512 triggers are sent changing the time distance of the fast reset and L1 triggers.
    For CBC3.0, this test sometimes fails for having invalid pipeline address for some small amount of data. Might be a problem of timing for the data passing through the different clock domain.
  - All 512 L1 counter values are created for all 32 buffers.
    L1 counter values are also broken for some small amount of data for 3.0 which might also be caused by the timing issue.

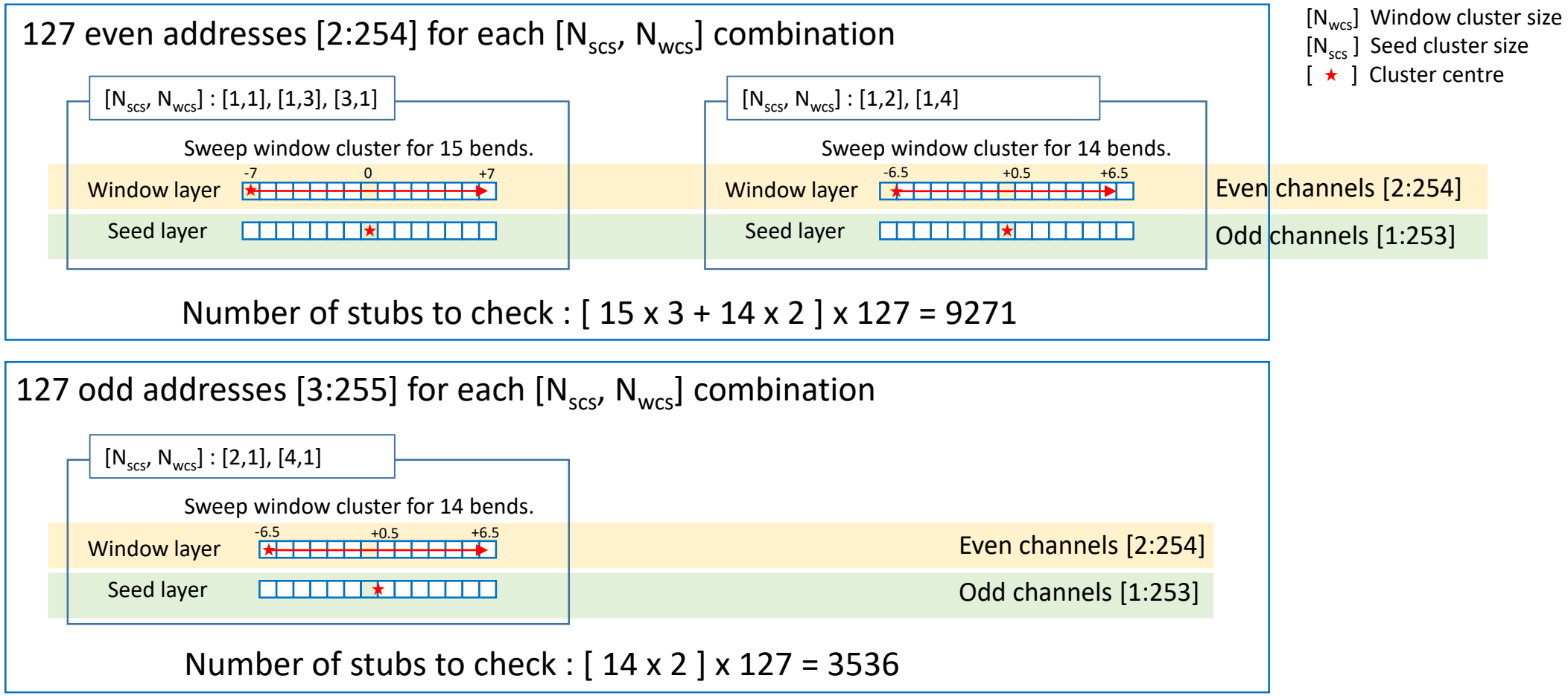
Two CBC3.1 wafers do not have any chip showing this problem ☺

Stub logic check

all stubs are created masking channels

Stub address check

- Combinations of # of strips 1-4 in clusters on seed & window layers, with either cluster width is 1. Swipe through all addresses 2 to 255 for all bends

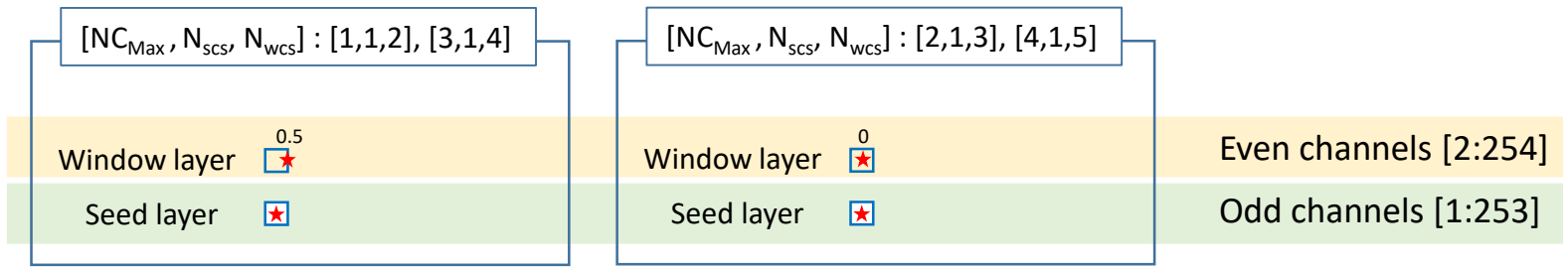


Total number of stubs to check : 12827

Cluster width discrimination

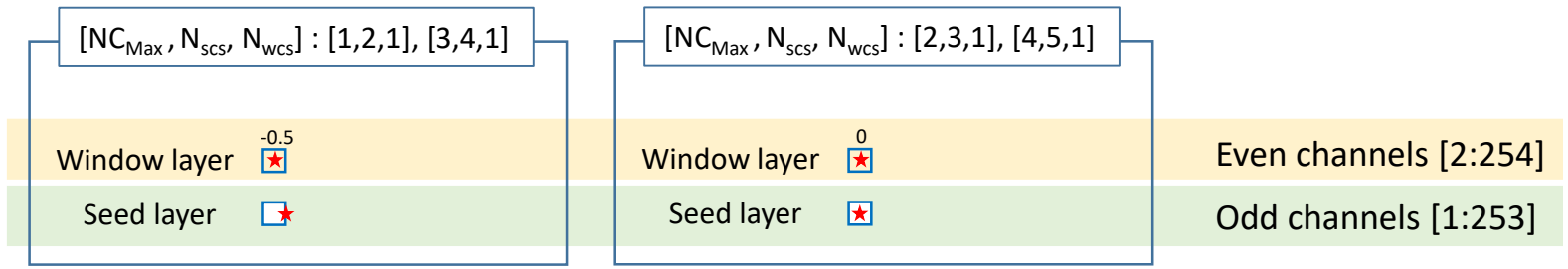
- Keeping one cluster width 1, create the other cluster that width is max. cluster width + 1, changing the max. cluster width to be 1 to 4.

Single strip width cluster on seed layer, 127 addresses for each [NC_{Max} , N_{scs}, N_{wcs}]



Number of stubs to check : [2 + 2] x 127 = 508

Single strip width cluster on window layer, 127 addresses for each [NC_{Max} , N_{scs}, N_{wcs}]



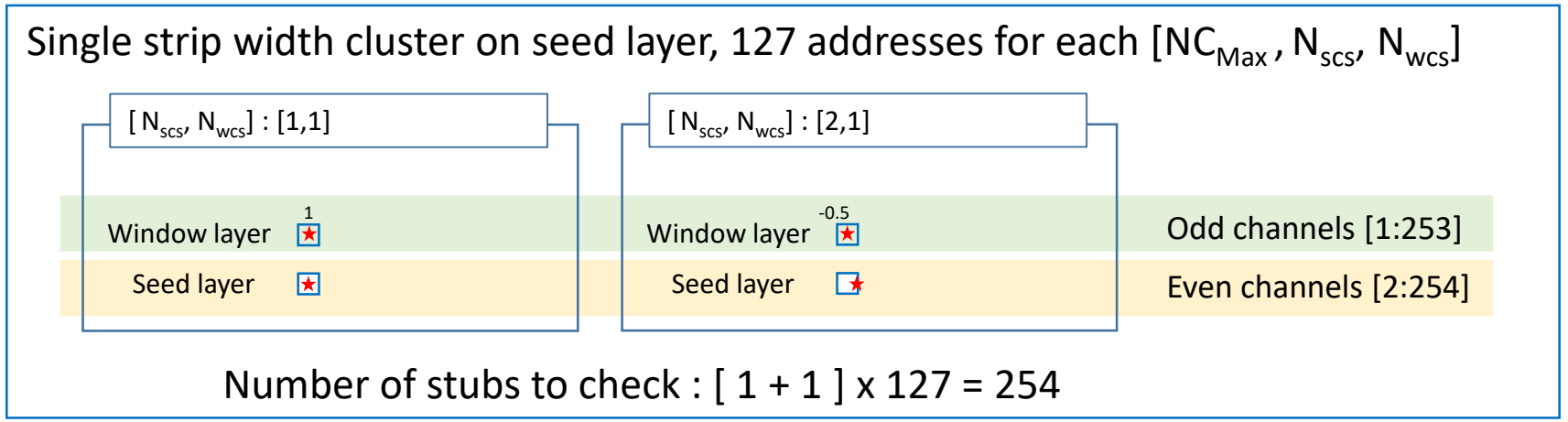
Number of stubs to check : [2 + 2] x 127 = 508

Total number of stubs to check : 1018, but no stub should come out.

[N_{wcs}] Window cluster size
[N_{scs}] Seed cluster size
[★] Cluster centre
[NC_{Max}] Max. cluster width

Layer swap

- With max. cluster width 4, # of strips in window layer 1, the seed clusters are created for all addresses 2 to 255 with 1 or 2 strip clusters and bend is 0 for single strip, -1 for 2 strip clusters for layer swap on. The addresses and bends are checked.



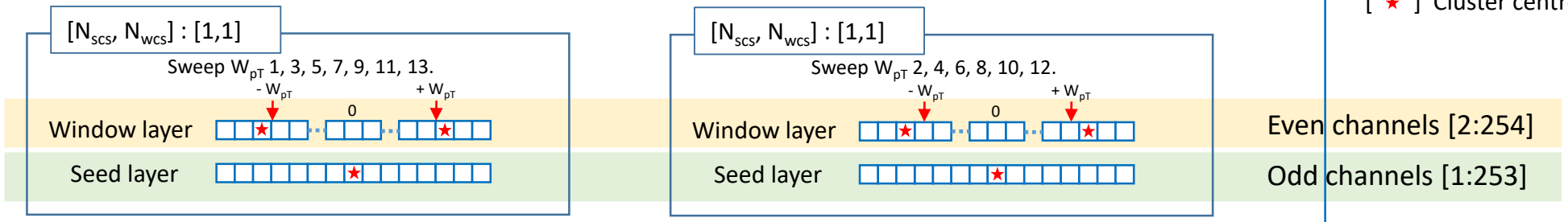
[N$_{wcs}$] Window cluster size
[N$_{scs}$] Seed cluster size
[★] Cluster centre

Total number of stubs to check : 254

Stub pT selection check

- For pT width (W_{pT}) 1 to 13, clusters with 1 or half strip outside the pT width for both bend directions are created for 1 & 2 strip width clusters on seed. Swipe through all addresses 2 to 255 for all bends

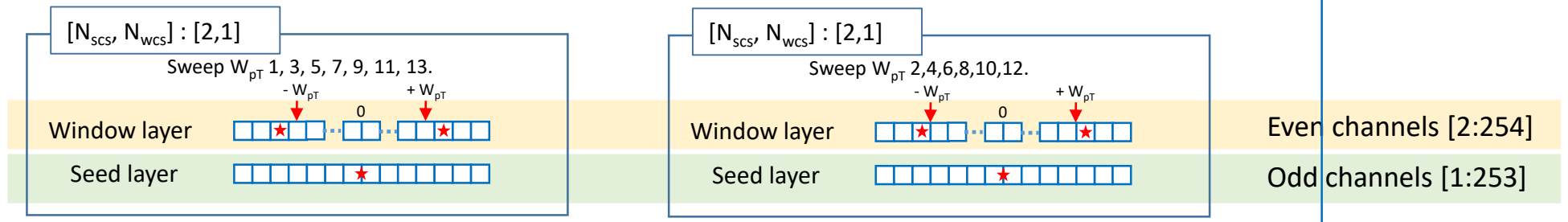
2 stubs for each W_{pT} [1:13] for even addresses [2:254]



Number of stubs to check : [2 x 13] x 127 = 3302

[N_{wcs}] Window cluster size
[N_{scs}] Seed cluster size
[★] Cluster centre

127 odd addresses [3:255] for each [N_{scs}, N_{wcs}] combination

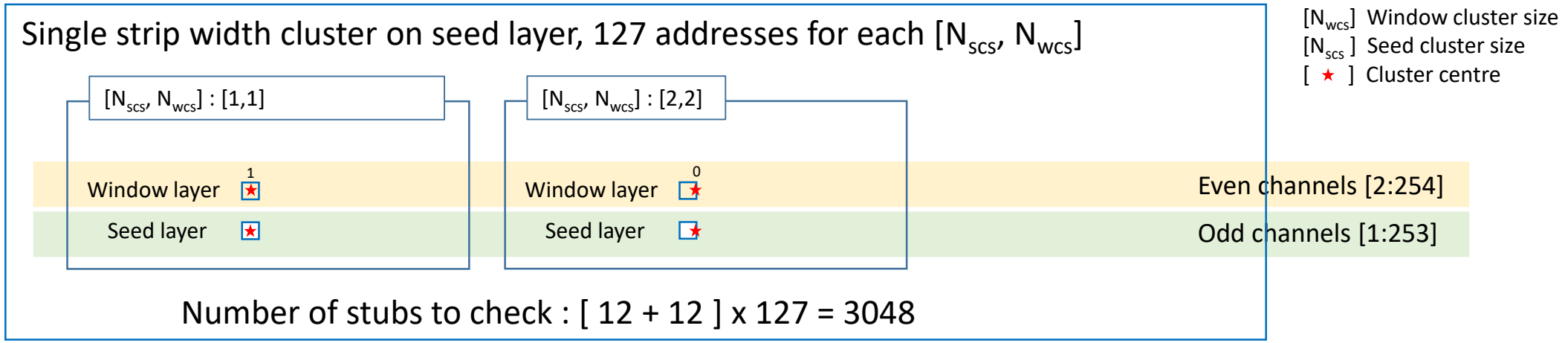


Number of stubs to check : [13 x 2] x 127 = 3302

Total number of stubs to check : 6604, but no stub should come out.

pT Window Offset check

- For all 12 offset values, a pair of clusters on top of each other is created for 2 to 255 address. Consistency of the bend from CBC with the offsets are tested.



Bent LUT table are coded with half strip resolution for the window -3.0 to 3.0 (corresponds to the offset range).

Total number of stubs to check : 3048

HIT detection and HIP suppression

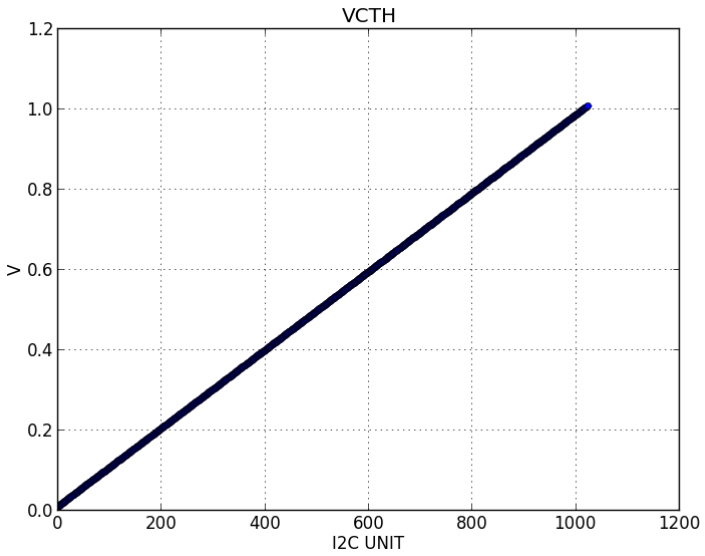
- These are checked different combination of settings for all stub addresses with bend 0 with masking channels.

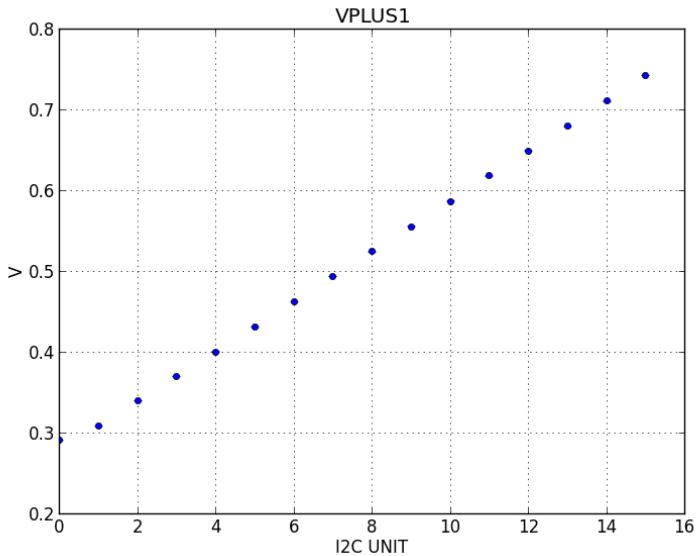
HIP suppression			Pipeline & stub input hit logic	CBC output
Enabled/Disabled	Source	Count		
Disabled	OR	3	SAMPLED	Hits & stubs
Disabled	OR	3	FIXED PULSE WIDTH	No hit no stub
Disabled	OR	3	OR	Hits & stubs
Disabled	OR	3	HIP supp. logic output	Hits & stubs
Disabled	SAMPLED	3	HIP supp. logic output	Hits & stubs
Disabled	SAMPLED	0	HIP supp. logic output	No hit no stub
Enabled	SAMPLED	0-7	HIP supp. Logic output	No hit no stub

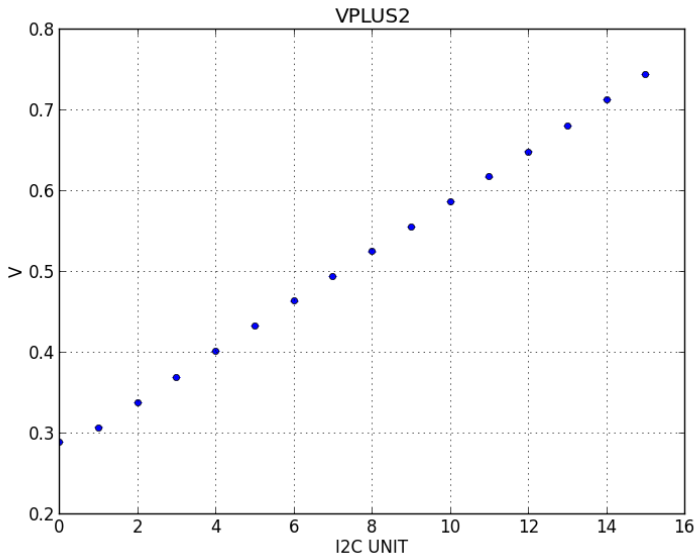
Bias sweep and AMUX readings

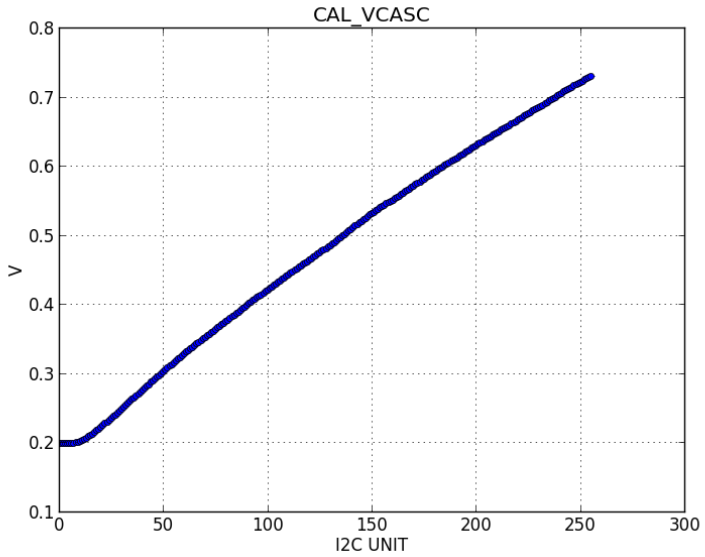
- Sweep and measure bias voltages, VCTH, VPLUS, VPLUS2, CAL_VCASC via Analogue Mux
- Sweep and measure current for IPRE1, IPRE2, IPSF, IPA, IPAOS, ICOMP, CAL_Ibias
- Measure all individual AMUX parameters wait values have settled to 0.5%

Bias Voltage sweep, read from AMUX

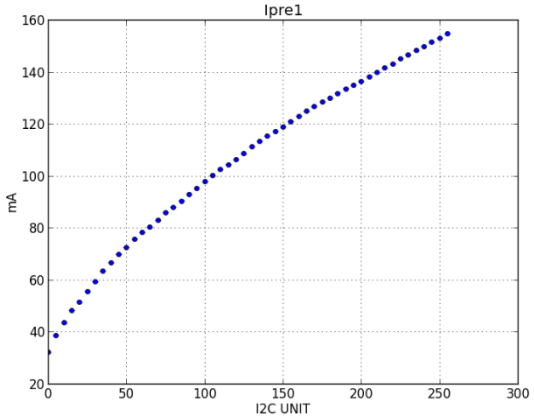


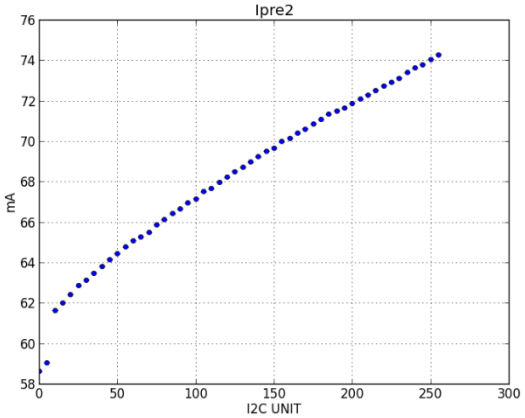


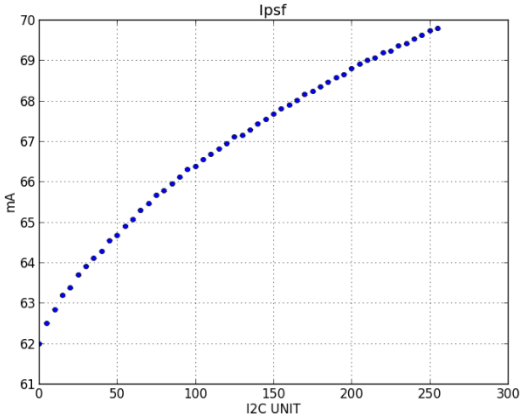


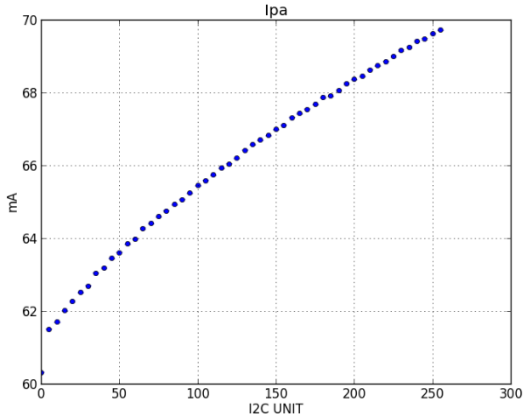


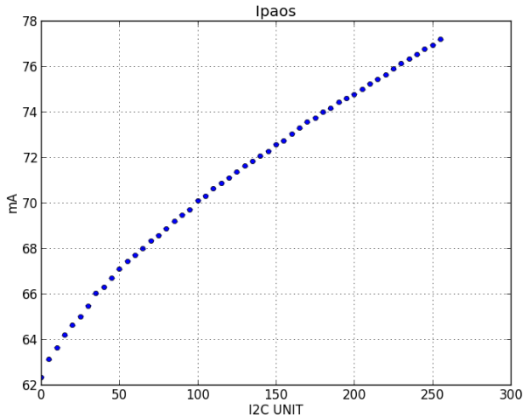
Bias current sweep and current measurement

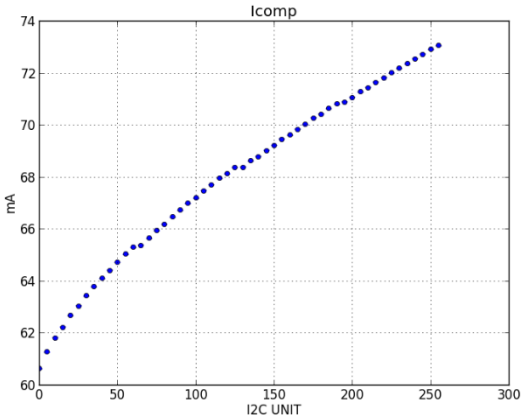


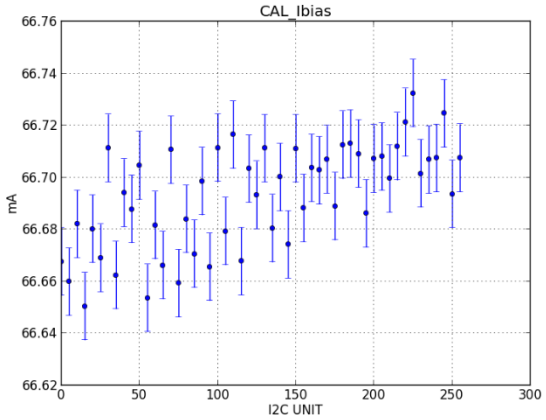






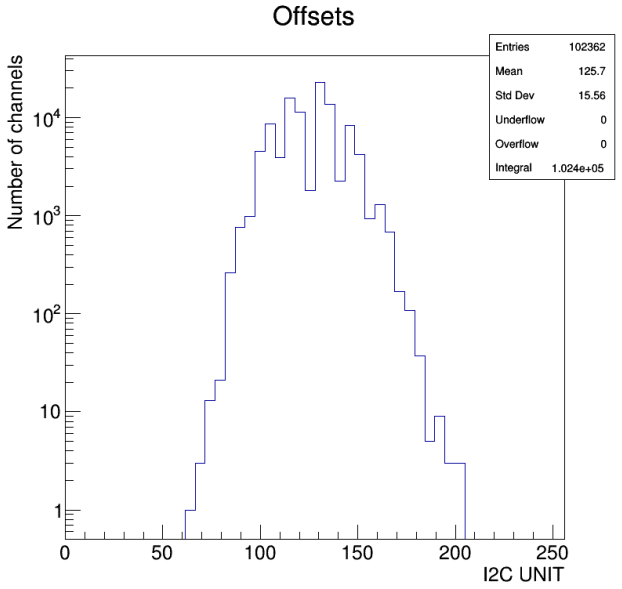


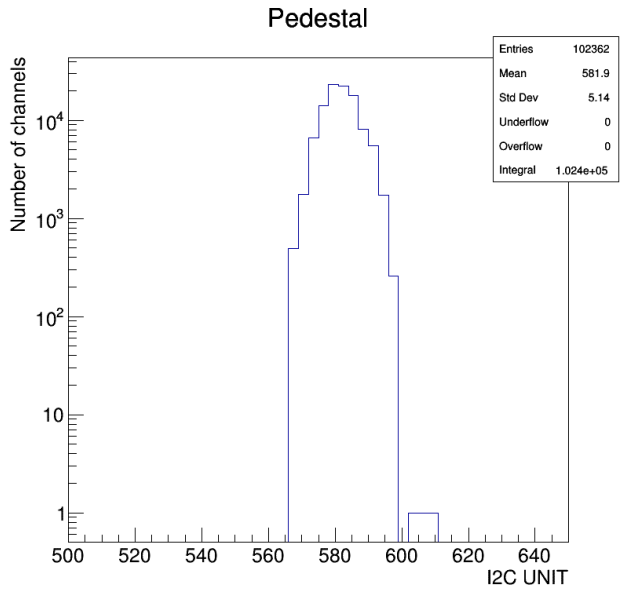


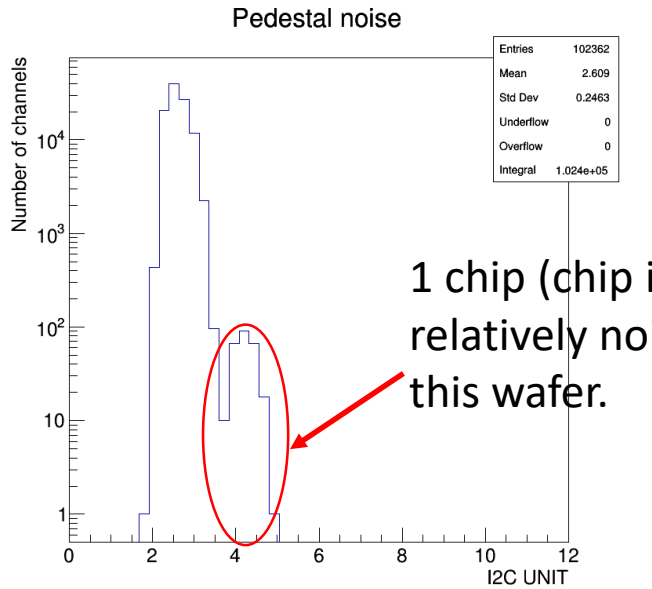


Post analysis on good chips

Offsets, s-curve mid-points & noise from good chips in CBC3.1 wafer A0QIWTH (403 good chips)

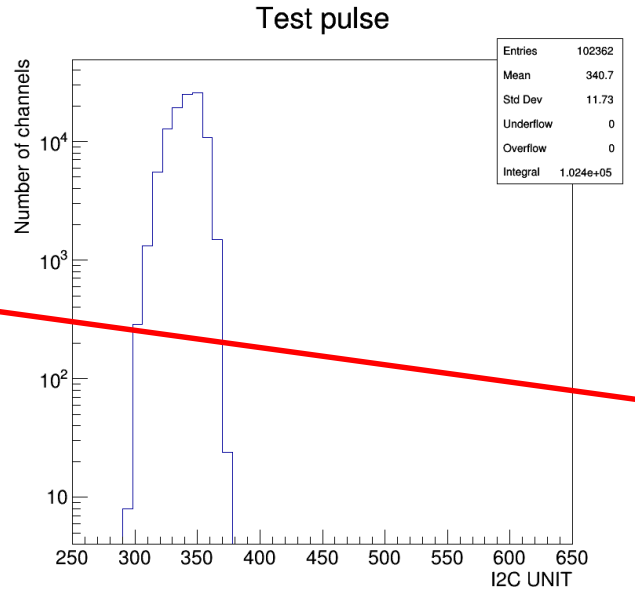


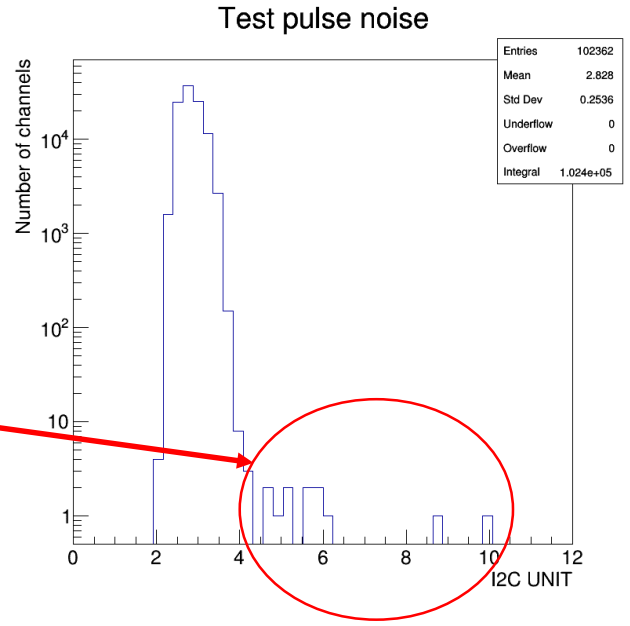




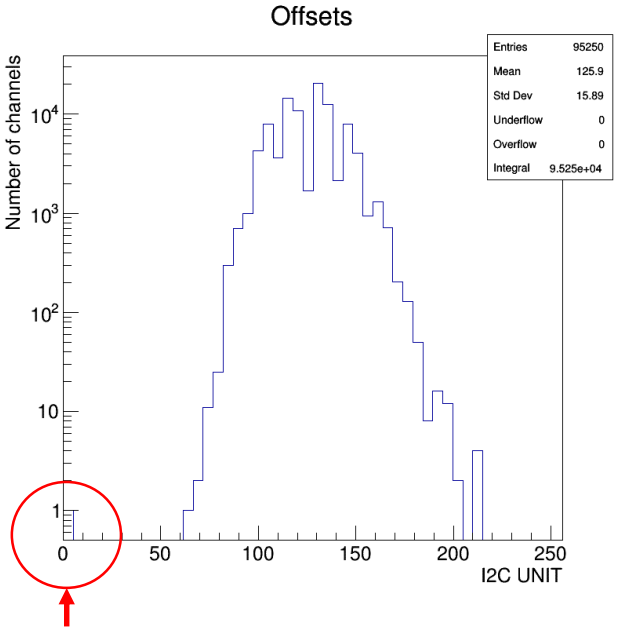
1 chip (chip id=10057) has relatively noisier channels this wafer.

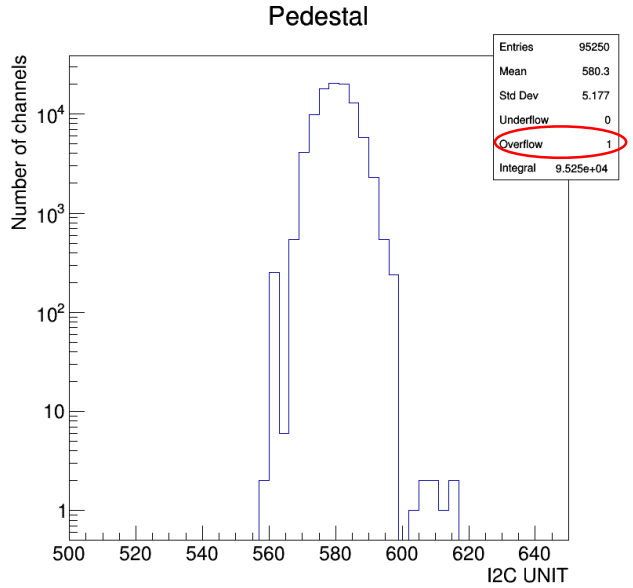
3 chips has some noisier channels.
10 channels in chip 10193,
1 channel in 10022,
1 channel in 10507

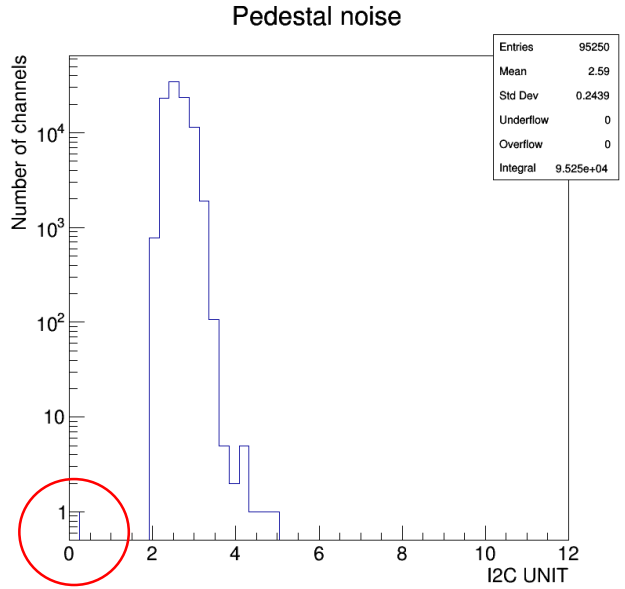




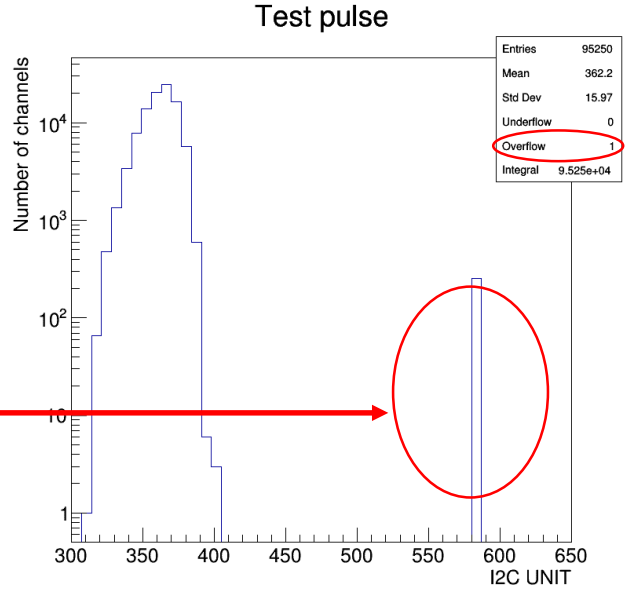
Offsets, s-curve mid-points & noise from good chips in CBC3.1 wafer A2QIWRH (375 good chips)

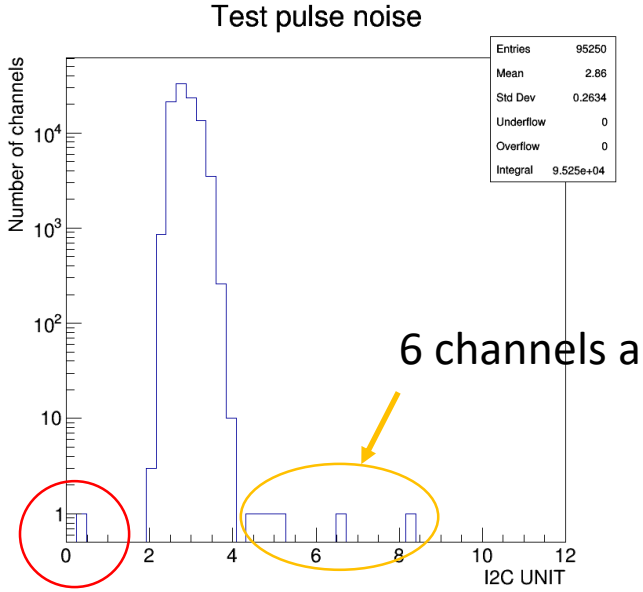






1 channel has offset = 0
This channel has
abnormal pedestal ~710, and the noise ~0.1
& abnormal test pulse ~710, and noise ~0.3.





All the gains in 1 chip is 0
(The channel with offset = 0 is in this chip).

6 channels are noisier.

1 good chip (chp id = 10785) in this wafer has 1 bad channel and test pulse is not working.

Offsets & pedestal tuning, pedestal & test pulse s-curve, gain check

Some more selections should be in the wafer testing

- Offset tuning

  No valid value check is done. ***<- The value must be at least 0 nor 255.***

- Pedestal & test pulse (60 [I2C unit] ~ 5 fC) S-curve check

  S-curve fit must be successful.

  No parameter check is done. ***<- Some loose cut would be useful.***

- Gain check

  Each channel's gain to be < mean +/- 20 (~10%).

In case of 24 CBC3.0 wafers,

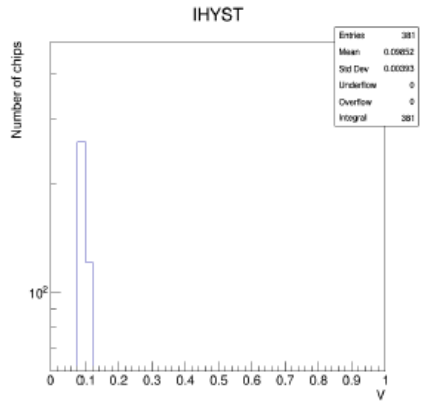
- Offset == 0 or 255 selection picked up 4 bad chips (6 channels)

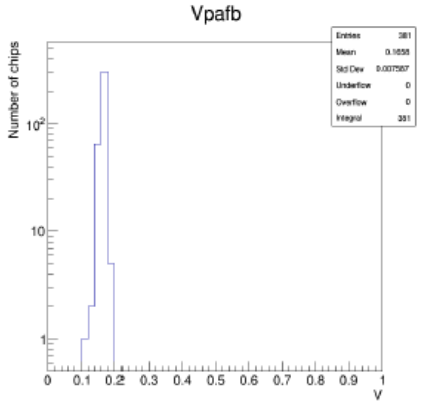
  chip 9915 in VZCURHH, chips 9570, 9561, 9585 in VZCUN1H

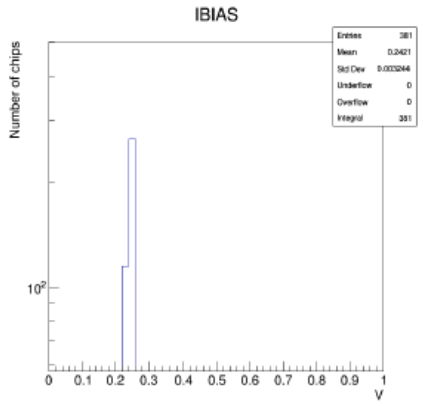
- The test pulse S-curve mid-point > 500 selection picked up 4 bad chips.

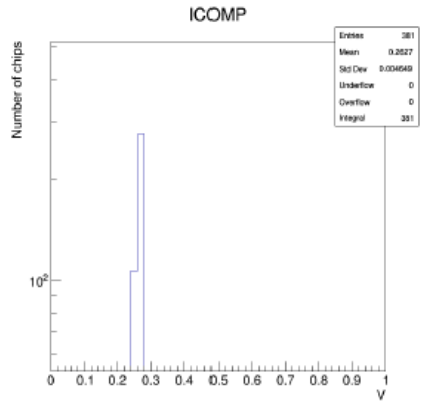
  chip 5471 in V6CUMCH, chip 8471 in VVCUPMH, chip 9915 in VZCURHH, chip 9271 in VYCUPJH

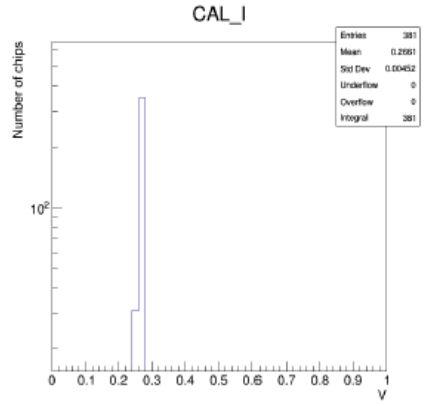
AMUX parameters, settled values of good chips in CBC3.1 wafer A0QIWTH (403 good chips)

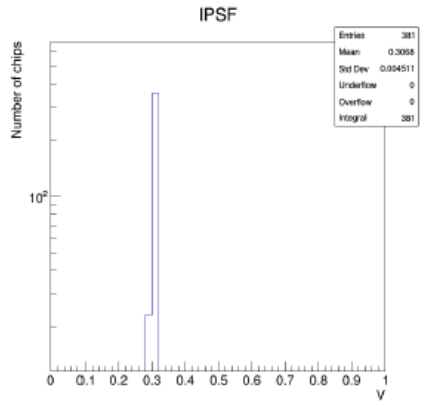


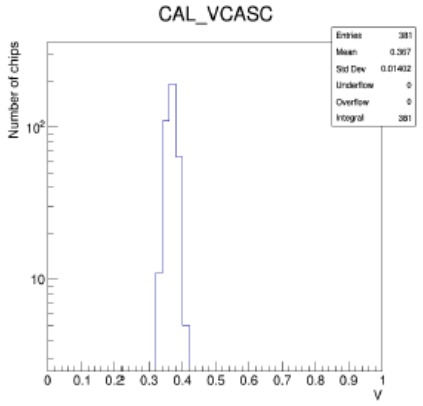


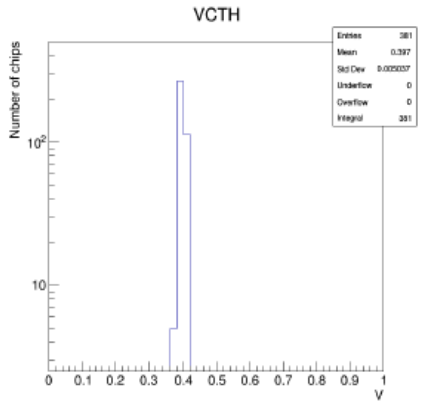


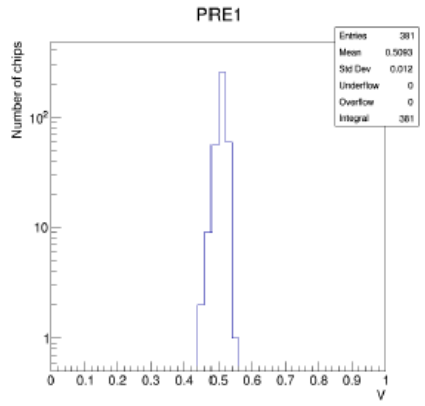


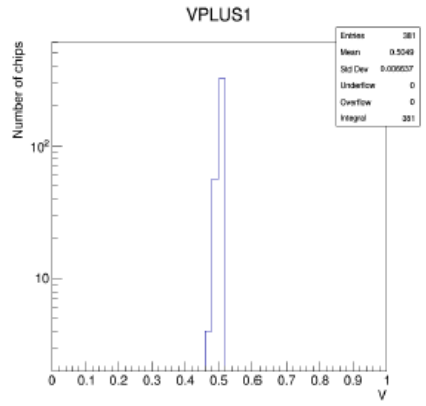


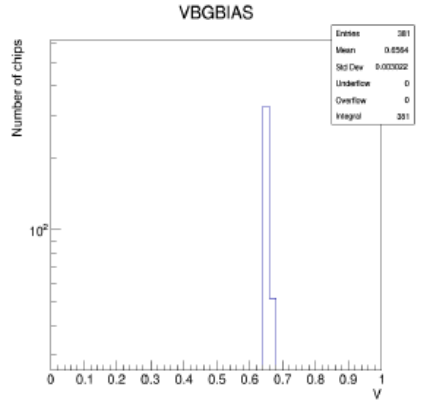


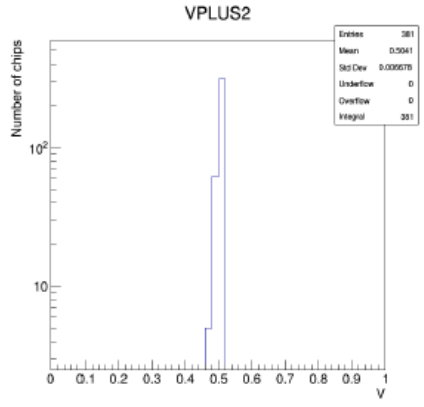


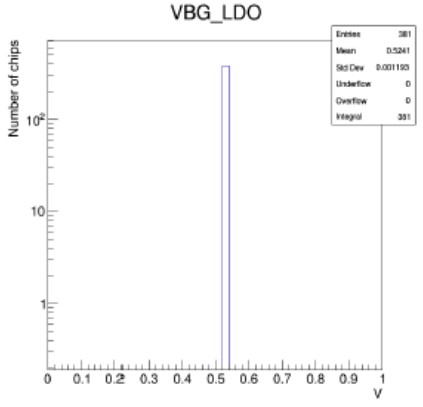


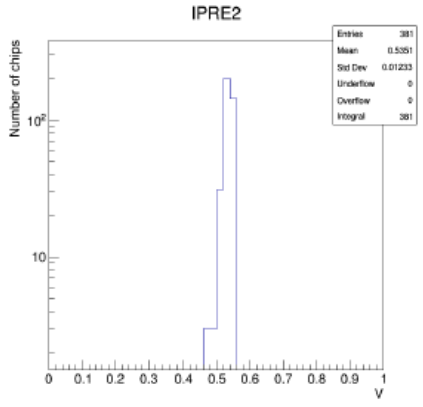


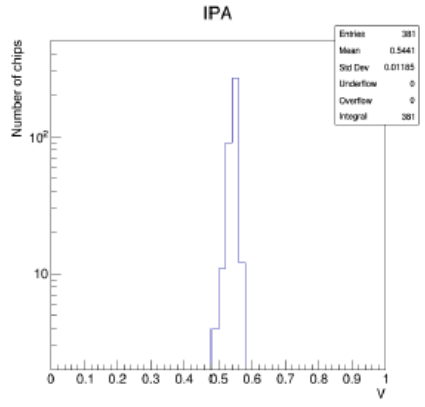


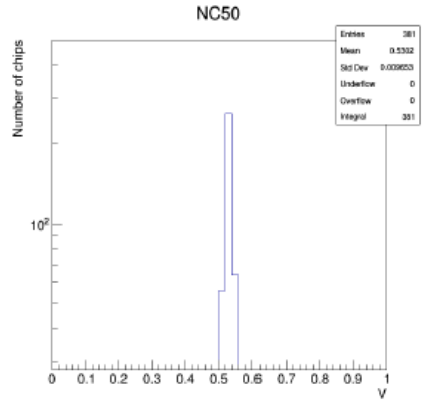


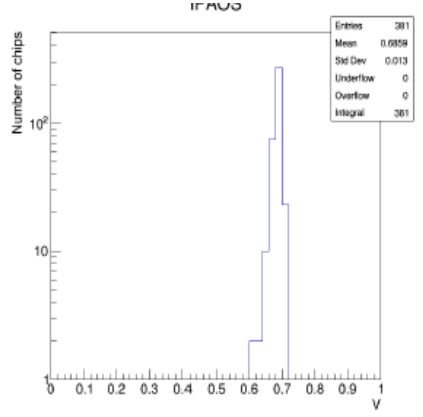










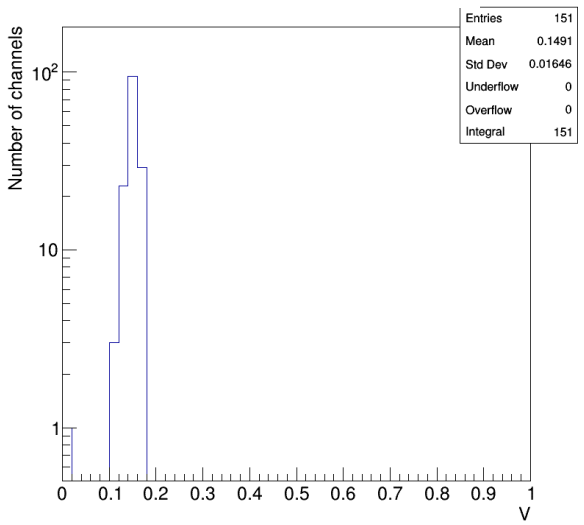


No strange values are found in this wafer.

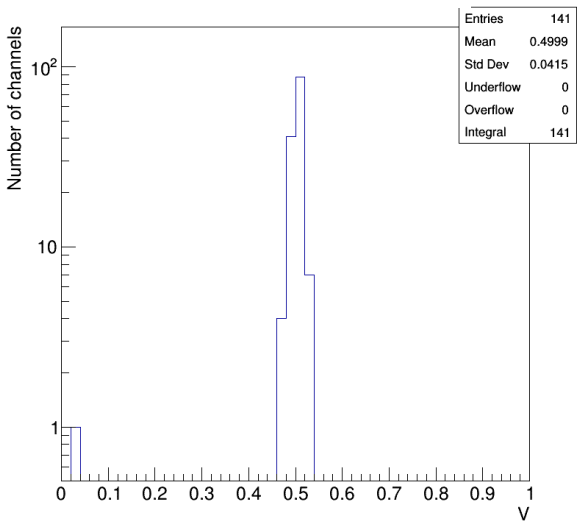
Some AMUX values in good chips are found to be off the main distributions in the wafer (All of those are in CBC3.0 wafers).

- Chip 8380 in VUCUPNH very low Vpafb
  - No other issue is found in the data.
- Chip 7668 in VRCUPRH very low IPRE1
  - very strange current reading. Initially shows nearly 200 mA and currnt bias scan show ~0 mA.
- Chip 5986 in V8CUMAH has IPRE1 ~ 1
  - Ipre1 bias setting does not have an impact on the current on the chip, staying ~31 mA.
- Chip 5383 in V5CUMDH has larger VCTH voltage.
  - VCTH scan shows a kink.

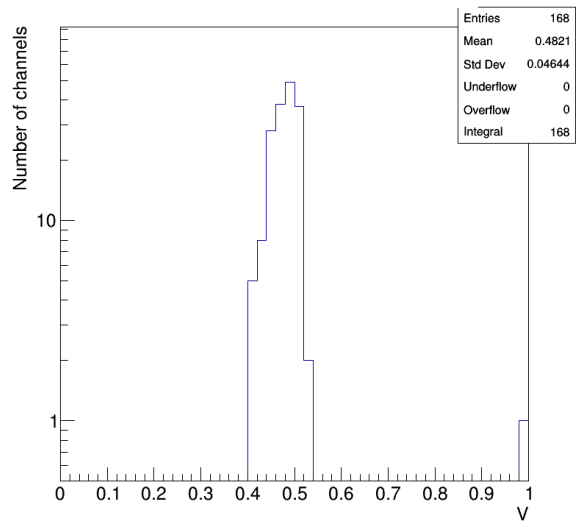
VUCUPNH Vpafb



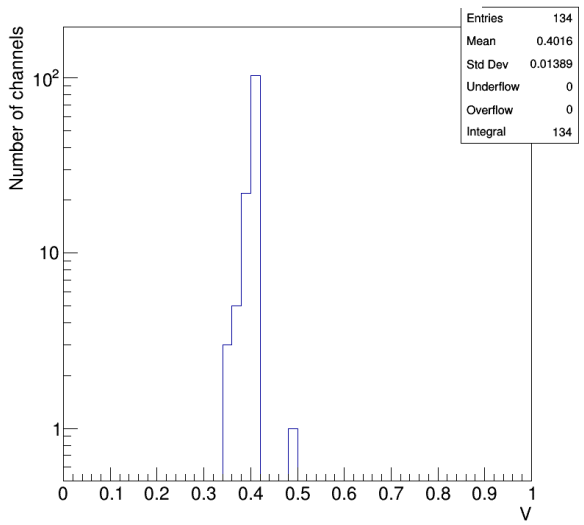
VRCUPRH IPRE1



V8CUMAH IPRE1



V5CUMDH VCTH

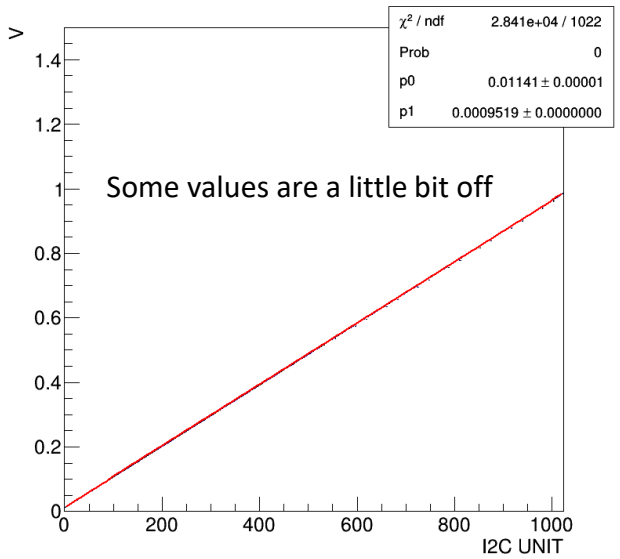


Loose cuts on AMUX measurements will be added in future wafer test

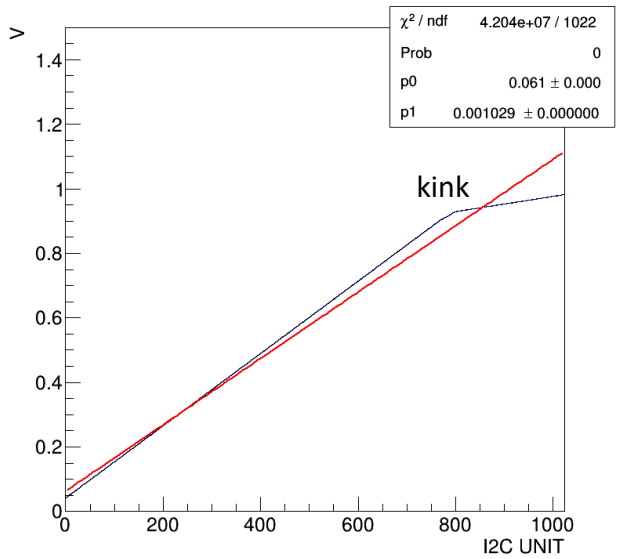
VCTH scan check

- VCTH scan data were fitted with 1st polynomial and 2 chips are found to have worse fit.

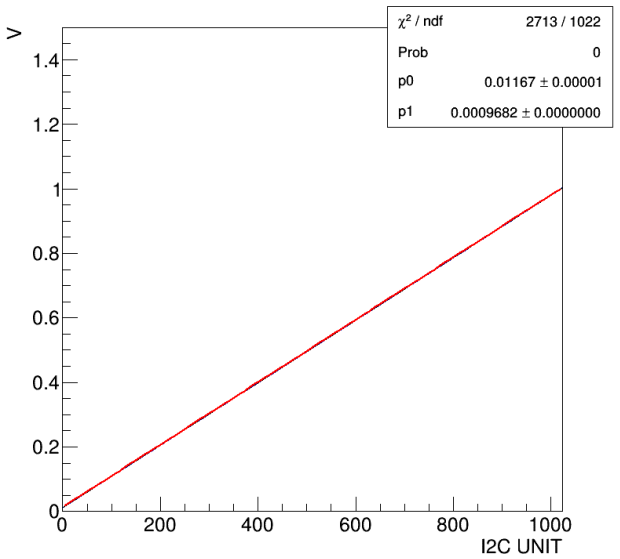
Chip 6439 in VJCUMZH



Chip 5383 in V5CUMDH



Good scan example



Data in black & fit function in red

VCTH value(AMUX) of chip 5383 was measured to be higher than other chips for VCTH setting at 400 (I2C)

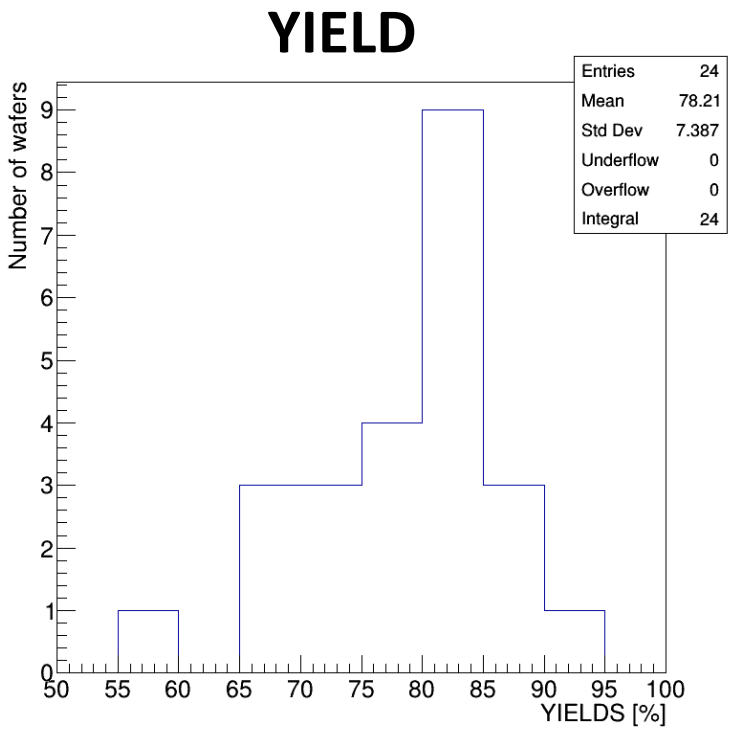
VCTH scan fit will be added in future wafer test

Summary of post analysis on ‘good’ chips

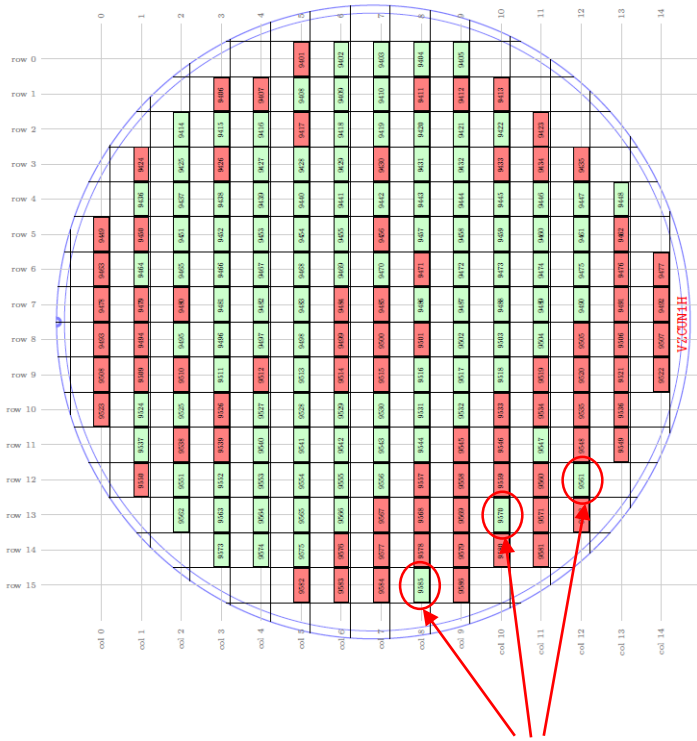
- Analysis is not yet completed.
- A very small fraction of chips are found to be problematic.
- Some more requirements turned out to be useful in the automated wafer testing.

Statistics

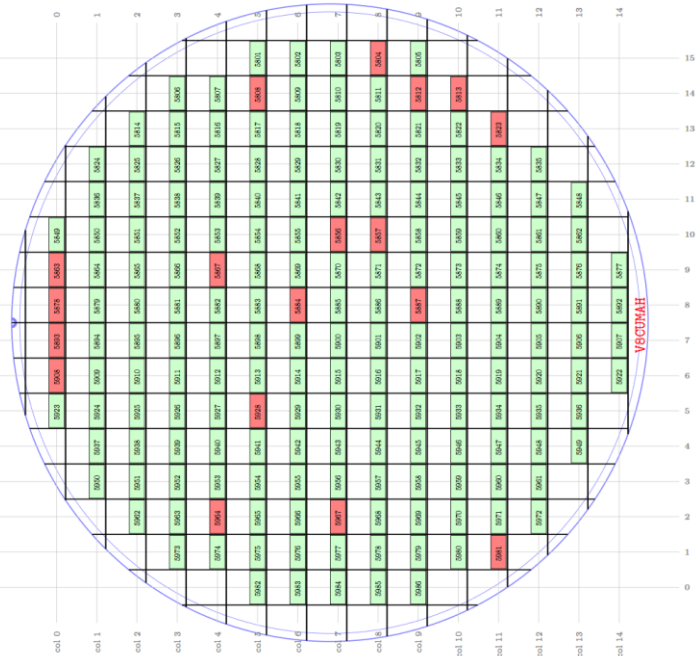
CBC 3.0 Yield variation



VZCUN1H
Worst yield 58%



V8CUMAH
Best yield 90%



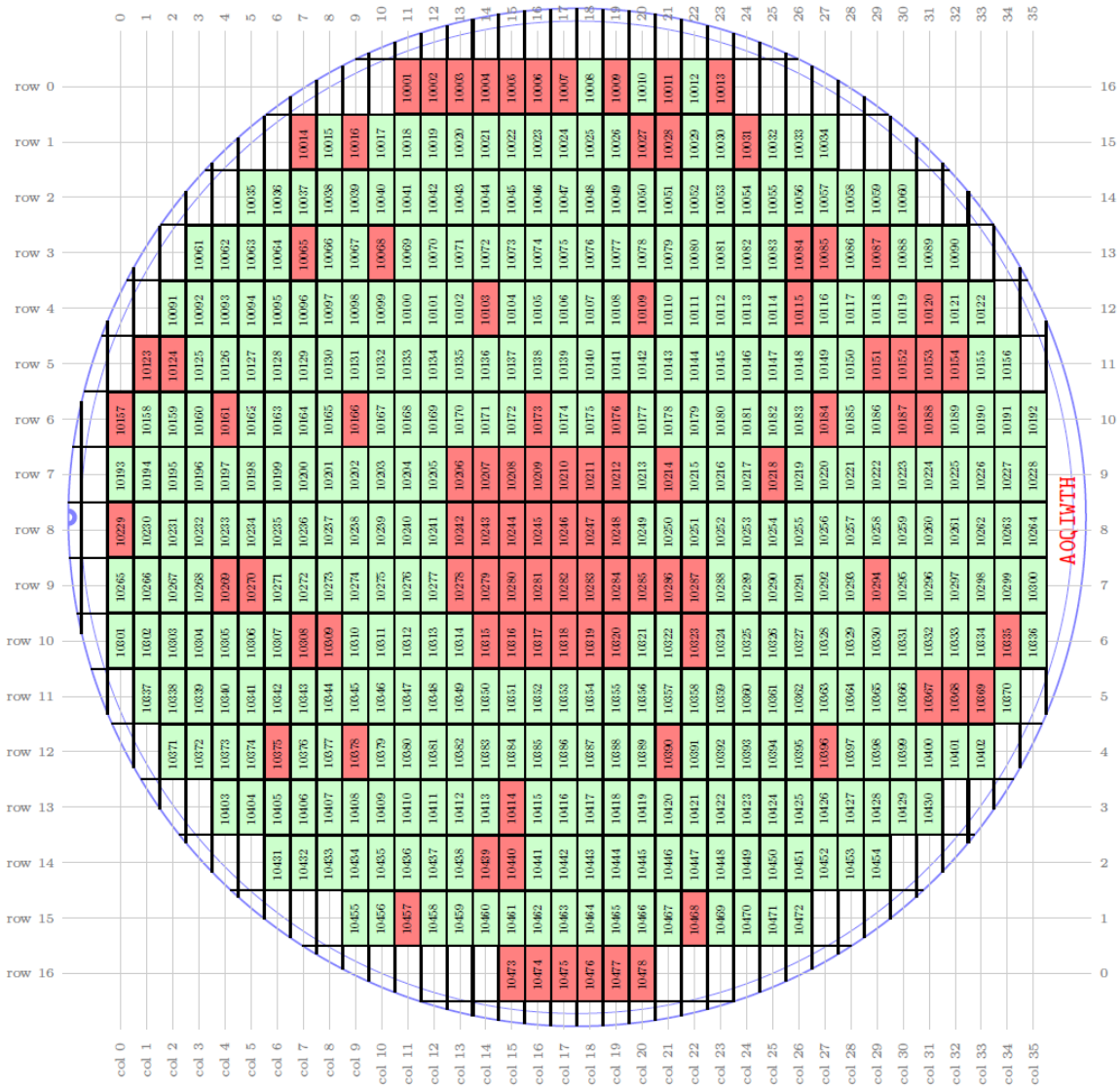
Some offsets are bad (most channels are working).

Errors from 24 CBC3.0 wafers (rate is calculated for # of chips with each error)

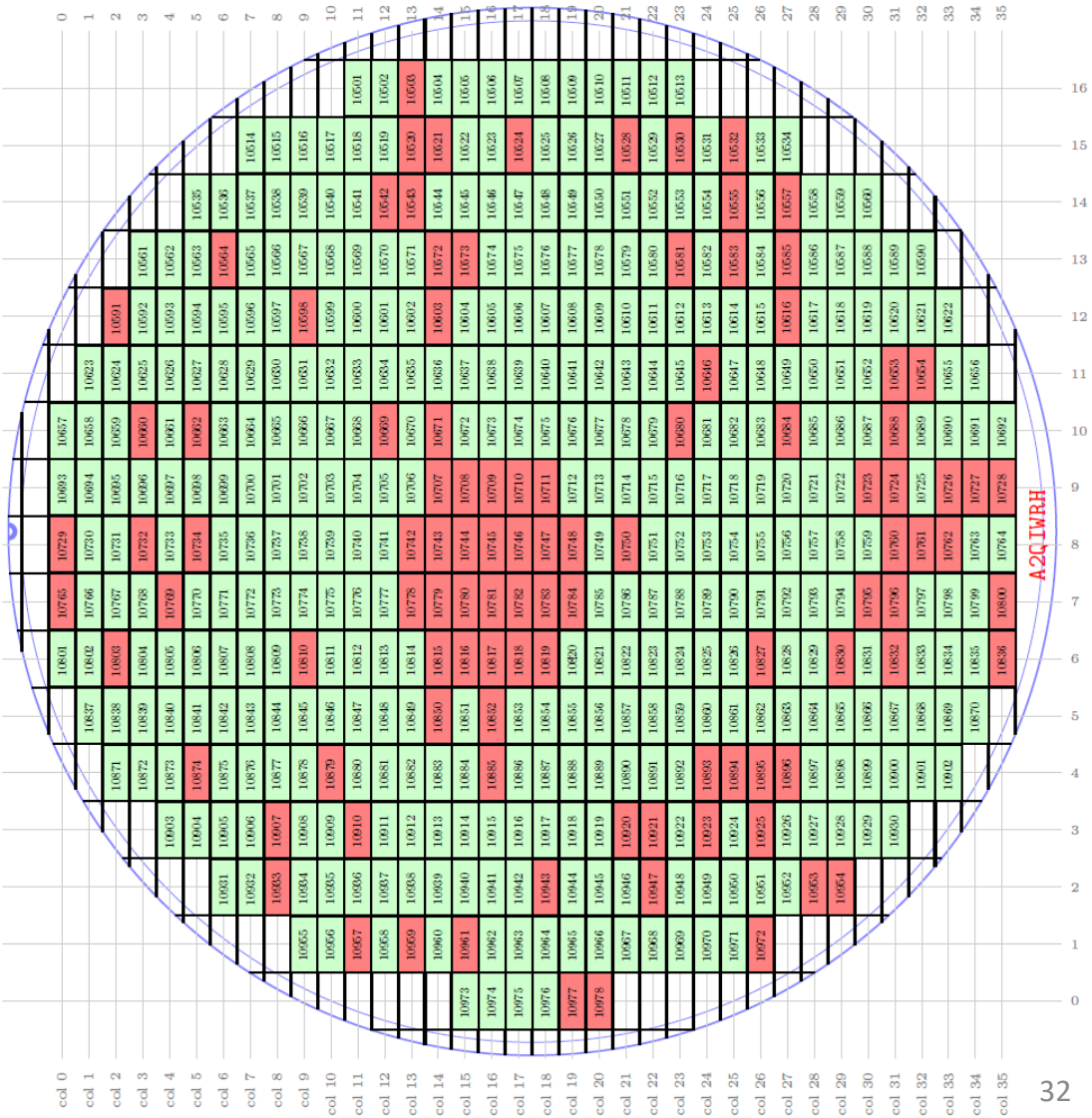
Error type	Error rate [%]	Description
CBC DAQ or I2C errors	4.8	CBC I2C communication error and DAQ errors.
I2C stuck bits	0.0	Bits are stuck to 0/1 on I2C registers
Fuse errors	0.7	Burned values are incorrect. All the errors are due to a bad procedure which was fixed.
Current problem	0.1	
VDDA invalid value	0.1	
Bad channels	3.3	Channels with bad offset, s-curve for pedestal, or s-curve for test pulse
Pipeline data check	1.5	
Buffer ram	6.4 (*0.1)	It seems like that most errors are timing error of pipeline address data passing clock domains. * 0.1 % chips had wrong bits on channel hit data, stuck bits on pipeline address, or L1 count.
Channel mask	0.0	
Stub logic	1.2	
Hit detect and HIP suppression	0.2	
DLL	0.0	
FCI	0.5	
AMUX measurement	0.1	Values from AMUX do not settle under 0.1%
Orbit reset	0.9	Happens for CBC3.0 randomly. Sometimes orbit reset does not reset the L1 counter. Flagged the chip to bad if it happens in case.
Crashed or other error	2.9	Probably 2.1 % of those are backend problem. Some (<0.6) are crashed fitting s-curves. This is fixed and will be moved to bad channels category.
Total (4464 chips were tested.)	23	

CBC 3.1 Yields and Wafer maps for the two tested wafers

A0QIWTH Yield = 80 %



A2QIWRH Yield = 78 %



Errors from 2 CBC3.1 wafers (rate is calculated for # of chips with each error)

Error type	Error rate [%]	Description
CBC DAQ or I2C errors	3.5	CBC I2C communication error and DAQ errors.
I2C stuck bits	0.1	Bits are stuck to 0/1 on I2C registers
Fuse errors	2.8	Burned values are incorrect. All the errors are due to a bad procedure which was fixed.
Current problem	0.1	
VDDA invalid value	0.2	
Bad channels	4.5	Channels with bad offset, s-curve for pedestal, or s-curve for test pulse
Pipeline data check	1.4	
Buffer ram	0.1	**No error on pipeline address & L1 count.**
Channel mask	0.0	
Stub logic	2.8	
Hit detect and HIP suppression	0.0	
DLL	0.0	
FCI	4.6	All of these were caused by software bug. Most probably all chips are o.k.
AMUX measurement	0.1	Values from AMUX do not settle under 0.1%
Orbit reset	0.0	**The L1 counter reset instability seems to be fixed in CBC3.1.**
Crashed or other error	0.5	All crashed by the S-curve fit. This is fixed and will be moved to bad channels category.
Total (956 chips were tested)	21	

backup

Time required for the test

Breakdown for the tests which take more than 1 sec

Test	Time [sec]
S-curve check for pedestal and test pulse, gain check	7
Measurements of all individual AMUX parameters	6
Sweeping settings and measure the bias voltages	5
Offsets and pedestal tunings	3
Stub checks	2
Sweeping settings and measure the bias currents	2
Bandgap tuning, bandgap and chip ID register fuse blowing	2
Sum of above	27
Total time for a single chip wafer testing	30