CBC3.1 testing update

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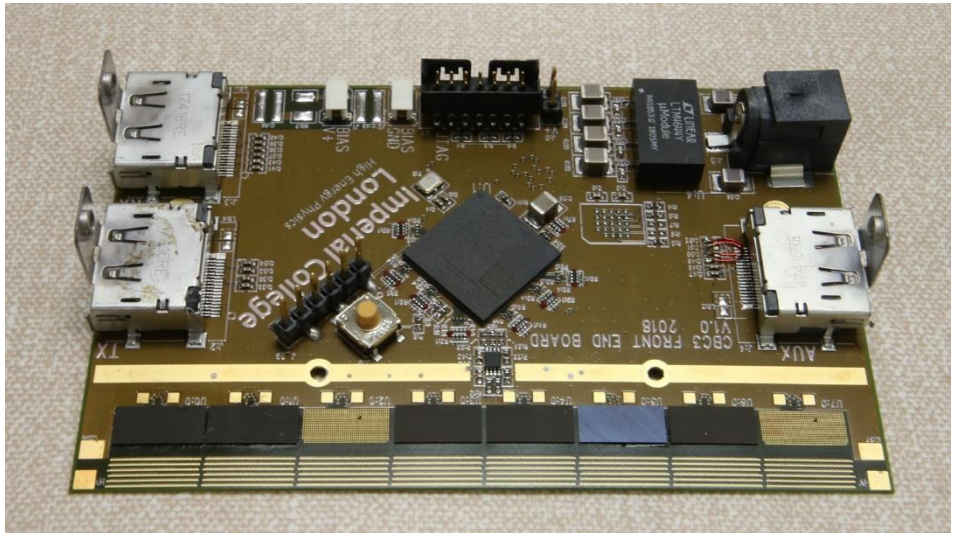
CBC testing status

- **TID test was done in Nov.**
- **Wafer testing for the remaining CBC3.1 wafers.**
- SEU test is planned and booking request for a beam 25 & 26 in Feb. 2019 is sent to Christophe.
- Supply voltage scan (0.99-1.40 V) where CBC3 spec. is VDDD : 1.2V +/- 10%, VDDA > 1 V.
  ~15 chips are selected for each wafer and analysis is on going.
- Supply voltage (0.99-1.40 V) & Temperature (-40 to 30 °C @air) scan
  7 single wire-bonded chips are placed in an environmental chamber and analysis is on going.
- Hybrid with bump-bonded CBC3.1
  The inter-chip connection has been validated with this system.

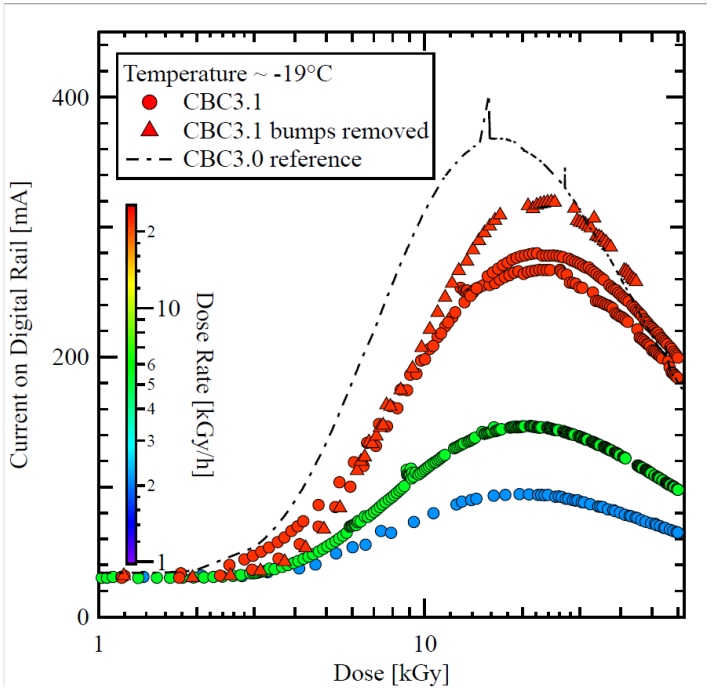


TID test

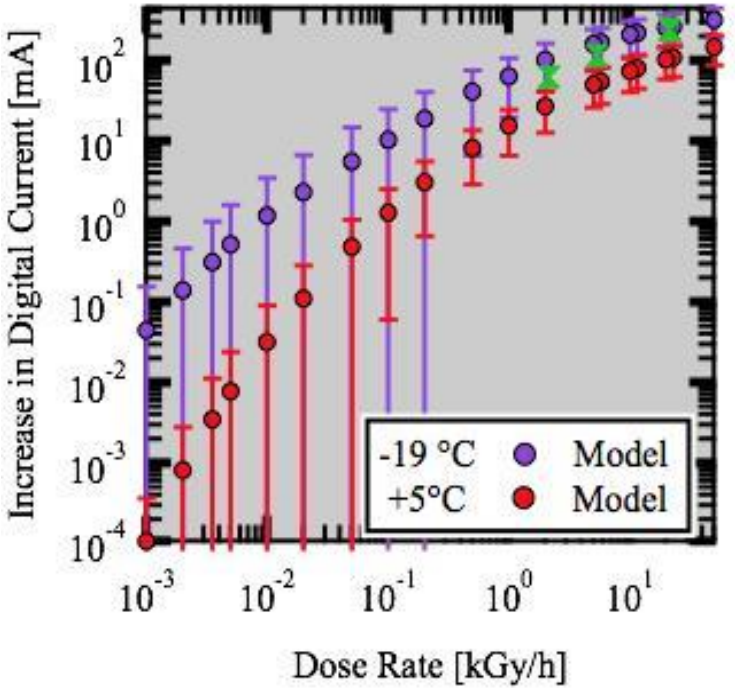
- @CERN, 12-18 in Nov. by Sarah & Tom
- 3 different dose rates [2-20 kGy/h] for w & w/o bumps at ~ -19 °C

  The chips are already bumped for this TID test different from the test with CBC3.0 and bumps are manually removed for a couple of chips as much as possible.

Digital current



Digital current peak measurements & extrapolation



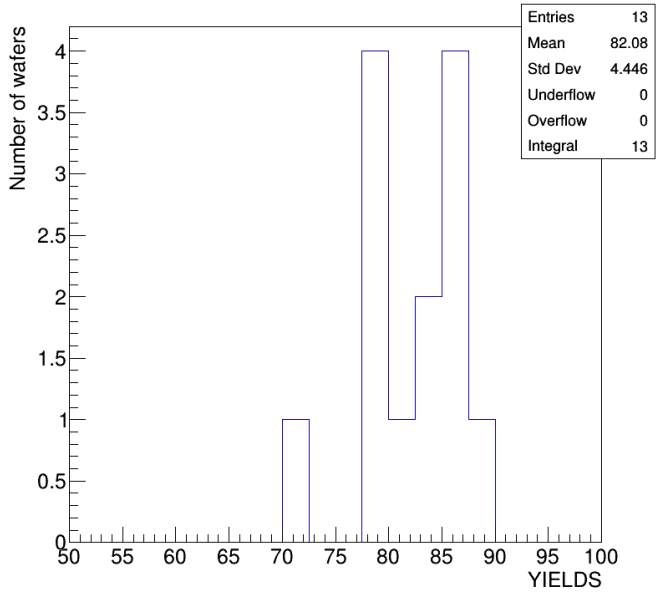
CBC3.0 (purple & red)
CBC3.1 (green)

Max dose rate @ 2S Module : 10-2 [kGy/h]

Yields of 13 CBC3.1 wafers

Preliminary

- Yield is 82 % in average over 13 wafers.



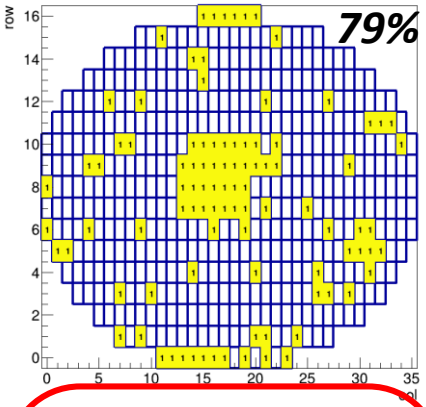
- Errors happened for more than 1% of the chips are in the following,
  - Errors in Stub test ~ 1.2 %,
  - Errors in Pipeline test ~ 1.7 %,
  - I2C errors or CBC data broken ~ 5.8 %
  - gain problem ~ 5.8 %
  - Software bug ~ 1.0 %

Wafer maps

Preliminary

Bad chips are coloured in yellow.
The top left of each map is the yield of the wafer.

A0QIWTH



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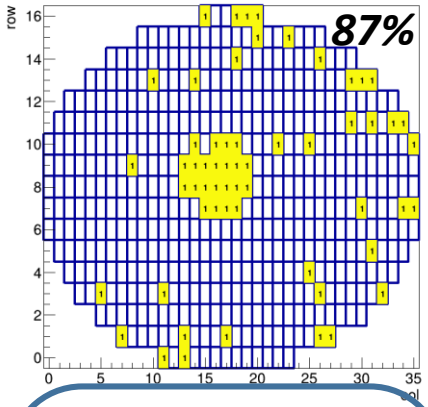

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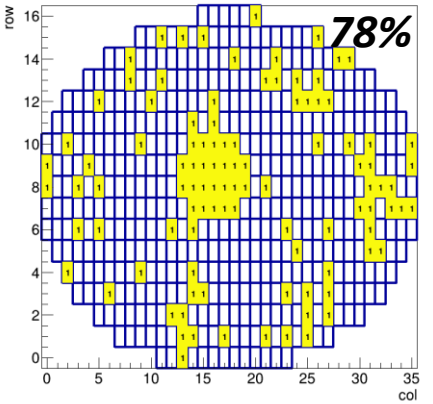

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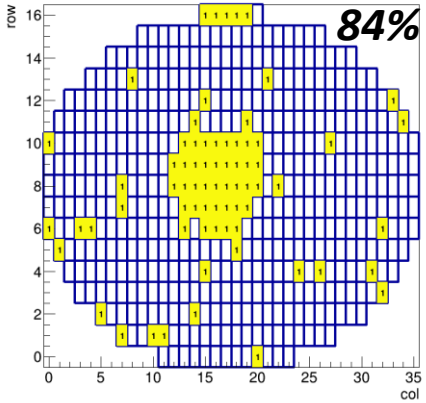

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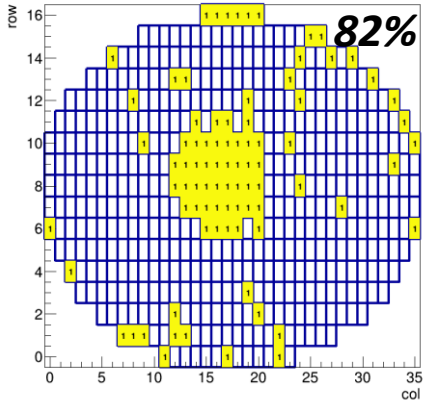

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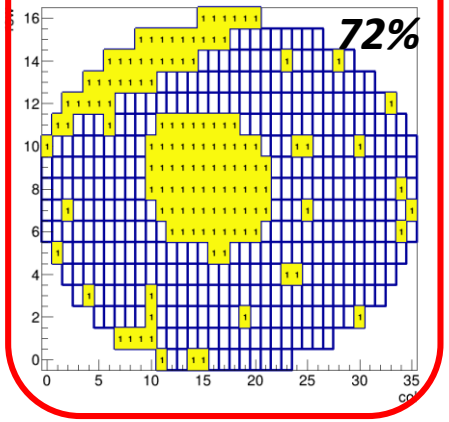

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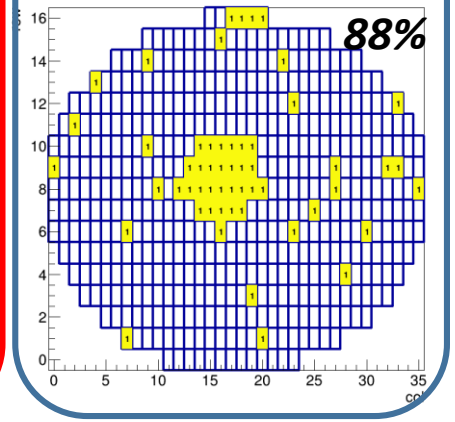

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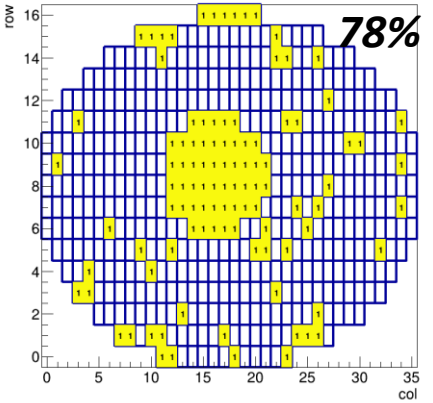

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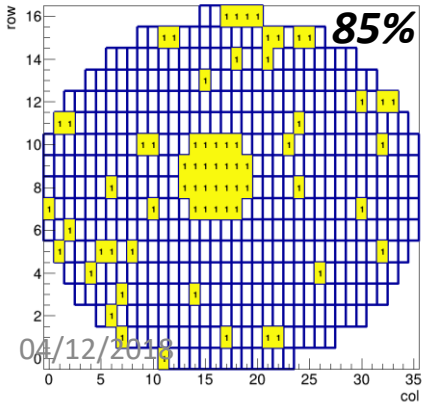

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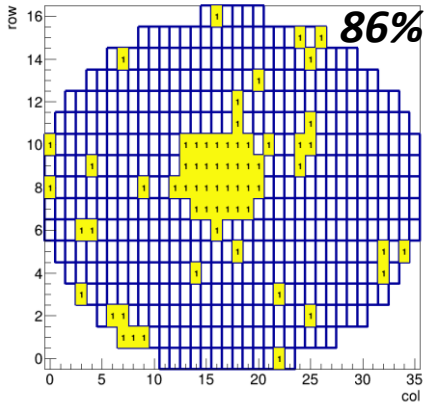

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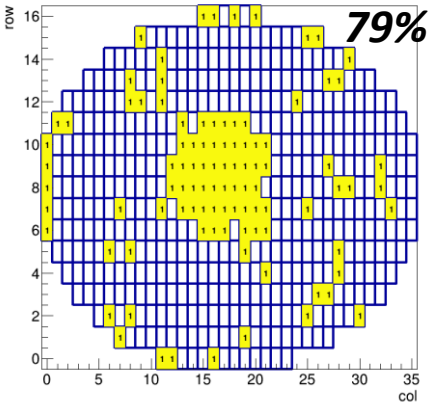

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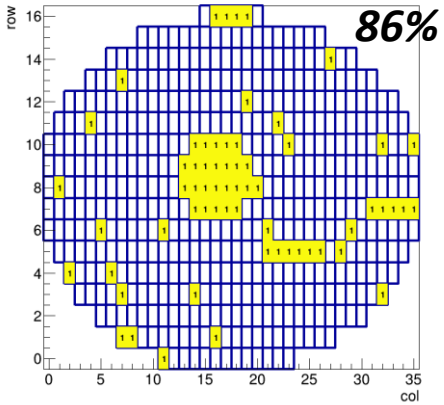

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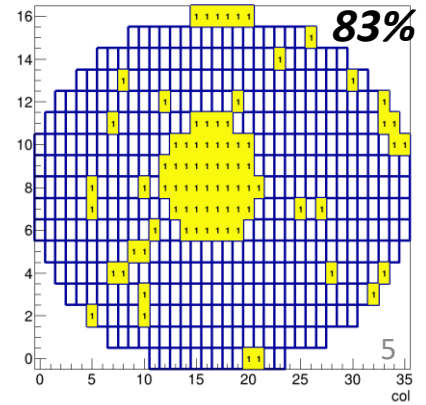
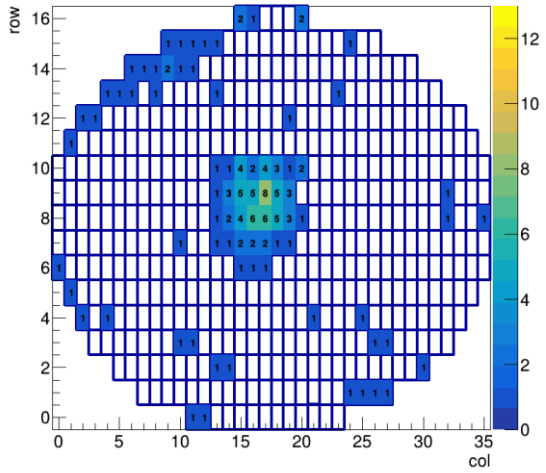


Error maps for 13 wafer all together

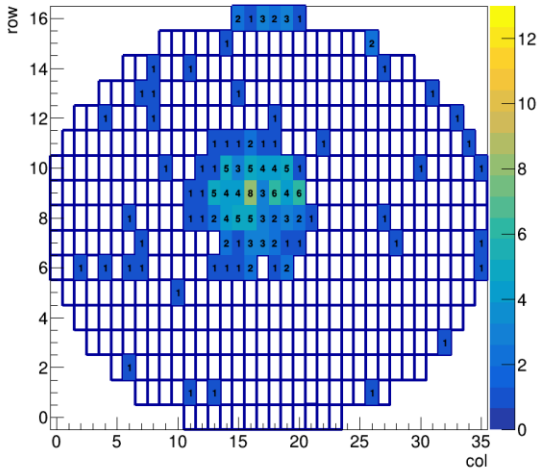
Preliminary

Map of the number of chips with errors in 13 wafers

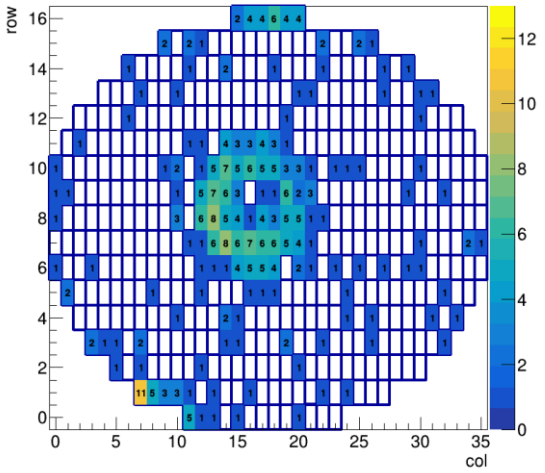
I2C errors



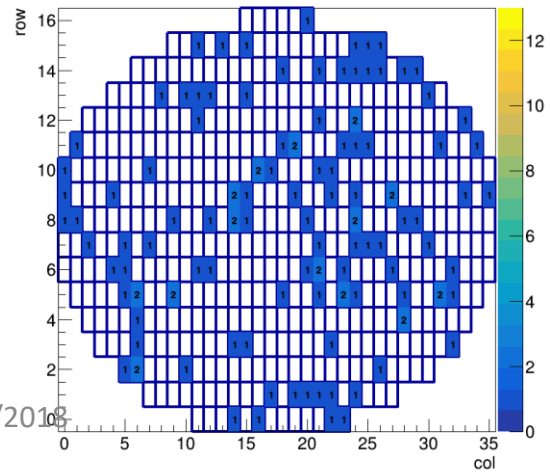
DAQ errors



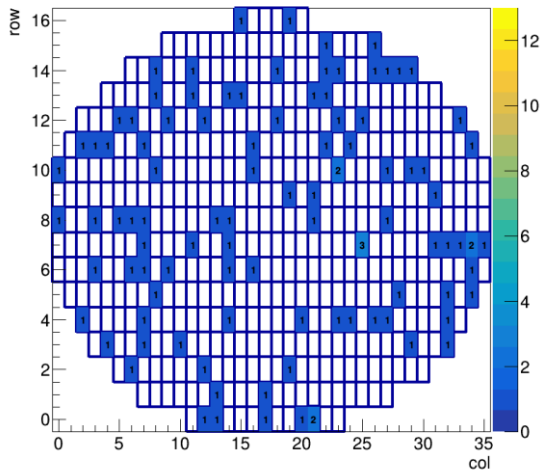
Gain errors



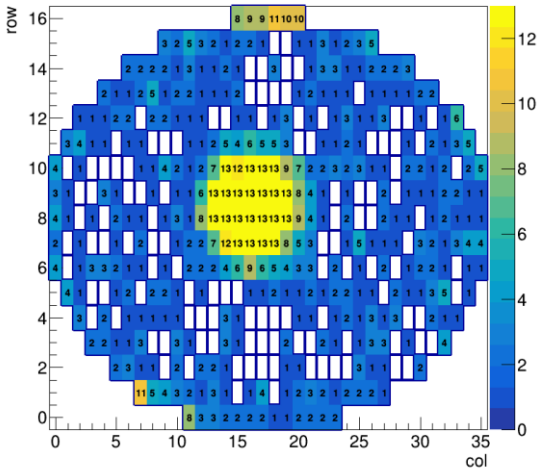
Pipeline test errors



Stub test errors



All errors



Summary

- TID result for CBC3.1 looks consistent with that for CBC3.0.
- 13 wafer testing result show an yield issue in the centre of wafers, but yield is not low, 82% in average.
- Beam time is booked on 25 & 26 in Feb. 2019 for SEU test.
- Some other tests are on going at IC and results will come soon.