CBC 3.1 testing status report

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Modifications in CBC 3.1

Green : verified
Blue : Any issue has not been observed
Yellow : to be concluded.

- ✓ Stub logic bugs (Invalid stubs and bad stub addresses and bend codes) are corrected.
- ✓ L1 Data Serialiser
  (frame length is not always 950 ns and frames are corrupted sometimes for some DLL settings in CBC3.0 for consecutive triggers) looks stable.
- ✓ Default settings for the bias currents changed (Total current ~ 72mA at power up).
- ✓ Unreliable L1 counter reset signal seems to be solved.
- ✓ Nearest Neighbour signal swapping is corrected. (Verified by two CBC 3.1 hybrid at IC)
- ✓ Re-timing registers for L1 triggered data outputs shows much better matching with trigger data.
- ✓ SEU improvements to I2C registers has been tested at proton beam at Louvain last week.
  Analysis is on going.
- ✓ testsBurn33 tied off to vdd has been verified
- ✓ Extra Bumps Grounded
- ✓ Ball specification: 129 um for CBC3.1 while 150um for CBC3.0 (63% of the material).
  Smaller balls: less forgiving to PCB imperfections.
- ✓ Nearest Neighbor Logic Test Function is incorporated in the stub tests.

Data output timings

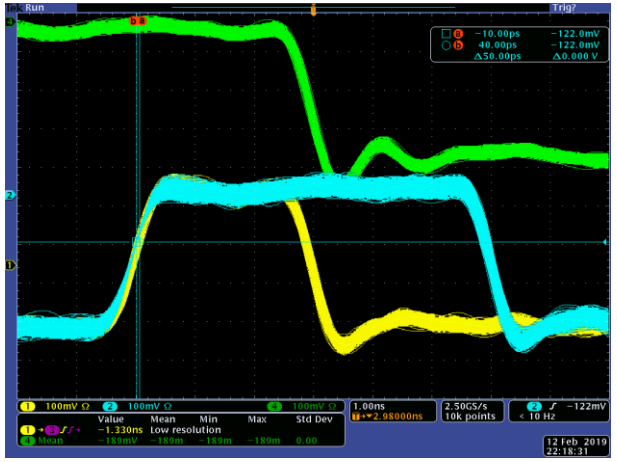
- For CIC, some data output response timings for fast commands are measured as done for CBC3.0.
  - ✓ L1 counter reaction to orbit reset is improved.
  - ✓ L1 triggered data takes more time (some BX) to come out than CBC3.0 from L1 trigger.

    If data are taken identifying the frame header, the DAQ is not affected by this change.
- L1 triggered data timing is aligned better with trigger data.

  L1 triggered data header come out ~400 ps slower than sync bit in CBC3.0

CBC3.0

CBC3.1



Wafer testing

- 13 CBC3.1 wafers are tested
  - Reported in Outer tracker electronics WG meetings

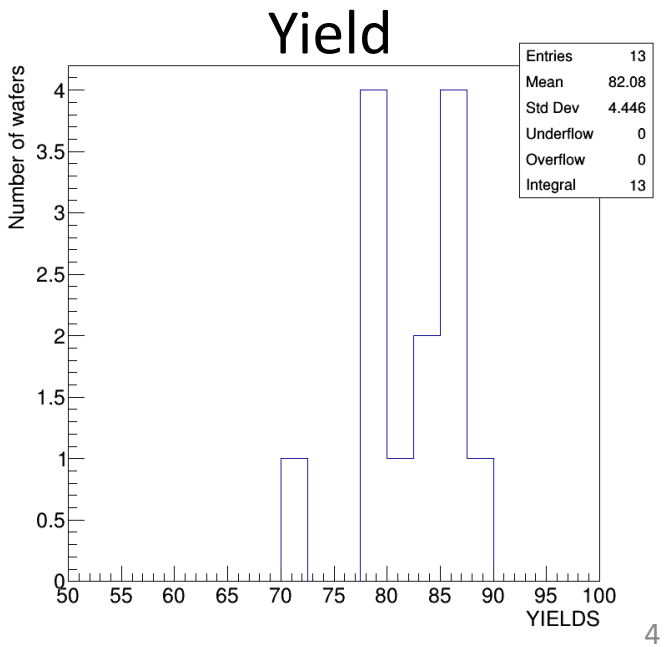
https://indico.cern.ch/event/769416/contributions/3197393/attachments/1747444/2829832/WaferTest_06112018.pdf
https://indico.cern.ch/event/772629/contributions/3210714/attachments/1766304/2867915/CBC3_20181204.pdf

- Yield ~ 80%
- All 13 wafers have bad chips in the central regions.

  Production problem?

  ✓ The error symptoms and yield patterns are informed to the manufacturer.

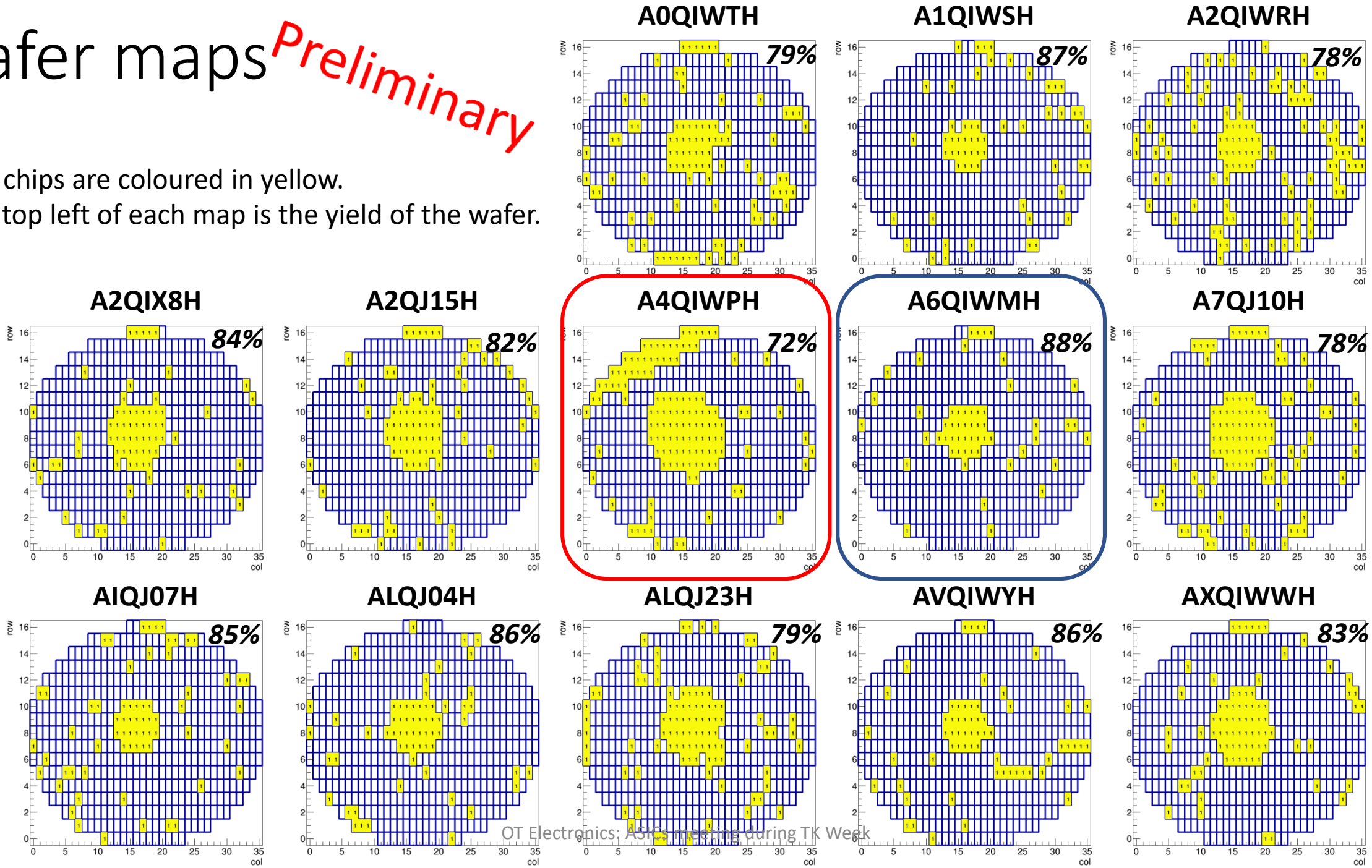
  ✓ 2 lots of 24 wafers will be produced to see if modified process would improve the CBC yield.
  The order of the first lot has been placed and fabrication process started.



Wafer maps

Preliminary

Bad chips are coloured in yellow.
The top left of each map is the yield of the wafer.

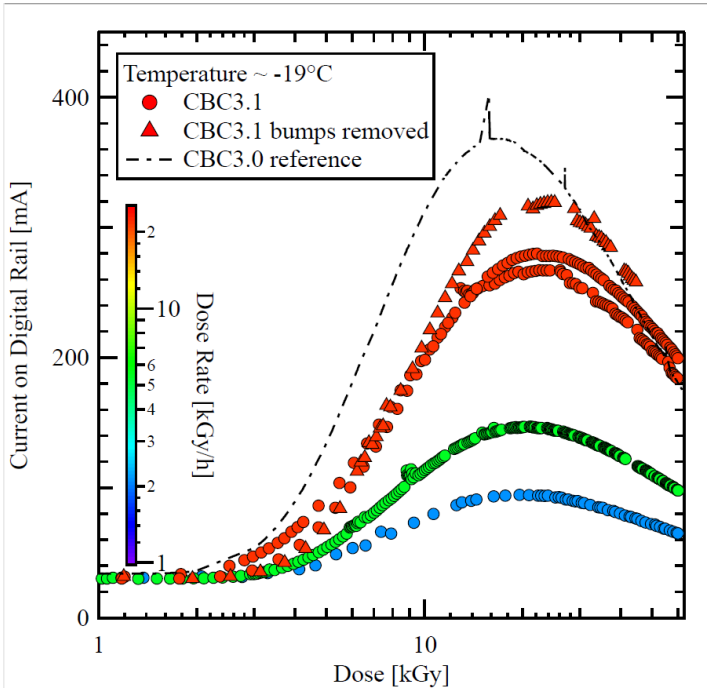


Radiation tolerance tests

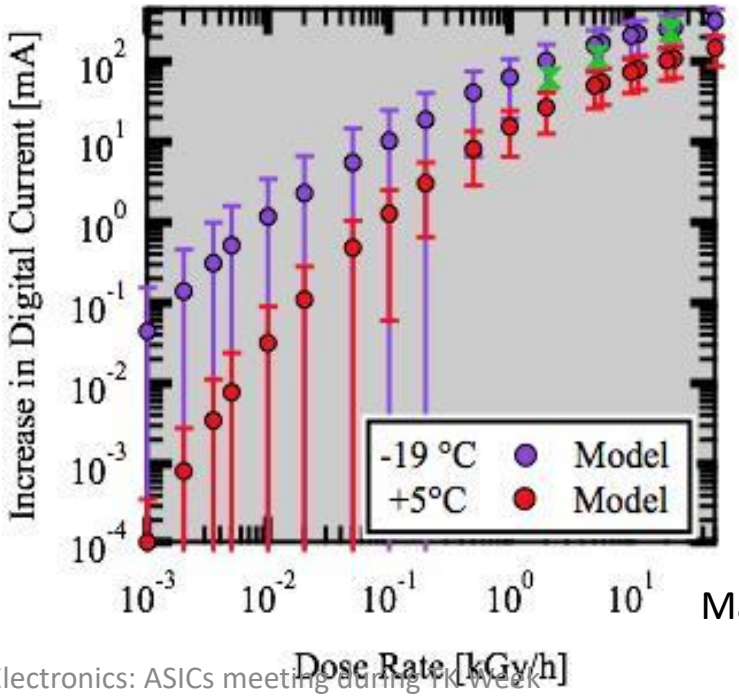
TID test

- @CERN, 12-18 in Nov in 2018. by Sarah & Tom
- 3 different dose rates [2-20 kGy/h] for w & w/o bumps at ~ -19 °C
  The chips are already bumped for this TID test different from the test with CBC3.0 and bumps are manually removed for a couple of chips as much as possible.
- The result is the same as CBC3.0.
  No function degradation is observed. There is a small digital current increase.

Digital current



Digital current peak measurements & extrapolation



CBC3.0 (purple & red)
CBC3.1 (green)

Max dose rate @ 2S Module : 10^{-2} [kGy/h]

SEU test

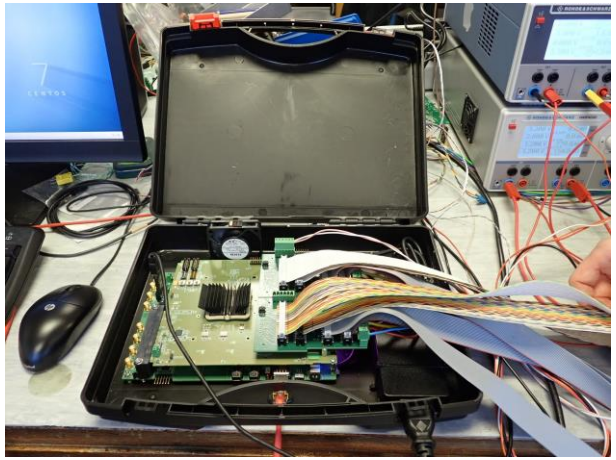
- LiF at Louvain
  - Proton beam from cyclotron with the max. energy at 62 MeV and the flux ~2×10^8 $cm^{-2}s^{-1}$.
    - ✓ The flux is ~67 times the HL-LHC (~ 3×10^6 $cm^{-2}s^{-1}$, 3 x the flux in the middle region by FLUKA),
    - ✓ the cross section of the proton energy corresponds to the average in the tracker at the LHC.

    M. Huhtinen and F. Faccio, "Computational method to estimate Single Event Upset rates in an accelerator environment," NIM A, vol. 450, pp. 155–172, 2000
  - Participants

    Johan, Kirika from IC, & Christophe at Louvain
- 25th & 26th in Feb. 2019
  - ~16 hours of beam time (The beam monitoring data will be provided.)
  - ~ 1000 hours at HL-LHC (~40 days).
- Data
  - I2C register bit flips
  - L1 data frame (error bits, L1 trigger counter, pipeline address, hit data)
  - Trigger data (stubs)
    Some SEU events are observed. The analysis result will be shown soon.

SEU test

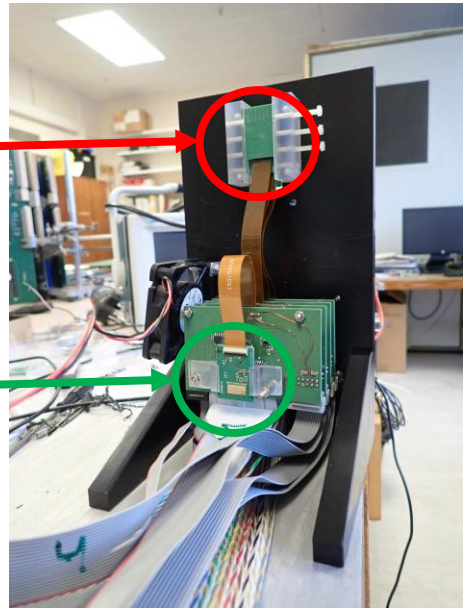
Backend FC7

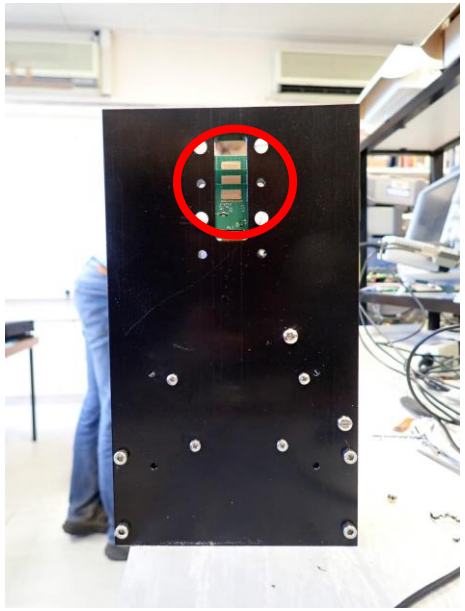


3 CBCs
in the beam

1 CBC
off the beam

Frontend

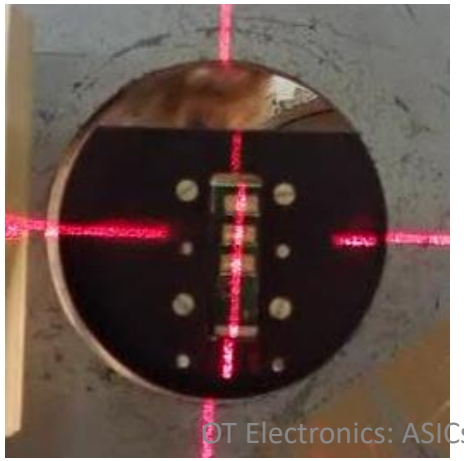




FC7 off the beam
behind a lead wall

Beam line side view

3 CBCs in the window



Beam line view from down stream

Supply voltage range over different temperature

- LDO measurement requires narrower range of VLDOI (VDDD) than manual (1.2 V +/- 10%)
  - Mark Raymond measured 1.15V as the minimum VLDOI at room temperature.
  - https://indico.cern.ch/event/613723/contributions/2474070/attachments/1417085/2170028/CBC3_status_Feb_2017.pdf
  - <- Higher minimum supply voltage at low temperature.

Summary

- CBC3.1 chips are performing well in the testings.
- The data from the beamtest for SEU tolerance test will be shown soon.
- An order for additional CBC3.1 lots of 24 wafers has been placed to see the process changes implemented recently for this technology by GF improve the CBC3.1 yield or not.