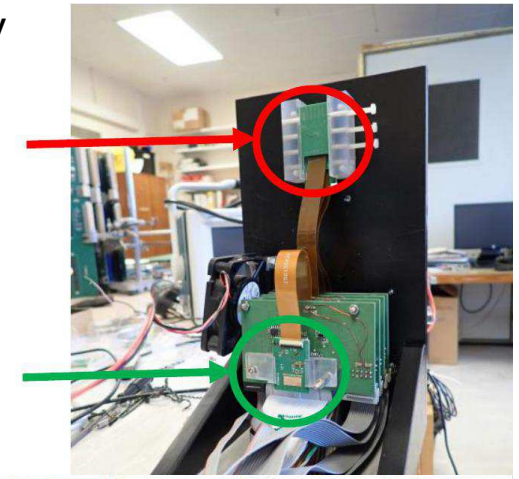
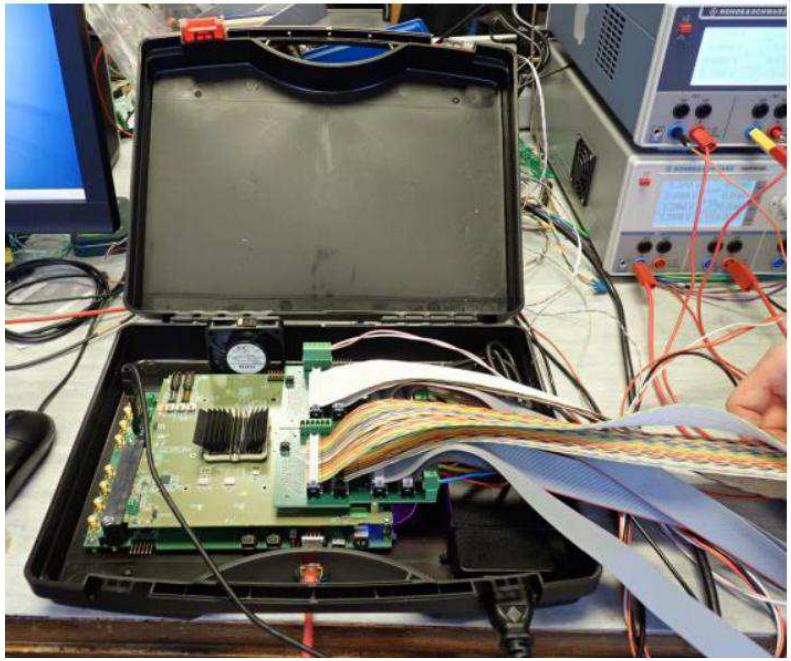
Summary: CBC3.1 status and Flip-chip testing

- SEU tests performed in Leuven la Neuve on 25-26th of February
  - SEU test data analysis in progress
- Supply voltage range tests over temperature
  - Initial tests performed late 2018
  - More comprehensive tests to follow
  - LDO PSRR vs dropout
  - LDO dropout vs temperature
  - Analog front-end performance
- Re-commissioning of wafer probe station in new room, tests of new probe card and other updates for next batch of wafers
- Wafer probers soon to be relocated to new lab
- Further test to verify performance at high (random) trigger rate





Lab relocation

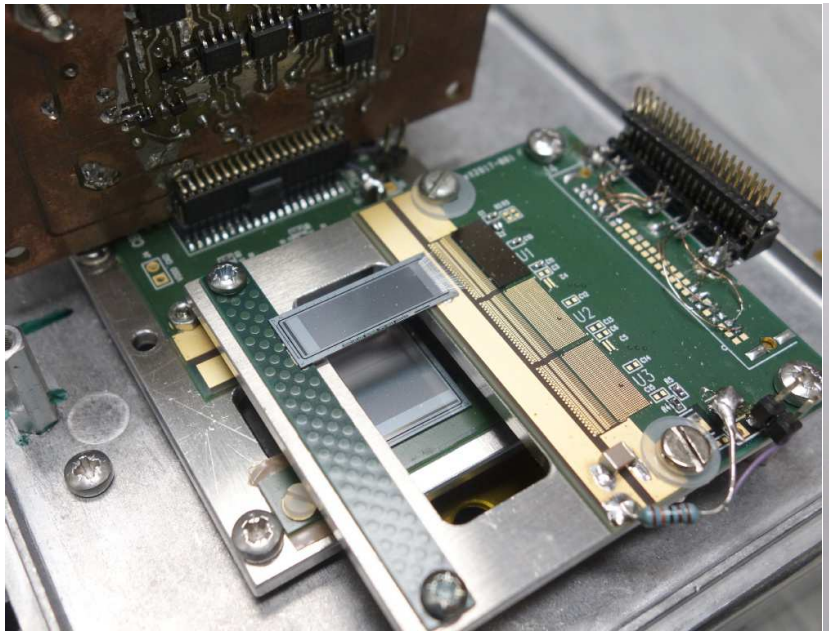
- Air-conditioner still not commissioned
- Portable cleanroom commissioning on the 9th
- Wafer probers, et.c. to be moved before 31 May

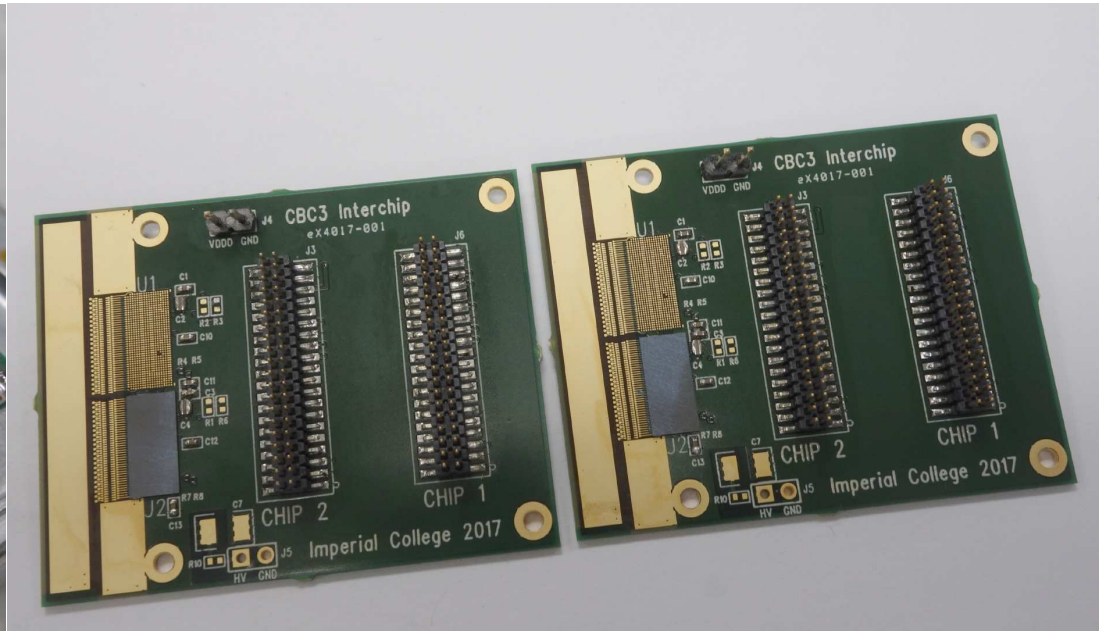
Flip-chip assembly at IC, Background

- Started by MR using CBC2 in early 2015
- CBC2 used high-lead balls, 327°C melting point
  - Not to be confused with leaded solder (40% lead)
  - Melting point too high for our reflow ovens
  - FR4 decomposes rapidly at these temperatures
  - Attempts with using lead-free paste to create a lower melting point alloy during soldering were unsuccessful
- CBC3.x uses lead-free balls (≈220°C)
  - Soldering temperature is no longer a problem
- Breakout of 6 rows of balls of input channels at 250um pitch requires dense PCB

First 2 batches of PCBs

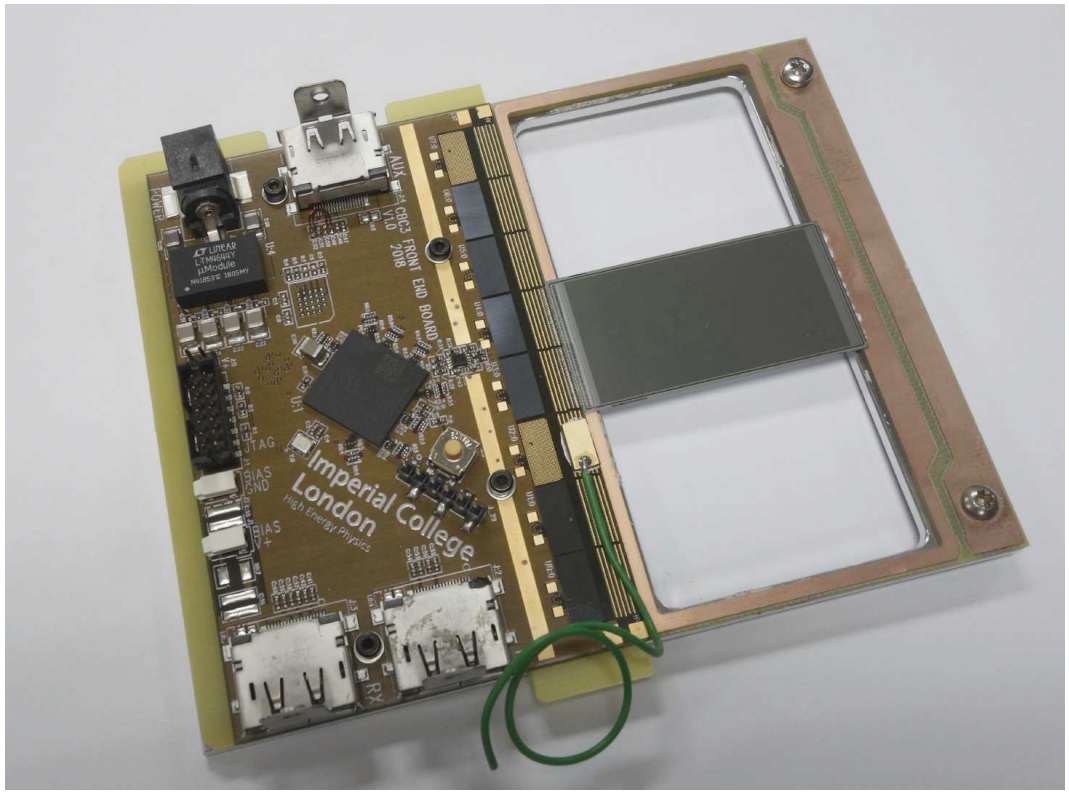
- 6-layer PCB manufactured by Exception PCB
- Layer 1-2, 2-3 (and 4-5, 5-6) microvias ($\approx$ 160um)
- Only 2/3rds of inputs connected (breakout on top 4 layers)
- Imperfect ground connectivity in the middle of the chip
- Potential for wicking along top traces





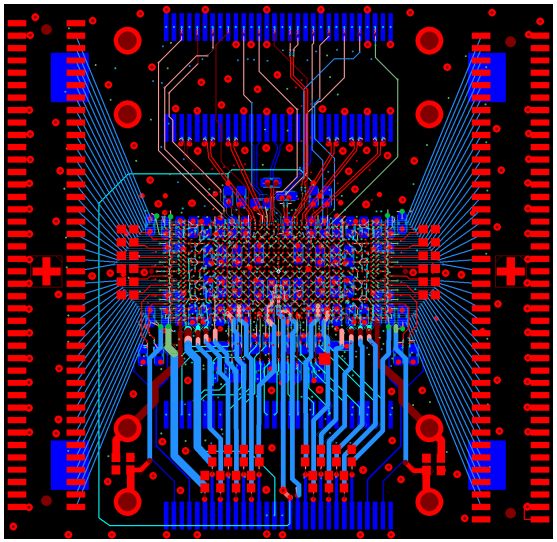
Current PCBs

- 125um micro-vias between all 6 layers
- All inputs connected, breakout on layer 2-4
- Bonding pads on both sides to enable double-sided module
- 0.8mm thickness makes board handling a bit delicate
- Integrated FPGA and DC-DC converter to enable self-contained module
- Manufactured by Somacis (also manufactures PCBs for for MP7, Serenity)



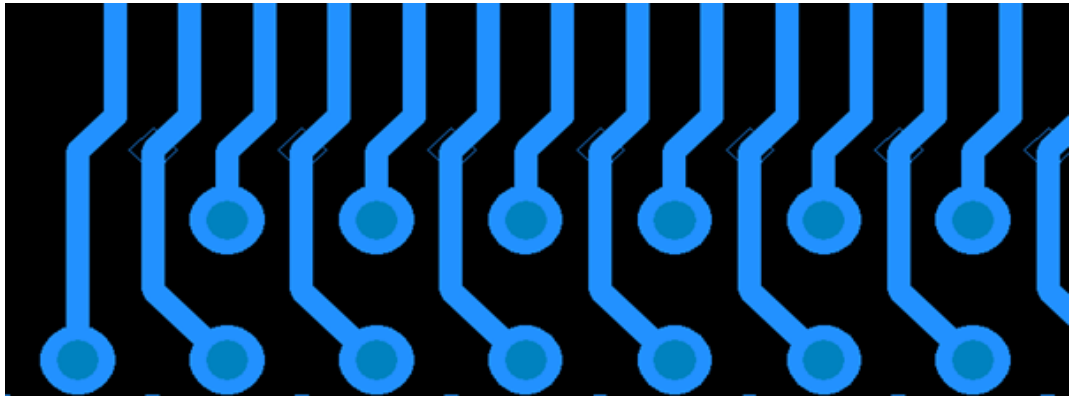
Next generation PCBs (in production)

- 8 layers but only micro-vias between 4 outermost layers
- Breakout on layer 2-4
- 1.3mm thickness for better stiffness
- One version with integrated FPGA and DC-DC converter to enable self-contained module
- One version with just decoupling capacitors, kapton cables to interface boards
- Panel shared with HGCROCv2 test board
  - 300um pitch
  - Large number of individual supply voltages (accessible for test purposes)

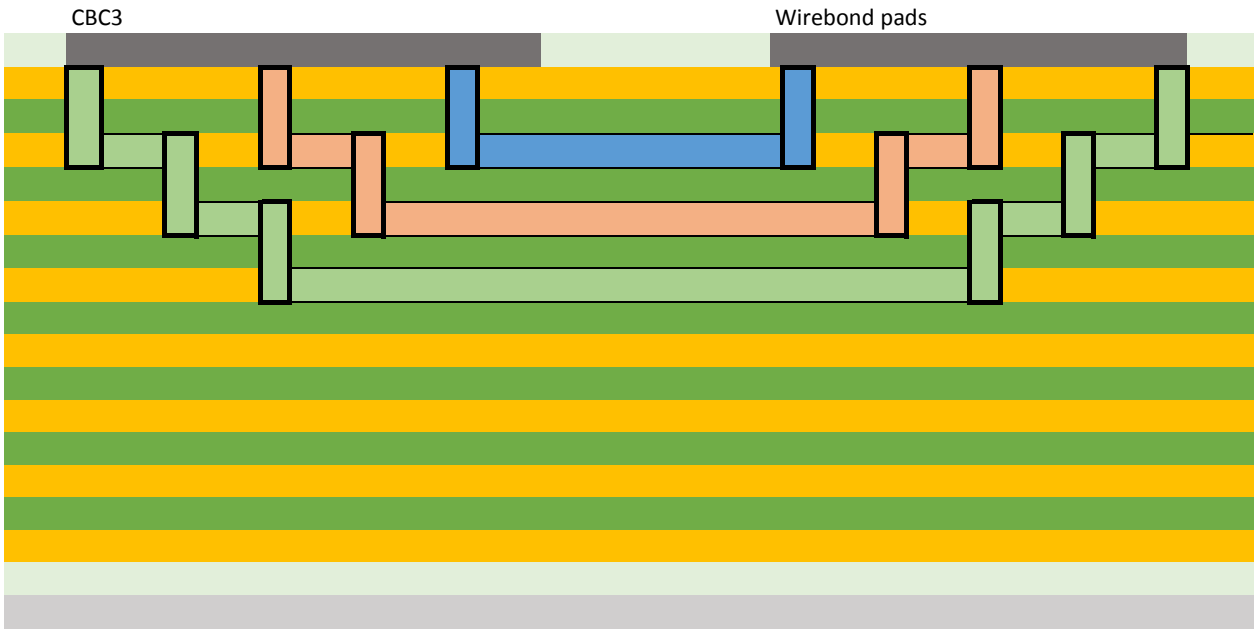


Routing density

Breakout of 2 rows of balls at 250um per layer, 40um traces, 42.5um spacing

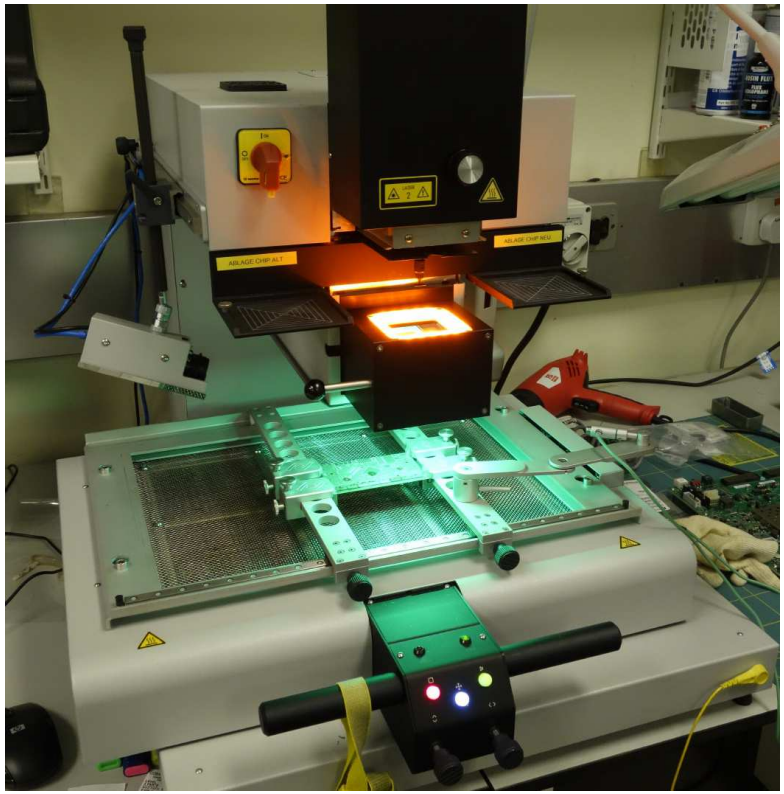


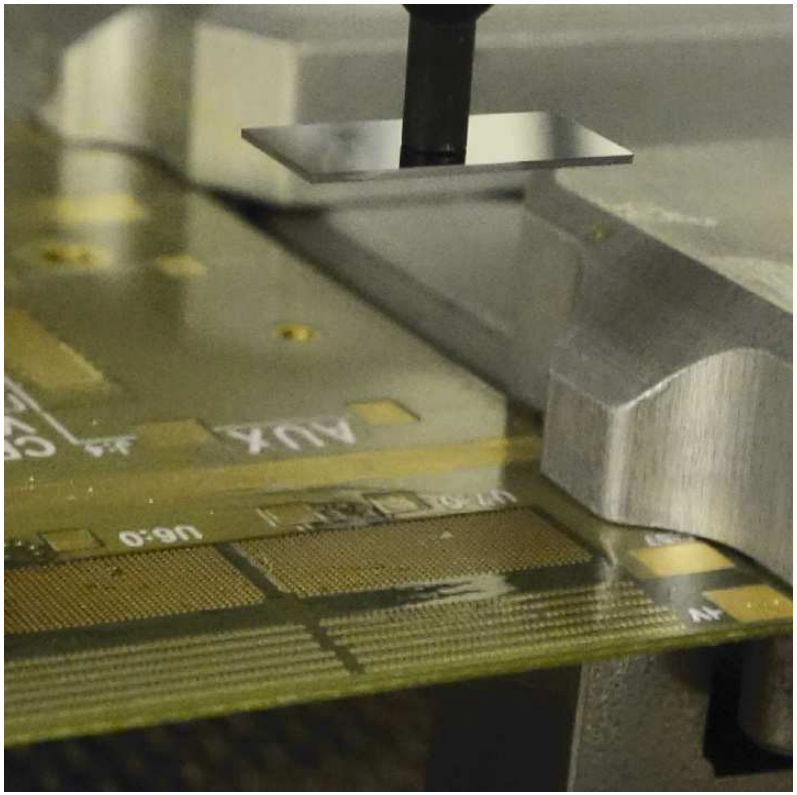
No breakout routing on top layer to avoid wicking along traces



Placement using BGA rework machine

- No solder paste
- Thin coat of sticky flux on PCB (stickiness simplifies handling)

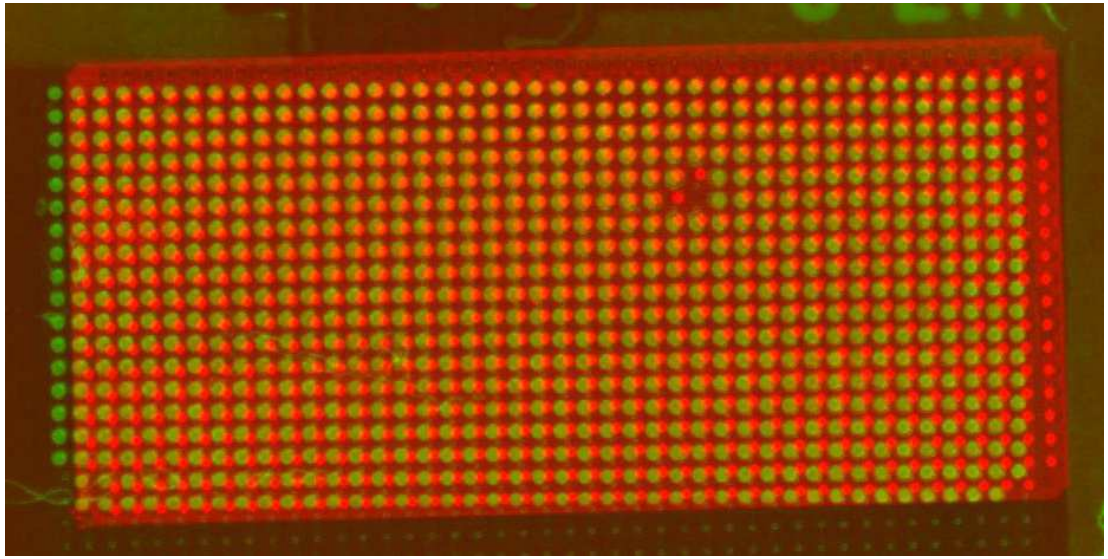




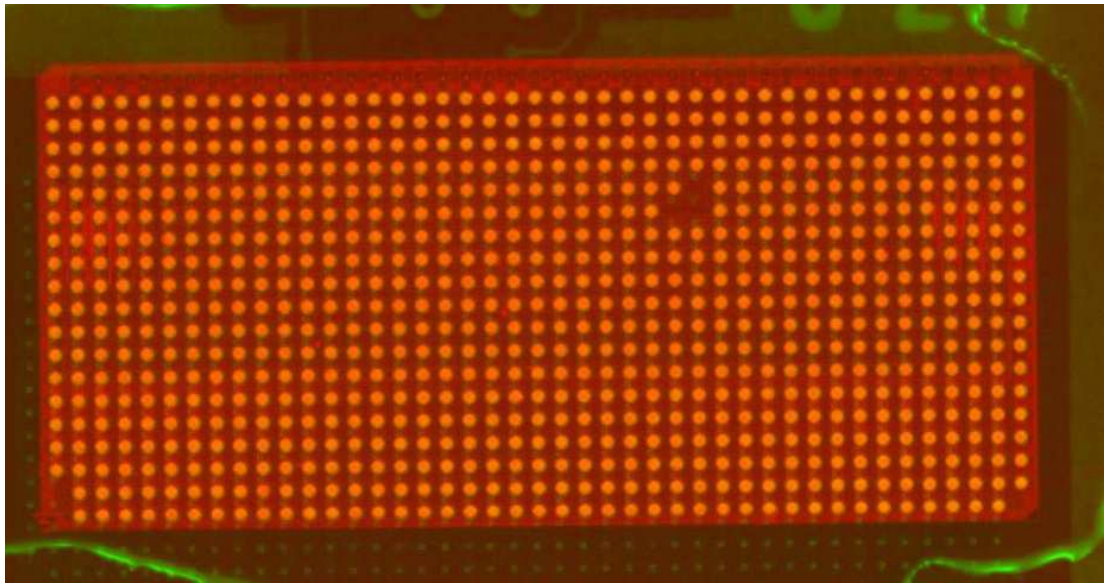
Manual optical alignment

- Board features green
- Chip features red

Misaligned

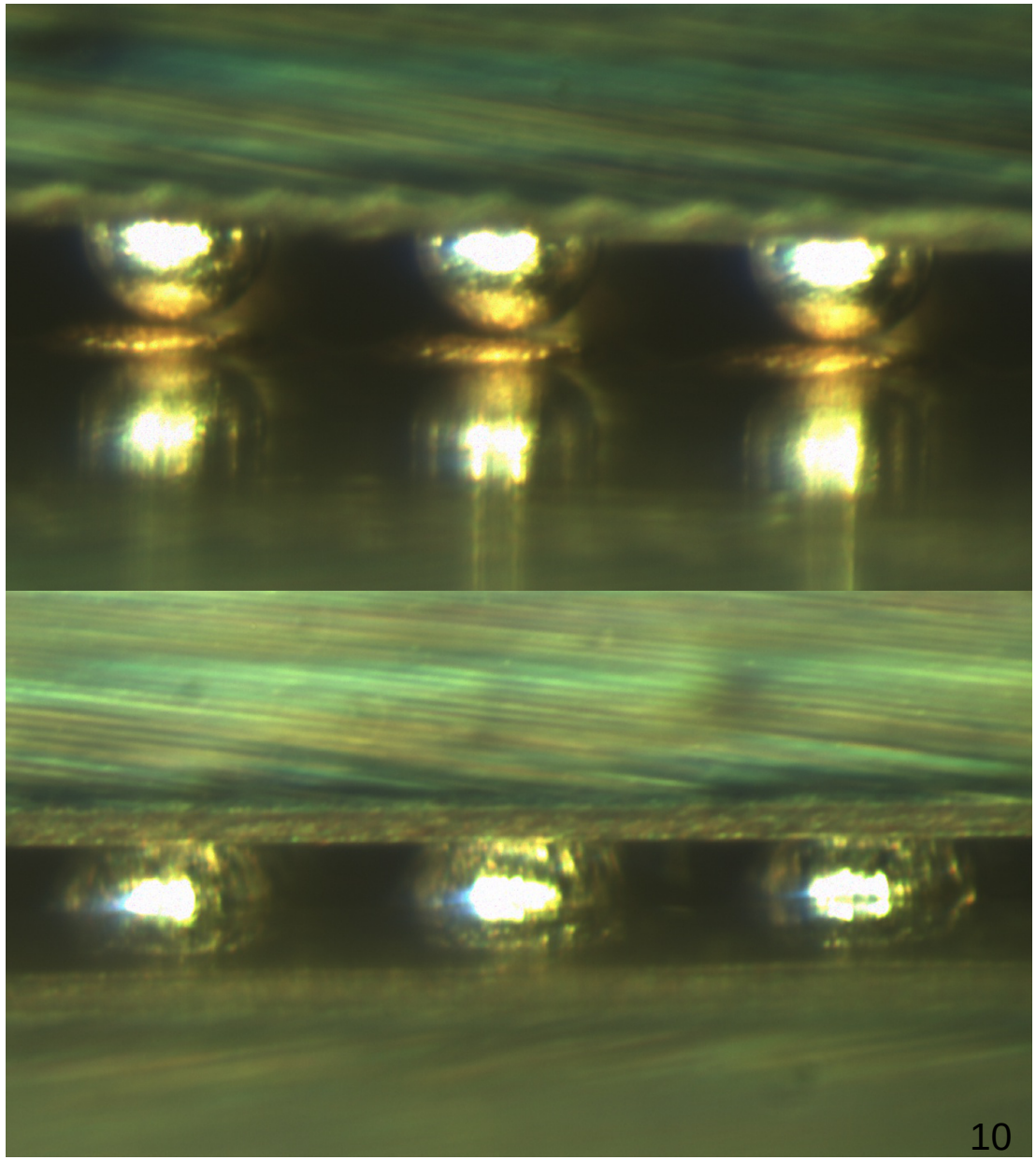


Aligned



Inspection, before and after soldering

- Normal inspection microscope tilted board
- Requires some free space around chip
- Specialized BGA inspection devices offered insufficient resolution



Conclusions

- In-house assembly of flip-chip circuits for testing purposes feasible without specialized equipment
- Soldering failures can usually be fixed by applying more flux and re-running the reflow cycle
- Chip removal and placement of a new chip is also entirely feasible
- Enables quick tests (if the PCB is ordered in advance) and small-volume special purpose assemblies
- Tin-lead or lead-free balls required
- No need for solder paste printing
- Keeping at least one side of the chip free of topside components greatly simplifies inspection
- CTE mismatch gives rise to visible bending of large chips, may affect reliability, but no evidence of failures yet