8CBC3.1 hybrid + CIC mezzanine : first results

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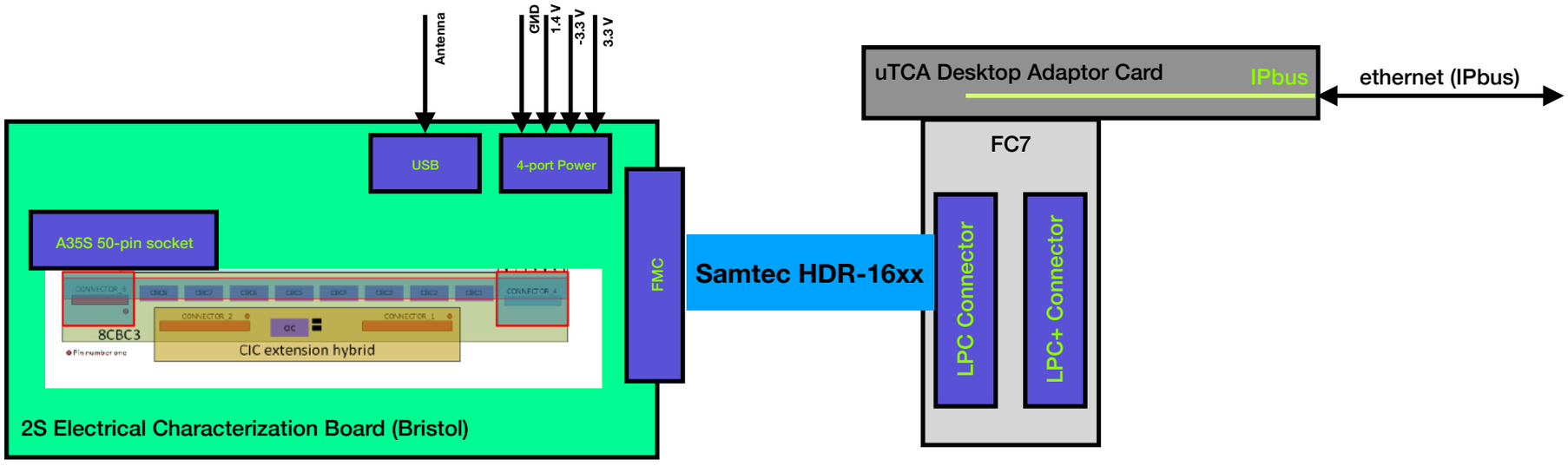
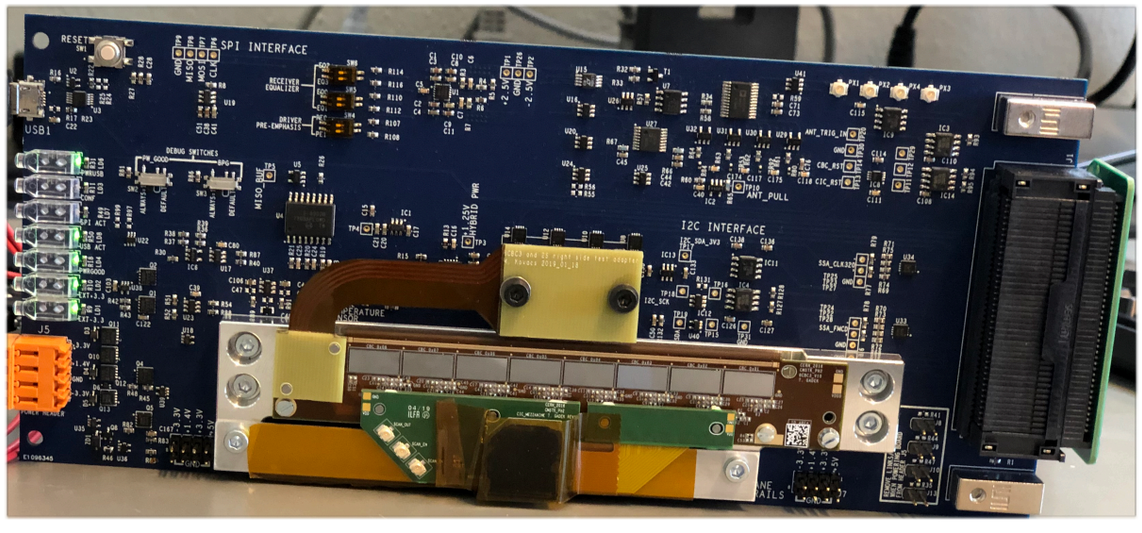
2S FEH prototype (CBC3.1 + CIC) : First Results

Read-out system for electrical readout of 2S FEH prototype

- FC7 based read-out system using :
  - 2S electrical characterization board for translation and buffering of output lines from CIC
  - 8 CBC3.1 hybrid with a CIC extension hybrid
  - Firmware for readout and control of a 2S FEH prototype
  - Software for readout and control of a 2S FEH prototype based on simple python scripts (stand-in for Ph2_ACF)





2S FEH prototype (CBC3.1 + CIC)

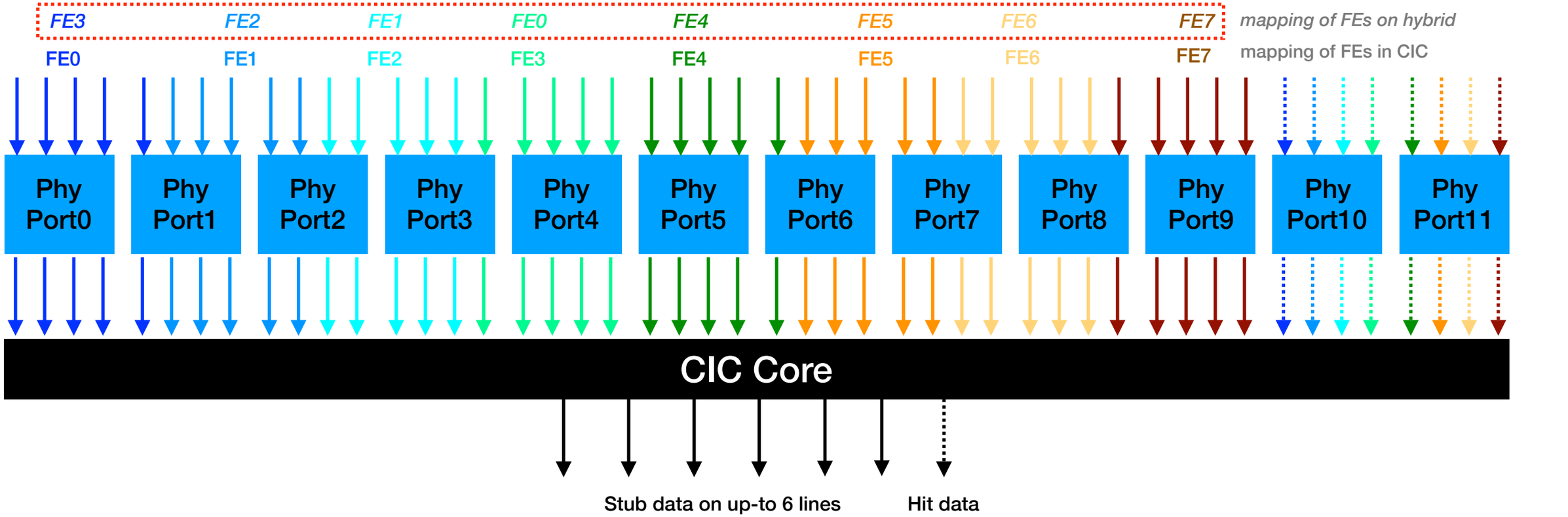
First tests on 2S FEH prototype

- Week of the 15th April spent testing read-out system and performing first checks on the 2S FEH prototype :
  - M. Kovacs organized presence of experts for the entire week
  - power-up checks on 2S electrical characterization board performed at Bristol the previous week
  - experience in operating/working with the CIC courtesy of the stand-alone CIC set-up used for DAQ development
- Once basic connectivity between different components in the set-up was established set-up was used to :
  - confirm connectivity between CIC mezzanine and 8CBC3.1 hybrid
  - demonstrate that stand-alone CIC initialization sequence can be performed with the 2S FEH
  - demonstrate that output of CIC (for hits) is consistent with what we expect from the CBCs under different conditions
  - confirm validity of the automated BX0 identification in the CIC

2S FEH prototype (CBC3.1 + CIC)

Confirming connectivity between CBCs and CIC

- CIC debug mode in which CIC core is bypassed and the output of any given phase aligner port is routed directly to the output lines of the CIC used to verify that all 8 CBCs, once configured, output the expected phase and word alignment patterns :
  - phase aligner ports 0 - 9 are used to phase align the (40) stub data lines from the 8 CBCs (5 per CBC) connected to the CIC
  - phase aligner ports 10 - 11 are used to phase align the (8) hit data lines from the 8 CBCs (1 per CBC) connected to the CIC



- Phase alignment patterns on CBCs are generated by setting a low threshold on all 8 CBCs (so all channels always contain a hit) and using the channel masks to generate stubs with addresses and bends that produce this pattern on the stub output lines

Output from FE0 : CBC configured to output phase alignment pattern (1010) on SLVS lines 0,1,3

	Stub Address 0	Stub Address 1	Stub Address 3	Stub Bend (Stub 0 and Stub1)	Sync Bit, Status bits, Stub Bend (Stub 2)
Clk0:	01010101	10101010	00000000	10101010	10100000
Clk1:	01010101	10101010	00000000	10101010	10100000
Clk2:	01010101	10101010	00000000	10101010	10100000
Clk3:	01010101	10101010	00000000	10101010	10100000

pattern also appears here because sync bit is always there and hit OR logic is enabled

2S FEH prototype (CBC3.1 + CIC)

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- Goals of the week were to :
  - confirm connectivity between 2S electrical characterization board, FC7, and 2S FEH
    - ✓ is the CIC receiving the clock and hard reset signals?
    - ✓ is the CIC receiving the fast commands?
    - ✓ do all chips respond to I2C read and write commands?
  - confirm connectivity between CIC mezzanine and 8CBC3.1 hybrid
    - ✓ do the configured CBCs output phase and word alignment patterns ?
  - demonstrate that stand-alone CIC initialization sequence can be performed with the 2S FEH
    - ✓ can the complete initialization sequence be performed on the 2S FEH?
  - record response to a resync and effect on Bx0

2S FEH prototype (CBC3.1 + CIC)

CIC Initialization Sequence

- Initialization sequence based on CIC1 power on and initialization guide provided by Lyon : same sequence used for the CIC standalone DAQ tests

CIC Power on Sequence

Step	Action
	Enable CIC Alim
	Launch the CIC Clock generation @320MHz
	Set the active low CIC Hard Reset to '1'
	increase the dll current
Phase Alignment	set the phyport in auto startup mode
	apply a SoftReset
	release the SoftReset
	check all dll are correctly locked
Phase Alignment	Apply signals to the CIC inputs
Phase Alignment	Check that all the channels are correctly locked
FC Locking	Launch the emission of the FC frame to the CIC
FC Locking	Check fc decoder locking state
FC Locking	Send a Resync
FC Locking	Check fc decoder correctly receive a Resync
Word Alignment	Set the pattern you want to use to align each trigger line
Word Alignment	Disable the using of the external alignment value
Word Alignment	Ask for the auto alignment
Word Alignment	Resync
Word Alignment	Send continuously the patterns on every line for each enabled FE
Word Alignment	check if the alignment is correctly done
Word Alignment	Deassert the wa request

Phase and word alignment patterns used in initialization sequence

Pattern	SLVS1	SLVS2	SLVS3	SLVS4	SLVS5
phase alignment	0b01010101	0b10101010	0b00000000	0b1010 1010	0b1010 0000
phase alignment	0b10000000	0b10000001	0b10101010	0b1010 1010	0b1010 1010
word alignment	0b01111010	0b10111100	0b11010100	0b0001 0011	0b1010 0001

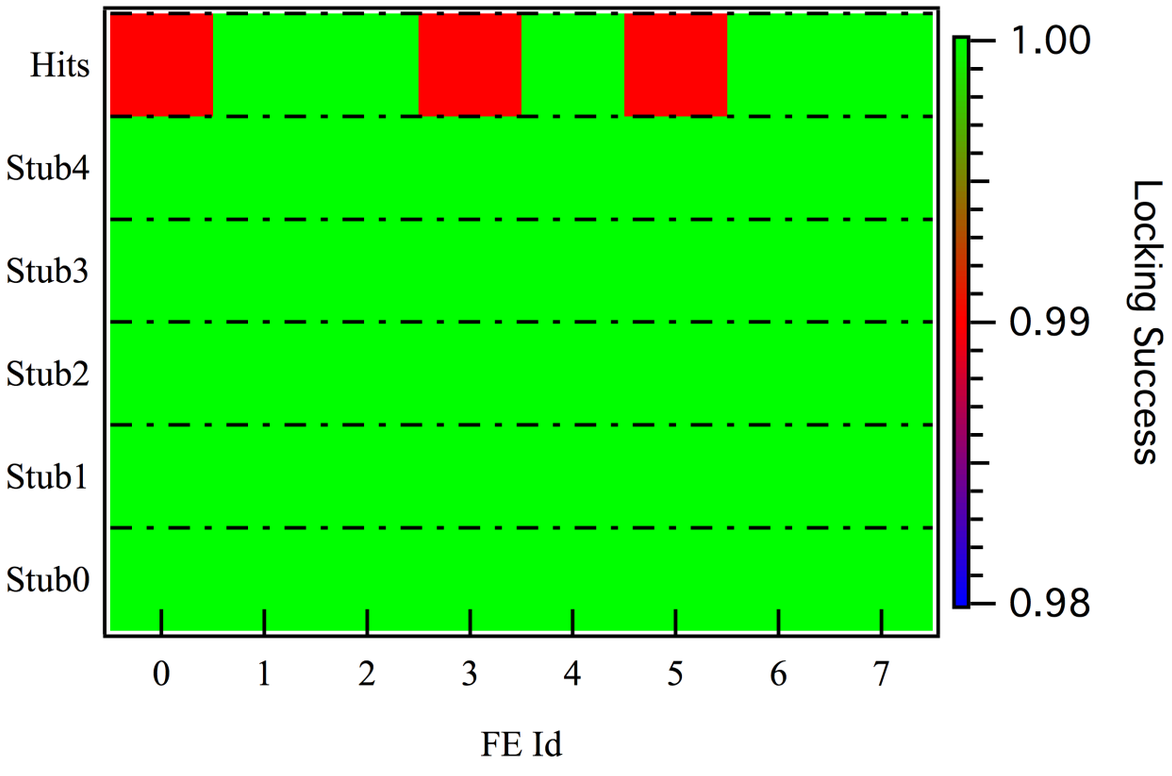
- Phase and word alignment steps require configuring the CBCs to generate specific patterns on each of the 6 output lines (5 stubs, 1 hit)
  - Patterns produced by lowering threshold and masking all channels but those required to generate stubs/bends/hits corresponding to patterns needed for specific alignment procedure :
    - tuning of the data on the hit lines also requires sending L1 triggers to the CBCs; triggers generated internally in the FC7 at 1MHz and back-pressure is disable
  - Phase alignment done in three steps; impossible to generate a 10101010 pattern on all 5 stub data lines* simultaneously
    - first on three of the six stub lines (SLVS0 , SLVS1 , SLVS3 for all CBCs)
    - then on another three of six stub lines (SLVS2 , SLVS3 , SLVS4 for all CBCs)
    - then on the last SLVS line containing hit data(SLVS5 for all CBCs)
  - Word alignment done in one step on the 5 stub data lines (SLVS0, SLVS1, SLVS2, SLVS3 , SLVS4)

2S FEH prototype (CBC3.1 + CIC)

CIC Initialization Sequence : Phase alignment on hit and stub data lines

- Execute CIC initialization sequence and request CIC to identify phase on 8x6 SLVS lines from CBCs with the phase aligner running in auto-startup mode
    - Perform phase alignment sequence and check that all channels locked correctly (read-back I2C registers from CIC) :
        - the stub data lines from the CBCs preceded by configuring CBCs so that phase alignment pattern appears on 3 lines at a time
        - the hit data lines from the CBCs preceded by configuring CBCs so that phase alignment pattern appears in hit data
        - allow 1 s for automated phase aligner block to run

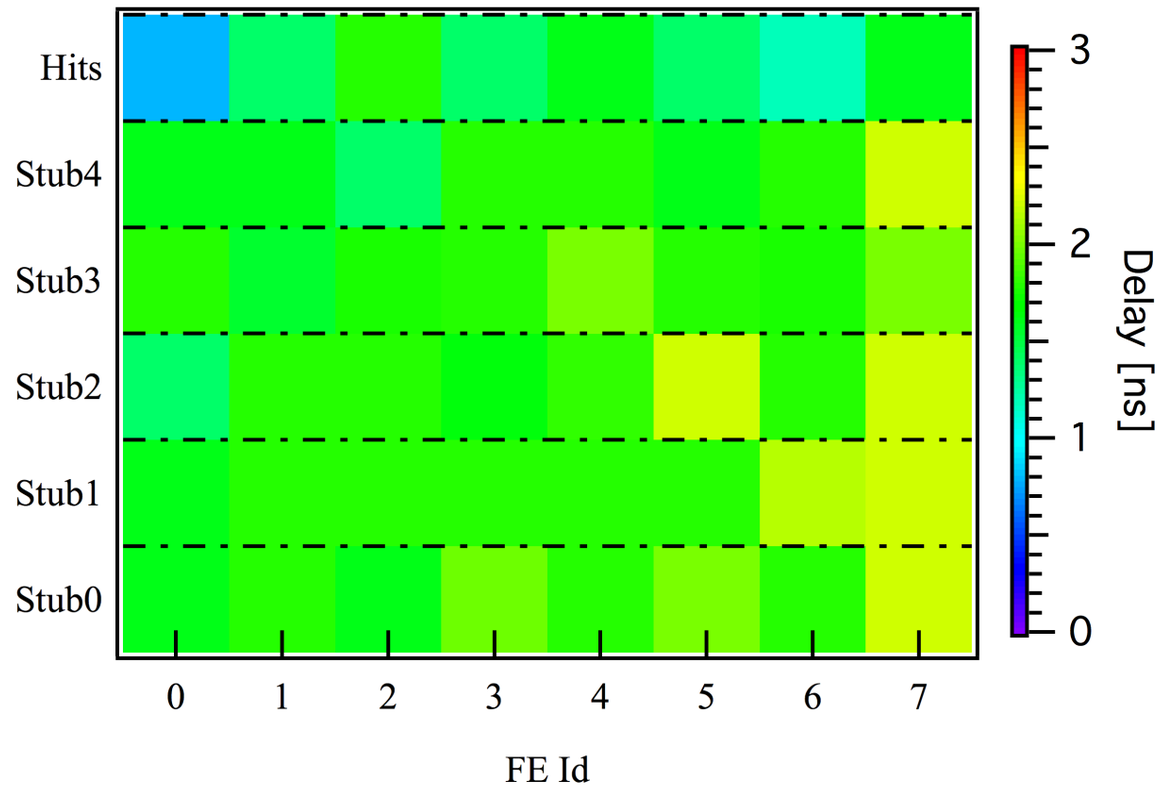
Automated phase alignment locking Success per FE



x100 iterations - 100% success on all but hit lines

1/100 failures on hit lines shown (also fails word alignment)

Average reported phase per FE [0.8 - 2.2ns]



2S FEH prototype (CBC3.1 + CIC)

CIC Initialization Sequence : Data quality check after phase alignment (hits only)

- Execute CIC initialization sequence and request CIC to identify phase on 8x6 SLVS lines from CBCs with the phase aligner running in auto-startup mode
  - Perform phase alignment sequence and check that all channels locked correctly (read-back I2C registers from CIC) :
    - the stub data lines from the CBCs preceded by configuring CBCs so that phase alignment pattern appears on 3 lines at a time
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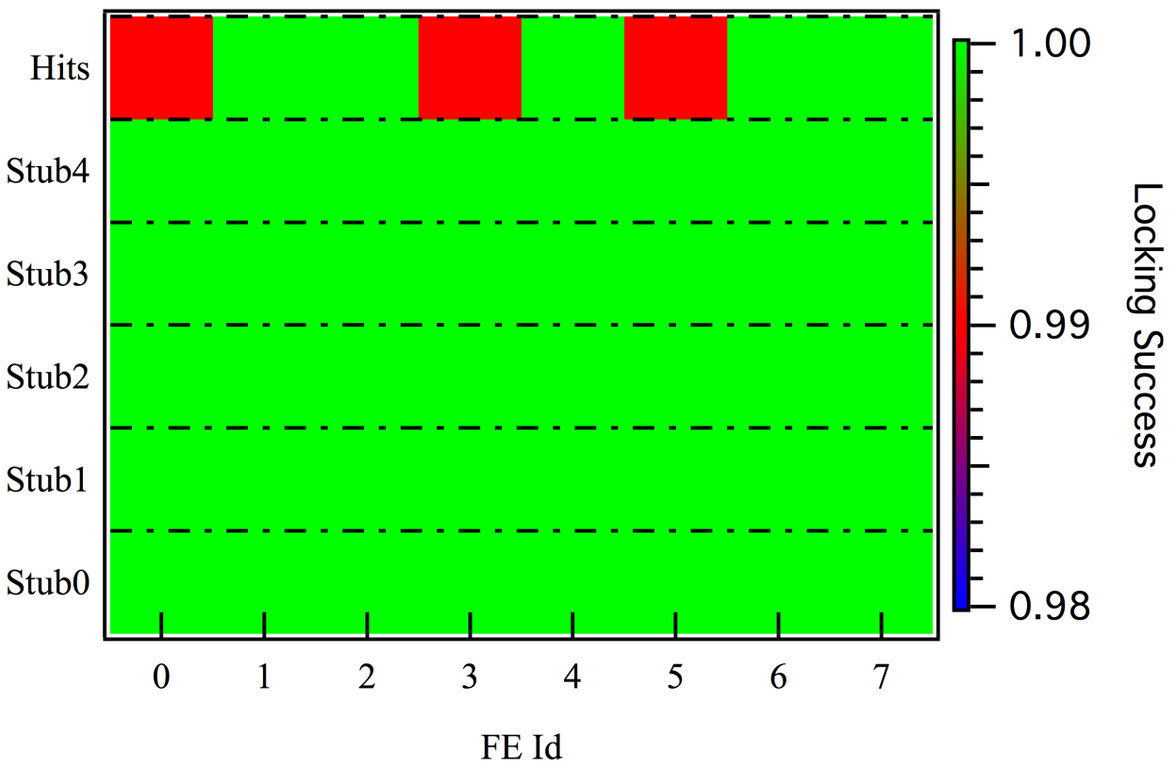
    - allow 1 s for automated phase aligner block to run

Automated phase alignment locking Success per FE



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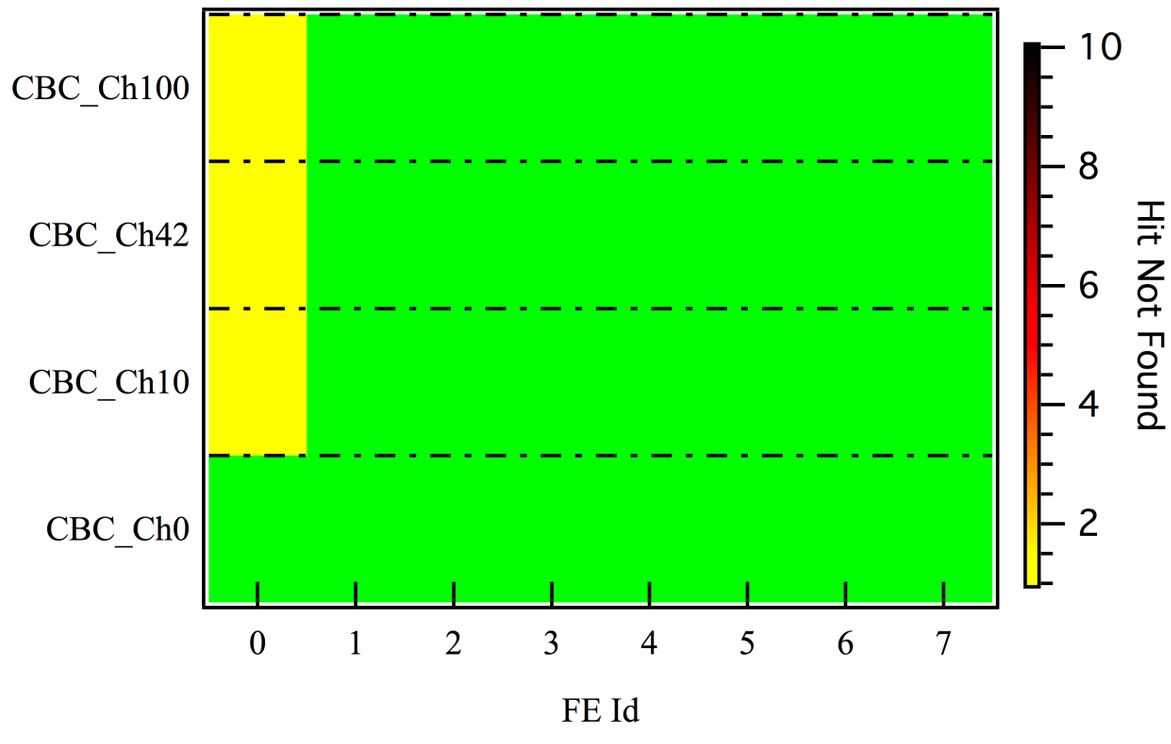
1/100 failures on hit lines shown (also fails word alignment)

Mismatches in connected CBCs



validation with stubs still not completed!

- Checking data post CIC initialization sequence using a given hit pattern [all channels except for 0, 10, 42 and , 100 masked]
  - configure CBCs to continuously output a specific hit pattern (CIC outputting unsparsified CBC data)
  - read-back and decode CIC hit (L1) data and check for any mismatches

2S FEH prototype (CBC3.1 + CIC)

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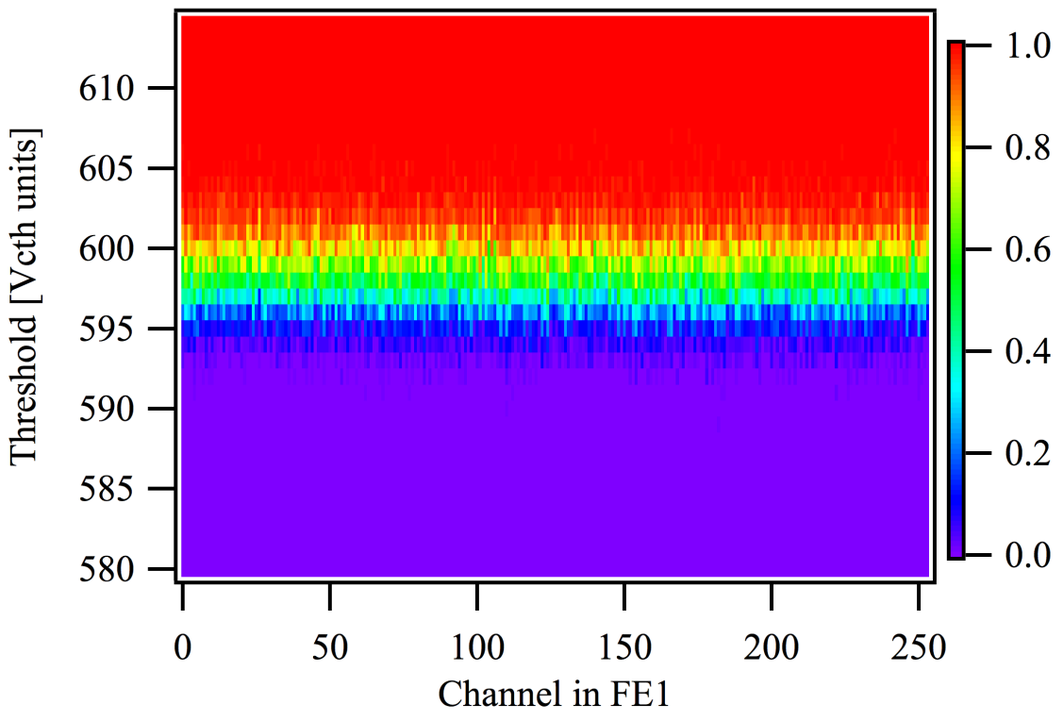
  - experience in operating/working with the CIC courtesy of the stand-alone CIC set-up used for DAQ development
- Goals of the week were to :
  - confirm connectivity between 2S electrical characterization board, FC7, and 2S FEH
    - ✓ is the CIC receiving the clock and hard reset signals?
    - ✓ is the CIC receiving the fast commands?
    - ✓ do all chips respond to I2C read and write commands?
  - confirm connectivity between CIC mezzanine and 8CBC3.1 hybrid
    - ✓ do the configured CBCs output phase and word alignment patterns ?
  - demonstrate that stand-alone CIC initialization sequence can be performed with the 2S FEH
    - ✓ can the complete initialization sequence be performed on the 2S FEH?
  - demonstrate that FE ASICs (CBCs) on hybrid can be configured correctly for data taking
    - ✓ can we measure the pedestal and noise on all 8 ASICs on the hybrid?
  - confirm validity of the automated BX0 identification in the CIC
    - ✓ use automated BX0 identification in CIC to measure the delay (in 40 MHz clock cycles) between the reception of a resync (fast reset) and the reception of the first data packet with a predefined pattern
    - ✓ record response of all 8 CBCs on hybrid to a fast reset (Resync)

2S FEH prototype (CBC3.1 + CIC)

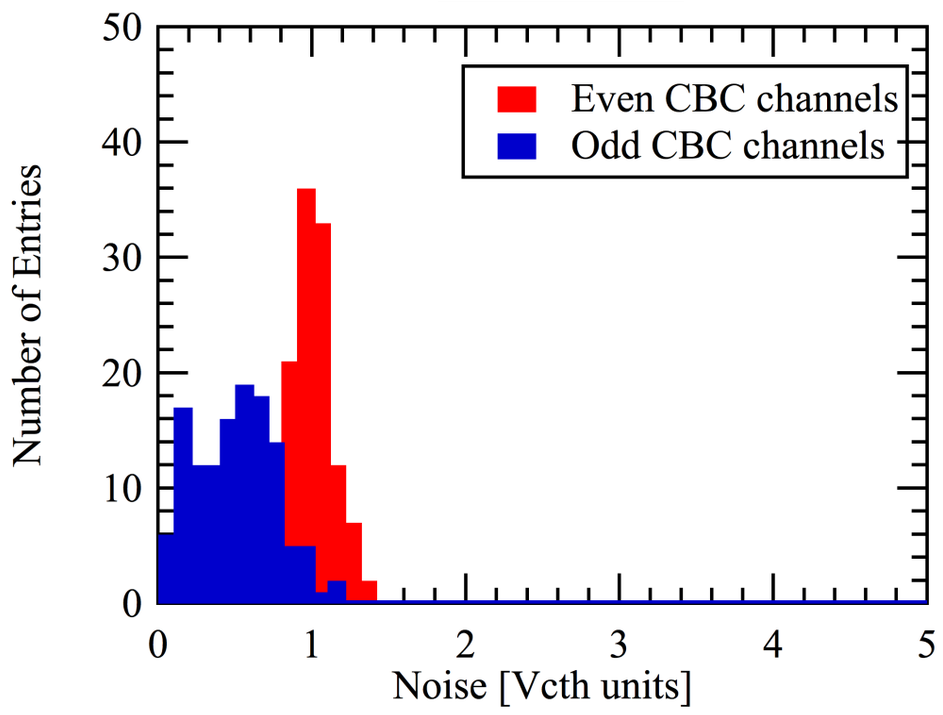
Equalize response of CBCs : offset tuning and pedestal/noise measurement

- Ensure that CBCs are tuned correctly (uniform response across all channels)
  - configure CIC to output CBC hit data in unsparsified mode
  - triggering and event generation using standard μDTC firmware (internal trigger generation + DDR3 readout)

CBC1 S-curves



Noise in CBC1



to be verified with Ph2_ACF

Generic L1A chip event format (μDTC)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	Error Code				Hybrid ID								Chip ID				Total L1A Data Size (128bit words)											
1																	Chip Type				Frame Delay (Timeout Counter)											
2	Chip Header Space																															
3	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
4	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
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...	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
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2S FEH prototype (CBC3.1 + CIC)

CIC BX0 alignment Sequence

- BX0 alignment sequence based on CIC1 power on and initialization guide provided by Lyon : same sequence used for the CIC standalone DAQ tests

CIC BX0 Alignment Sequence

Bx0 Alignment	Chose the trigger line used to perform this alignment
Bx0 Alignment	Disable the using of the external alignment value
Bx0 Alignment	Ask for the auto alignment
Bx0 Alignment	Resync
Bx0 Alignment	FE chip send the recognizable pattern
Bx0 Alignment	check if the alignment is correctly done
Bx0 Alignment	Deassert the auto Bx0 request

Patterns used in BX0 alignment sequence

Pattern	SLVS1	SLVS2	SLVS3	SLVS4	SLVS5
bx0 alignment	**0b00010010**	**0b00100010**	**0b01000010**	**0b00100010**	**0b10000010**

- BX0 alignment require configuring the CBCs to generate specific patterns on **any** of the 5 stub lines :
  - line to perform alignment on configurable in CIC
- Require pattern to appear in exactly one bunch crossing (to avoid any ambiguity in the measurement); therefore patterns are produced in a slightly different way than the other alignment procedures :
  - on-chip test pulse used to generate hits in channels belonging to a specific group of channels in each of the 8 CBCs
  - channel masks used to generate stubs with seed positions and bends that match the alignment pattern on each of the 5 stub data lines
  - a dedicated triggering finite-state-machine in the uDTC is used to generate triggers that consists of :
    - a fast reset (fast command recognized by the CBC and the CIC) a wait for N clock cycles
    - a test pulse trigger (fast command recognized by the CBCs); this initializes a test pulse from the on-chip test pulse generator circuit
    - a wait for M clock cycles
    - an L1A/trigger (fast command recognized by the CBC and the CIC)

2S FEH prototype (CBC3.1 + CIC)

CIC BX0 alignment Sequence : confirm uniform response across hybrid

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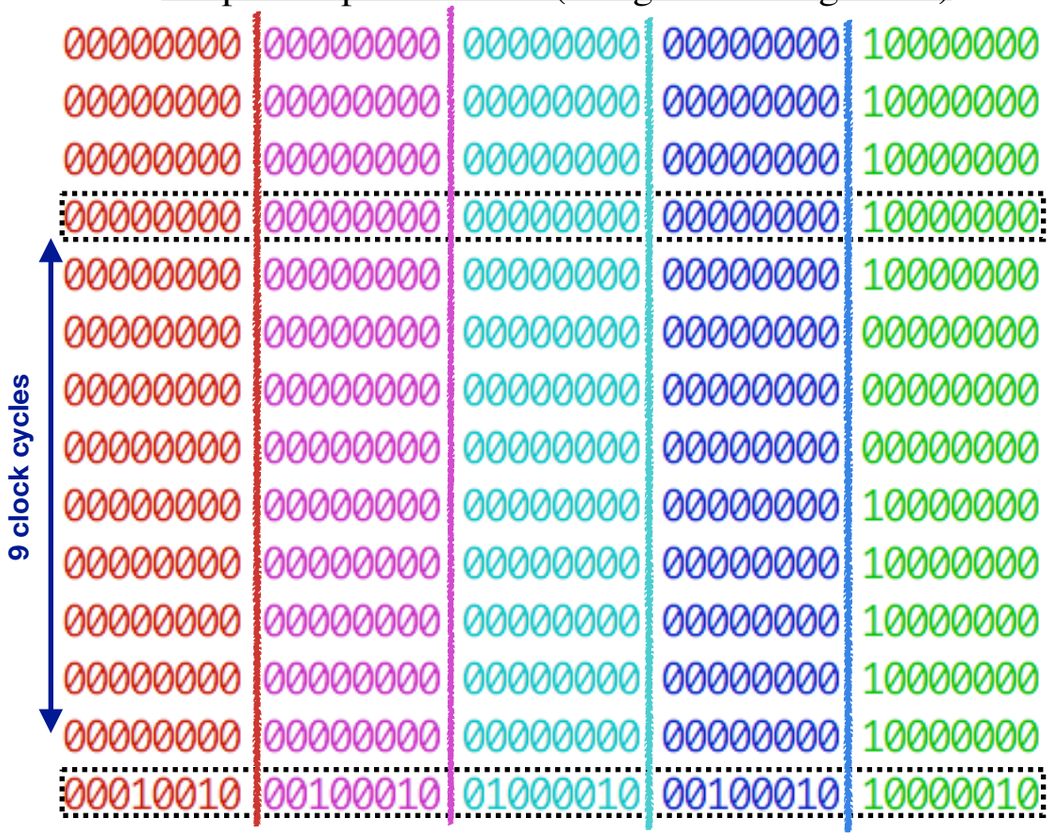
- CBCs configured to generate BX0 alignment pattern on each of the SLVS lines in turn

Scoped output of CBCs (using CIC debug mode)



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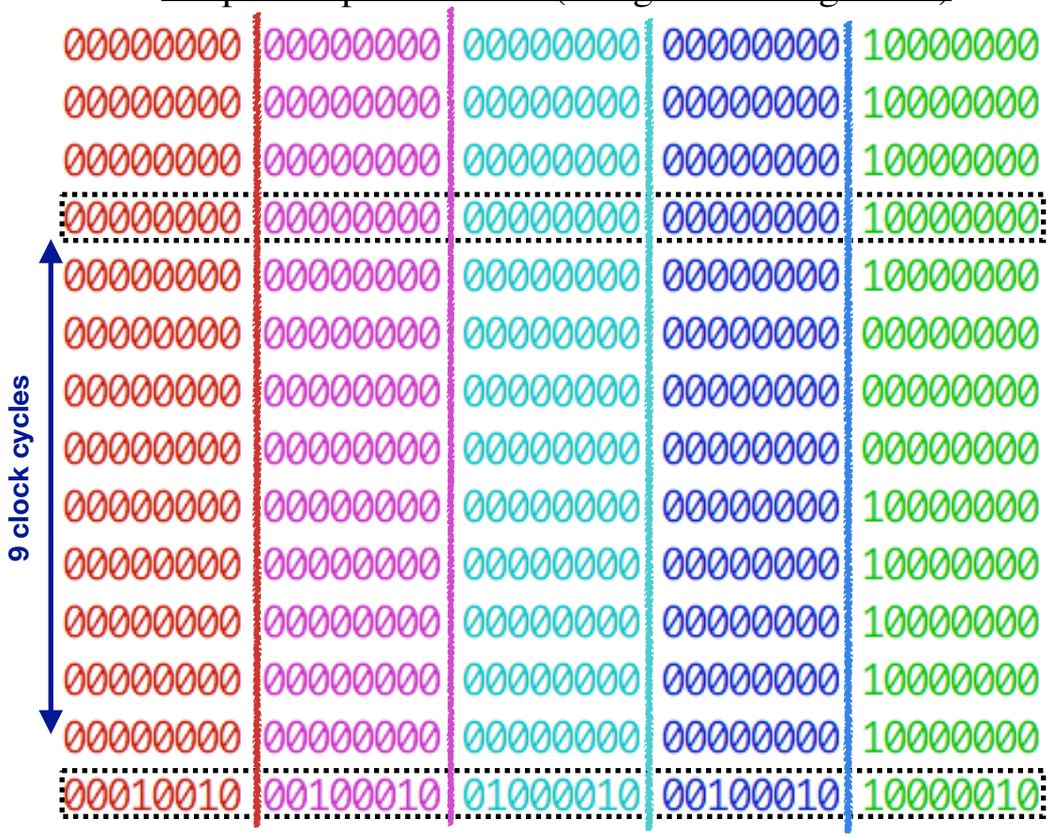
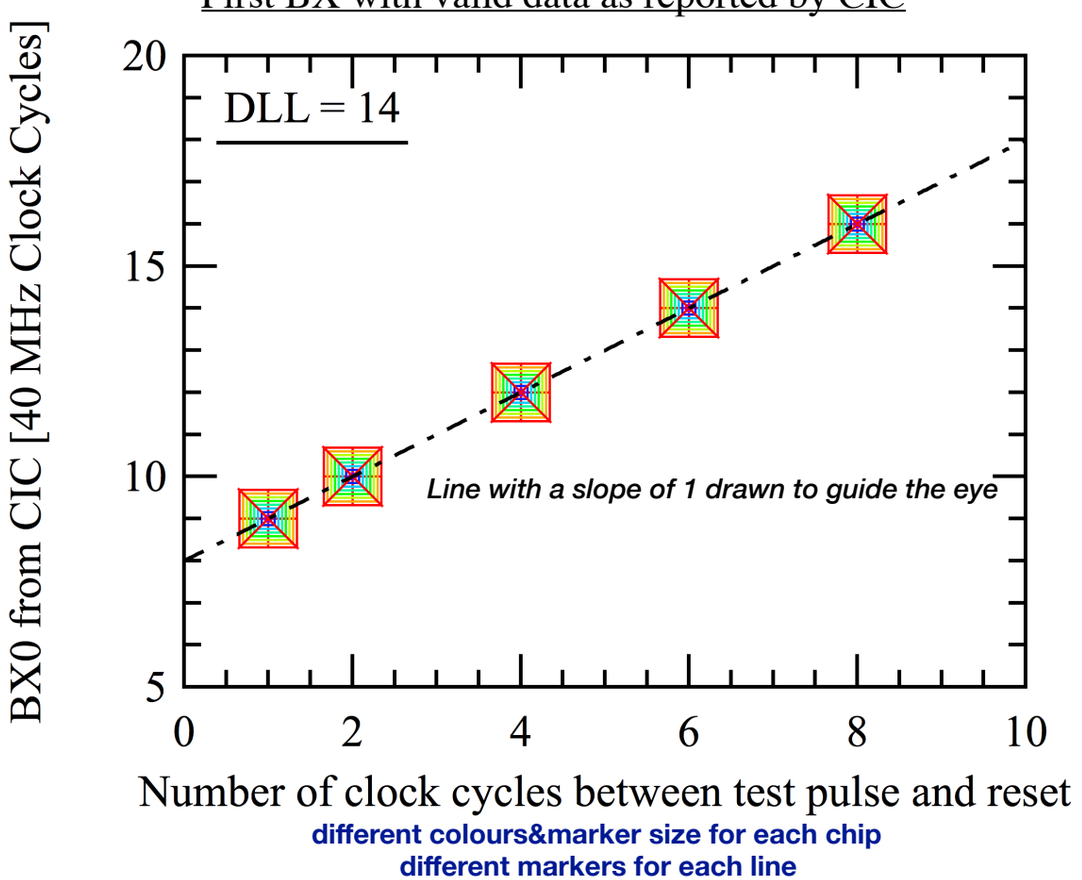
- CBCs configured to generate BX0 alignment pattern on each of the SLVS lines in turn
- Delay (in 40 MHz clock cycles) measured by the CIC recorded for all CBCs and SLVS lines:
  - delay is the same for all lines on a hybrid (for a given DLL setting)
  - delay varies as the time between the fast resync and the injected pattern is varied (time between resync and test pulse trigger)

Scoped output of CBCs (using CIC debug mode)





2S FEH prototype (CBC3.1 + CIC)

Follow-up tests on 2S FEH prototype

- Perform data quality checks on stub data (similar to what was done for hit data)
- Use set-up to further investigate response of FE ASCICs to fast commands (resyncs , orbit resets, etc.)
- Repeat tests on all available hybrids
- And a lot more …

Back-up

2S FEH prototype (CBC3.1 + CIC)

CIC Initialization Sequence [comparison with theoretical calculations]

- Execute CIC initialization sequence and request CIC to identify phase on 8x6 SLVS lines from CBCs with the phase aligner running in auto-startup mode
  - Perform phase alignment sequence and check that all channels locked correctly (read-back I2C registers from CIC) :
    - the stub data lines from the CBCs preceded by configuring CBCs so that phase alignment pattern appears on 3 lines at a time
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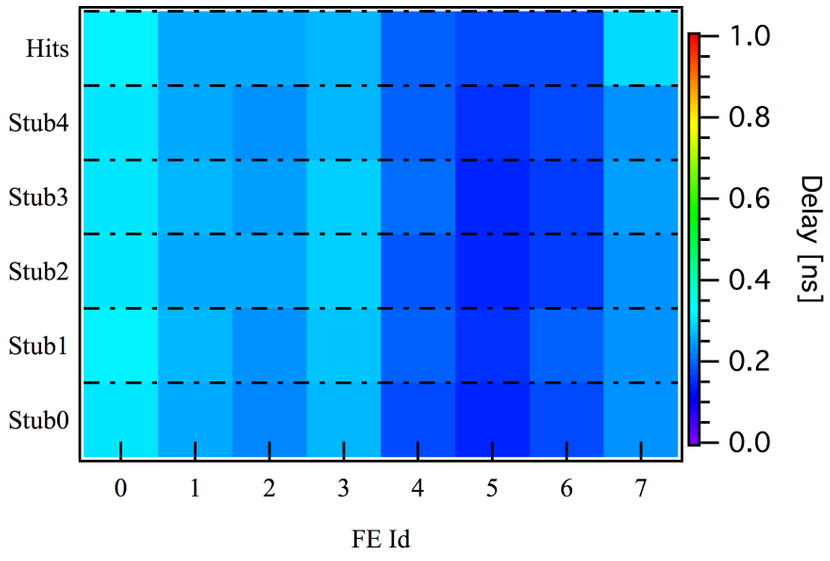
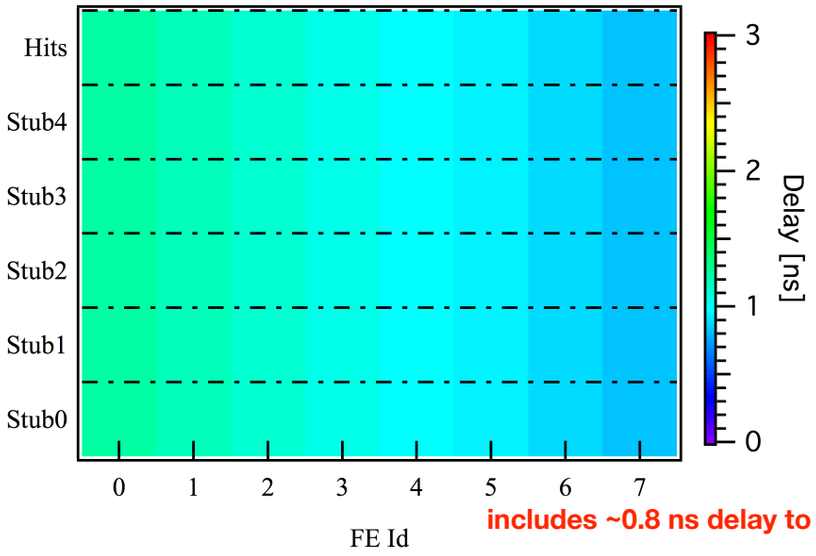
    - allow 1 s for automated phase aligner block to run

Theoretical Line on hybrid from Mark [0.2-0.3 ns]



Theoretical clock delays on hybrid from Mark [0.84-1.25ns]



includes ~0.8 ns delay to CIC

Average reported phase per FE [0.8 - 2.2ns]