CBC3 summary

2019-05-13

Overview of CBC and history

- **APV25** used in current CMS outer tracker, wire-bonded, 0.25um CMOS (1999).
- **CBC1** 128 channels, 40 MHz serial readout (L1 triggered data only) and integrated DC-DC converter for powering from 2.5V. Wire-bonded, 0.13um CMOS (2011).
- **CBC2** 254 channels to support 2-sensor hybrids with stub generation logic, but no stub readout data link. Stub-present flag was used for evaluating the stub logic. Bump-bonded but retains one row of wire-bond pads for testing (2013).
- **CBC3** Full stub generation logic, DC-DC converter removed, first wafers available late 2016.
- **CBC3.1** Bug fixes and minor improvements, first wafers available September 2018.
- No further revisions foreseen, design project formally ended at the end of March.

Basic Characteristics

- 254 Channels, 512 element pipeline.
- 1 MHz average readout rate, up to 32 consecutive triggers.
- Stub finding logic for generating trigger stubs with programmable window size and offset between sensors
- Fast command input and data output at SLVS levels at 320Mbit/s.
- Integrated DLL for adjusting the event sampling time with 1ns resolution.
- Designed for 5cm N-in-P sensors strip sensors.
- 1.2-1.25V power supply, 500uW/ch.

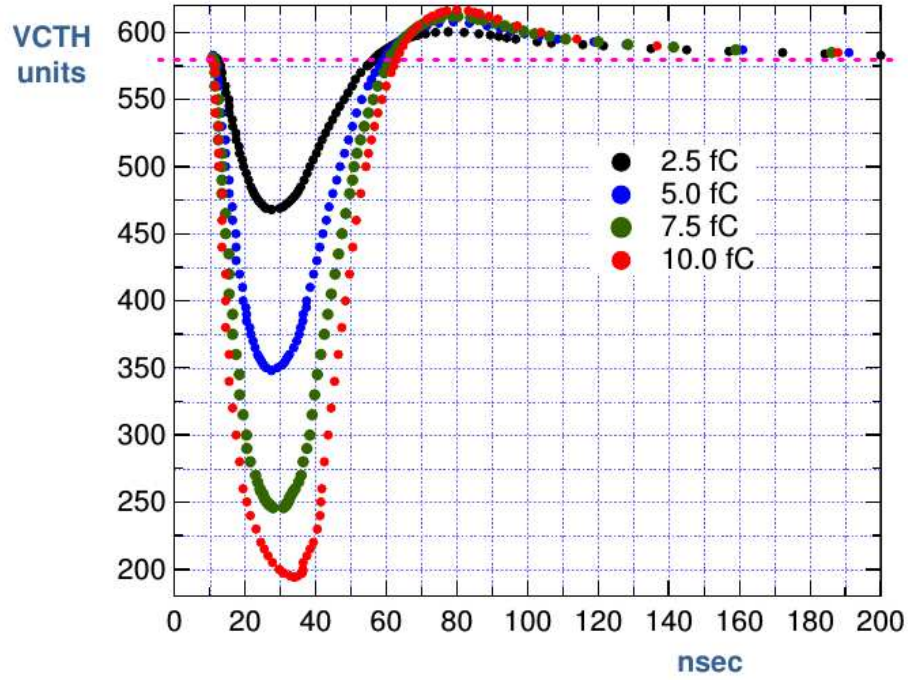
Recommended settings can be found at:
http://www.hep.ph.ic.ac.uk/ASIC/cbc3/cbc3i2c/CBC_I2CREGS_PAGE1_EXAMPLE.txt

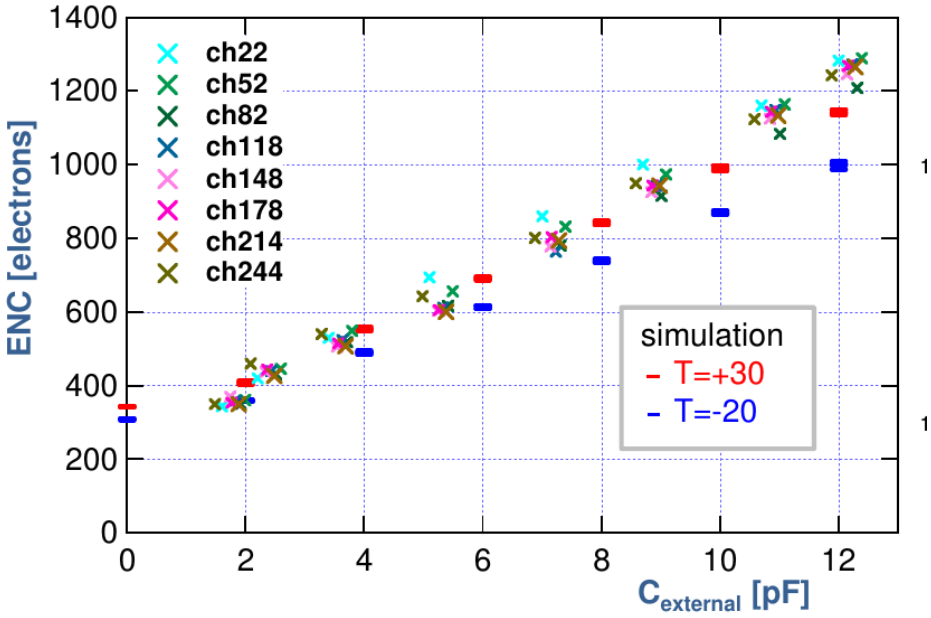
Power consumption

State	I_{VDD} (Digital)	I_{VLDOI} (Analog)
CBC3 Unconfigured or hard reset	30.5mA	100.7mA
CBC3.1 Unconfigured or hard reset	30.5mA	≈48mA
Configured for normal operation	30.5mA	79.5mA
Worst-case increase due to TID at CMS	+3.5mA	
Ipre1 register MSB set SEU (never seen yet)		+70mA
Manufacturing variations	≈2mA	±11mA

See also:
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2018_05_09_power_0509.pdf
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2018_12_05.txt
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2018_12_04_CBC3_20181204.pdf

Pulse shape and noise characterization

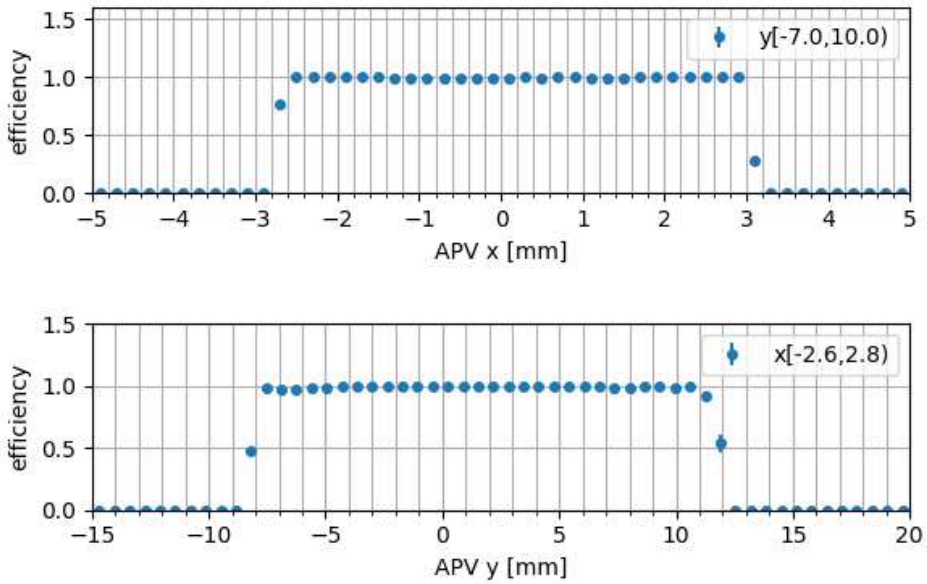


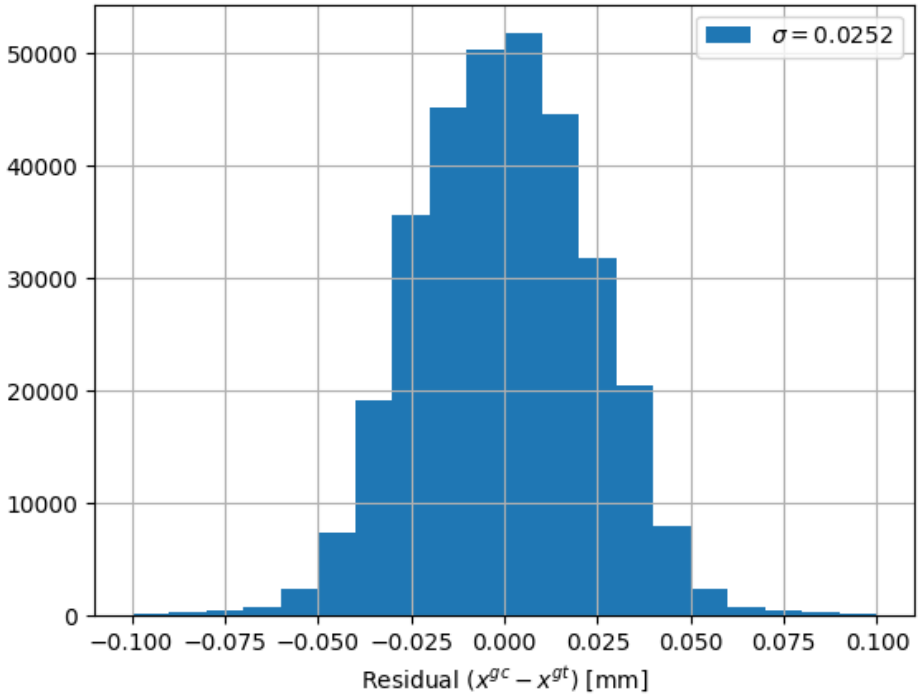


- Peaking time <20nsec.
- Pulse return to baseline within 50 nsec.

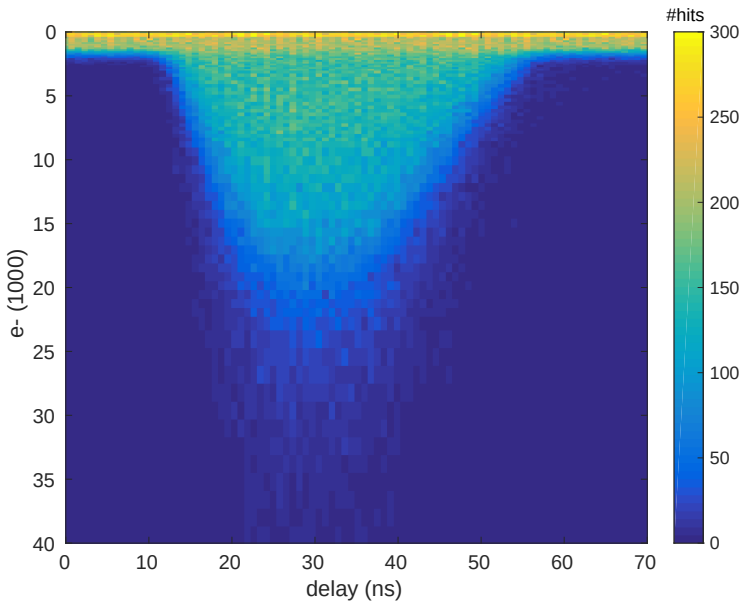
For more details see:
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/CBC3_FE_measurements.pdf

Beam tests



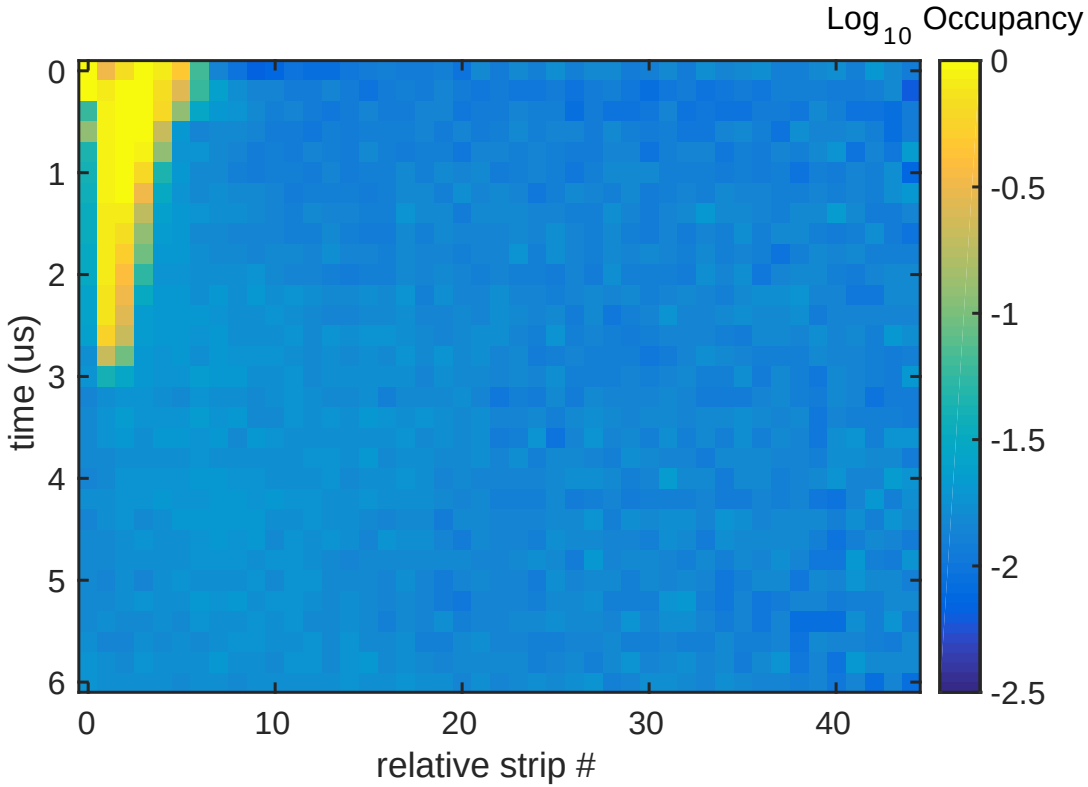


- $> 99.5\%$ efficiency.
- 25um resolution (as expected).
- Pulse shape according to expectations.



HIP-like tests with Xenon Ions, V_b=-64V

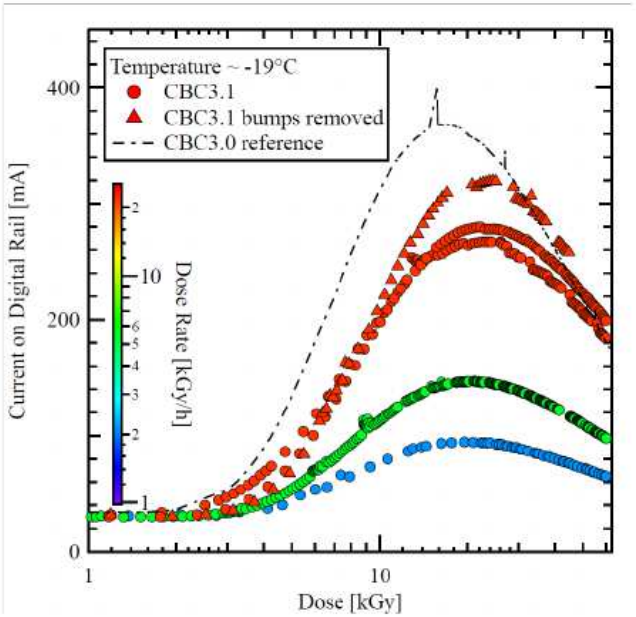
- Xe^{+54} deposits about 3000 MIP at full bias.
- Sensor operated at reduced bias to reduce overload.
- Q ≈ 1700 MIP at V_b=-64V corresponds to just over 4 pC (worst-case HIP).
- HIP effect localized and decays reasonably quickly.



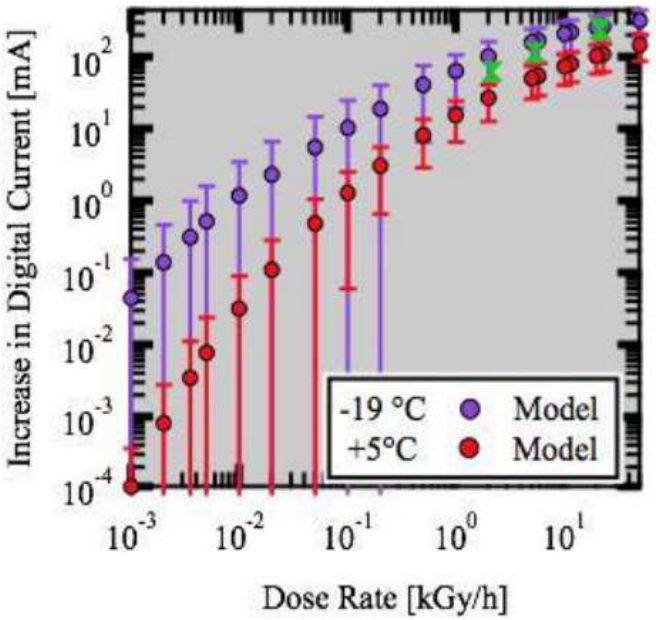
For additional measurements and simulations see:
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2017_12_12_tw_dec2017.pdf
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/CBC3_FE_measurements.pdf

TID effects

Digital current



Digital current peak measurements & extrapolation



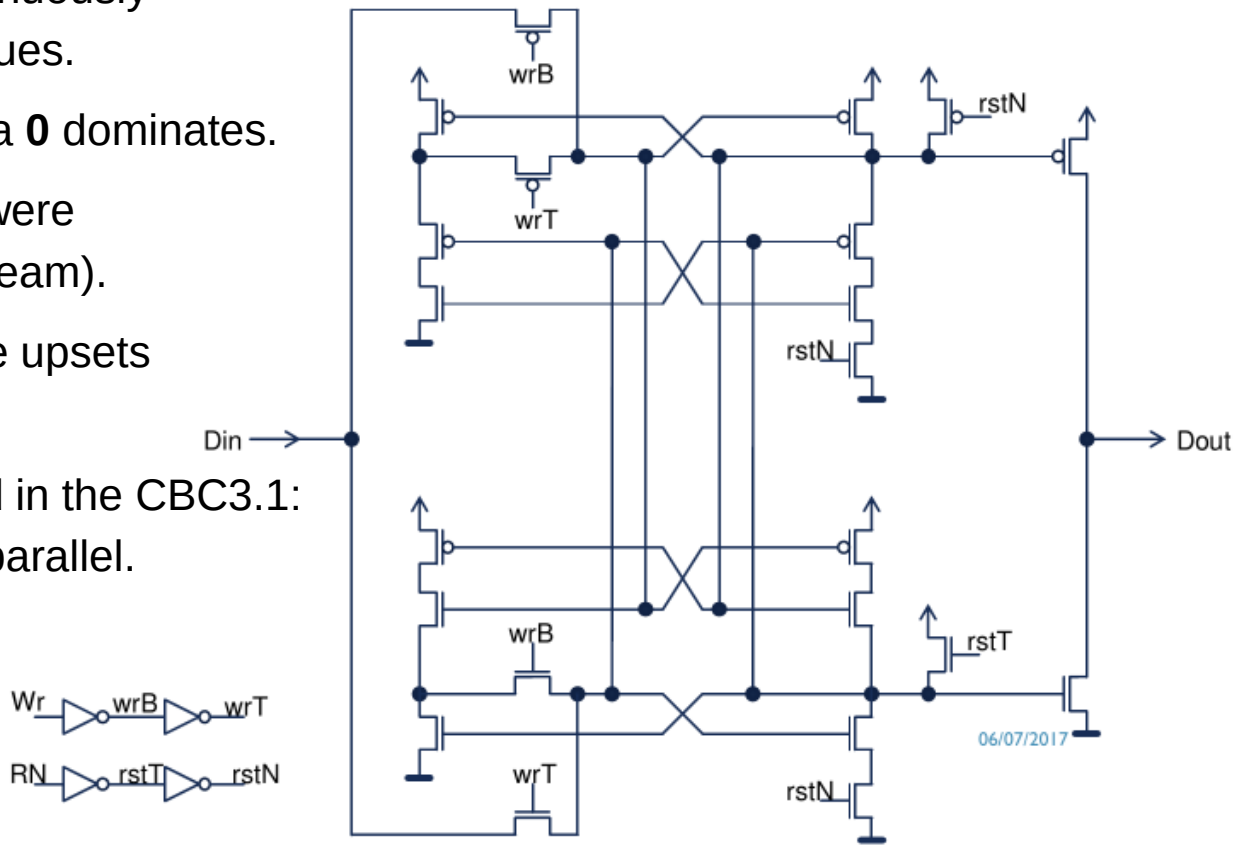
CBC3.0 (purple & red)
CBC3.1 (green)

- No functional problems or performance degradation observed.
- Expected increase in CBC current consumption: less than 3%.

http://www.hep.ph.ic.ac.uk/ASIC/dmray/CBC_documentation/CBC3_IrradReport_TrackerWeek_July2017.pdf
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2018_12_04_CBC3_20181204.pdf

SEU characteristics, CBC3.0

- Estimated upset rate at the CMS estimated to: 0.031$\pm$20%(stat)upsets per hour per chip (at a flux of 3 10^{6}cm^{-1}s^{-1}).
- Baseline mitigation strategy to continuously read back and rewrite corrupted values.
- “Reset” upsets that changes a **1** to a **0** dominates.
- “Write” upsets that changed **0** to **1** were observed in a CBC3.0 in a Xe^{54+} beam).
- Dominant mechanism seemed to be upsets to the local rstX and wrB inverters.
- Attempt to reduce rate implemented in the CBC3.1: wire nodes of the local inverters in parallel.



http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/CBC3_IrradReport_TrackerWeek_July2017.pdf

SEU characteristics, CBC3.1

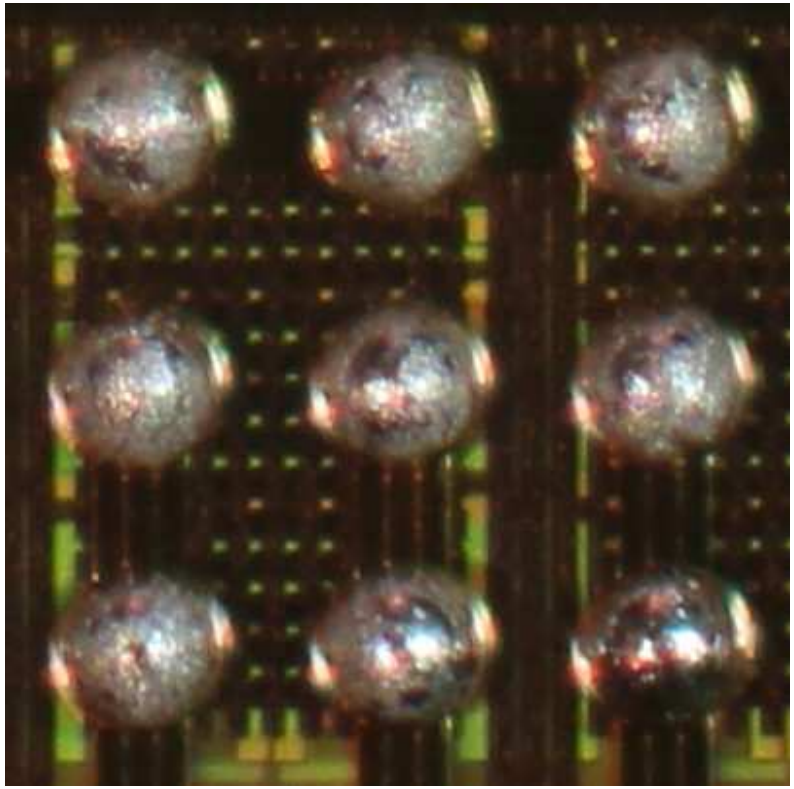
- $\approx$ 3x statistics compared to CBC3.0 tests.
- 0.027$\pm$11%(stat) upsets per hour per chip.
- “Reset” upsets seems much less common.
- “Write” upsets from **0** to **1** now dominates.
- Logic value dependence allows rate to be reduced by making last write 0x00.
- “Write” upsets also seems to have occurred also on the CBC2 (completely different implementation of the registers).
- No evidence that read-back interferes with front-end operation.
- Worst-case: performing read-back at a duty-cycle of 0.12% would reduce error rate in innermost layer to below 0.1%.
- No plans for further changes to the CBC planned.

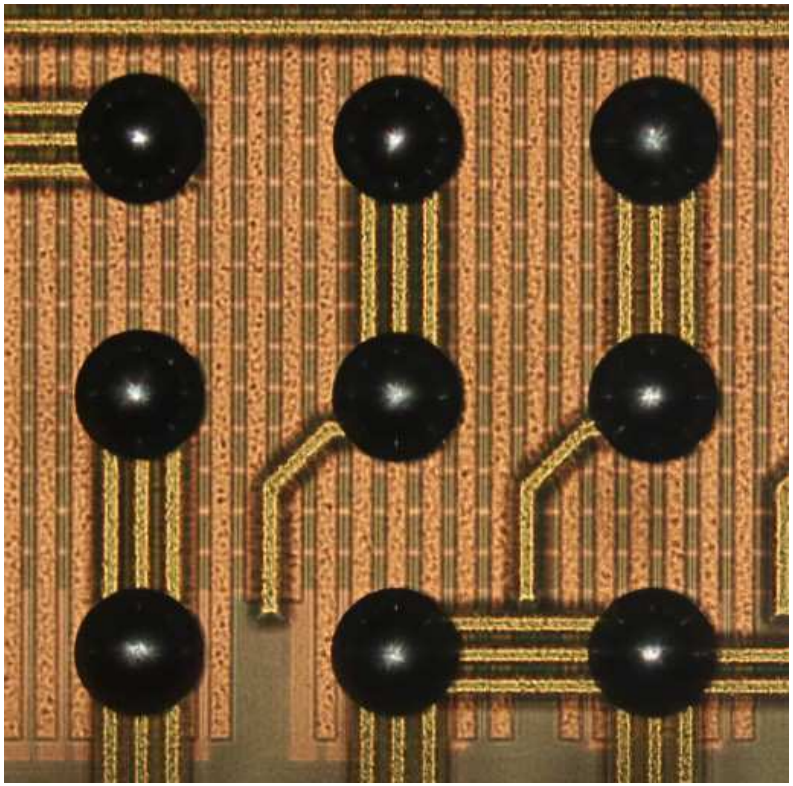
Thermal and supply voltage characteristics

- No issues with start-up issues at low temperature.
- Slightly higher supply voltage (1.25V nominal) may be advisable at low temperature. Testing continues.
- Logic simulations OK for all corners at -30, synthesized logic specified for down to -50.
- The Pipeline Address field (normally just for debugging, not used by CMS) in L1 packet may not be reliable at extreme operating conditions.

Bump bonding

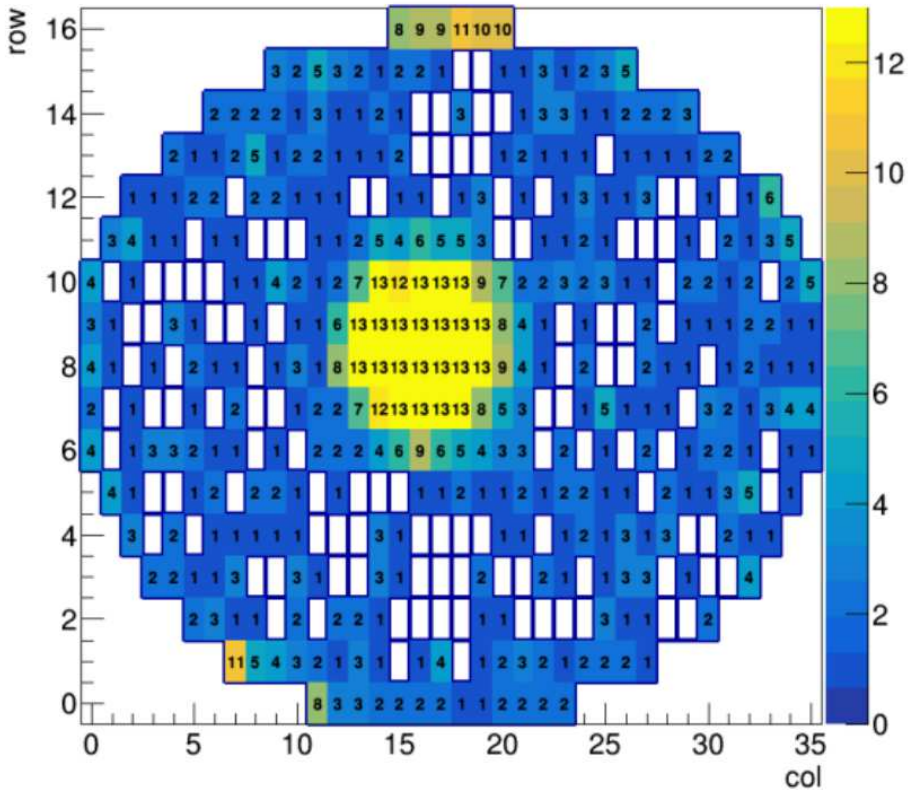
- First lot of CBC3.0 bumped by Pactech got low quality bumps and low bumping yield.
- Subsequent CBC3.0s and CBC3.1 bumped by Amkor with significantly higher quality, but the balls are smaller.
- Lead-free balls made in-house assembly of test boards and modules possible, shortening the time from die availability to tests of bump-bonded chips.





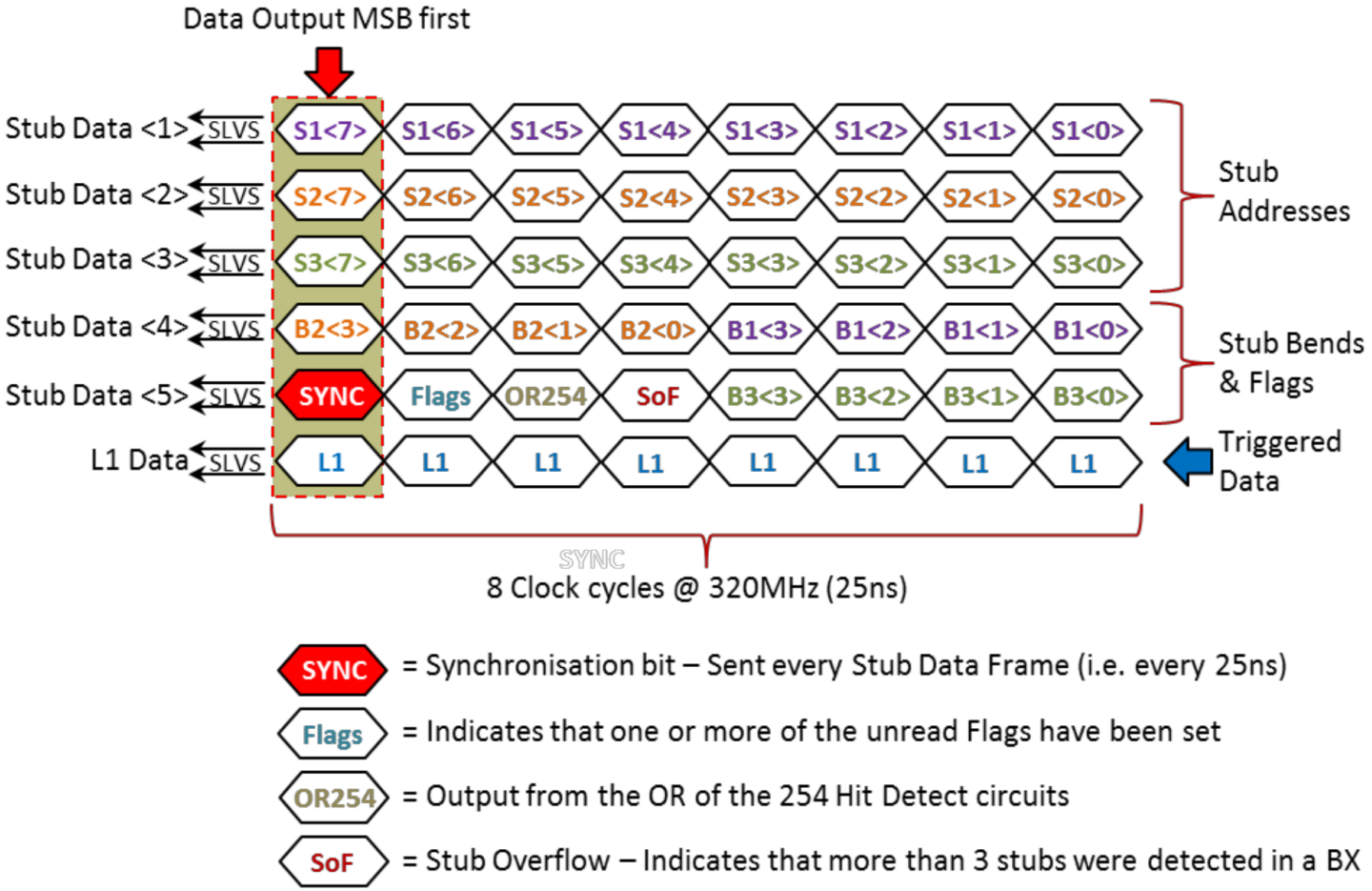
Wafer testing and yield

- Clearly more faulty chips close to the center of the wafers.
- Average CBC3.1 yield: 82% (first lot).
- Possibly due to high metal density, may go away as GF tunes the processing.
- New lot of wafer on order, significantly higher yield is expected if the tuning works.



For details regarding tests see:
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2018_11_06_WaferTest_06112018.pdf
http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2018_12_04_CBC3_20181204.pdf

Output data format



- The delay between physics event and the stub data output depends only on the DLL setting.
- More details regarding delays and the transient behavior after reset can be found in the manual.

Digital logic issues of the CBC3.0

- Incorrect stub address and bend codes in some cases.
- Stubs with a bend out side of the configured window size wasn't suppressed.
- The L1 data serializer fails for consecutive triggers at some DLL settings.
- L1 counter reset was unreliable.
- The inter-chip signals for detecting stubs that span 2 chips had signals swapped on one side of the chip, interchip test registers has been added.
- Default bias setting meant high power consumption at start-up.
- Supply voltage for programming fuses was not properly terminated.

All of these has been verified to be resolved in the CBC3.1.

However, the following should be observed also for the CBC3.1:

- L1 FIFO overflow must not be permitted (i.e. using trigger rules) as the overflow behavior is undefined and not production tested.
- The test pulse circuit should be disabled when changing DLL setting.
- It may be necessary to ignore the PA field of the L1 data at extreme operating conditions even though the chip otherwise functions as expected.

Documentation

- General:
  http://www.hep.ph.ic.ac.uk/ASIC/
- Past presentations:
  http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/