SEU test analysis result for CBC3.1

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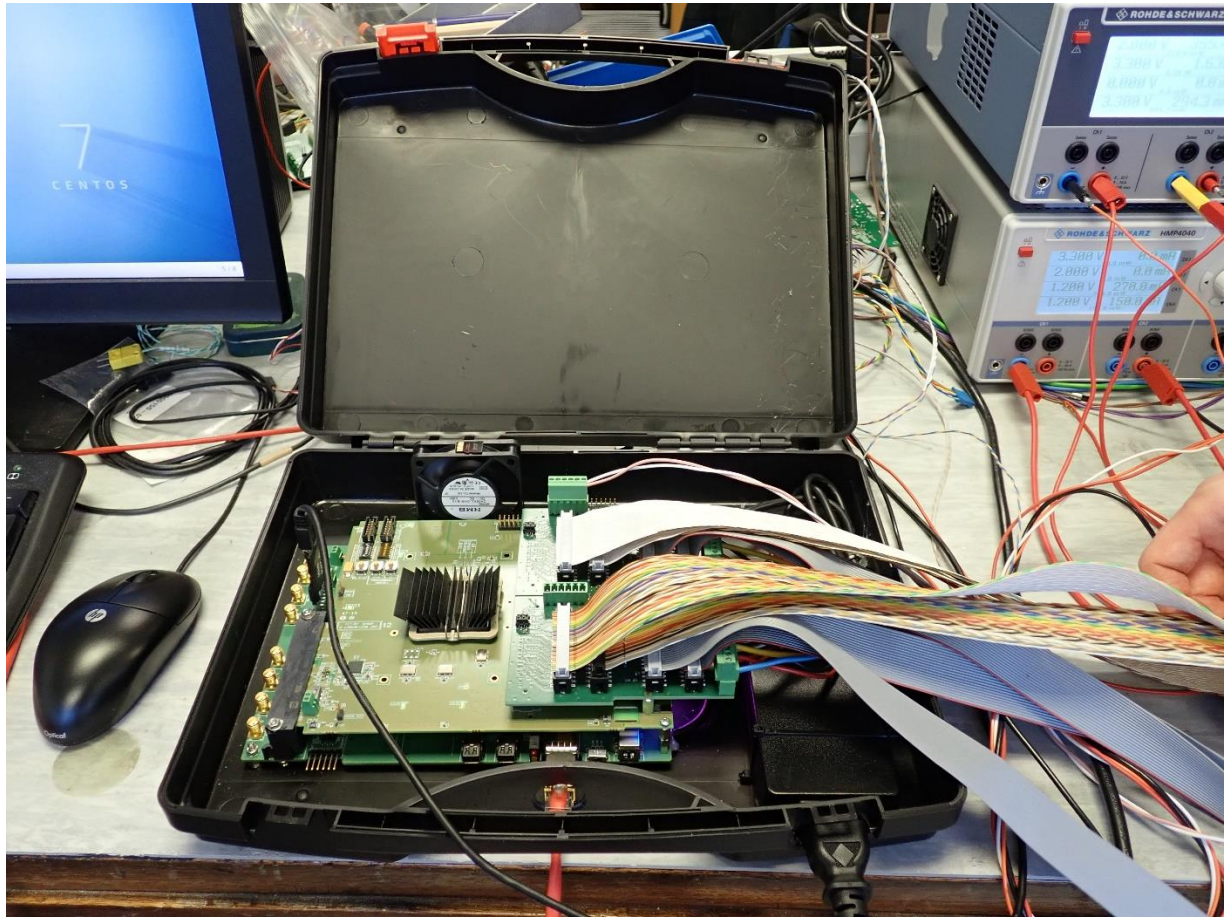
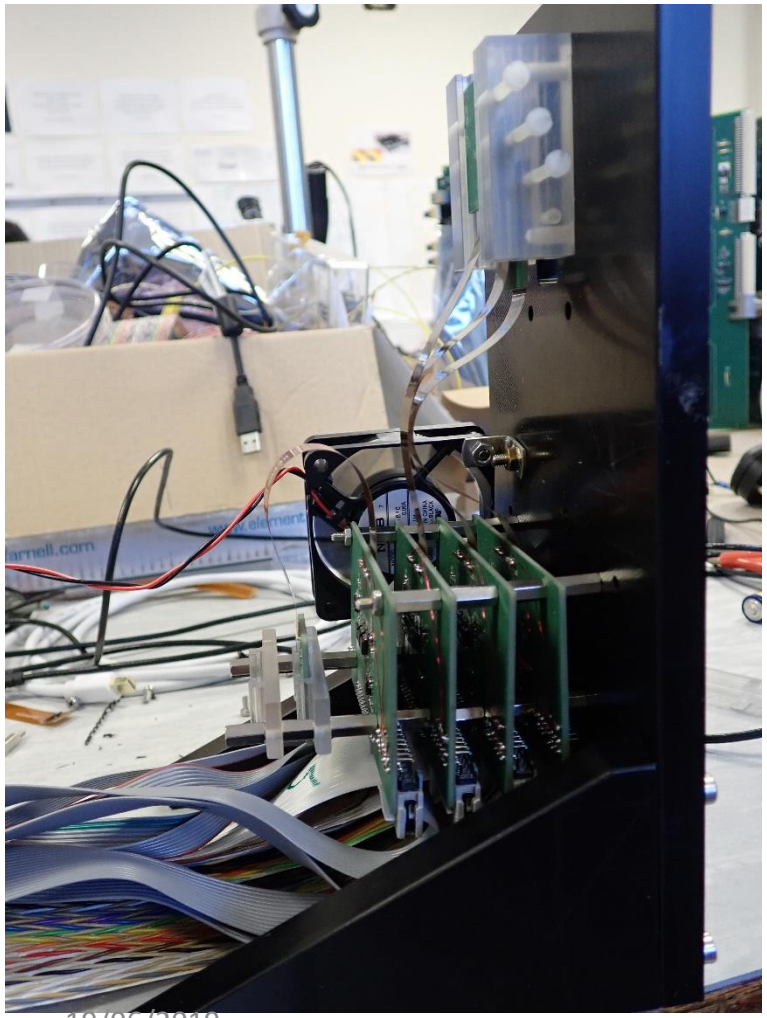
Backend

The cables between frontend and backend are 2m in length.

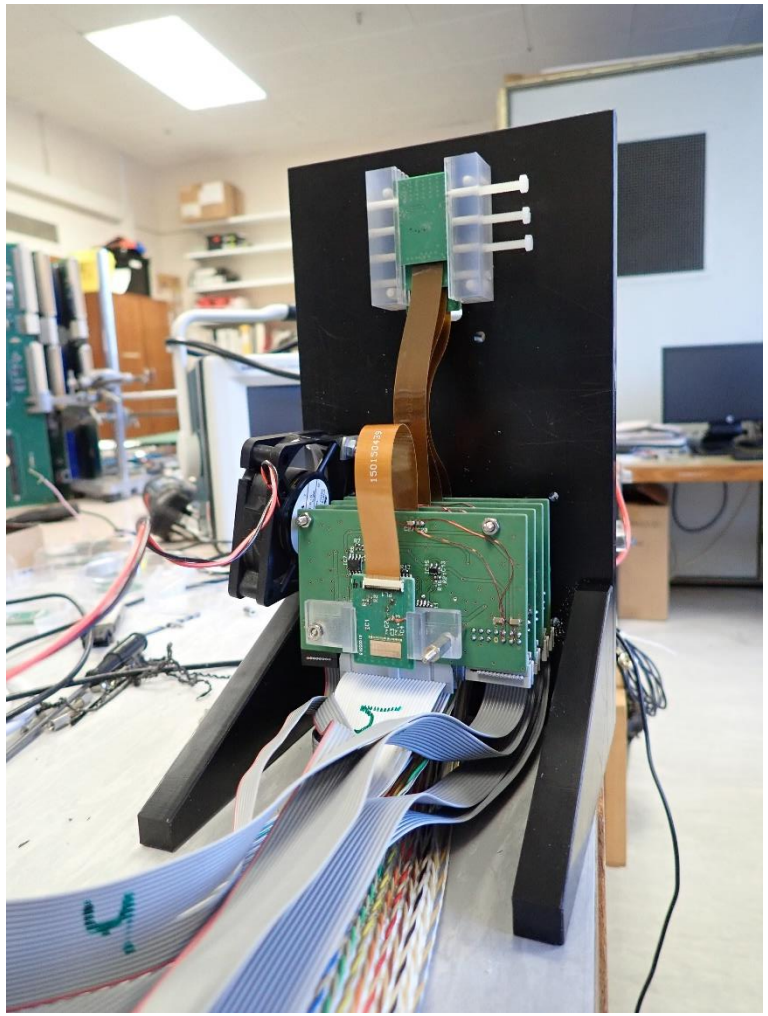


Frontend

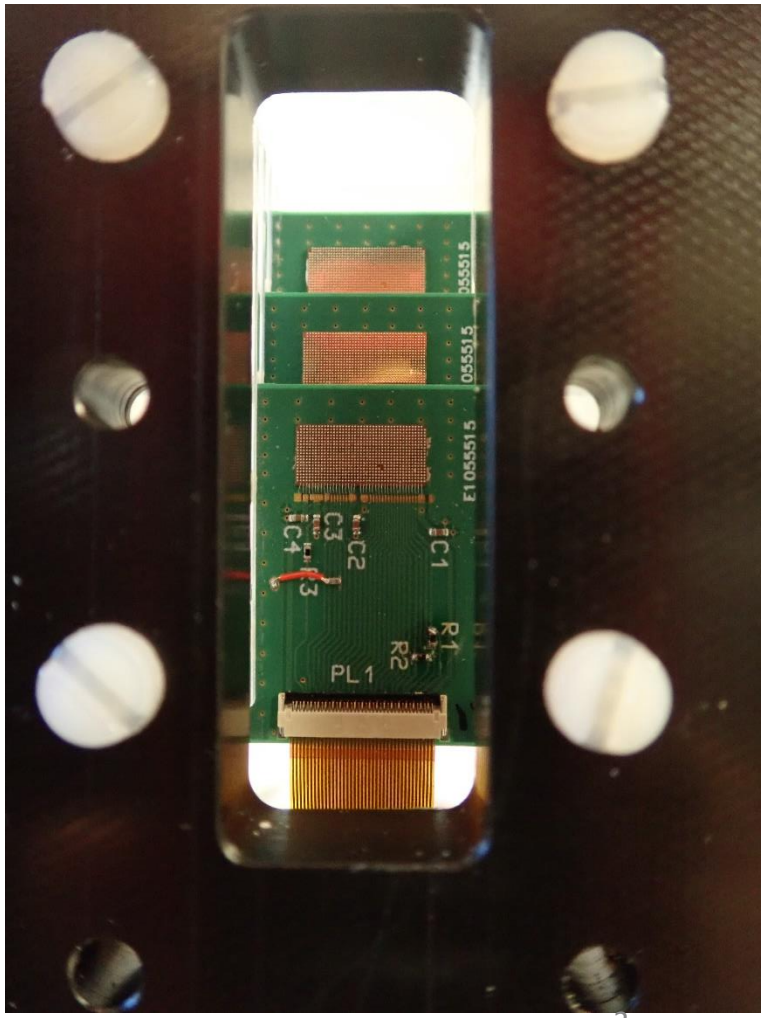
Side view



View from downstream

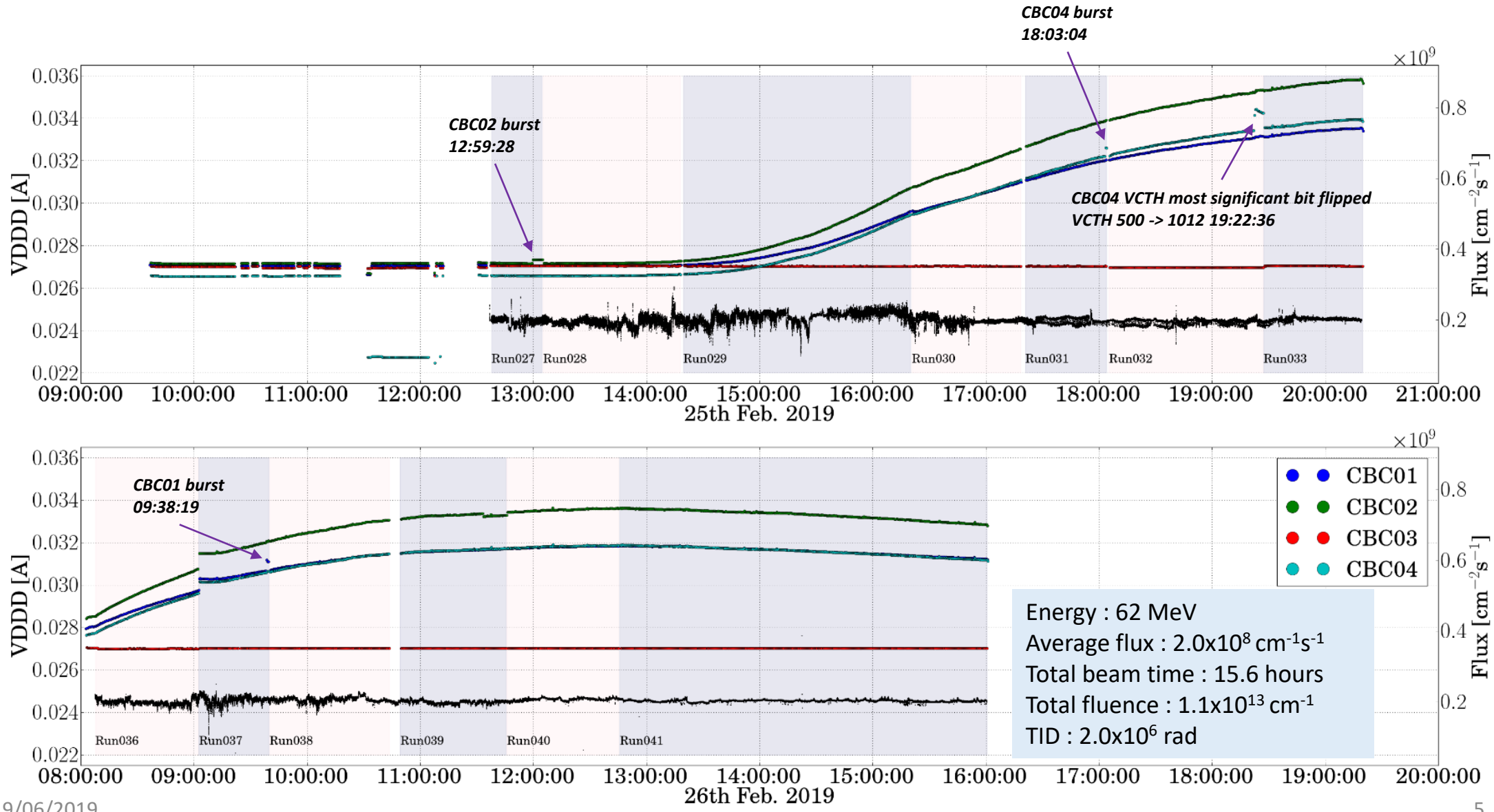


View from upstream



In the beamline

VDDD currents & beam flux



DAQ errors

- No pipeline logic error for total 3662 sec for 3 CBCs.
  - Upper limit for HL-LHC : 3.14×10^{-6} / sec / chip.
- Some unexpected hit events.
  - Total 66 channels had unexpected hits in 7.3×10^{7} events.
  - 0.04 hit error / event (in entire 120K CBCs). <- negligible.
- No stub error is observed in 7.3×10^{7} events.
  - Upper limit of wrong stub data (in a chip) for HL-LHC : 1.8×10^{-5} / event (in entire 120K CBCs) <- Totally negligible.

I2C registers

I2C register check

- 81 of 8-bit register bit flips events were observed.

CBC version	SEU rate / hour / chip in HL-LHC
CBC3.0	0.031 +/-20%(stat)
CBC3.1	0.026 +/-11%(stat)

HL-LHC flux : $3 \times 10^6\ cm^{-1}s^{-1}$

- We are confident that the SEU are happening on write & reset strobe nodes. This makes analysis very complicated.
  - Systematic errors should be on the estimated rates from I2C configuration and the last written value
    - The rate depends how many bits are different from the default or the last written value
    - The flip rates seem to be different for the flip to the default and the last written value, and also 0 ->1 and 1->0
- Multiple bit flips are observed in a single 8-bit register, which was not the case for CBC3.0.
  - This is explained by the change made in CBC3.1, where reset/write lines for each bit is connected to each other within the 8-bit register.
- There were 3 burst of bit-flips in which all the control registers in page 1 flipped to the default values. Similar situations are observed with CBC3.0 with faulty frontend interface card.

8-bit I2C register SEU breakdown

The register configuration :

- Control registers were configured as the recommended values for the experiment.
  Two configurations with VCTH : 500 (0x1f4) & 700 (0x2bc)
- Half the offsets were set to 0x7f and the other half were 0x80. The last written values were set to 0x00, 0xff, 0xc1, 0x55, 0x41 during the test.

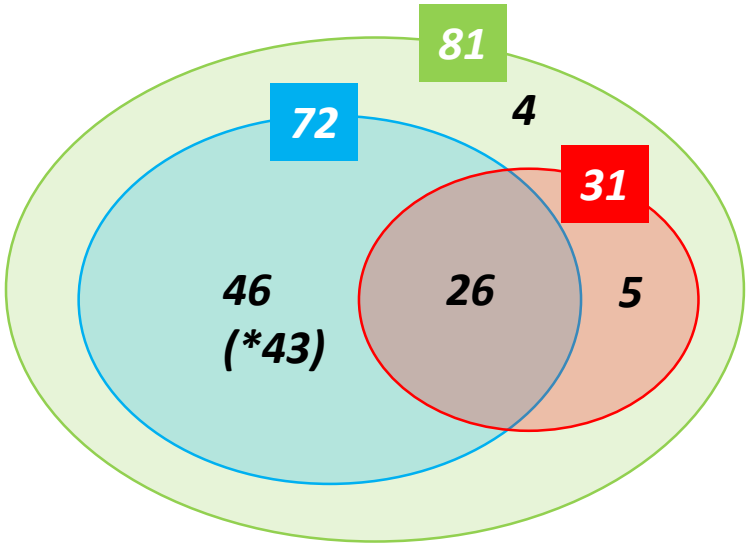
# of bits which could flip to the default value or the last written value per chip
(The numbers are listed for 2 VCTH settings, 500 & 700 respectively.)

The last written value	# of bit set to 0 The default : 1	# of bit set to 1 The default : 0	# of bit set to 0 The last written value : 1	# of bit set to 1 The last written value : 0	# of bit set to 0 The default & the last written value : 1	# of bit set to 1 The default & the last written value : 1
0x00	153 / 152	945 / 945	0 / 0	1414 / 1415	153 / 152	1414 / 1415
0xff	153 / 152	945 / 945	1242 / 1241	0 / 0	1242 / 1241	945 / 945
0x41	153 / 152	945 / 945	- / 308	- / 1059	- / 457	- / 1327

The result

- **Total 81 of 8-bit register bit flips**
- **72 registers had bit-flips to the value consistent with the last written value**.
  - 43 multiple bit flips happened only when the bits are flipped to the last written values. Only 1 event had 1->0 transition 0xff -> 0x00. Other bit flips are all 0->1.
  - 29 single bit flips consistent with the last written value, 0x7f->0xff.
- **31 registers had bit-flips to the values consistent with the default values**.
  - Bit-flips of 5 registers are not consistent with the last written value and all 1->0.
  - 24 bit-flips consistent with the last written value are all 0x7f->0xff, other 2 are 0x7f->0x00. (All of these are offsets and the default values are 0x80.)

Observed bit-flip categorization



All bit-flips
Bit-flips to the last written value
Bit-flips to the default value
The numbers are the count of 8-bit registers
(*) : multiple bit flips

The flip rate of 0->1 and 1->0

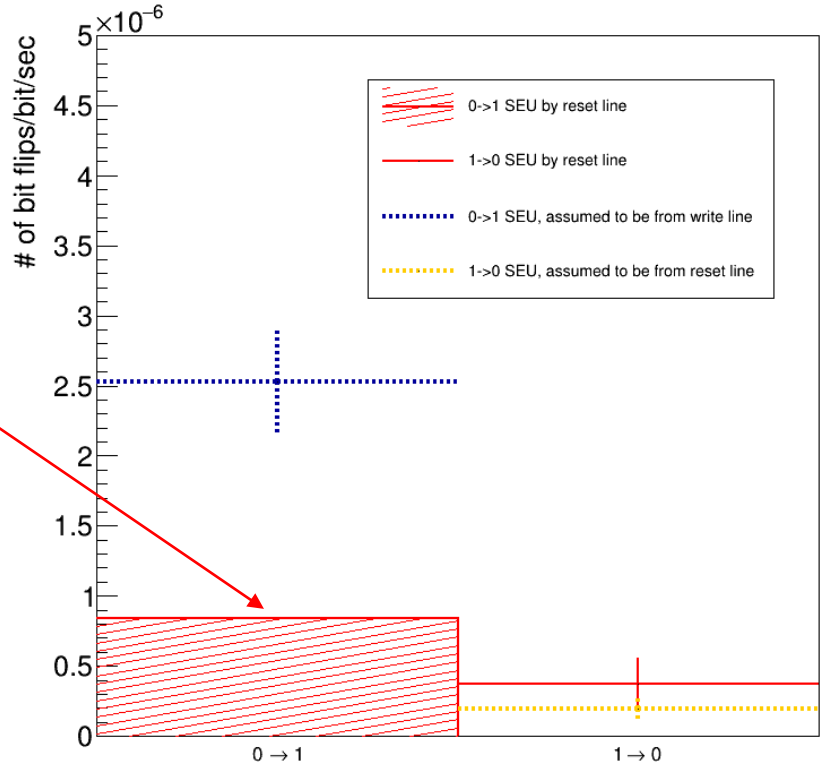
of bits which could flip to the default value or the last written value per chip
(The numbers are listed for 2 VCTH settings, 500 & 700 respectively.)

The last written value	# of bit set to 0 The default : 1	# of bit set to 1 The default : 0	# of bit set to 0 The last written value : 1	# of bit set to 1 The last written value : 0	# of bit set to 0 The default & the last written value : 1	# of bit set to 1 The default & the last written value : 1
0x00	**153 / 152**	945 / 945	0 / 0	1414 / 1415	**153 / 152**	1414 / 1415
0xff	153 / 152	**945 / 945**	1242 / 1241	0 / 0	1242 / 1241	**945 / 945**
0x41	153 / 152	945 / 945	- / 308	- / 1059	- / 457	- / 1327

- The bit-flip rate to the default value can be extracted with the last written value 0xff or 0x00
  - 0->1 bit-flip to the default values in the data were not observed. Upper limit is set.
- Looking at other data,
  - 0->1 bit-flip rate is relatively large.
    Most probably from the bit-flips to the last written value.
  - 1->0 bit-flips rate is consistent with the flip to the default values.
    The contribution from the flips to the last written value should be small.

Setting the last written value to 0x00 might help reducing the bit-flips.

The flip rates are for the testbeam
(but # of bits on the denominator was forgotten to be multiplied by 3)



Summary

- SEU rate on I2C registers on CBC3.1 seems to be similar to CBC3.0.
- Increased statistics supports that the mechanism of the SEU on I2C register is on the write and reset node.
- The SEU rate would depends on the last written value and register configuration.
- The data for CBC3.1 indicates that setting the last written value 0x00 gives order of magnitude lower than setting to 0xff.
- Overall 8-bit register bit-flip rate per chip at HL-LHC would be ~ 0.5 with the flux = 3×10^6 $cm^{-1}s^{-1}$
  (only 15 % of the registers are control registers)