# CBC3 lot2-3 wafer testing results

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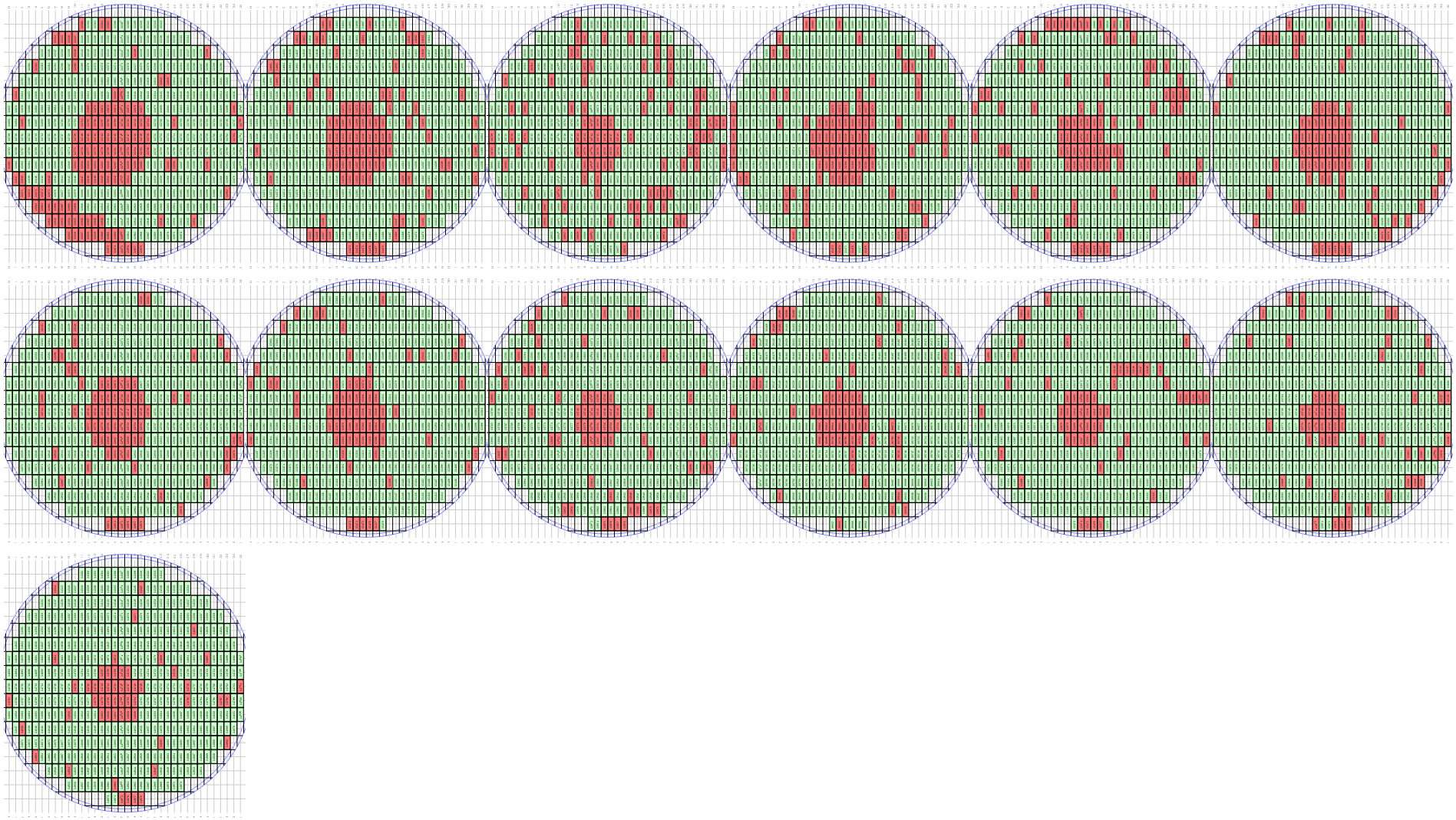
# CBC3 wafer testing

- Production test wafer testing perfomed, for details see:
  http://www.hep.ph.ic.ac.uk/ASIC/CBC_documentation/2018_11_06_WaferTest_06112018.pdf
- Reasonably comprehensive set of analog and digital tests
- Testing one wafer takes about 4.5h.
- Level of details regarding how each chip fails is limted
- First lot of 13 wafers exhibited clear pattern of low yield close to center of wafers.
- Process was tuned by GF using different machine for one processing step.

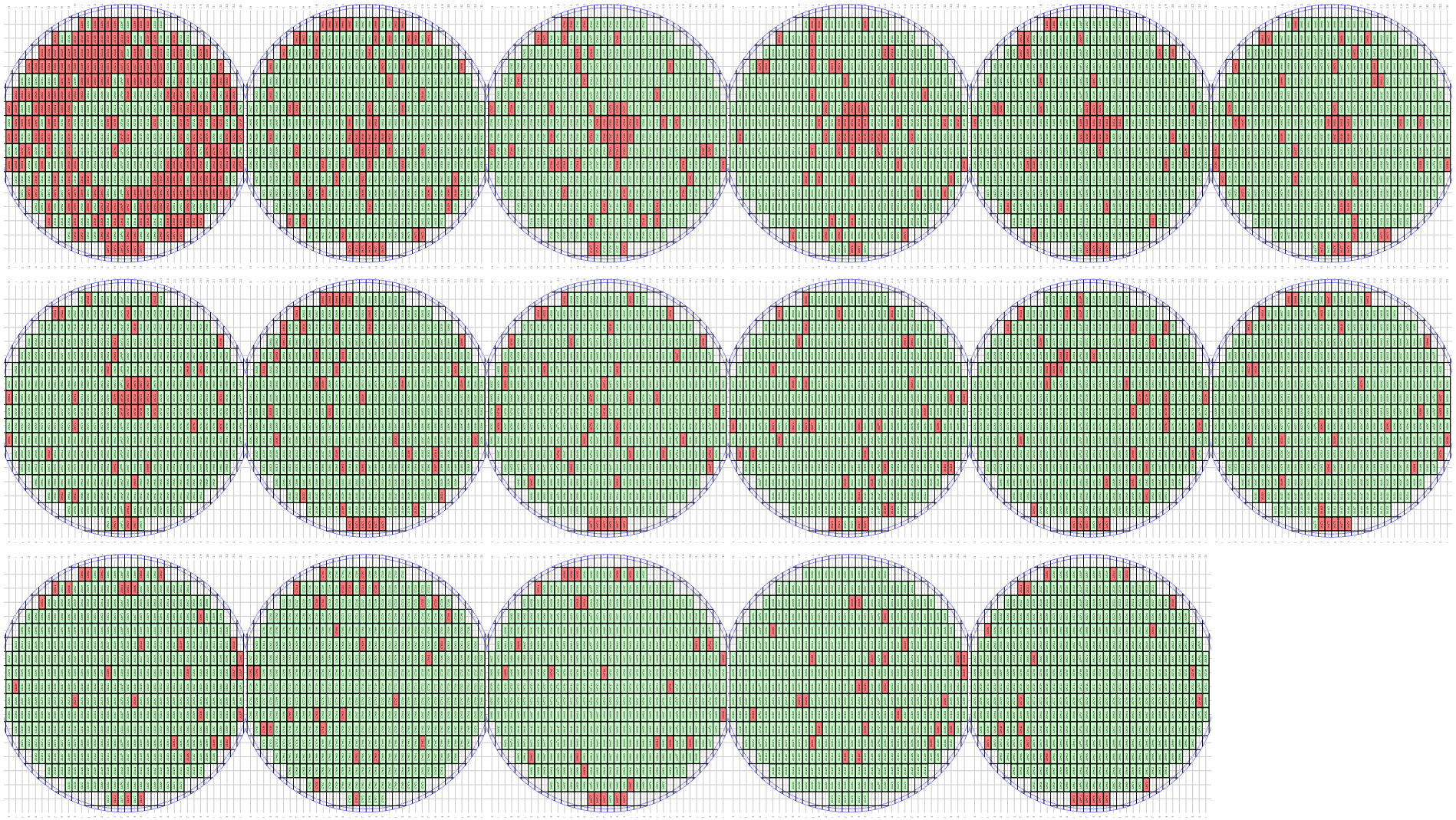
# Background: Lot 1 wafer maps (sorted by yield)



# CBC3.1 lot 2 and 3 wafer test results

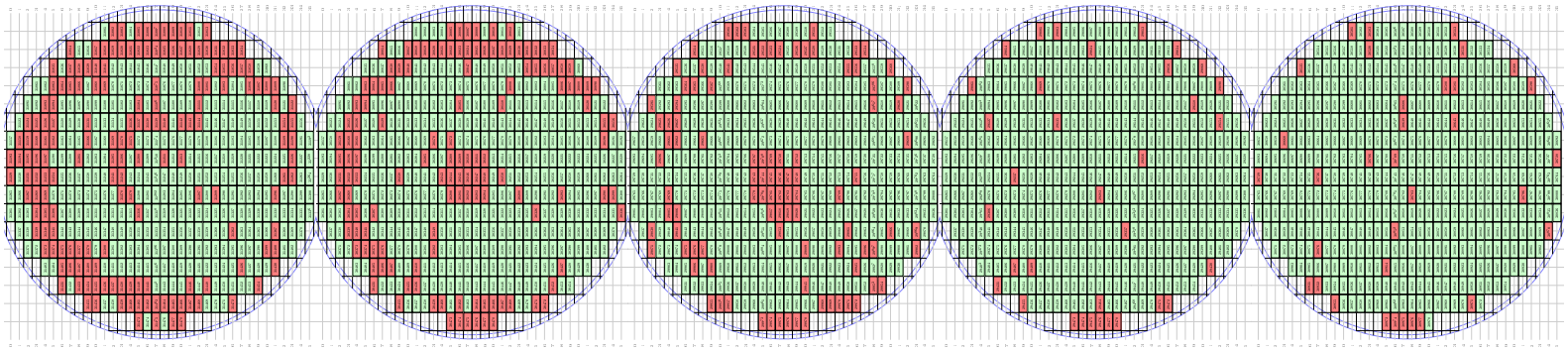
- Lots 2 and 3 consist of 24 wafers each, delivered 2nd and 26th of September.
- 17 wafers from lot 2 and 5 from lot 3 tested so far.
- Tests and work on test setup will continue with the goal to finish before Christmas.
- Lot 1 yield: 82.5%, Lot 2 so far: 88.5%, Lot 3 (so far): 80.3%.
- Significant fraction of new wafers doesn’t exhibit a low yield area.
- A new pattern of low yield close to edge on some wafers.

# Lot 2 wafer maps (sorted by yield)



Sorted by yield.

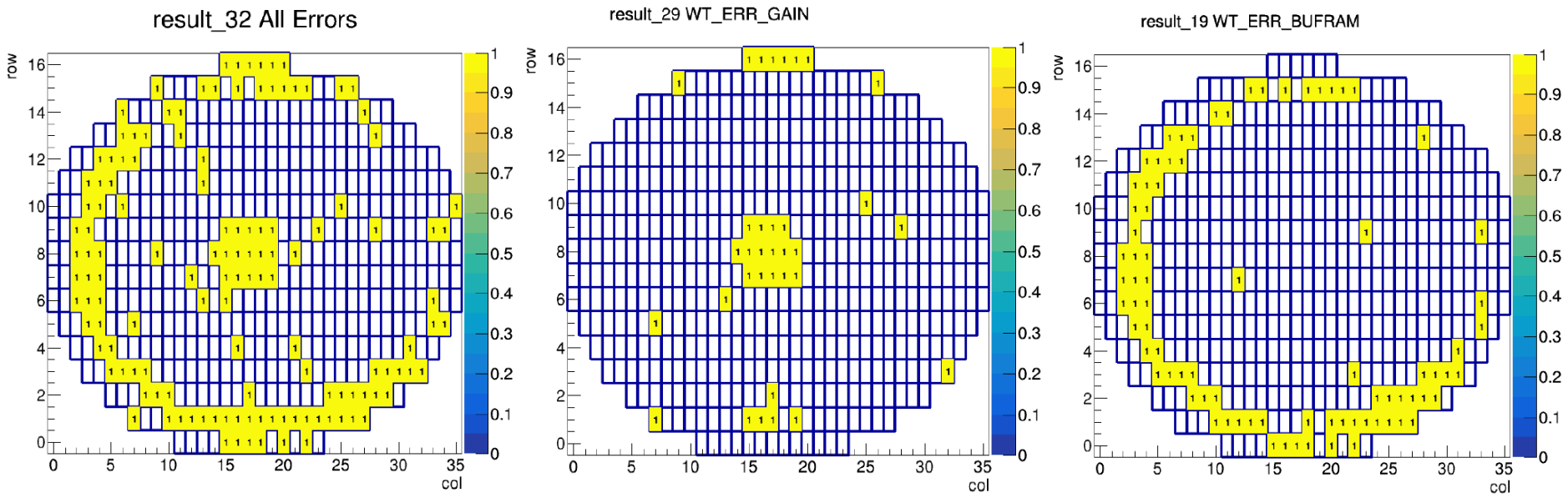
# Lot 3 wafer maps (sorted by yield)



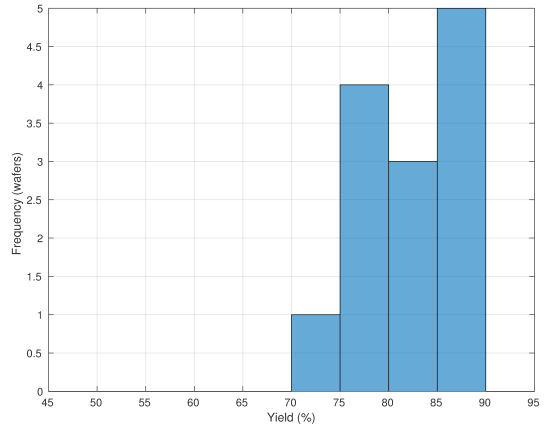
Sorted by yield.

- Failures related to single channel data seems to dominate in the center of wafers
- Failures related to output data seems to dominate in the ring

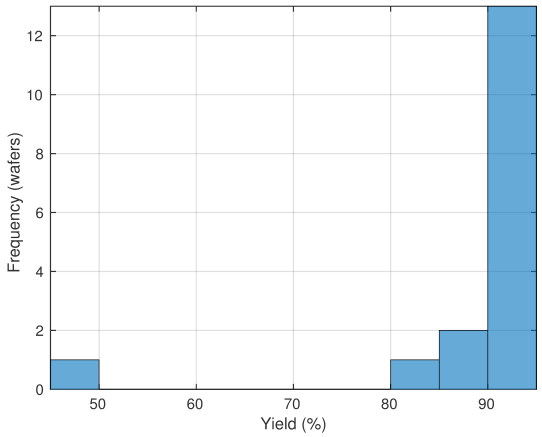
# Examples of failure modes



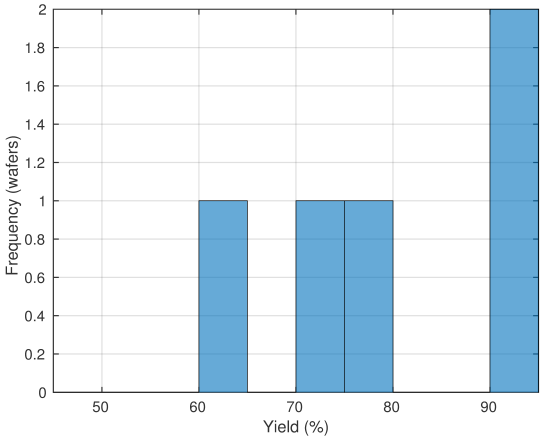
# Yield histograms




Lot 1




Lot 2




Lot 3

## Summary

- 22 wafers from lots 2-3 tested (out of 48).
- Lot 2 exhibits high yield so far, with reduced area of clusters of low yield compared to Lot 1, but one outlier.
- Some patterns seen on wafers in Lot 3 observed, will be monitored as more wafers are tested.