CBC3 Hit Detect Logic for CMSSW

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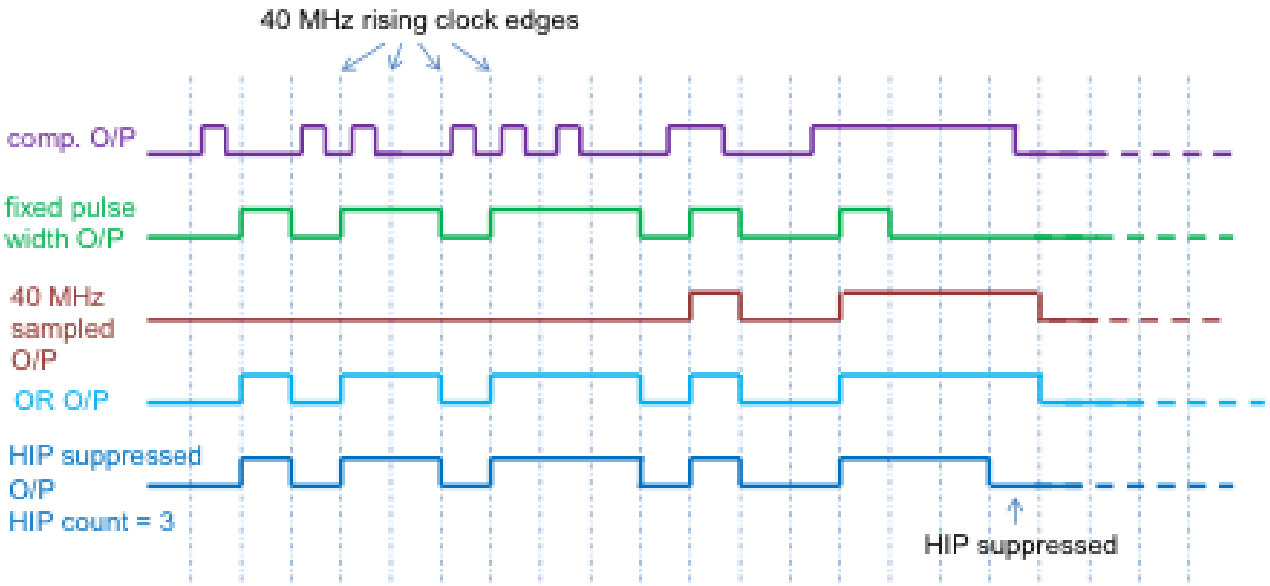
Introduction

- A parametrization of CBC3 signal shape
  - it was determined in the lab by S.S. El Nasr-Storey, S. Mersi, G. Zevi Della Porta et al. (talk)
  - it was implemented in CMSSW by S. Dutta and S.Sarkar (talk)
    Input to signal shape are:
    - deposited charge
    - particle time of flight corrected for the time required to reach the module (reference: center of the module)
- A realistic simulation of CBC3 must implement Hit Detect Logic.
  This talk is an attempt to document "our" interpretation of the Hit Detect Logic described in the CBC3 manual in view of the implementation in CMSSW code (class `SSDigitizerAlgorithm`)

CBC3 Hit Detect Logic

- From CBC3 technical specs manual



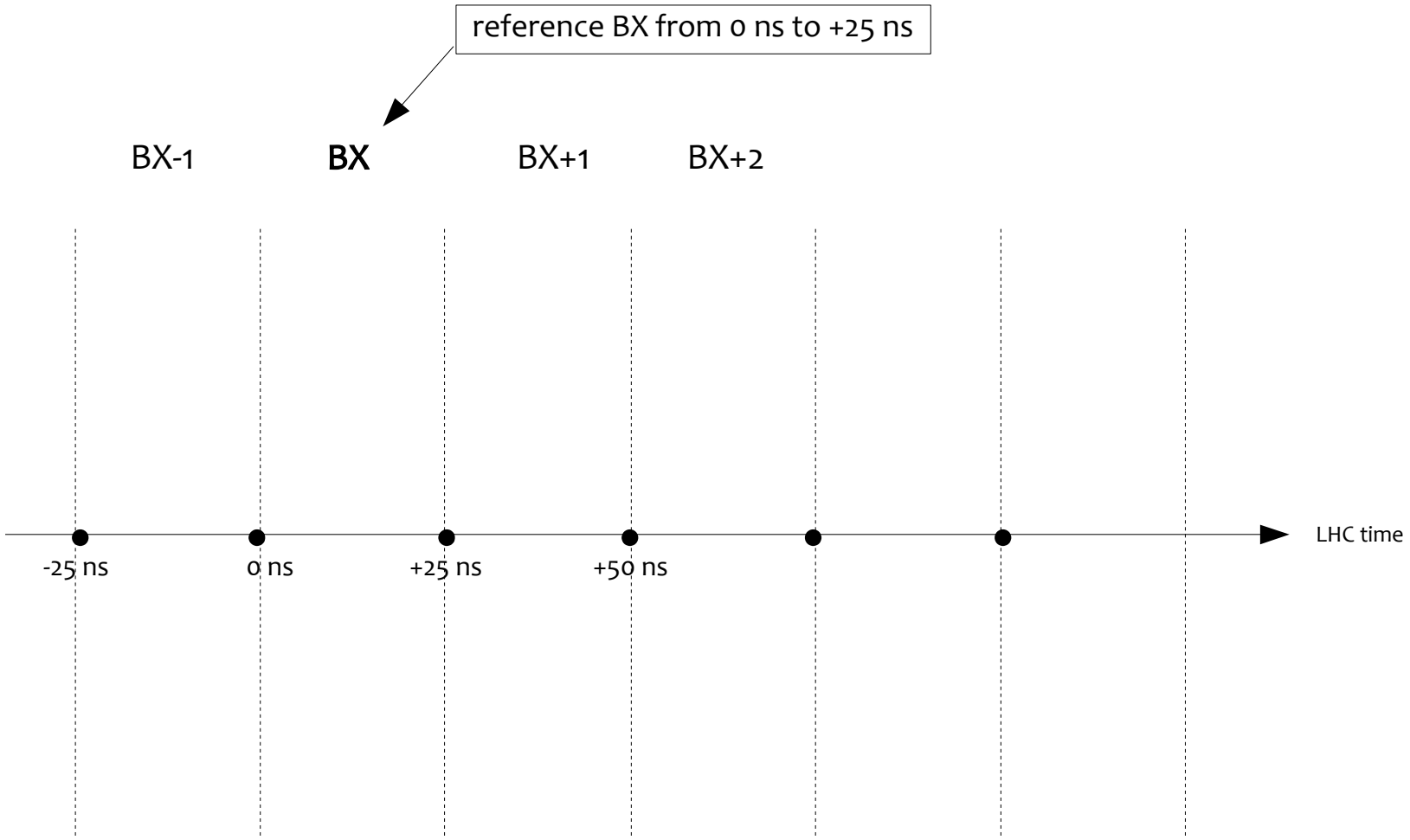
Suchandra has started to implement in CMSSW only these two modes

→ fixed pulse width looks for a rising edge on the comparator O/P and produces a single 40 MHz clock cycle pulse beginning at the next 40 MHz clock rising edge

→ sampled comp. O/P goes (or stays) high if the comparator output is high at the 40 MHz rising clock edge

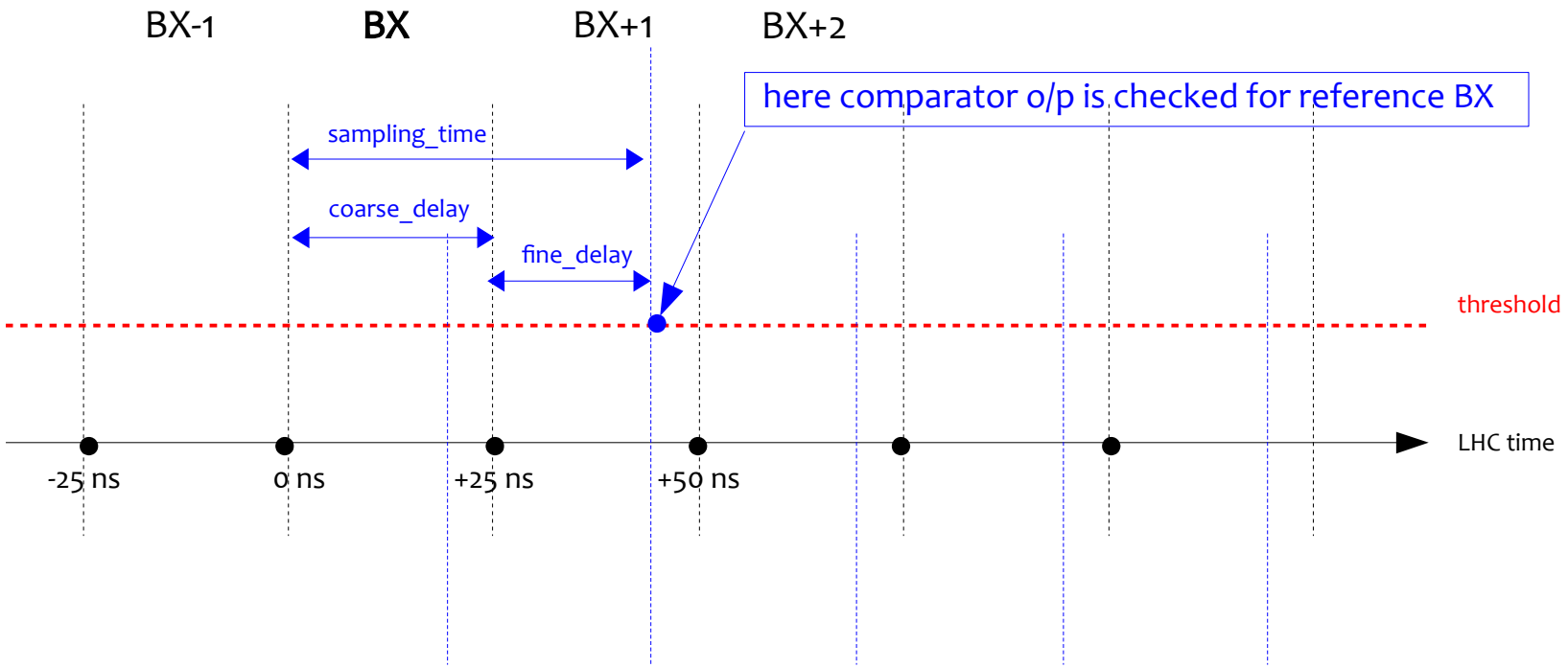
OR O/P is the logical OR of fixed pulse width O/P and 40 MHz sampled O/P

- In the following I will adopt the following (short) name conventions :
  - fixed pulse width => latched mode
  - 40 MHz sampled comp. O/P => sampled mode


reference BX from 0 ns to +25 ns
BX-1
BX
BX+1
BX+2
LHC time
-25 ns
0 ns
+25 ns
+50 ns

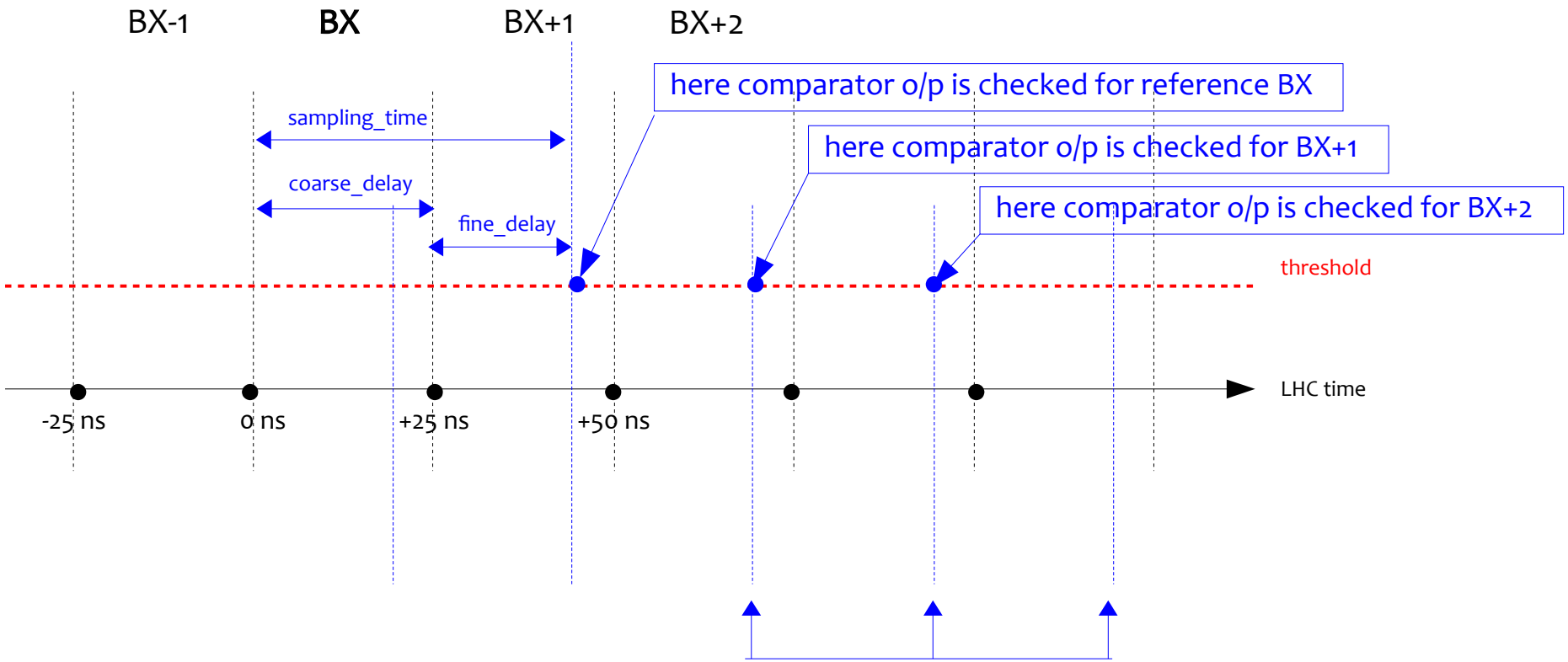
sampling_time = coarse_delay + fine_delay

with coarse_delay is in 25 ns steps
and fine_delay is in 1 ns steps



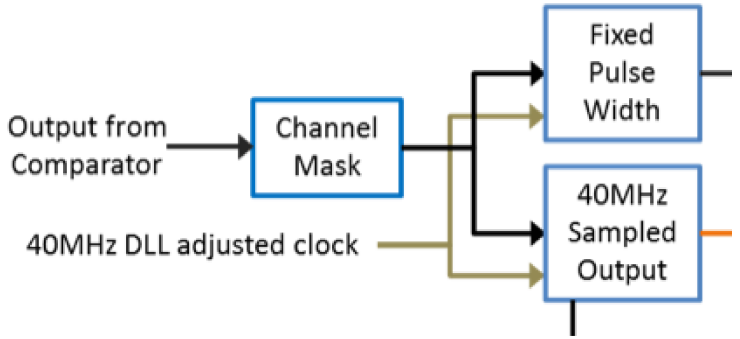
sampling_time = coarse_delay + fine_delay

with coarse_delay is in 25 ns steps
and fine_delay is in 1 ns steps



rising edges of the 40 MHz
DLL adjusted clock

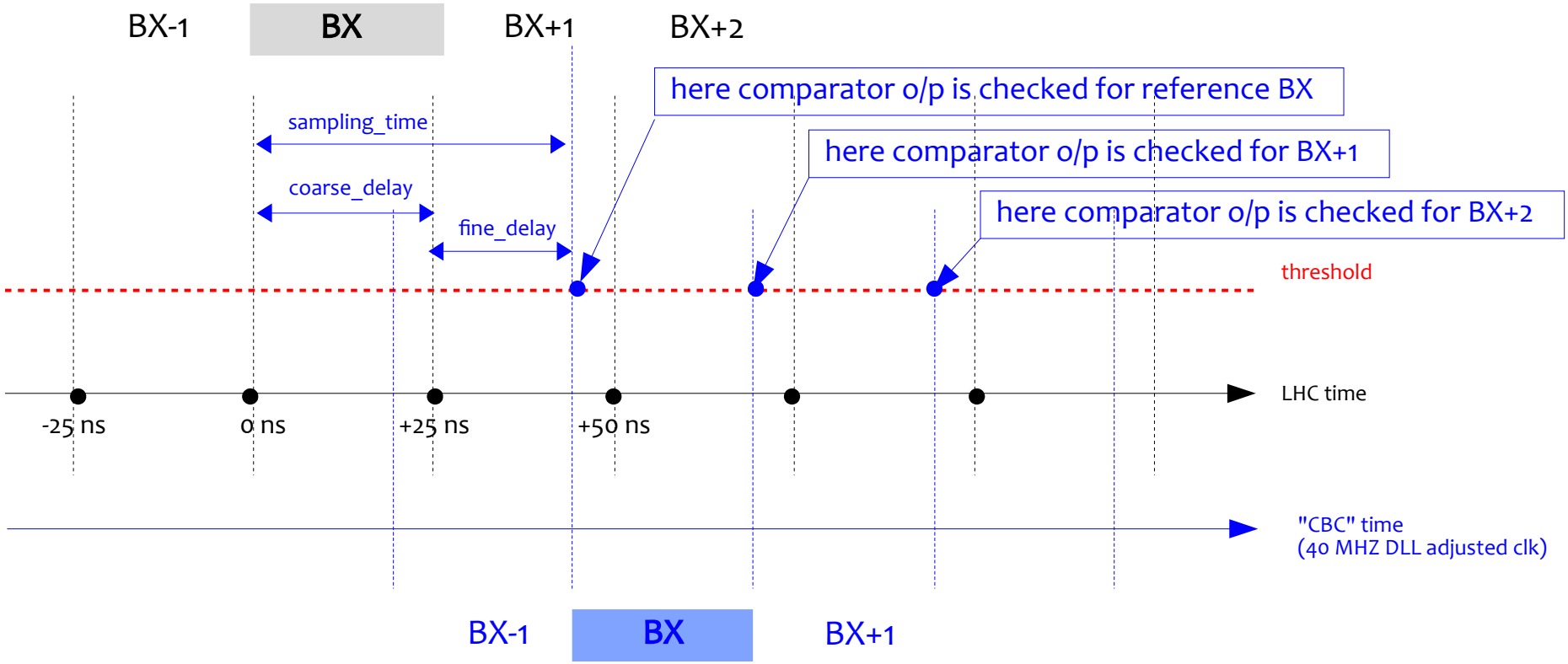
referred to as "CBC" time in what follows



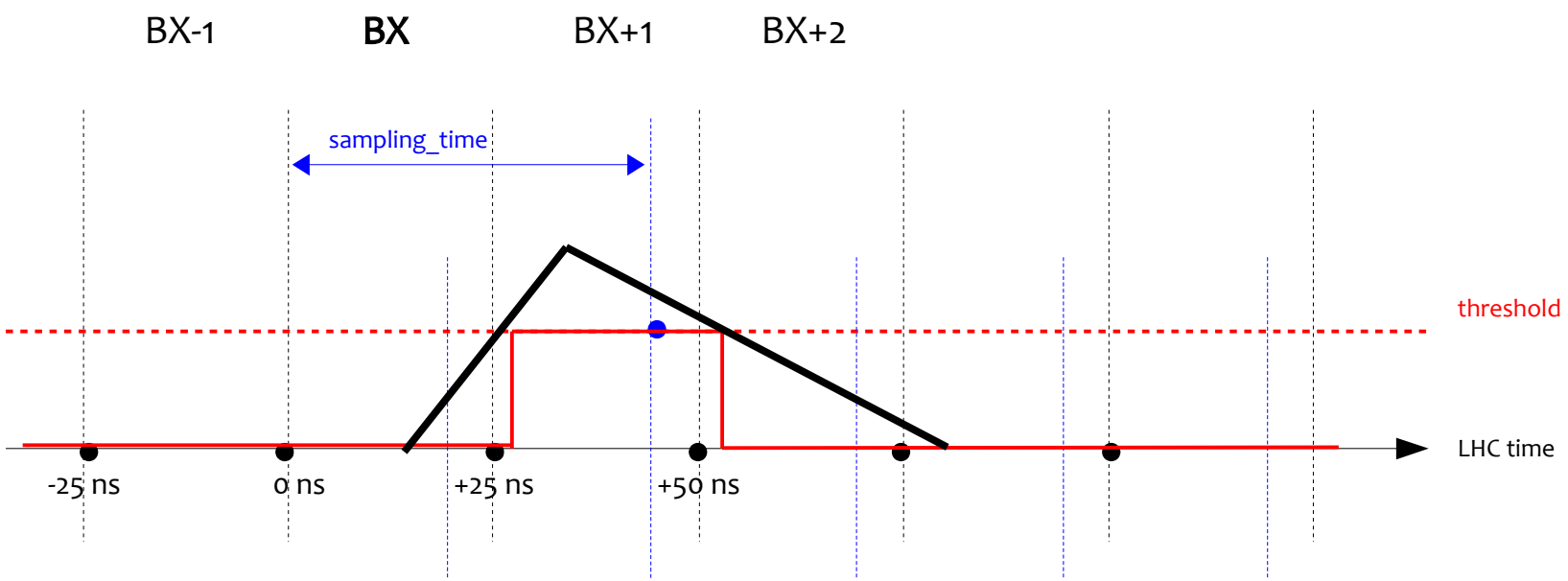
From CBC3 manual:
"The programmable DLL will allow for CBC3s to be tuned to the arrival time of the particles, thus adjusting for time-of-flight from the interaction point."

sampling_time = coarse_delay + fine_delay

with coarse_delay is in 25 ns steps
and fine_delay is in 1 ns steps



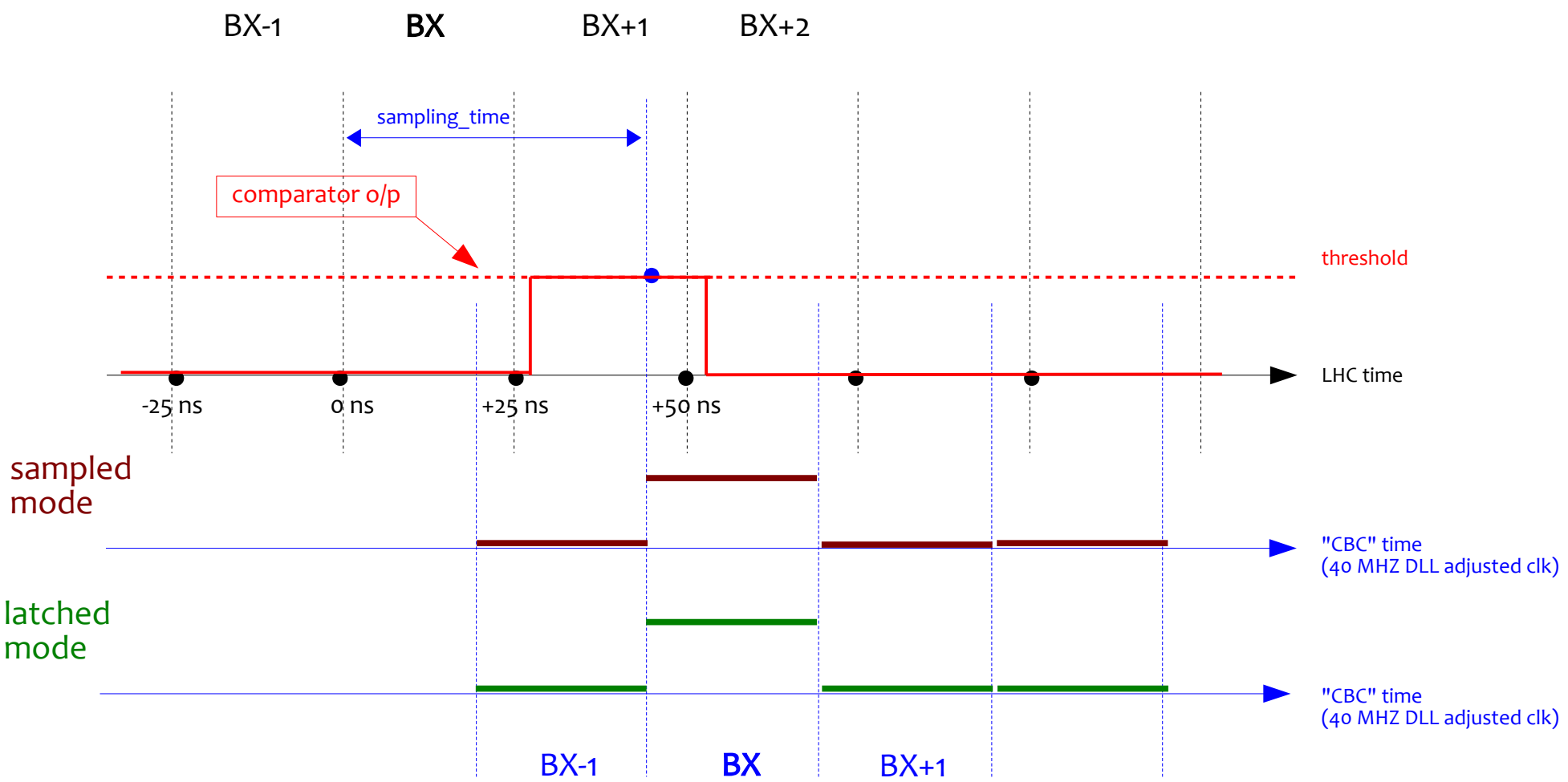
particle crossing sensor during reference BX: case A



- Disclaimer
  - "triangular" signal shape
  - choice of the sampling time

  in the sketch are just for illustration purpose

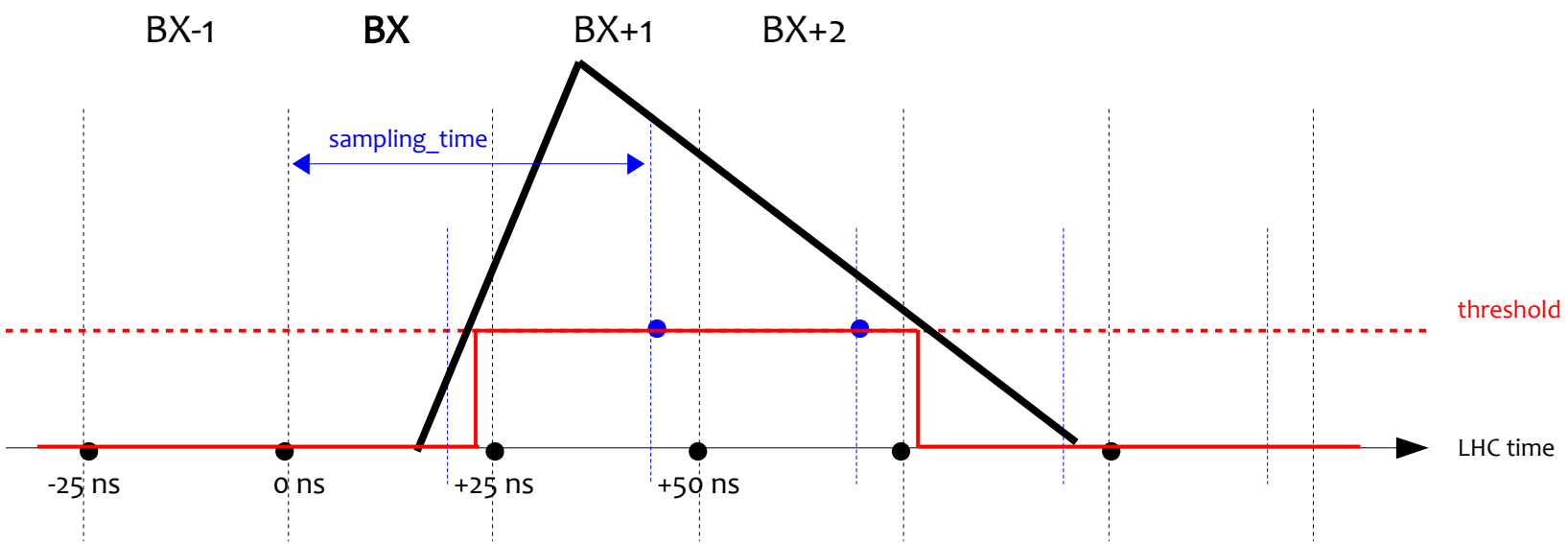
particle crossing sensor during reference BX: case A



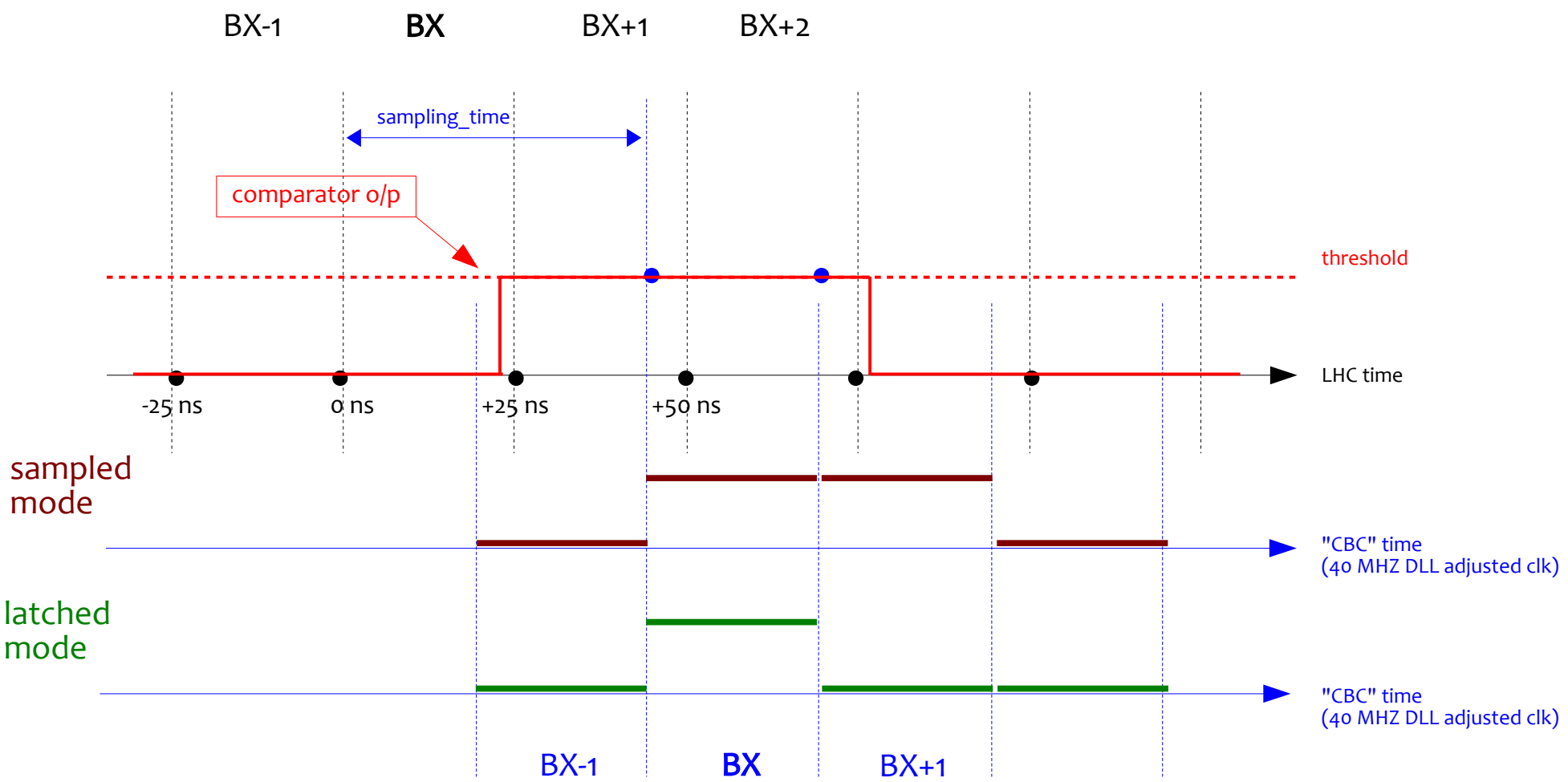
sampled mode: high if comp. o/p is high at the rising edge of the 40 MHz clock

latched mode: looks for a rising edge on comp. o/p and produces a 25 ns pulse beginning at the next 40 MHz clock rising edge

particle crossing sensor during reference BX: case B



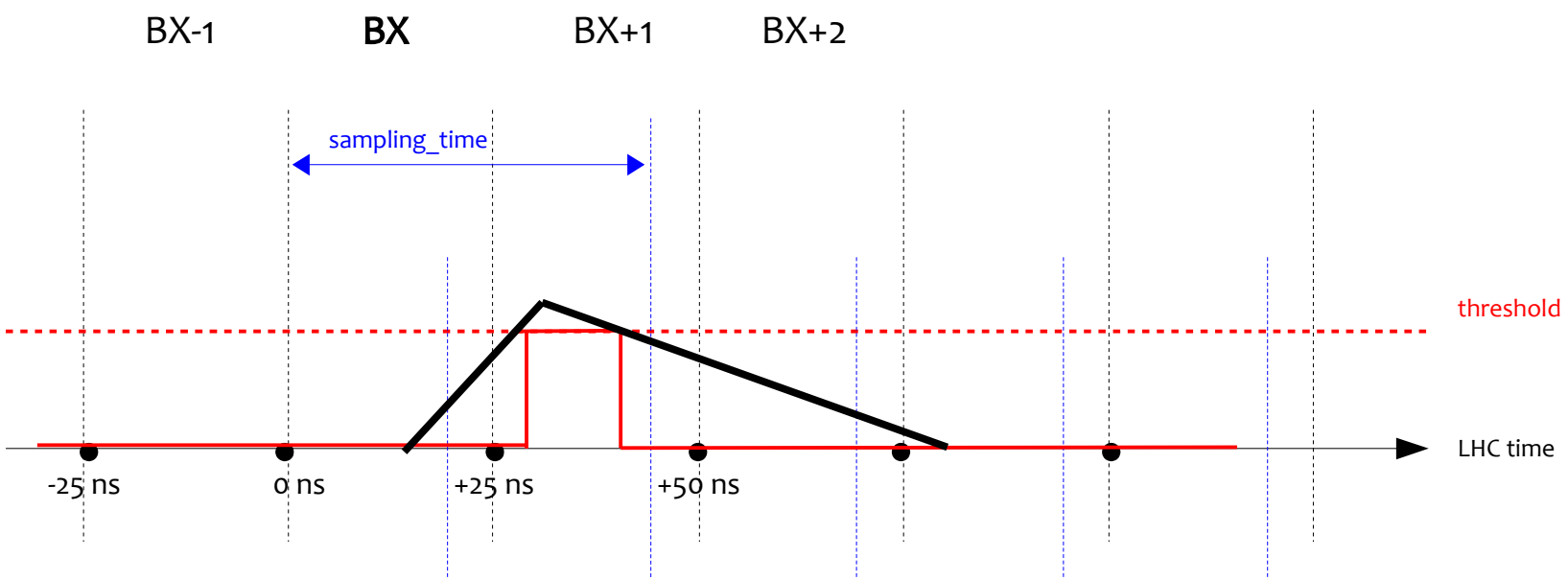
particle crossing sensor during reference BX: case B



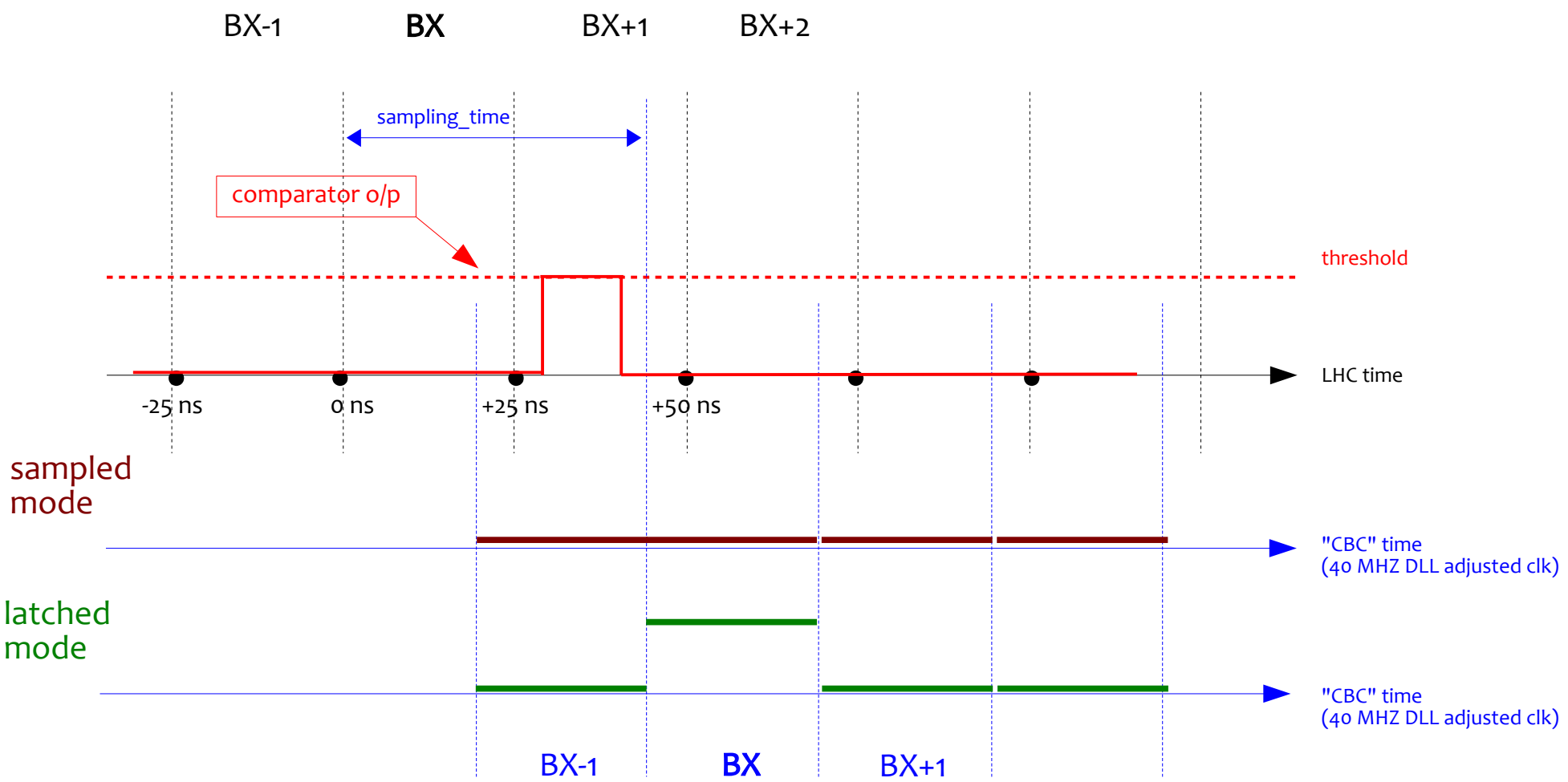
sampled mode: high if comp. o/p is high at the rising edge of the 40 MHz clock

latched mode: looks for a rising edge on comp. o/p and produces a 25 ns pulse beginning at the next 40 MHz clock rising edge

particle crossing sensor during reference BX: case C



particle crossing sensor during reference BX: case C



sampled mode: high if comp. o/p is high at the rising edge of the 40 MHz clock

latched mode: looks for a rising edge on comp. o/p and produces a 25 ns pulse beginning at the next 40 MHz clock rising edge

- Is this interpretation correct?