CERN ASIC WG
6.11.19

Summary of SEU rates in CBC2, CBC3.0 and CBC3.1

G. Hall, K. Uchida, J. Borg, M. Prydderch
(& Mark Raymond)

The tests

- At Louvain Light Ion Irradiation Facility (to whom many thanks)

Table 1: The beam parameters and exposure conditions

	2014	2017	2019
	CBC2	CBC3.0	CBC3.1
proton energy [MeV]	62	62	62
flux [10^8 cm^{-2}s^{-1}]	2.5	2.3	2.0
flux relative to HL-LHC	×73.5	×67.6	×58.8
beam exposure time [h]	12	14.6	(3×)15.6
total fluence [10^{13} cm^{-2}]	1.1	1.2	1.1
total radiation dose of CBCs in the beam [Mrad]	1.5	1.6	1.5

- All tests over two days
  - Flux almost two orders of magnitude higher than HL-LHC maximum, for 2S-modules
    - measured to <5%
  - CBC2: no reference chip
  - CBC3.0: reference chip outside beam
  - CBC3.1: reference chip outside beam, 3 CBC3.1s in beam

Reminder of CBC parameters

Table 2: Relevant CBC parameters

	CBC2	CBC3.0 / CBC3.1
Channels	254	254
Pipeline memory length	256	512
Storage buffer depth	32	32
I^2C registers	307	330 / 338
Data cells	73,536	138,592
Readout speed [MHz]	40	320
Data and header frame readout time [μs]	6.65	0.95
Stub resolution	1 strip	half strip
Stub readout	OR of all stubs	addresses & bends of up to 3 stubs

- Number of registers changed slightly, with some unused
  - Most of them store a single channel offset value
  - Few have much influence on CBC operation cf. performance, e.g. latency, R/W pointers,…
- Pipeline memory length increased, with latency
- Pipeline control logic uses Whitaker cells. Some changes between CBC2 and CBC3.
- CBC2 used triple majority logic in I^2C registers, CBC3 changed to Whitaker

What was tested

- NB procedures slightly different in each test,
  - reflecting chip changes (e.g. 40/320 MHz, Whitaker/triple majority logic)

- Pipeline logic
  - Send reset, start W/R pointers, issue trigger, check error bit, repeat…
  - If error bit = 0, no error in any of R/W counters or latency value in I^2C register

- Pipeline & buffer data contents – i.e. fake hits
  - Send many triggers, look for 1 in output, when 0 expected

- I^2C register values
  - Written to and read back via I^2C serial interface
  - Typically set so approximately equal number of 0 & 1 in contents
  - Periodic check, e.g. at 2s intervals

CBC3.1 contents for different settings

	Number of logic 0	Number of logic 1
Default settings	2026	614
Test configuration	1234	1406

Pipeline logic SEUs

- None observed in any test
  - CBC2: 1.2 x 10^4 s (3.33 h)
  - CBC3.0: 5040 s (1.4 h) (reduced duration due to procedure error)
  - CBC3.1: 3 x 3662 s (3.05 h)
  - Total exposure ≈ 520 h at HL-LHC (3 weeks operation)

- Compute 99% CL Poisson upper limit for HL-LHC

- CBC2: < 5.1 x 10^{-6} SEU.s^{-1}

- CBC3.0: < 13.5 x 10^{-6} SEU.s^{-1}

- CBC3.0 + CBC3.1: < 4.7 x 10^{-6} SEU.s^{-1}

implementation of logic was different in CBC3 compared to CBC2 so can't really combine statistics

Pipeline data SEUs – Fake hit rate

- CBC3.1 is the most relevant
  - Procedure problem affected CBC3.0 result

- Triggers sent at 20 kHz for 3662 s
  - Latency set to 12.5 µs to maximise sensitivity
  - 66 hits observed in 7.32×10^{7} triggers
  - Flux factor cf. CMS = x 58.8

- Fake hit rate = 2.0×10^{-11} per trigger in CMS
  - Expected occupancy = 1-2 %

I²C SEUs in CBC2

Table 5: Summary of CBC2 bit-flips in I²C registers. N^{cycle} is the number of 10 min periods used for each run.

Run	Beam	Number of bit-flips					I²C refresh	
		$0 \to 1$	$1 \to 0$	Total	N^{cycle}	Total/N^{cycle}	Hz	pulse length
Run 4	On	5	11	16	7	2.29±0.57	-	-
Run 6	On	1	5	6	7	0.86±0.35	1	1 msec
Run 8	On	6	4	10	6	1.67±0.53	10	1 msec
Run 9A	On	5	21	26	10	6.50±1.27	10	25 nsec
Run 9B	Off	0	0	0	3	0.00±0.00	10	25 nsec
Run 12	On	4	16	20	6	3.33±0.74	-	-
Total		21	57	78				

<- control run

- 78 SEUs observed, with 1->0 more frequent
- Multiple bit-flips more frequent than expected
  - 38 x 1-bit, 5 x 2-bit, 6 x 3-bit, 3 x 4 bit
  - suspicion that triple-voting logic had cells too close together
    - but this appears to be incompatible with circuit layout
- I²C SEU rate in HL-LHC: ~0.17 $CBC^{-1}h^{-1}$ (runs 4 & 12)

some doubts about refresh mechanism efficiency so not all data included

I^2C SEUs in CBC3.0

CBC3.0 settings & exposure times
Read interval = 5 m (* 5 s)

Setting type	time [h]
A: all 0xff	4.64
B: all 0x00	1.62
C: all 0x0f	2.80
D: 0x80/0x7f	2.49
D: 0x80/0x7f (*)	0.42

Table 7: Summary of CBC3.0 bit-flips in I^2C registers.

Setting type	Number of bit-flips		
	Total	$0 \rightarrow 1$	$1 \rightarrow 0$
A	14	0	14
B	2	1	1
C	4	0	4
D	5	0	5
Total	25	1	24

- Tests carried out with different contents written to registers
  - trying to obtain balanced mixtures of 0 & 1
- No multiple bit-flips observed
- 25 SEUs observed
  - 1->0 ~ 24 times more frequent than 0->1

- I^2C SEU rate in HL-LHC: 0.031 ± 0.006 $CBC^{-1}h^{-1}$

CBC3.1 I^2C design changes

- To reduce SEU rate:

The I^2C registers for the CBC3 were designed in such a way that the SEU-tolerant Whitaker register cell for each bit of an 8-bit register employs its own set of standard inverters to buffer the reset and write signals, and produce their inverse for the purpose of controlling both n and p-type transistor switches in the circuit. These inverters are small in dimension, resulting in small node capacitances that make the circuit more susceptible to upset when an ionising particle deposits charge on the sensitive nodes. This was reasoned to be the cause of the single bit-flips observed during testing of the CBC3. To counter this without major changes to the ASIC, it was shown by simulation that by merging together all of the reset lines, and likewise all of the write lines, for every bit across the 8-bit register, the effective capacitance of the sensitive nodes was multiplied eight times and required a greater charge deposit to cause an upset. The registers in CBC3.1 were re-wired to implement this strategy.

- This was expected to increase SEU resistance but at the potential expense of causing all 8 bits to be upset
  - simulations showed immunity to 864 fC: x30 greater than CBC3.0

I²C SEUs in CBC3.1

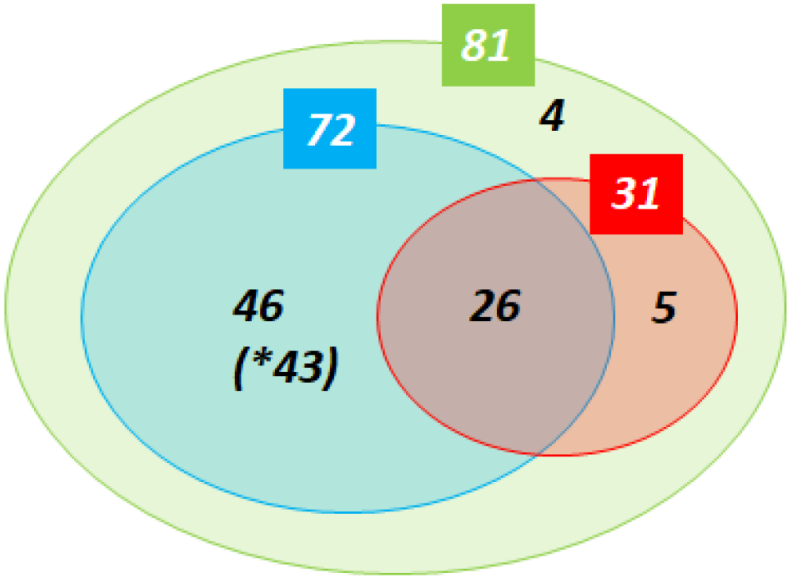
- Life is not so simple!
  - 15.4 hours used for I²C tests
  - Unlike CBC3.0 multiple bit flips observed
    - 38 x 1-bit
    - 10 x 2-bit, 3 x 3-bit, 9 x 4-bit, 4 x 6-bit 14 x 7-bit, 3 x 8-bit

- Gradually a possible pattern emerged
  - strongest correlation with last written value

CBC3.1 settings & exposure times
Read interval = 2 s

Last written value	time [h]
0xc1	1.66
0x55	2.01
0x00	0.96
0xff	0.72
0x00/0xff (*)	8.08
0x41	1.93

last written value
default value
neither



NB often LWV & default are indistinguishable

NB correlation with LWV means comparison with bits which changed – i.e. can't distinguish bits which were already identical to those in LWV

(* = multiple bits)

CBC3.1 I²C run details

- Data taken with different LWV, especially 0x00 and 0xff
  - to avoid possible TID effects, most data toggled between the two settings

Run ID	Last written value	duration [s]	No. SEU	rate [h^{-1}]
1	0xc1	1608	6	13.4 ± 5.5
2	0xc1	4370	10	8.2 ± 2.6
3	0x55	7241	13	6.5 ± 1.8
4	0x00	3464	0	0.0 ± 0.0
5	0xff	2579	6	8.4 ± 3.4
6	0x00/0xff	4916	10	7.3 ± 2.3
7	0x00/0xff	3152	3	3.4 ± 2.0
8	0x00/0xff	3277	5	5.5 ± 2.5
9	0x00/0xff	2232	5	8.1 ± 3.6
10	0x00/0xff	3814	2	1.9 ± 1.3
11	0x41	3372	2	2.1 ± 1.5
12	0x41 (*)	3561	0	0.0 ± 0.0
13	0x00/0xff	11694	19	5.8 ± 1.3
total		55280	81	5.3 ± 0.6

CBC3.1 I^{2}C results

- For similar exposure times
  - 3 SEUs with 0x00 (5.00 h) vs 47 with 0xff (4.76 h)
- Scaling to HL-LHC flux:

Table 14: Comparison of SEU rates in the CBC3.0 and CBC3.1 I^{2}C registers depending on the last written register value.

CBC version	Last write value	SEU rate at HL-LHC [/h/chip]
CBC3.0	–	0.031 ± 0.006
CBC3.1	all used	0.090 ± 0.010
CBC3.1	0xc1	0.164 ± 0.041
CBC3.1	0x55	0.110 ± 0.030
CBC3.1	0x41	0.018 ± 0.012
CBC3.1	0xff	0.168 ± 0.025
CBC3.1	0x00	0.010 ± 0.006

Conclusions

- CBC3.1 design changes did not act quite as expected but a strong correlation between SEU rate in I^2C registers and last written value was observed
  - Writing 0x00 is much more favourable, with SEU rate ~ 0.01 $CBC^{-1}h^{-1}$
- NB very few of the registers (<5%) have significant effect on operation
- Rate could be much further reduced by intermittent refresh
  - e.g. in orbit gaps or when other CMS resets are issued
- Comparison with other SEU rate measurements
  - almost no data is reported from CMS operations, and the only chips which appear to have been extensively evaluated are the APV25 and, to a lesser extent, the ATLAS SCT FE.
  - Few chips seem to have SEU rate specification, e.g.:

Radiation tolerance	500 Mrad, 1×10^{16} n_{eq}/cm^2 at −15 °C
SEU affecting whole chip	< 0.05/hr/chip at 1.5 GHz/cm^2 particle flux
Power consumption at max. bit/trigger rate	< 1 W/cm^2 including SLDO losses

Backup

Table 12: Summary of CBC3.1 bit-flips in I^2C registers for day 1 of the test. Columns I and II show if the bit-flips are consistent with the last written value, the default value, or neither. 1 = consistent, 0 = inconsistent.

Evt.	Page	Addr.	Written	Read	Default	Last written	I	II	1→0	0→1	# bfs
					Run ID 1						
1	2	0x7e	10000000	11000001	10000000	11000001	0	1	0	2	2
2	2	0xac	01111111	00111111	10000000	11000001	1	0	1	0	1
3	1	0x4d	01100110	11100111	01100110	11000001	0	1	0	2	2
4	2	0xfe	01111111	11111111	10000000	11000001	1	1	0	1	1
5	1	0x3c	11111111	01111111	11111111	11000001	0	0	1	0	1
6	2	0xdf	01111111	11111111	10000000	11000001	1	1	0	1	1
					Run ID 2						
7	1	0x3d	11111111	10111111	11111111	11000001	0	0	1	0	1
8	2	0x27	10000000	11000001	10000000	11000001	0	1	0	2	2
9	1	0x1c	10000100	10000101	00000000	11000001	0	1	0	1	1
10	2	0xfb	01111111	11111111	10000000	11000001	1	1	0	1	1
11	2	0xa7	01111111	11111111	10000000	11000001	1	1	0	1	1
12	2	0x70	10000000	11000001	10000000	11000001	0	1	0	2	2
13	1	0x13	00000000	11000001	00000000	11000001	0	1	0	3	3
14	2	0x7b	10000000	11000001	10000000	11000001	0	1	0	2	2
15	1	0x41	10101010	11101010	10101010	11000001	0	1	0	1	1
16	2	0x5a	10000000	11000001	10000000	11000001	0	1	0	2	2
					Run ID 3						
17	2	0x4d	10000000	11010101	10000000	01010101	0	1	0	4	4
18	2	0x73	10000000	11010101	10000000	01010101	0	1	0	4	4
19	2	0x9f	01111111	01111011	10000000	01010101	1	0	1	0	1
20	2	0x4f	10000000	11010101	10000000	01010101	0	1	0	4	4
21	1	0x15	00000000	01010100	00000000	01010101	0	1	0	3	3

Fake stub rate estimate

- Based on CBC3.1 fake hit rate = 2.0 x 10^{-11} per trigger in CMS
  - with latency set to 12.5 µs

- Scale for stub rate
  - rate = 2.0 x 10^{-11} x 40 MHz x (25 ns/12.5 µs) = 1.6 x 10^{-6} s^{-1}
  - x factor for number of channels per chip (=128?)
  - => 2 x 10^{-4} CBC^{-1} s^{-1}

- assumes that one bit is sufficient to fake a stub