CBC3.1 wafer testing update

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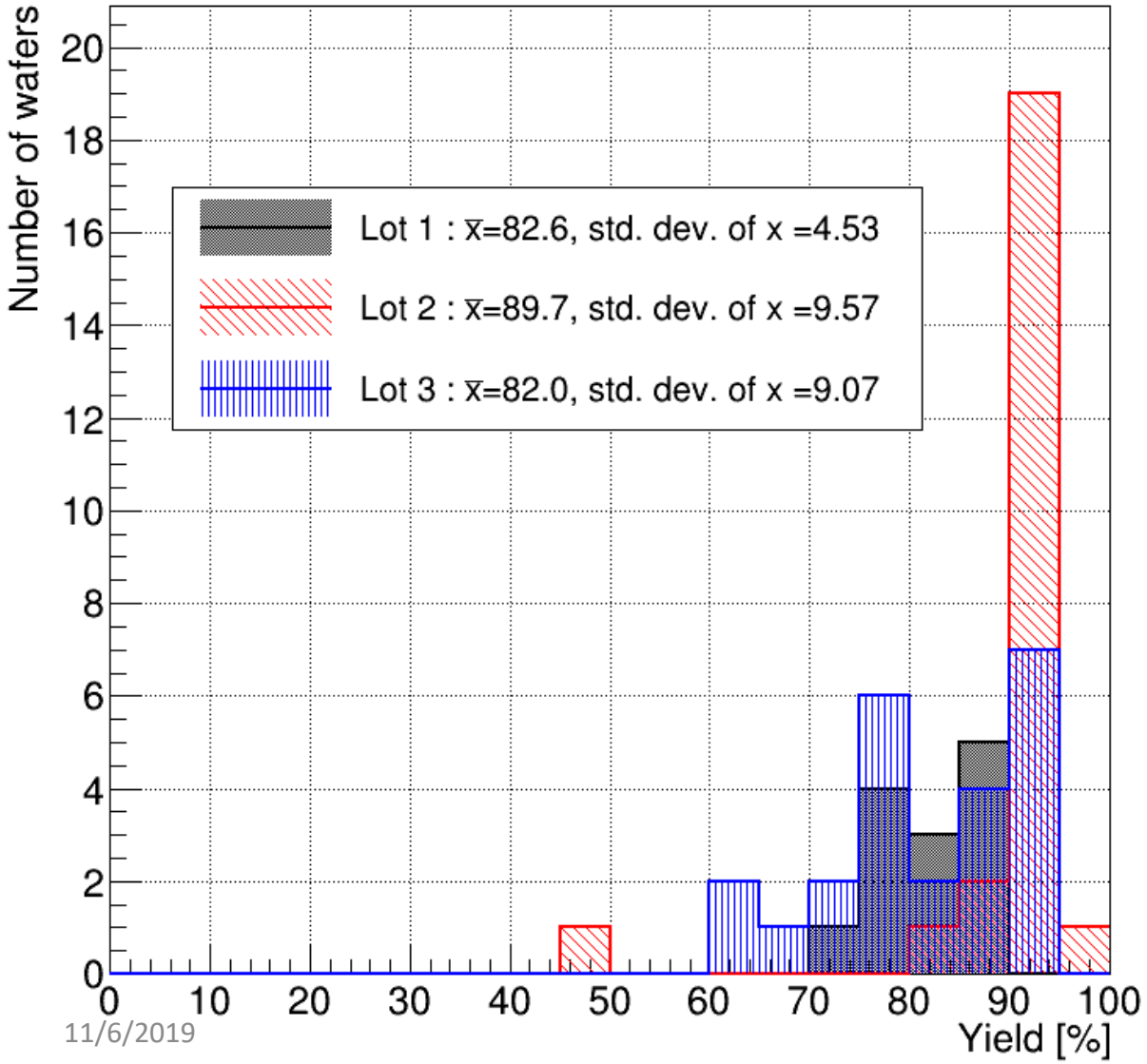
The last status and update

- The last month
  The test results of some wafers from lot2 & lot3 were reported.
  - 17 wafers from lot2 and 5 wafers from lot3.
  - The Yield of wafers from lot2 was very high, 88.5%.
  - A new pattern of bad chip distribution was observed on wafers from lot3 and the yield dropped to 80.3%.

- Update
  All the wafers from lot2 & lot3 have been tested. 24 wafers for each lot.

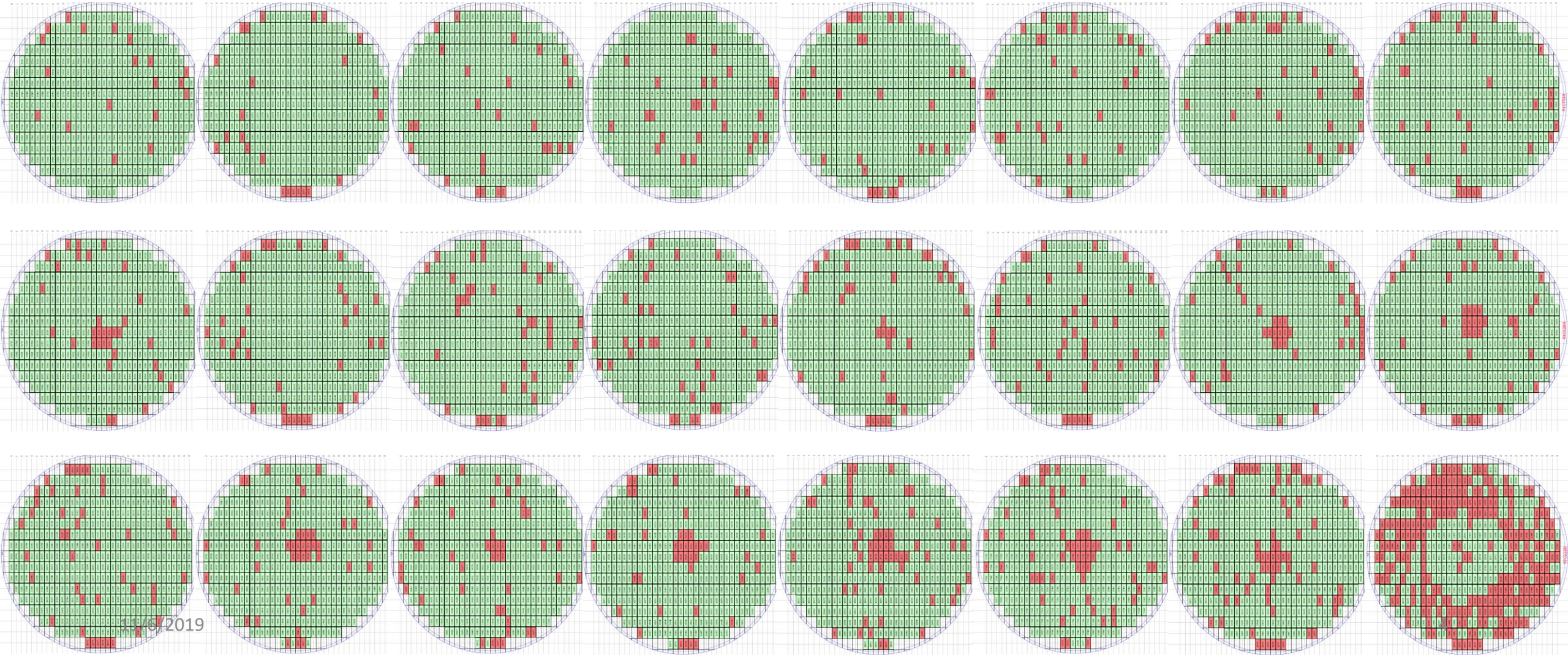
Yield for all the tested wafers



Yield of lot3 dropped compared with lot 2 and the distribution is wide.

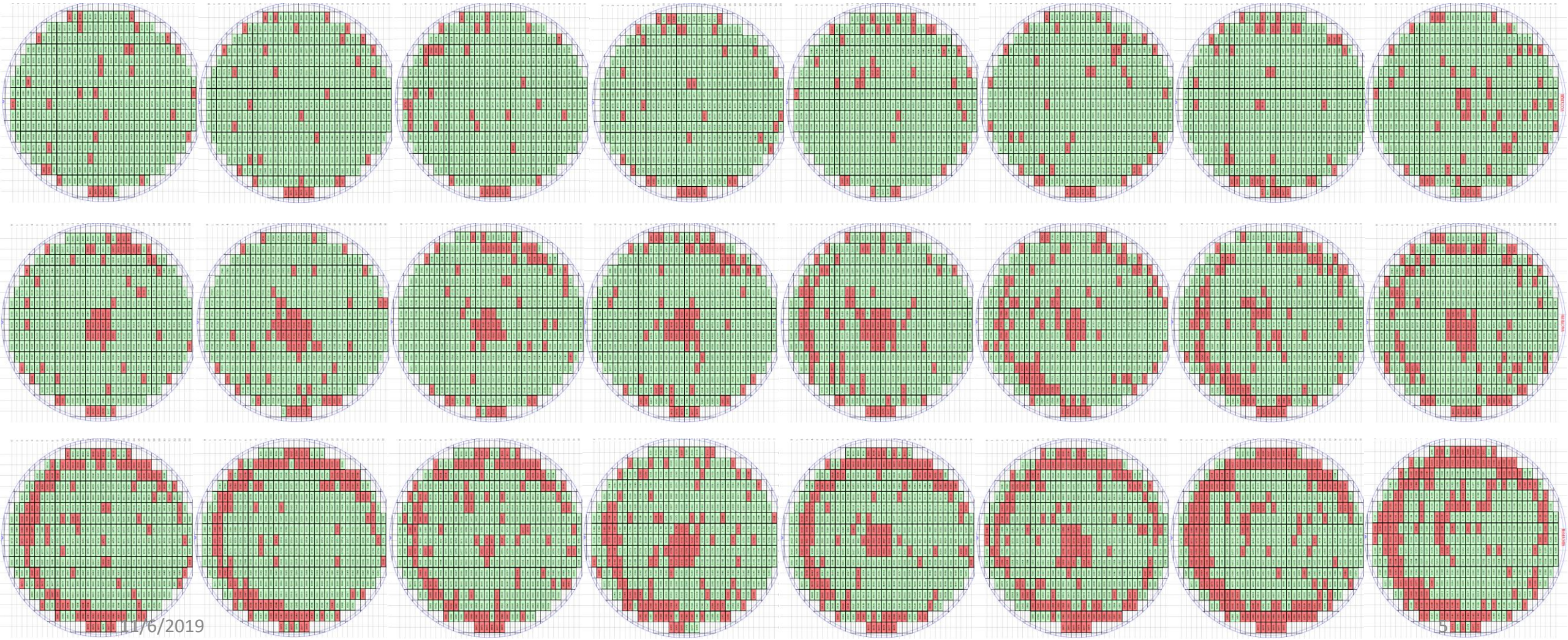
Lot 2 wafer maps (ordered by the yield)
good chip : green, bad chip : red

The central part is improved very much in lot2.

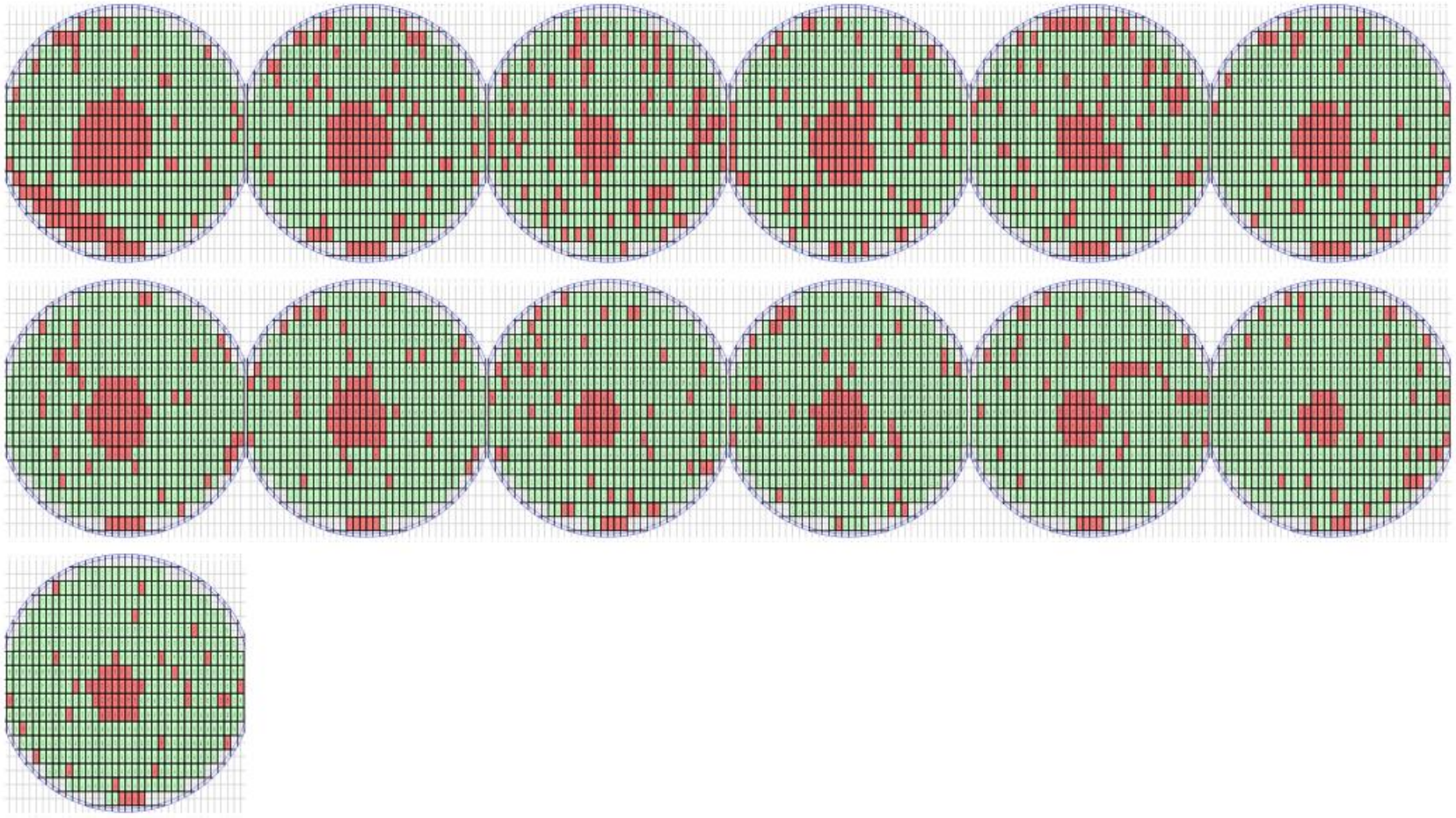


Lot 3 wafer maps (ordered by the yield)
good chip : green, bad chip : red

The central part is still better than lot1, but not as good as lot2.
New ring pattern at the outer part appeared.



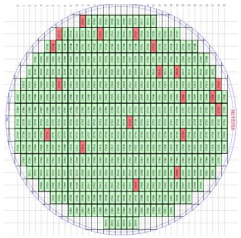
Lot 1 wafer map

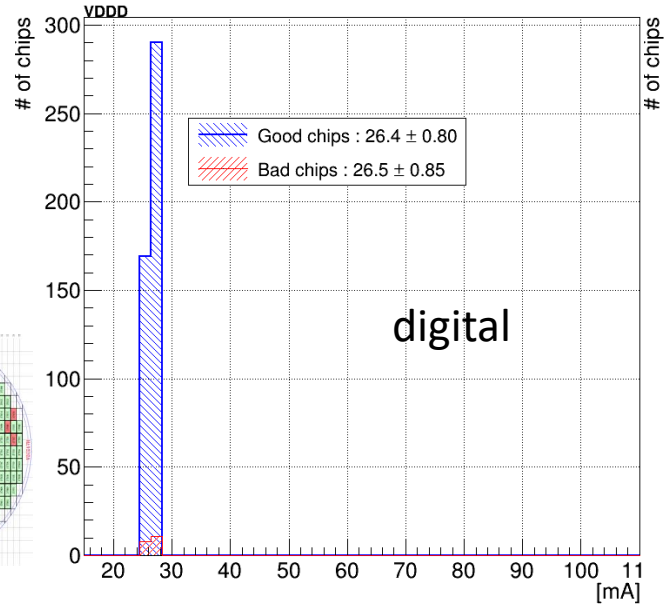


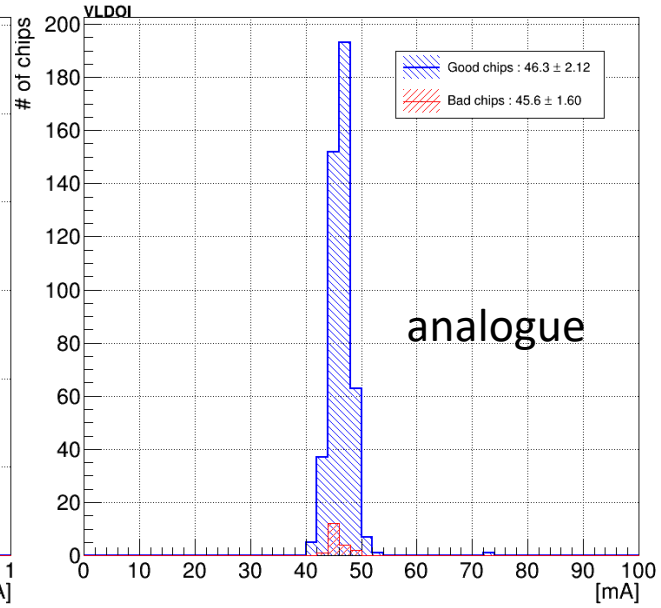
Current problem in the worst wafer from the lot 2

Currents just after power on for the best wafer and the worst wafer for digital and analogue

The best wafer, VZCZ17H : Yield 96.0%

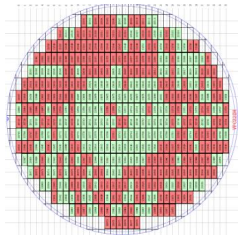


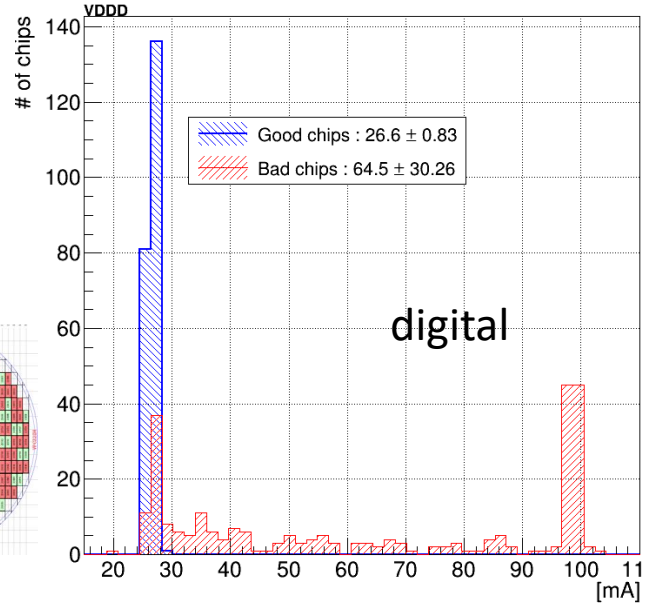


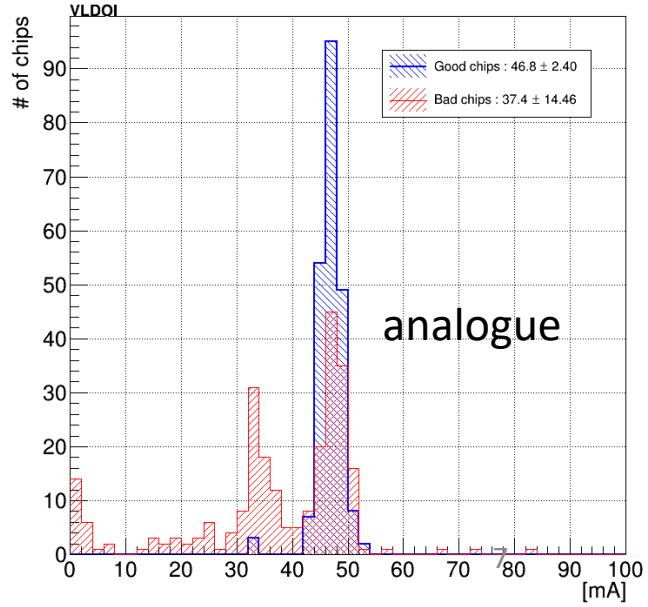


Bad chips in the wafer with the worst yield of this lot show abnormal currents.

The worst wafer, VPCZ2ZH : Yield 45.6%







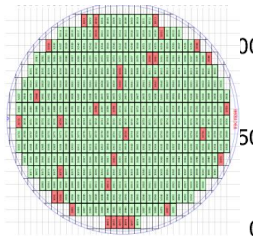
Current check on lot 3 wafers

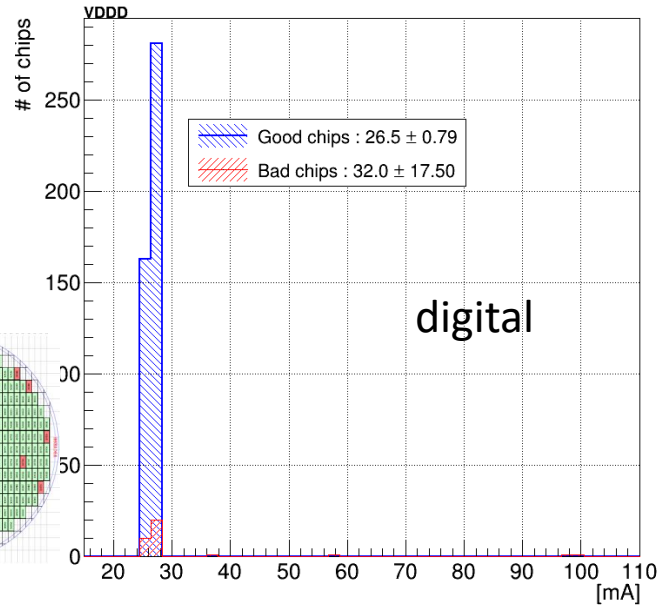
Currents just after power on for the best wafer and the worst wafer for digital and analogue

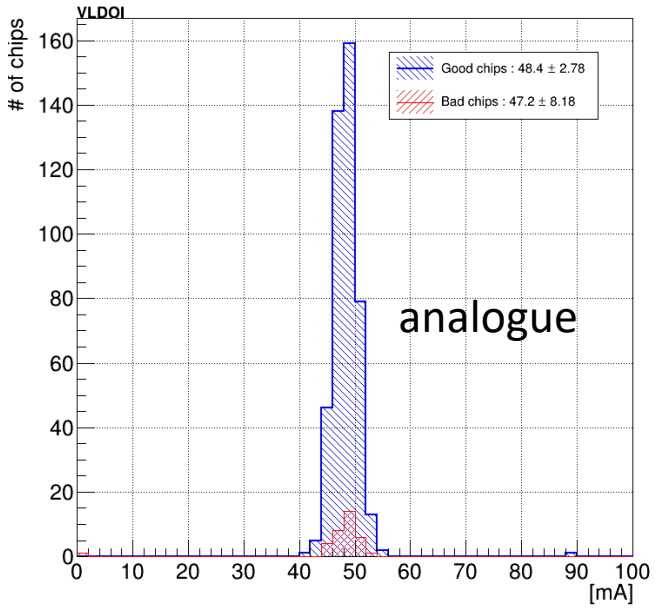
Bad chips in the wafer with the worst yield of this lot show normal currents.

-> different problem from the one in lot2.

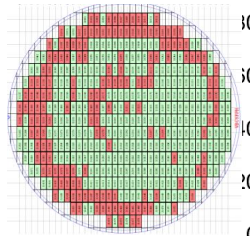
The best wafer, V9CYE9H : Yield 92.8%

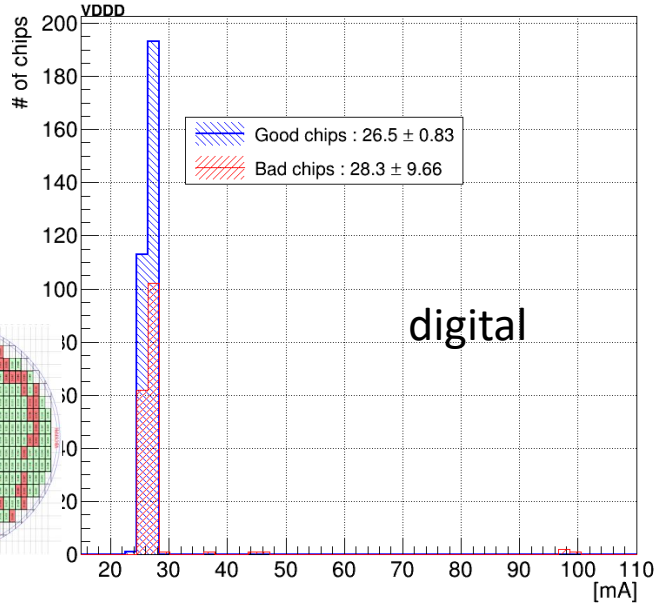


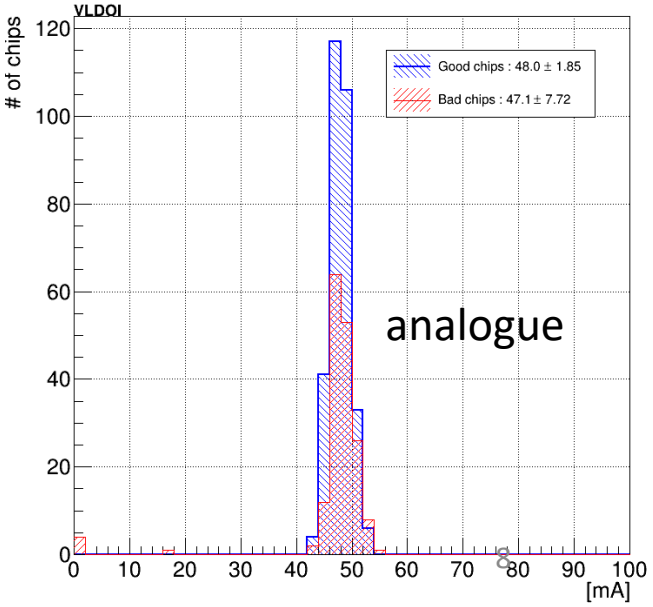




The worst wafer, VBCYFPH : Yield 64.2%





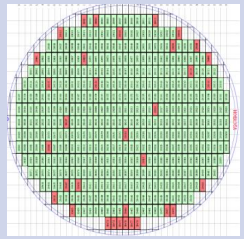
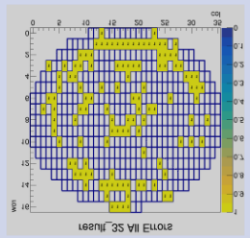
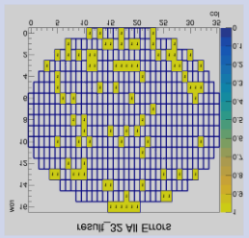
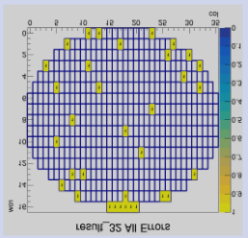
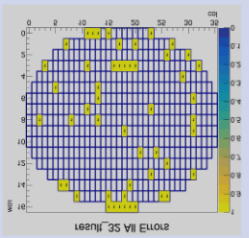
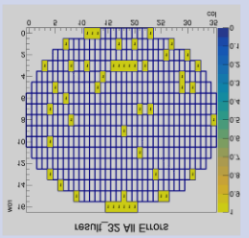
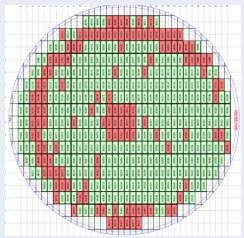
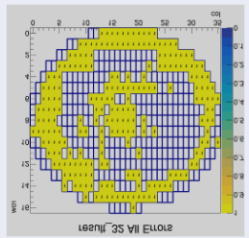
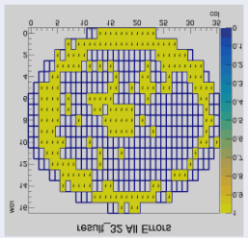
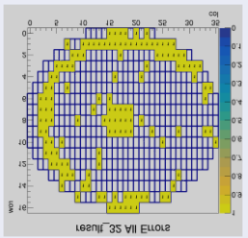
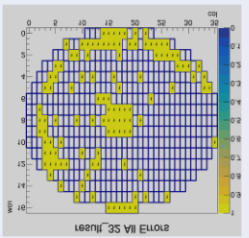
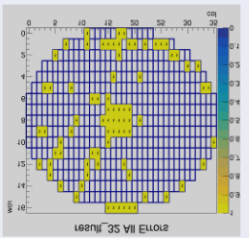


Voltage scan on lot 3 wafers

Input voltage : 1.08, 1.14, 1.26, 1.32 V for two wafers

The yield correlate with the input voltage.
Most of the errors seems to be in the pipeline value check in the data when consecutive triggers are sent to CBCs.
However, tuning the test pulse timing, even with the corrupt pipeline value, hit data comes out fine.

Input voltage [V]	1.08	1.14	1.20	1.26	1.32
V2CYB0H Yield [%]	75.3	82.8	92.8	89.3	89.7
V6CYDVH Yield [%]	53.3	60.2	72.3	75.9	83.2

Summary

- All the produced wafers for lot1(13), lot2(24), lot3(24) have been tested.
  - The lot2 shows very high yield except for one wafer which shows abnormal current values.
  - Some wafers show clear central pattern in the lot3.
  - New ring pattern at the edge of wafers appeared in nearly half of the wafers in the lot3.
- More analyses and voltage scan are work in progress.