

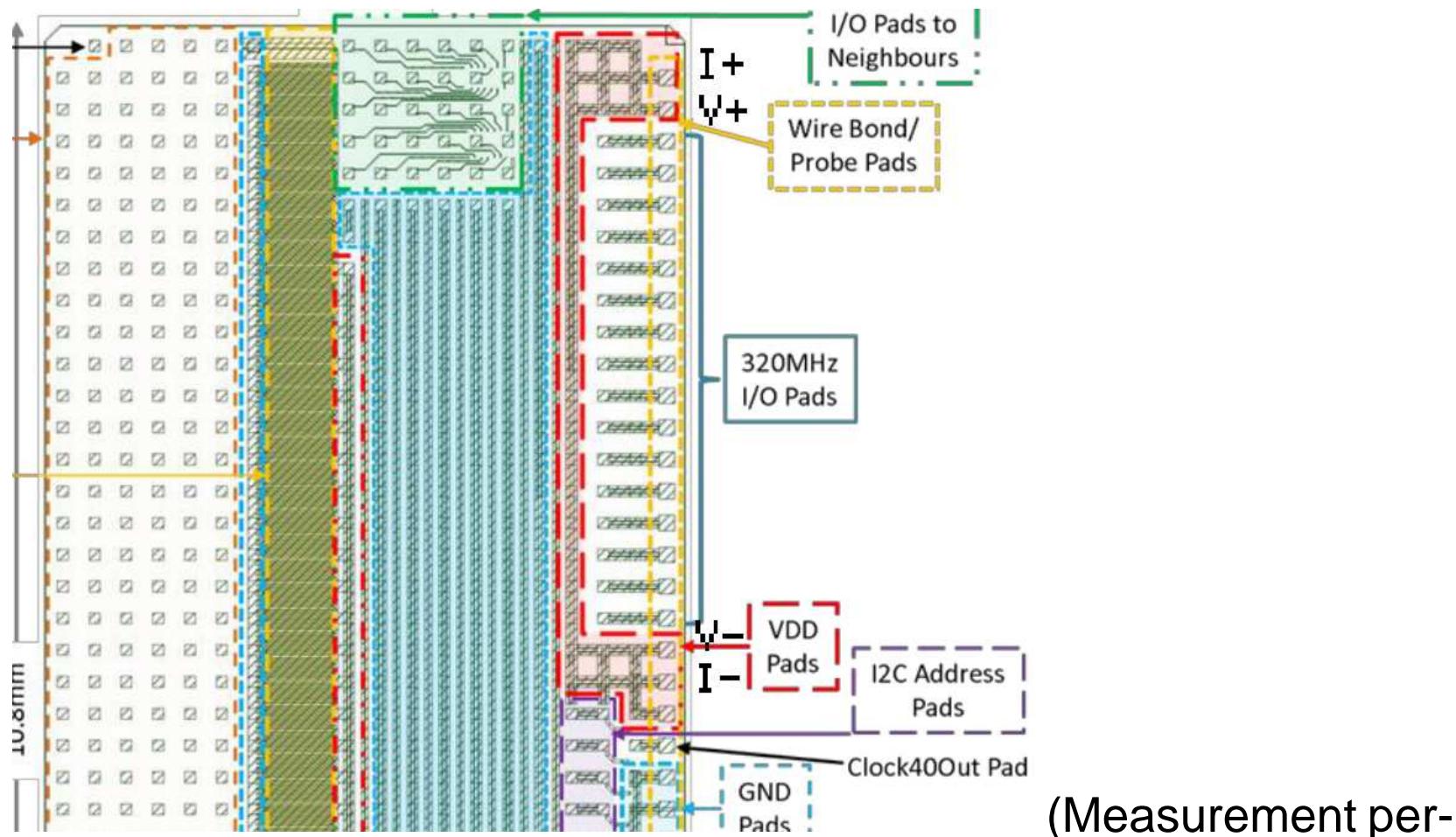
CBC3.1 VDDD metal resistance measurements

2019-12-18

Johan Borg

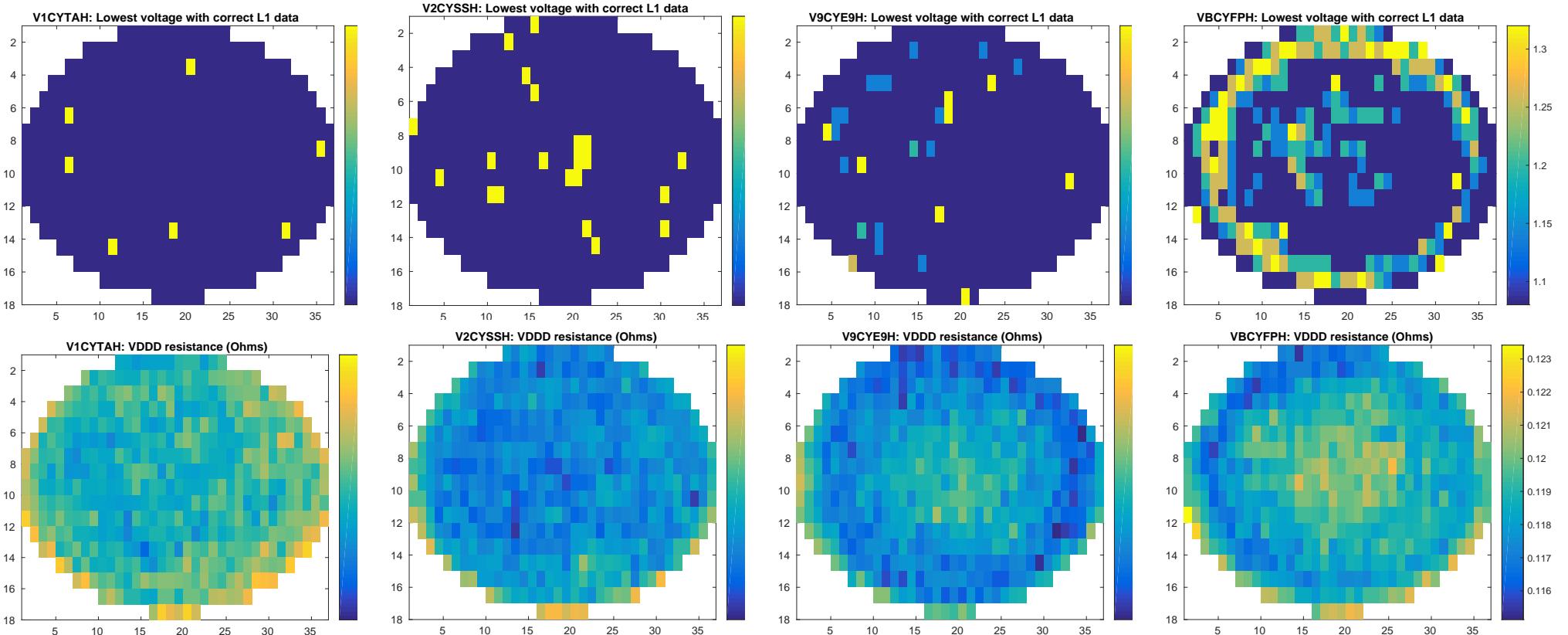
Imperial College London

Connections



formed using a Keithley 2110)

L1 Data errors vs metal resistivity



(from left to right: good lot 2 wafer, bad lot 2, good lot 3, bad lot 3)

Conclusions

- No clear correlation between metal resistance measurements and high required voltage
- Initial attempts to correlate bias voltages with supply voltage required for correct L1 data also failed to show significant correlation.
- Low-temperature wafer tests in progress.