CBC3 Lot2-3 wafer testing results

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with thanks to:

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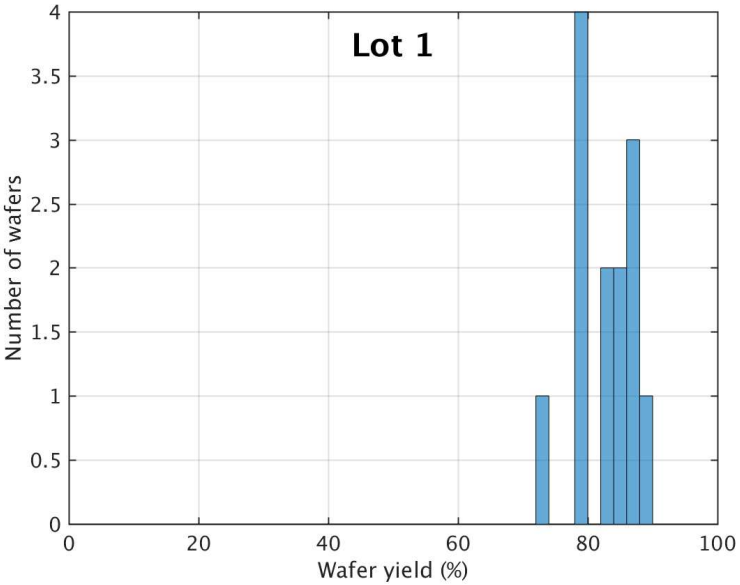
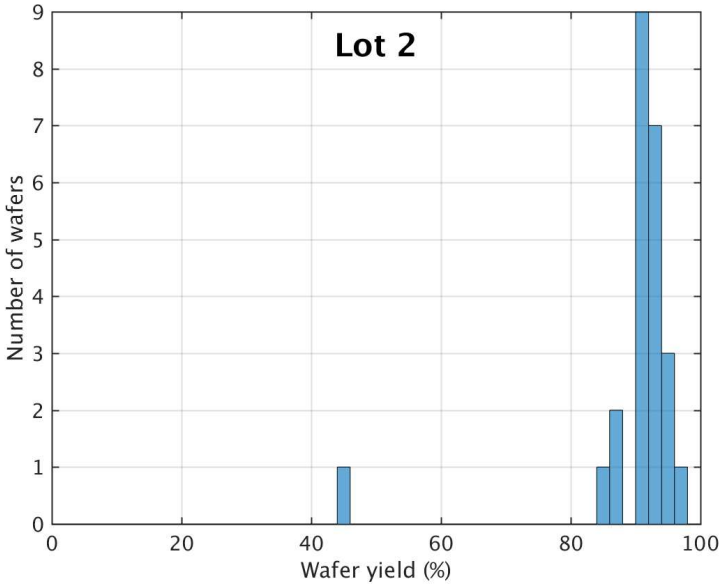
CBC3.x production overview

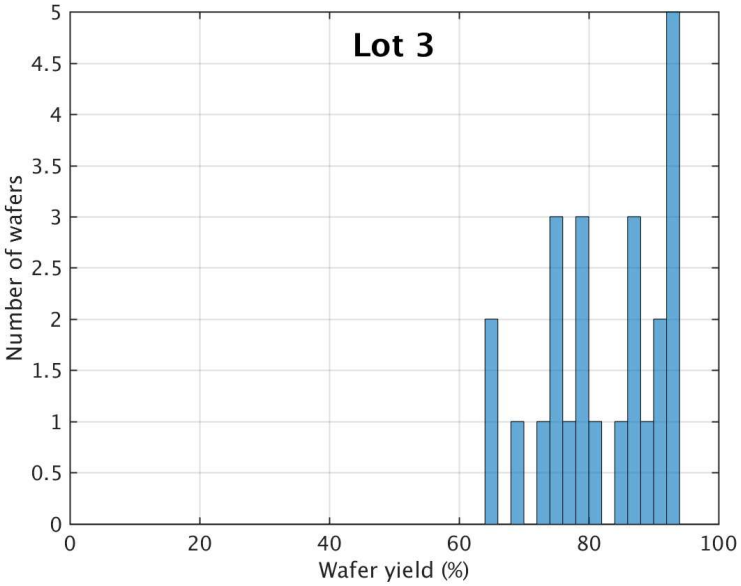
- CBC3.0 engineering run delivered December 2016
- CBC3.1 engineering run ("Lot 1") September 2018 exhibited pattern of low yields
- GF tuned process to improve yields.
- Lot 2 and 3 (24 wafers each) delivered 2nd and 26th of September 2019.
- Lot 2 shows clear improvement in yield
- Lot 3 exhibits lower yield for particular tests

Yield histograms





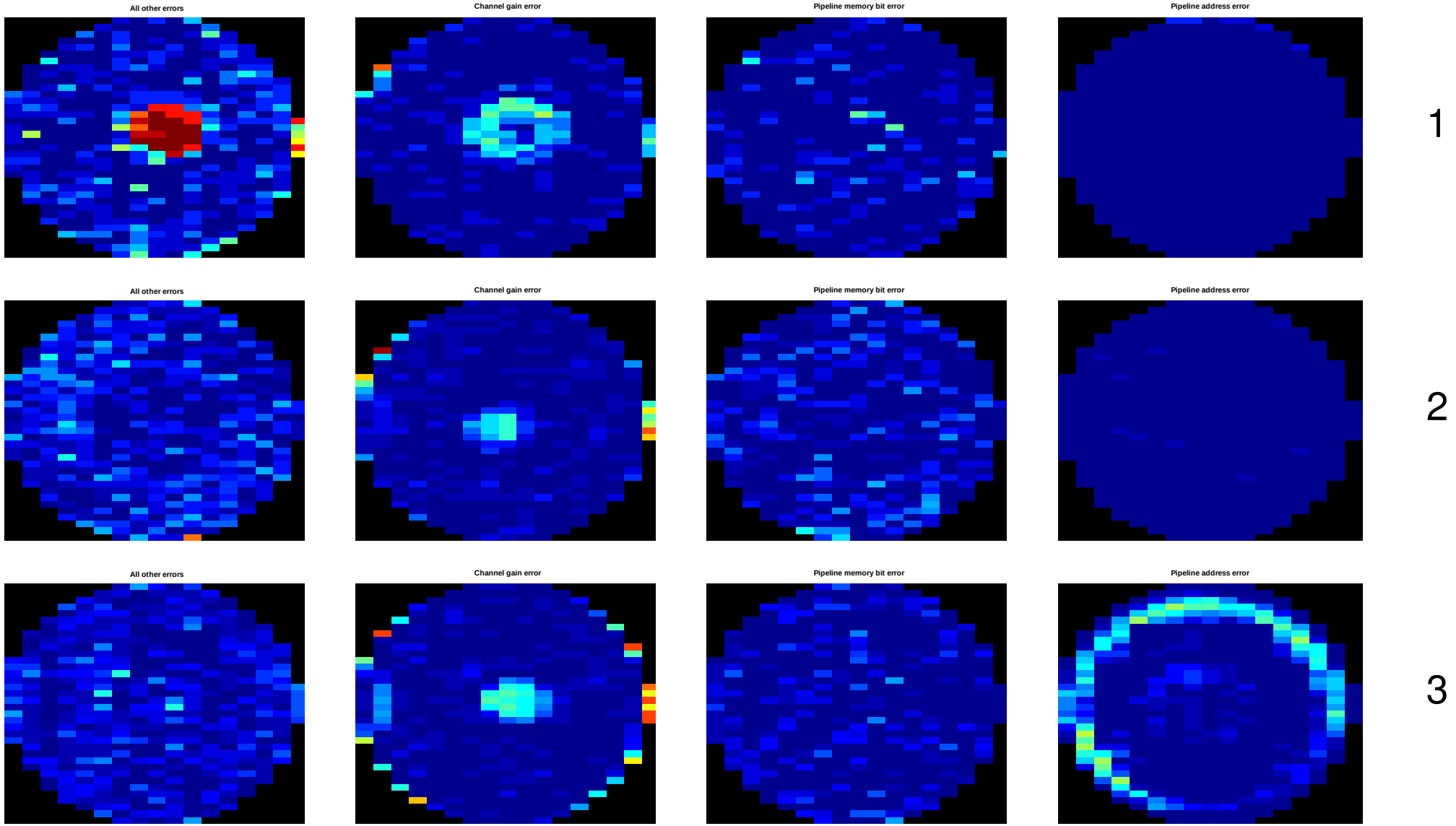
- Lot 1: 82.5%
- Lot 2: 89.7%
- Lot 3: 82.1%
- Large yield spread for Lot 3.



Failure mode definitions

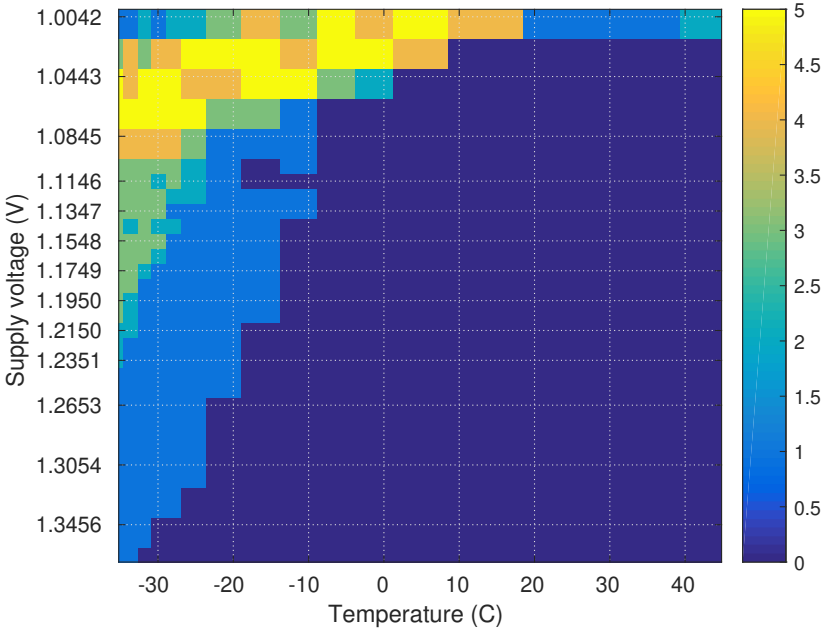
- **Gain**
  The gain of one or more channels deviates substantially from the norm
- **Pipeline bit**
  A stuck bit in the pipeline memory, affecting one channel once every 512BX
- **Pipeline addr**
  The pipeline address transmitted in the L1 data packet is corrupted. Doesn't affect the data.
- **Other**
  Any other failure: mostly interface logic, I2C register or stub decoding errors

Lot1,2,3 failure modes



Note the sharp circular pattern of errors on lot 3

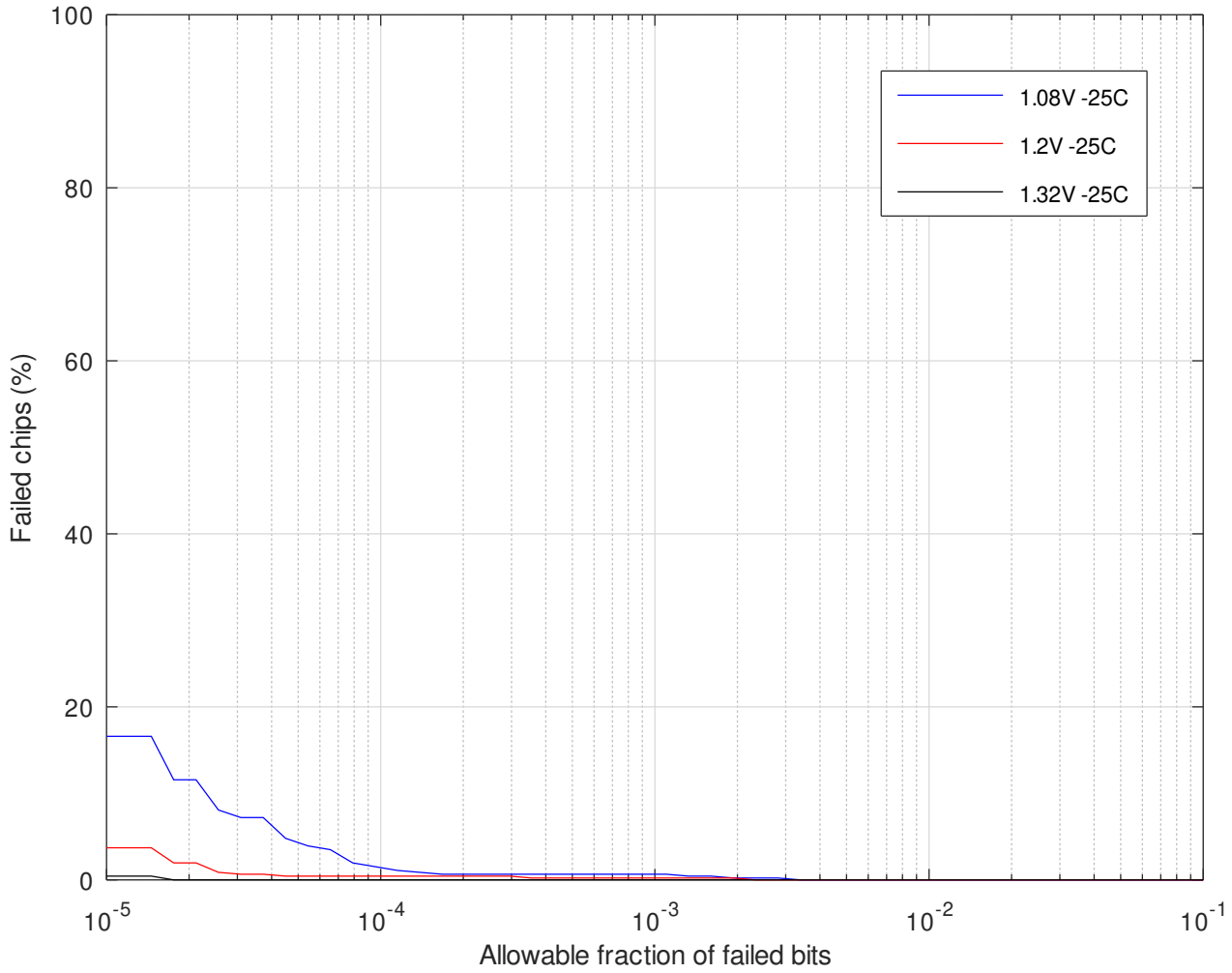
Lot 3 analysis



- Significantly more Pipeline address errors
  - Harmless during normal operation
  - Temperature dependence observed for wire-bonded Lot1 chips
- Some pipeline data memory errors observed at reduced supply voltage (see next slides)
  - No significant impact on performance expected unless fraction approaches detector occupancy
- Low temperature wafer tests implemented to study the impact on the yield in more detail
- To date one Lot 2 and one Lot 3 wafers have been re-tested over temperature and supply voltage, but the anomalous performance of Lot 3 is not yet understood

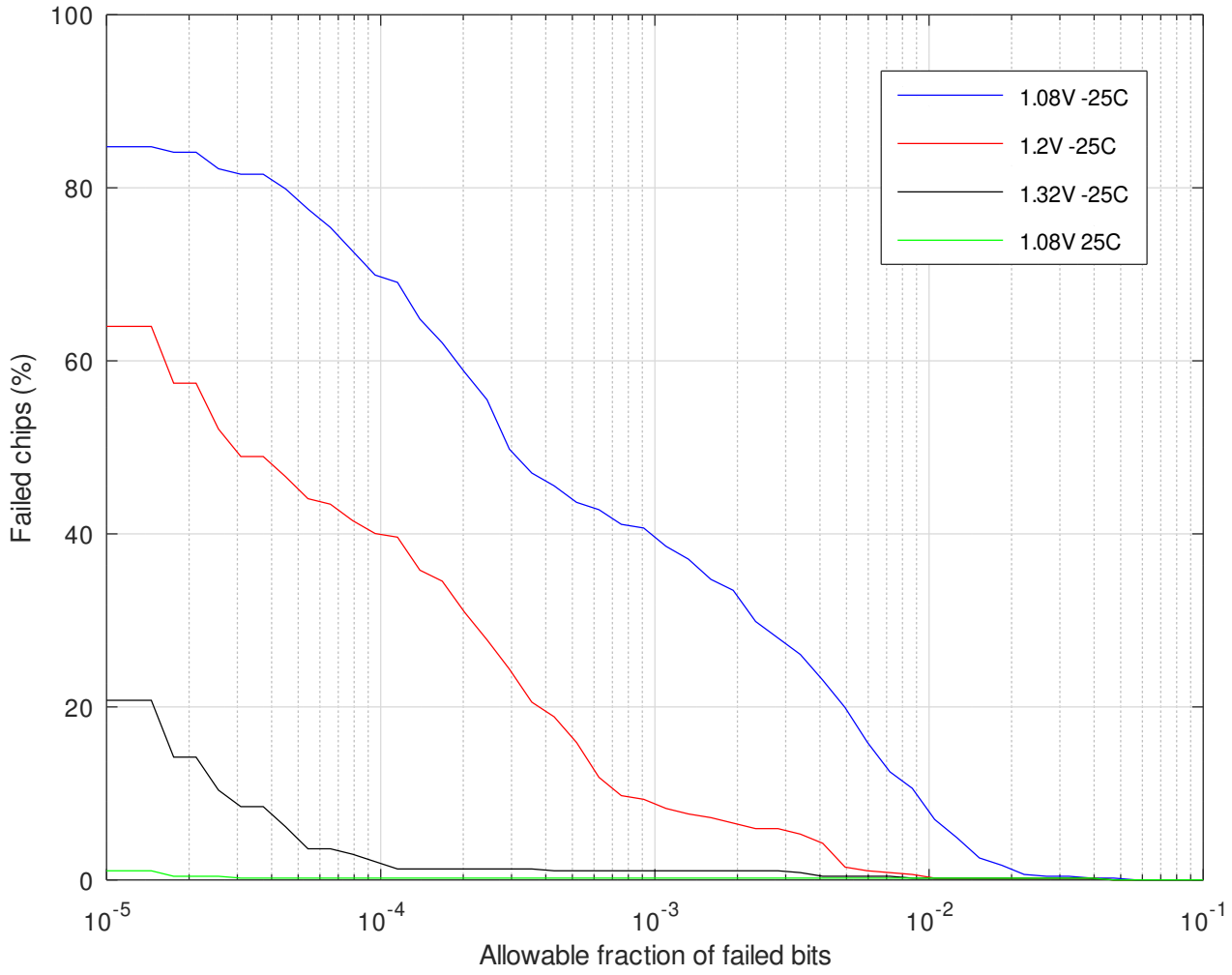
Lot 2 pipeline bit errors at -25

Lot 2 chips exhibits a small number of errors at low supply voltage



Lot 3 pipeline bit error at -25

Lot 3 is clearly different, reduced yield at nominal supply voltage.



Analysis of process control monitoring data from Fab

- Only data from 15 sites received
  - 5 measurements from 3 Lot 1 wafers
  - No lot 2 measurements
  - 5-15 (not everything was measured at every site) from a Lot 3 wafer
- All parameters within specification
- Worst NMOS and PMOS VT(sat) a bit worse on Lot3, but difference is not huge
- Doubtful whether any conclusions can be drawn from this limited dataset
- Is this all we can get from the fab?

Other activities

- Issues with probing seems to be more or less resolved. Currently blamed on contamination from silicone oil vapor from coolant system.
- Heat transfer fluid changed to ethylene glycol+water (rather viscous at -25, but works OK).
- 2 Wafers (one from lot 2 and one from lot 3) has been sent for dicing, to be returned on blue-tape to allow us to pick selected dies to test soldered.
- New probe cards ordered
- Design of new chuck for probe station completed, manufacturing pending.

PRR: preliminary 25th of March

Agenda:

- Context
  - CMS-OT electronic system
  - Contract framework with GF
- Status
  - Background
  - ASIC description, specifications
  - Test campaigns and results
  - System level verification framework and results
  - System tests and Beam tests
- Plans
  - Quality control, database, traceability, storage, transport, logistics, documentation
  - Production and test plans, resources, schedule