



Two-in-one module PT logic

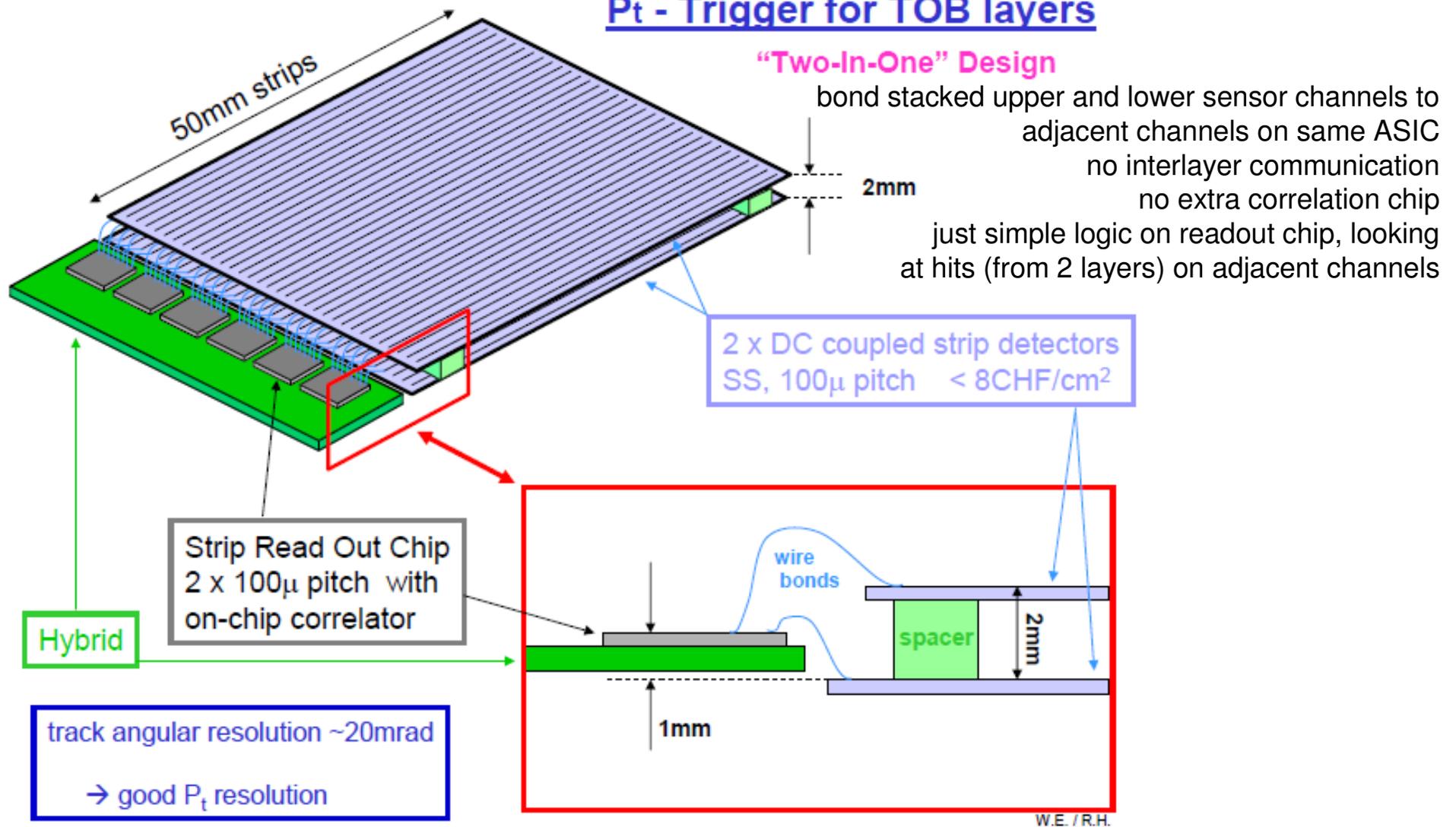
already have a prototype readout chip for short strips in hand

CBC (CMS Binary Chip) – see talk yesterday

will describe relatively simple changes which could be implemented to provide 2-in-1 triggering functionality

ACES Workshop, March 2011
Mark Raymond, Imperial College.

P_t - Trigger for TOB layers



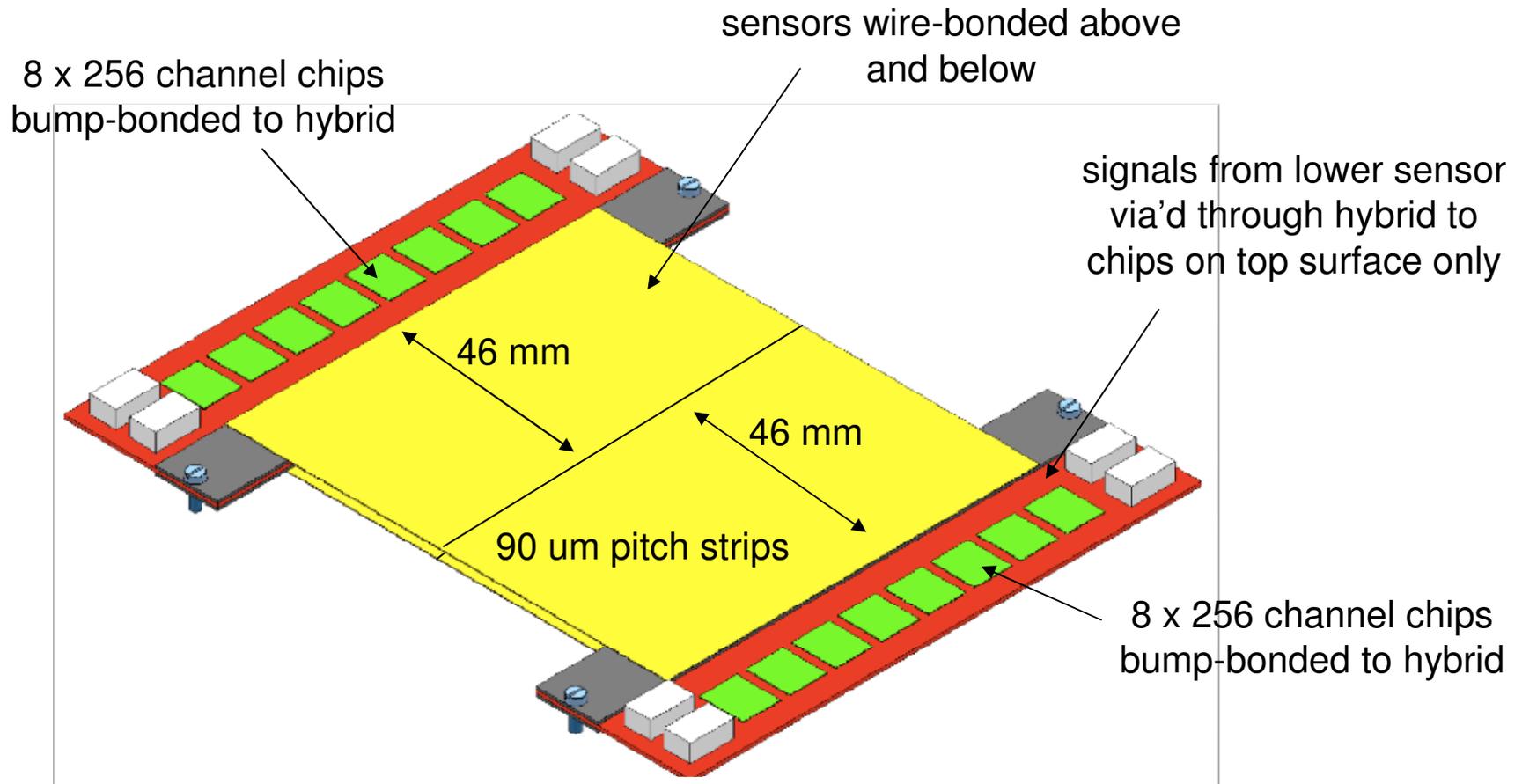
concept proposed by R.Horisberger and W.Erdmann (2008)

<http://indico.cern.ch/getFile.py/access?contribId=3&sessionId=0&resId=0&materialId=0&confId=36580>

much of the material in this talk is based on their proposal

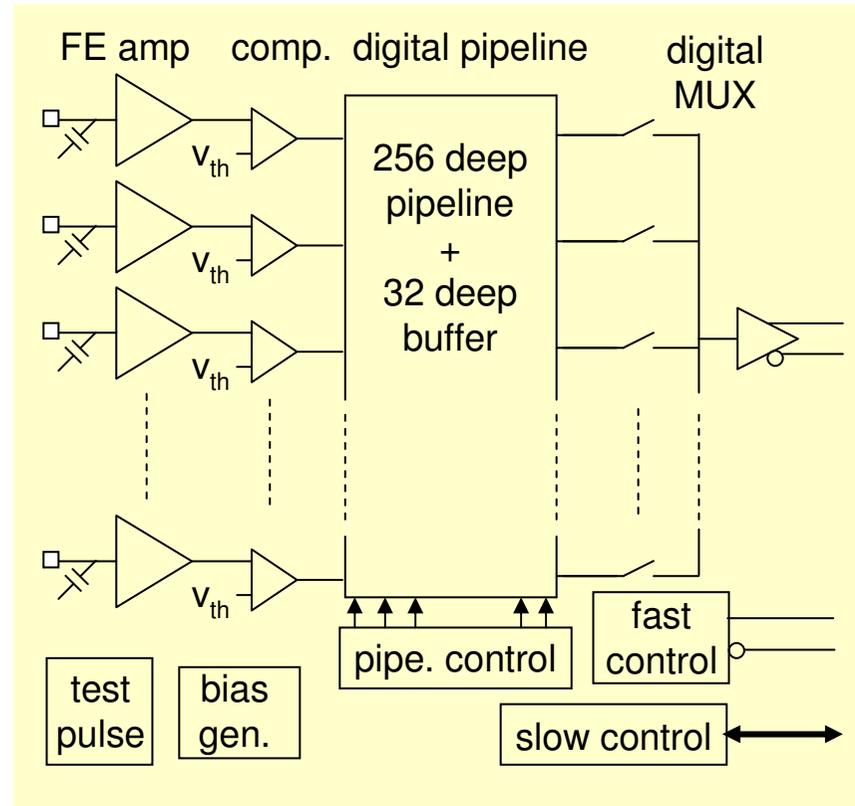
“hi-tech” 2-in-1 module concept

from Duccio Abbaneo’s talk yesterday



256 channels x 8 chips x 2 ends = 4096 electronics channels
2048 channels per sensor layer

CBC – current architecture



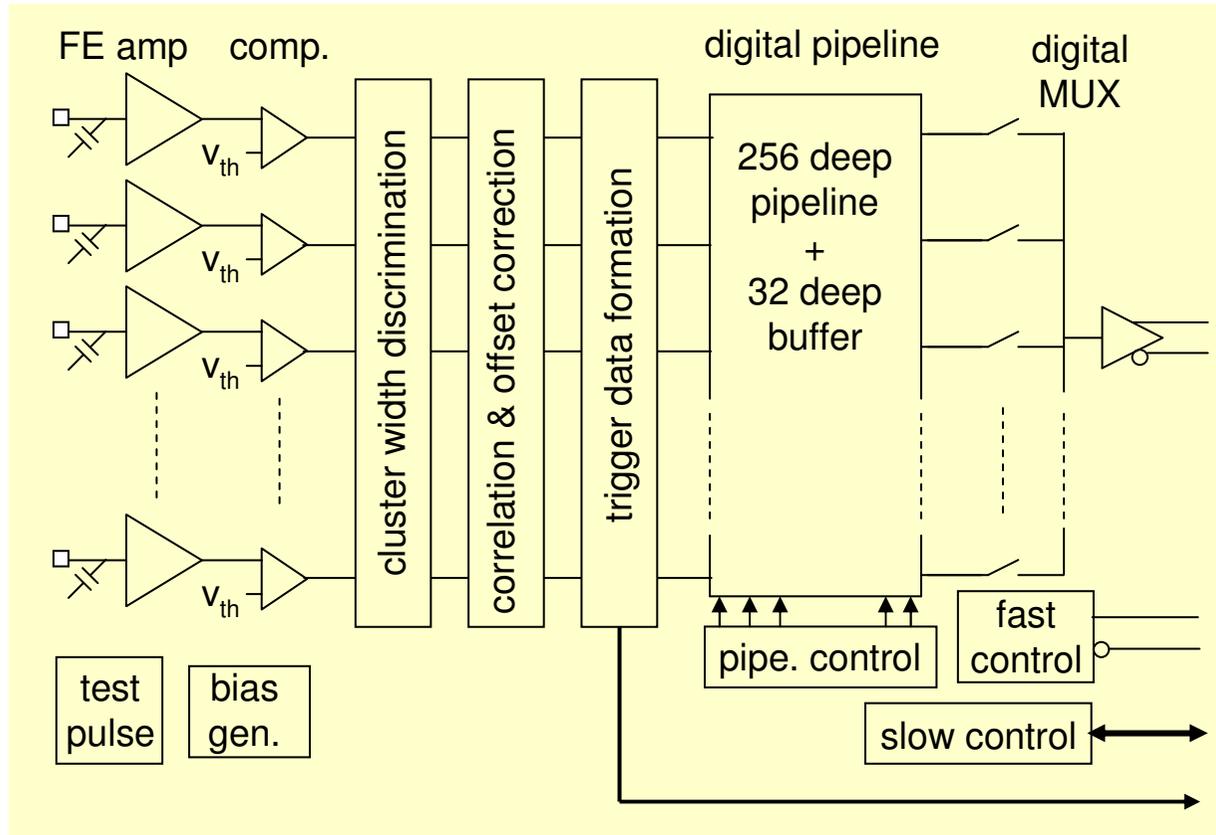
CBC prototype is 128 channel chip at the moment

current architecture implements unparsified readout of L1 triggered binary data

1st prototype is working (talk yesterday)

what changes are required if want to implement 2-in-1 triggering?

CBC + (2-in-1) triggering



3 new blocks

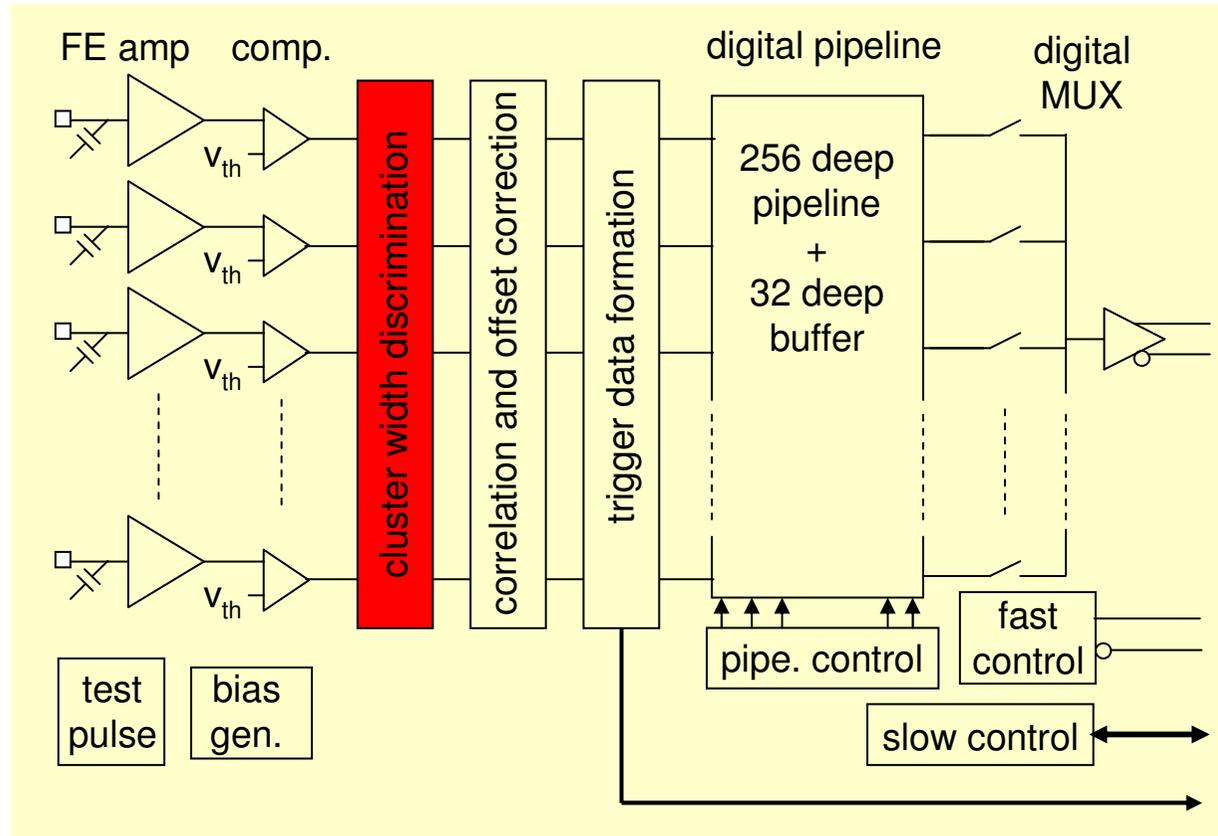
cluster width discrimination

correlation & offset correction

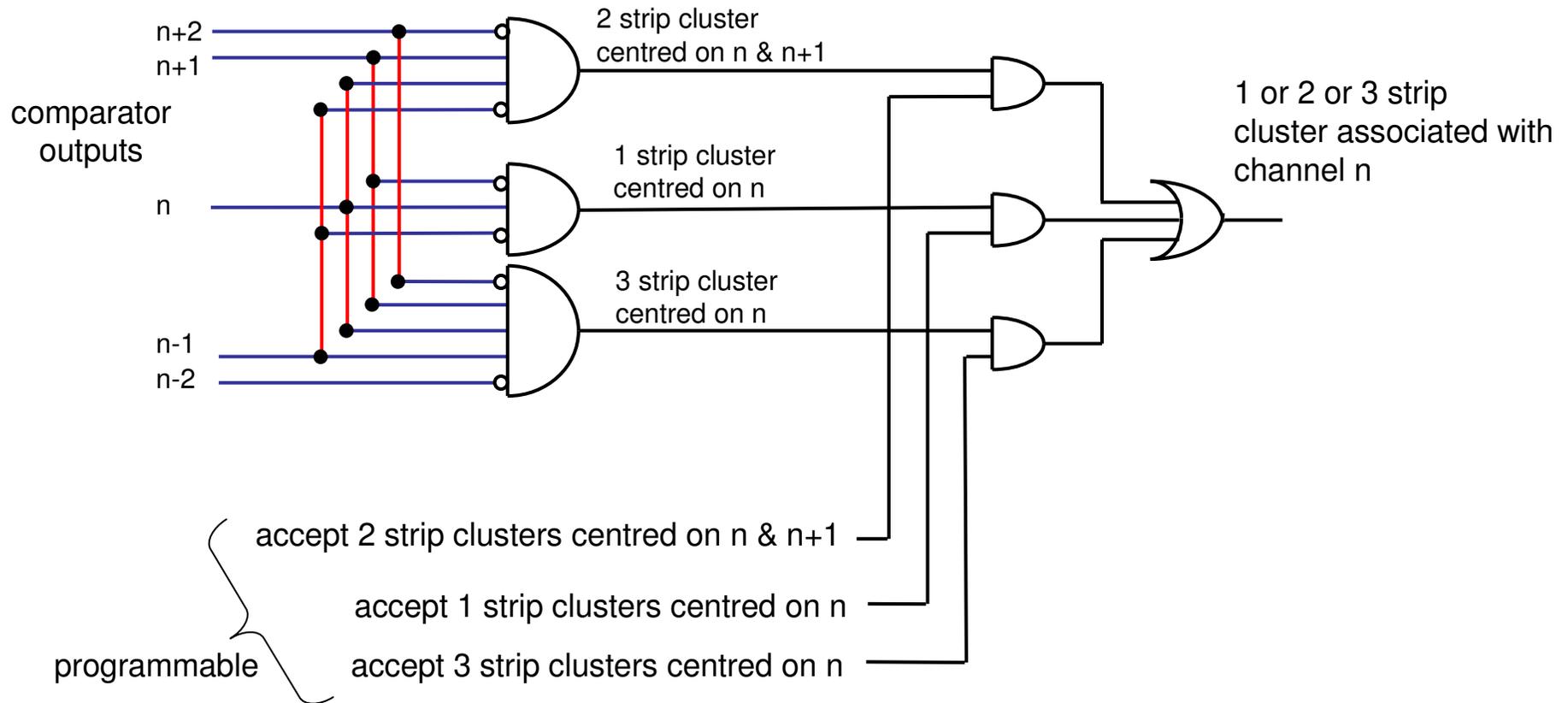
trigger data formation and off-chip transmission

also chip needs to be 256 channels wide – 128 channels from each layer

Cluster Width Discrimination

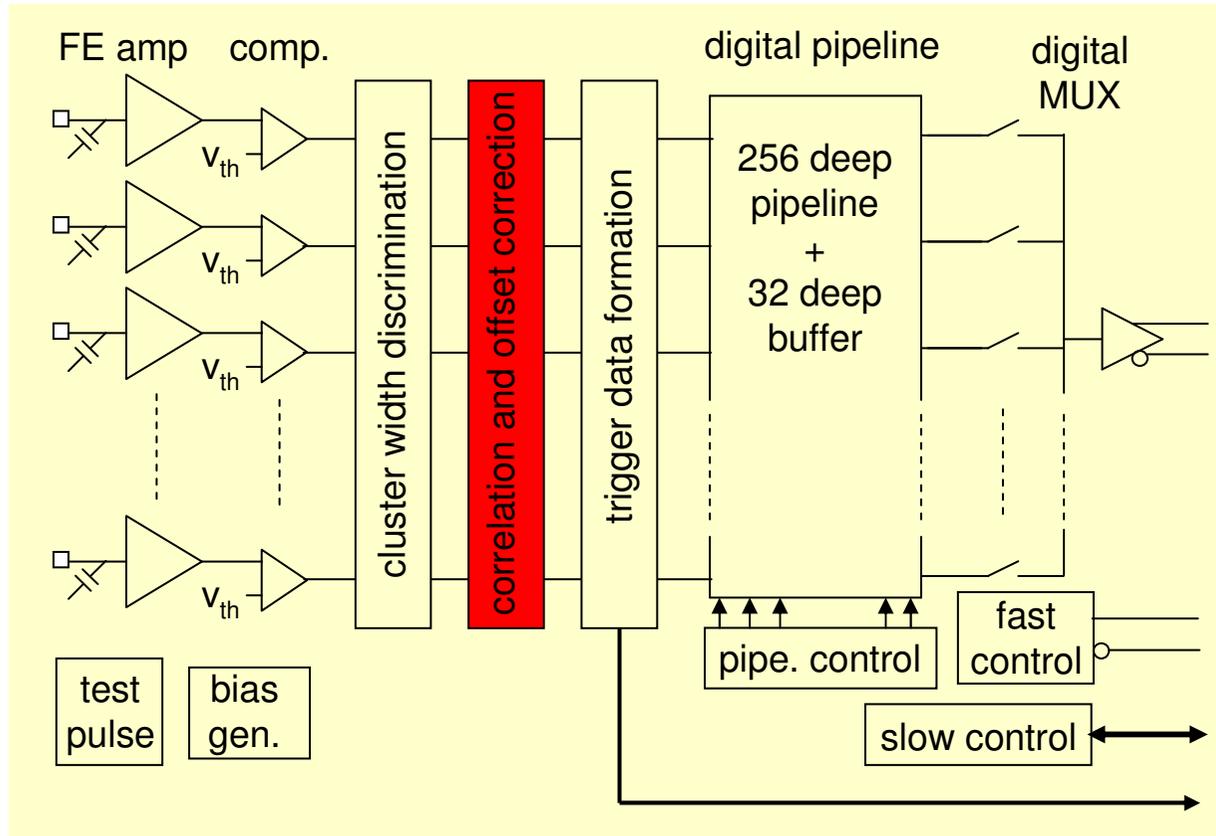


CWD logic

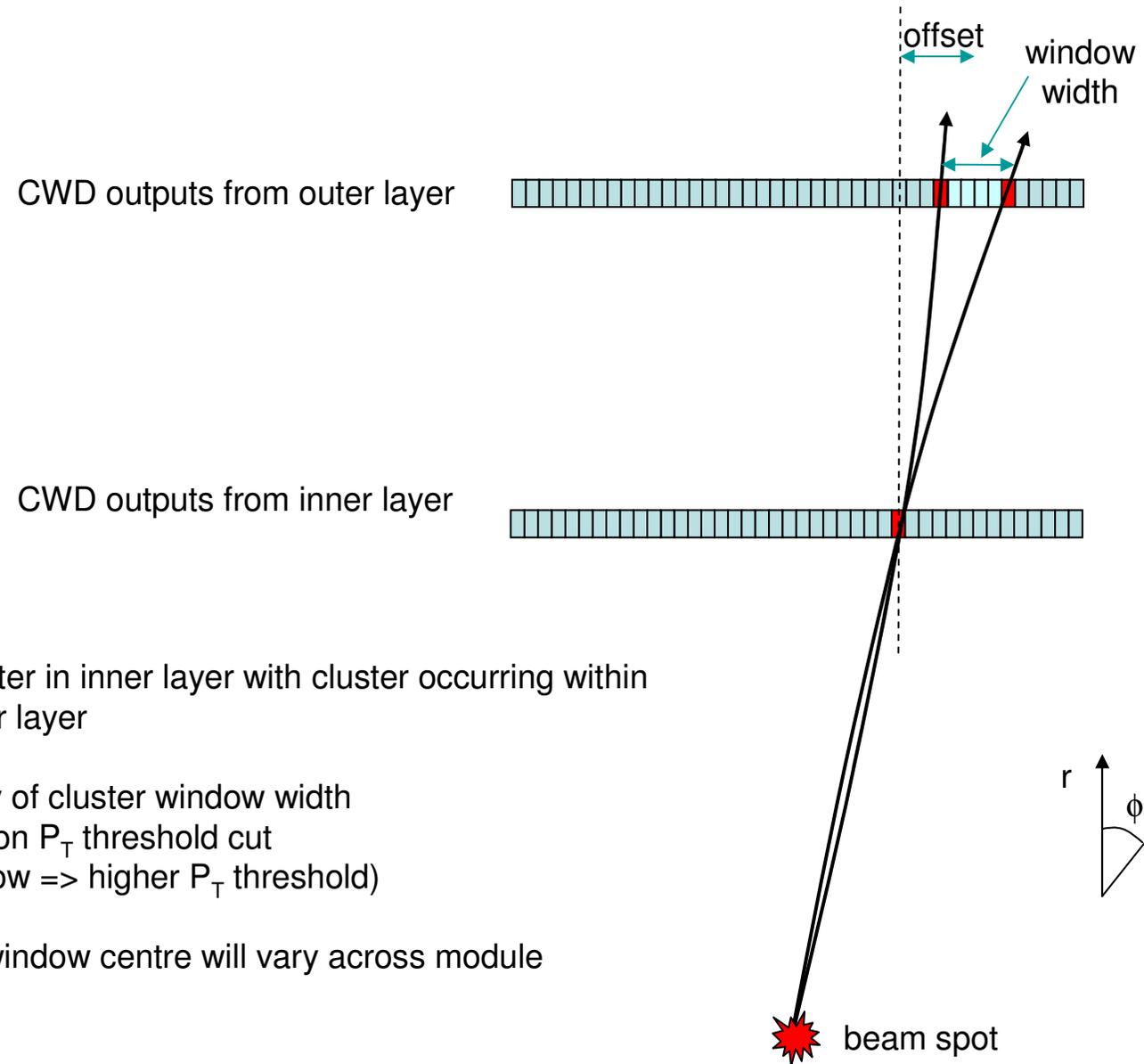


**$n-1$, n , $n+1$, ... are neighbouring channels on sensor layer (inner or outer)
but every other channel on chip
could increase to accept wider clusters if necessary**

offset correction and correlation



correlation

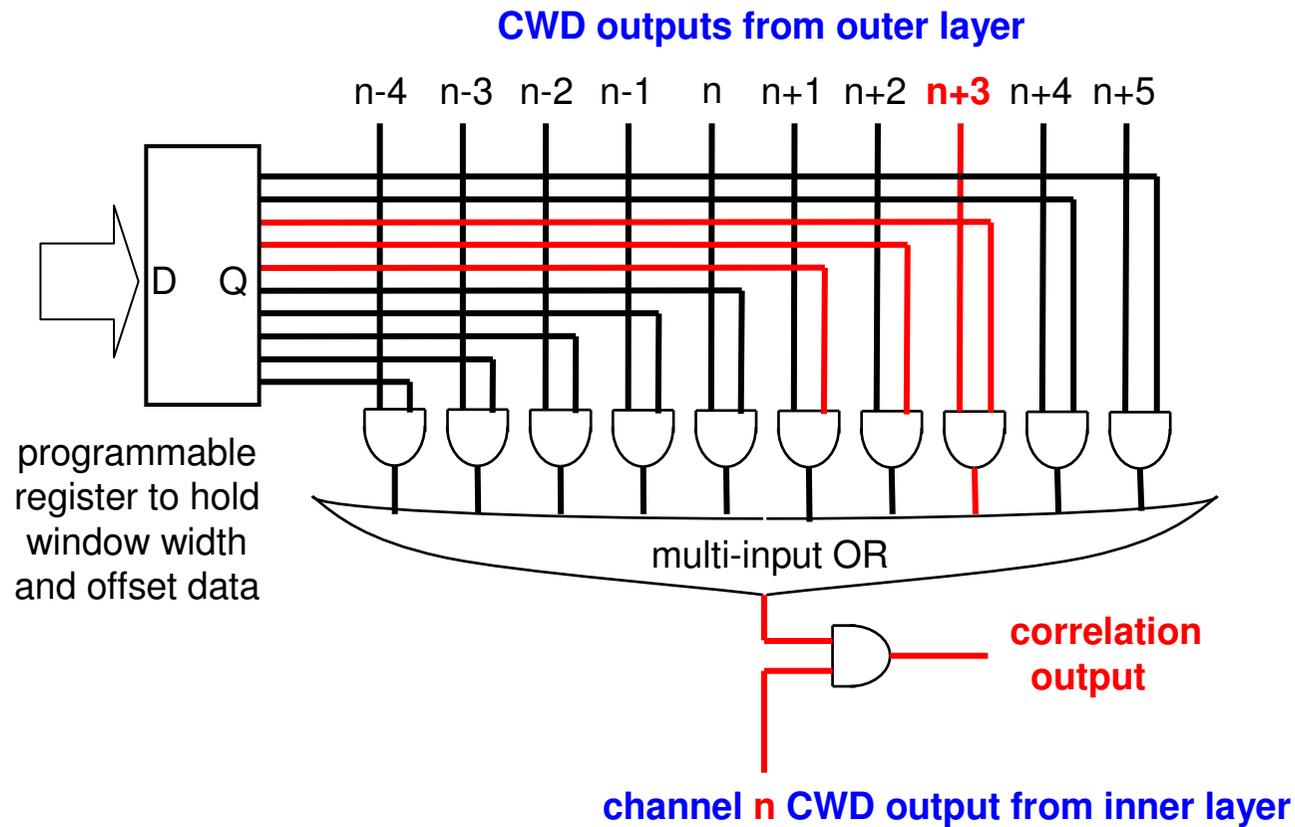


want to correlate cluster in inner layer with cluster occurring within a window in the upper layer

need programmability of cluster window width
width depends on P_T threshold cut
(narrower window => higher P_T threshold)

also lateral offset of window centre will vary across module

offset correction and correlation circuit



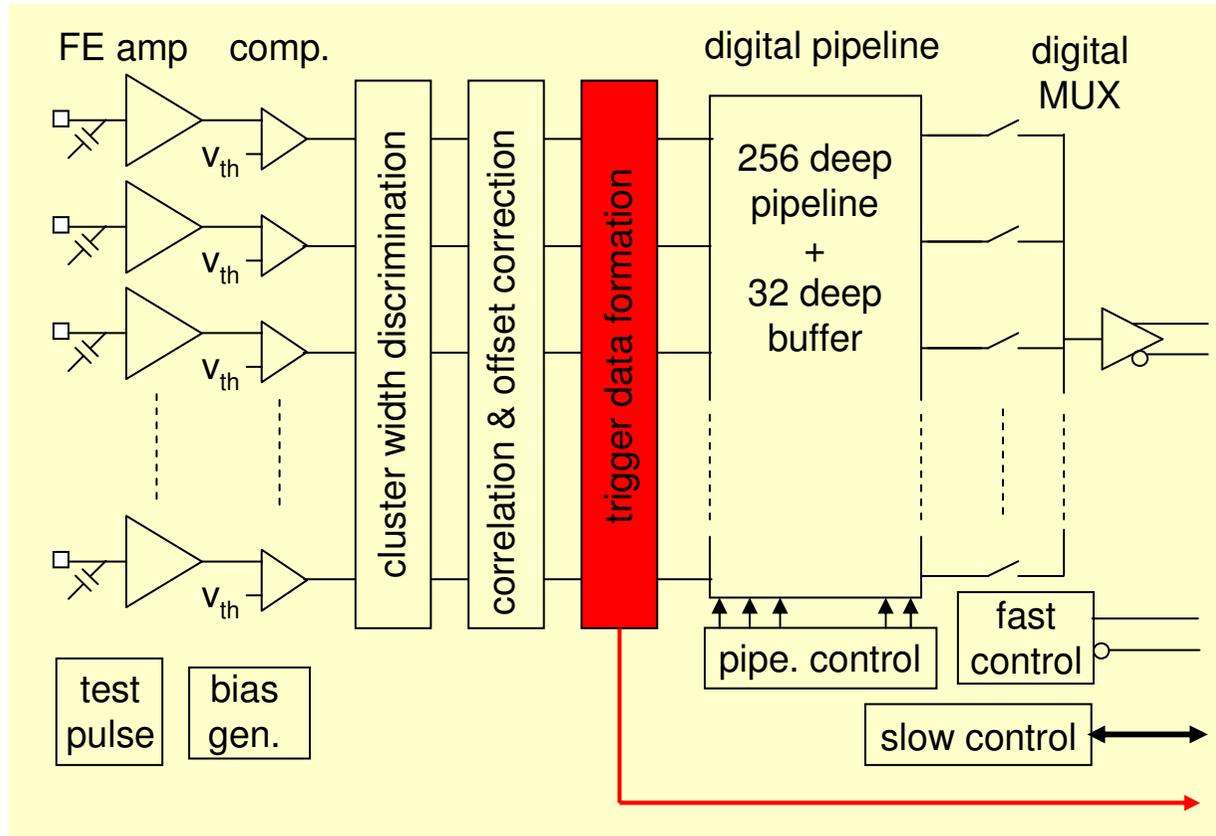
need one of these circuits on every channel

programmable register inputs to AND gates to allow for cluster window and offsets between layers
offset varies depending on location across sensor

in above example 2 channel offset applied to 3 channel window in outer layer

cluster on channel $n+3$ in outer layer correlates with cluster on channel n in inner layer

trigger data formation & transmission

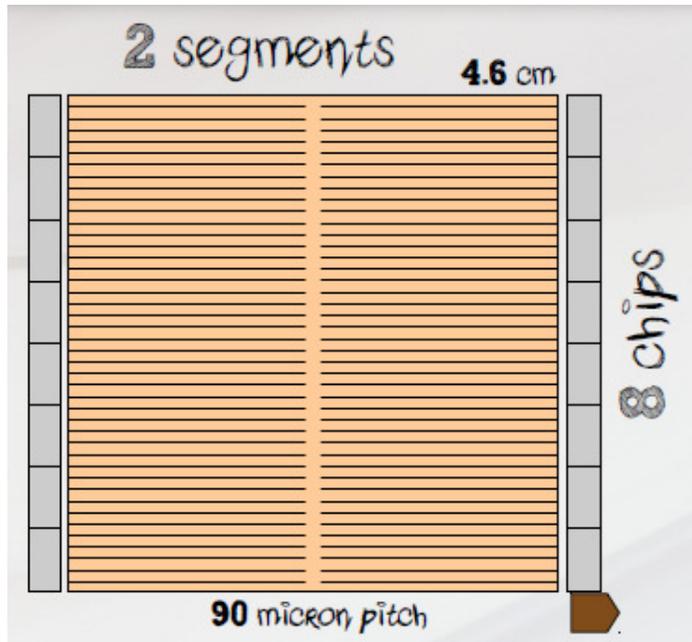


more than one way to do this

will describe an “electronically simple” solution

some numbers

outer tracker trigger module



assumption: 1 GBT / module

1 module has

$$\begin{aligned} &1024 \times 2 \text{ (layers)} \times 2 \text{ (halves)} = \mathbf{4096 \text{ strips}} \\ &8 \text{ (chips)} \times 256 \text{ (channels/chip)} \times 2 \text{ (halves)} \\ &= \mathbf{4096 \text{ electronics channels}} \end{aligned}$$

current GBT can provide 20 x 160 Mbps lanes
=> 3.2 Gbps

L1 triggered readout of unparsified data from CBCs
can combine 4 x 256 channel CBCs onto one 160 Mbps lane
=> 16 chips need 4 GBT (160 Mbps) lanes

can use remaining 16 x 160 Mbps lanes for trigger data
=> 2.56 Gbps
=> 64 bits per 25 nsec bunch crossing available
for trigger data

how to use the available bandwidth?

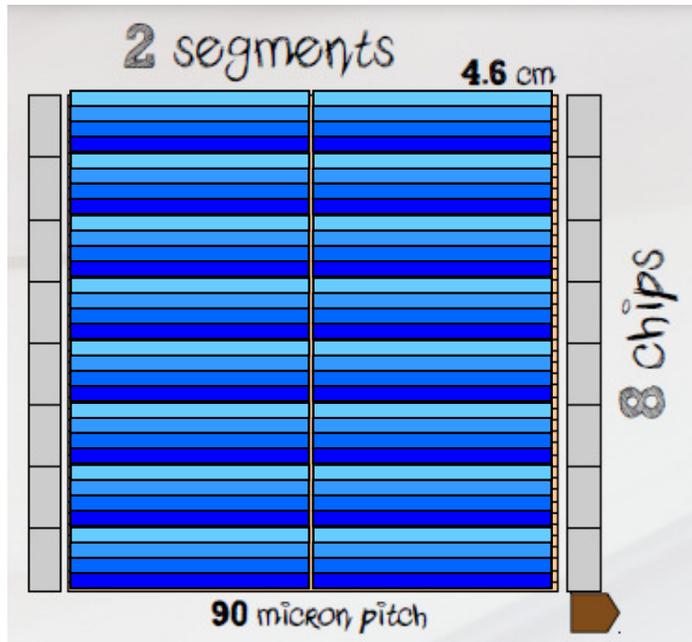
sharing 64 bits between 16 chips => 4 bits per chip (per BX)

a very simple idea

why not allocate each bit to report presence of a high PT stub in a specific area of the module?

module segmentation

outer tracker trigger module



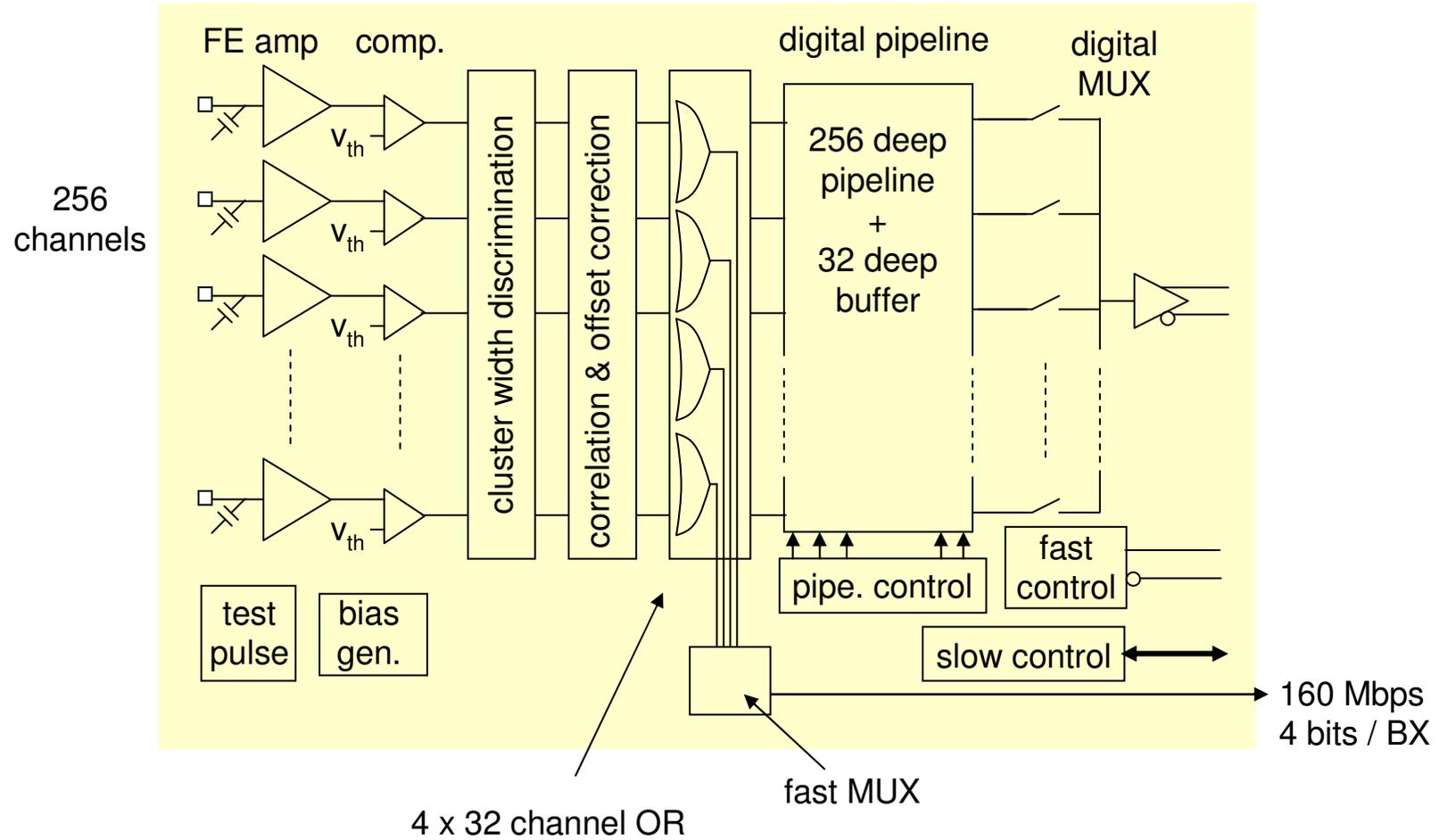
64 trigger contributing segments / module

so each chip produces a 160 Mbps trigger data stream (4 bit per BX) where an active bit indicates the presence of a high PT stub in an area corresponding to 32 stacked strips

=> trigger contributing segment area 3 mm x 46 mm

high PT stub occupancy of such an area small (in outer tracker)

CBC-t



summary

current CBC L1 triggered short strip chip can be adapted to provide 2-in-1 type trigger data for CMS outer tracker with relatively simple extensions

need

- cluster width discrimination
- offset and correlation
- trigger formation and transmission

have shown an implementation with straightforward combinatorial logic

some pros

- simple to implement (chip and system)
 - whole readout is unsparisified (trigger and triggered data)
- no occupancy dependent data volumes
 - => robust against sLHC accelerator operational changes

...

some cons

- inefficient use of GBT bandwidth => more associated power
- can 1 GBT / module be accommodated?

...

extra

cluster window width

$$\delta x = \delta r \times \frac{R[m] \times 0.6}{P_T[GeV]}$$

δx = displacement of hit in r/ϕ plane

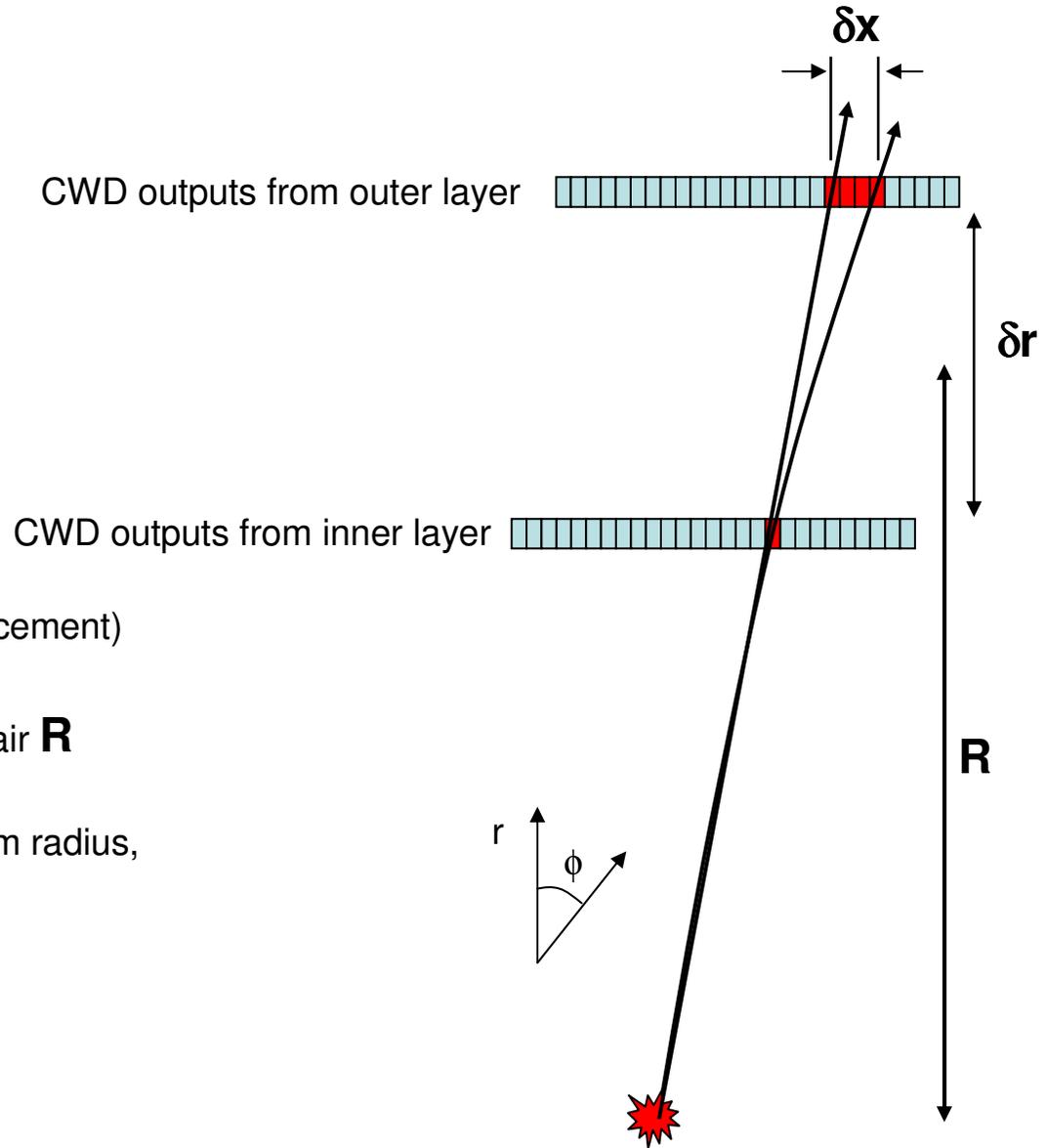
depends on

- P_T of track (infinite $P_T \Rightarrow$ no displacement)
- separation between layers δr
- average radius of triggering layer pair R

e.g. for 2 GeV track, triggering layer at 1 m radius,
2 mm separation between layers

$$\delta x = 600 \mu m$$

~ 7 strips at 90 μm pitch



offsets between layers

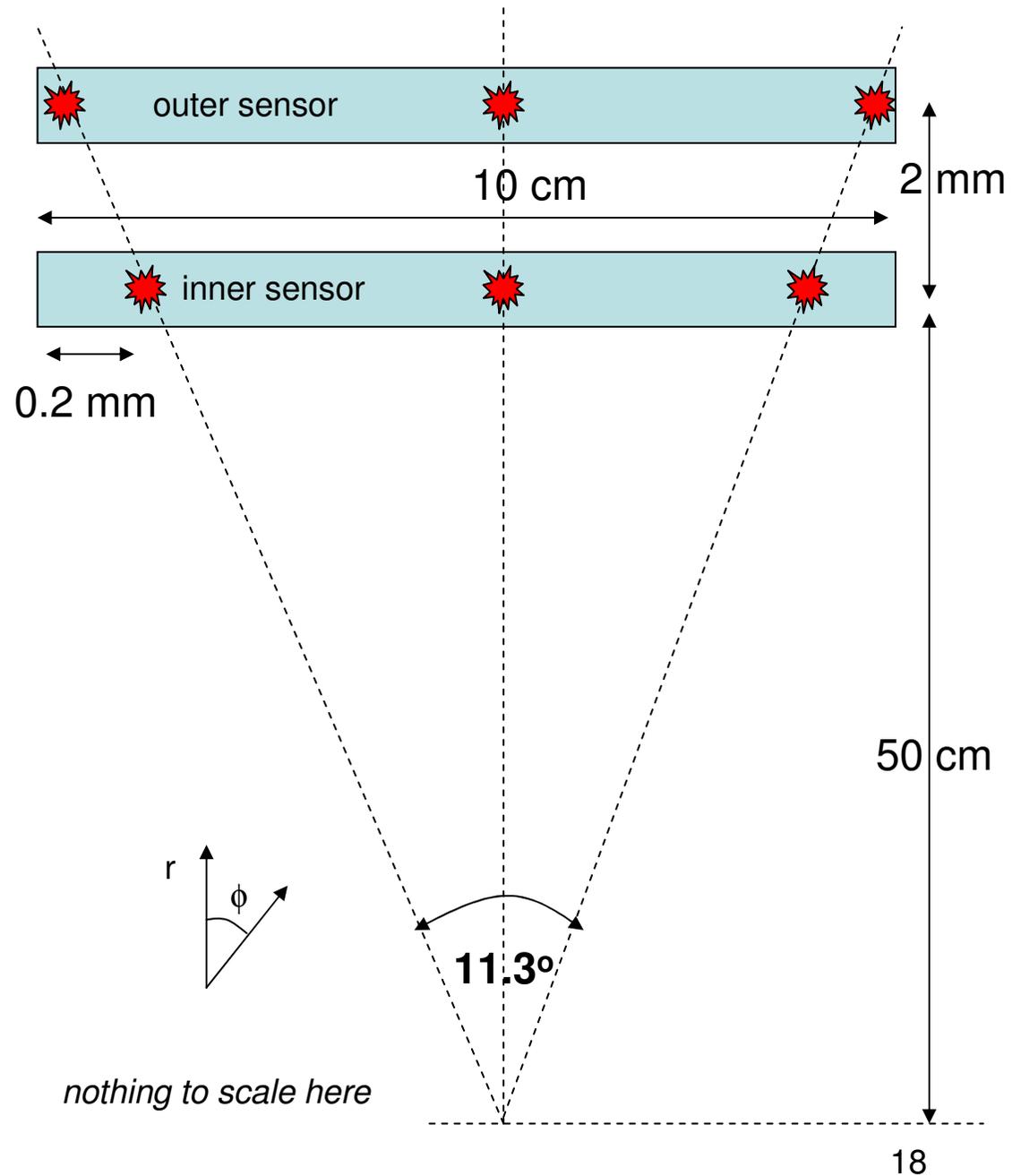
r/phi offset between clusters in closely spaced layers

worst case in innermost PT module

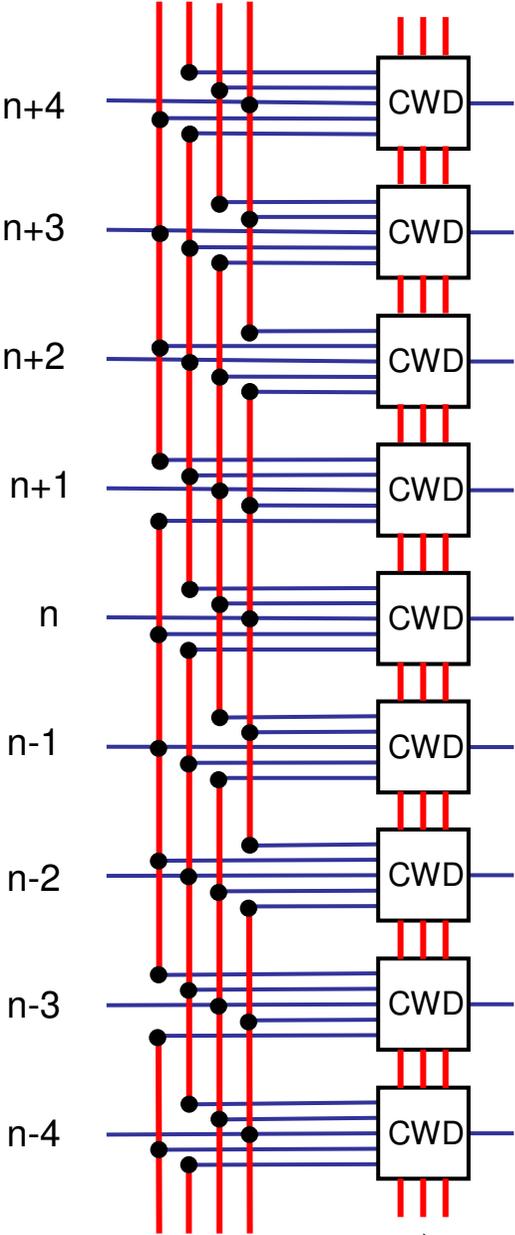
=> at 50 cm offset is 200 um for 2mm sensor separation

=> ~ 3 strips at 90 um pitch

need some way to account for this in the chip, variable over sensor width in r/phi



CWD logic routing



program cluster width accepted

offset correction & correlation routing

from front end, after CWD →

in this example, each outer layer channel feeds 5 nearest neighbours, each side

no hard limit, can be increased to more neighbours

