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The CMS binary chip for microstrip tracker readout at the SLHC

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ABSTRACT: A 130 nm CMOS chip has been designed for silicon microstrip readout at the SLHC. The CBC has 128 channels, and utilises a binary un-sparsified architecture for chip and system simplicity. It is designed to read out signals of either polarity from short strips (capacitances up to $\sim$ 10 pF) and can sink or source sensor leakage currents up to 1 μA. Details of the design and measured performance are presented.

KEYWORDS: VLSI circuits; Front-end electronics for detector readout

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1 Introduction

The high luminosity upgrade of the LHC, Super LHC (SLHC), is currently scheduled early in the next decade. Increased luminosity leads to a requirement for increased tracker granularity (channel density) in the experiments. The current CMS tracking detectors must be replaced and power delivery and consumption are major concerns. It is also necessary for the tracker to contribute information to the level 1 trigger system, to maintain the current average trigger rate of 100 kHz.

The current 0.25 μm CMOS analogue, un-sparsified readout [1] adopted for the LHC CMS tracker readout cannot be translated to SLHC. Off-detector links will be digital, and front end digitization of pulse height information would require sparsification to keep data volumes manageable, with increases in system complexity and associated power. We are therefore proposing to implement a binary un-sparsified architecture for the level 1 triggered readout of short strips in the CMS outer tracker, retaining chip and system simplicity at the expense of pulse height information.

The CMS Binary Chip (CBC), fabricated in 130 nm CMOS, is a prototype readout chip for short microstrips at SLHC. It has been implemented as a 128 channel chip to allow the performance to be studied in a full-size prototype containing most of the features required in a final system. The front end has been designed to be compatible with both sensor polarities, and can be DC coupled with the ability to sink or source leakage currents up to 1 μA. The CBC was fabricated in the second half of 2010, and chips have been under test since February 2011.

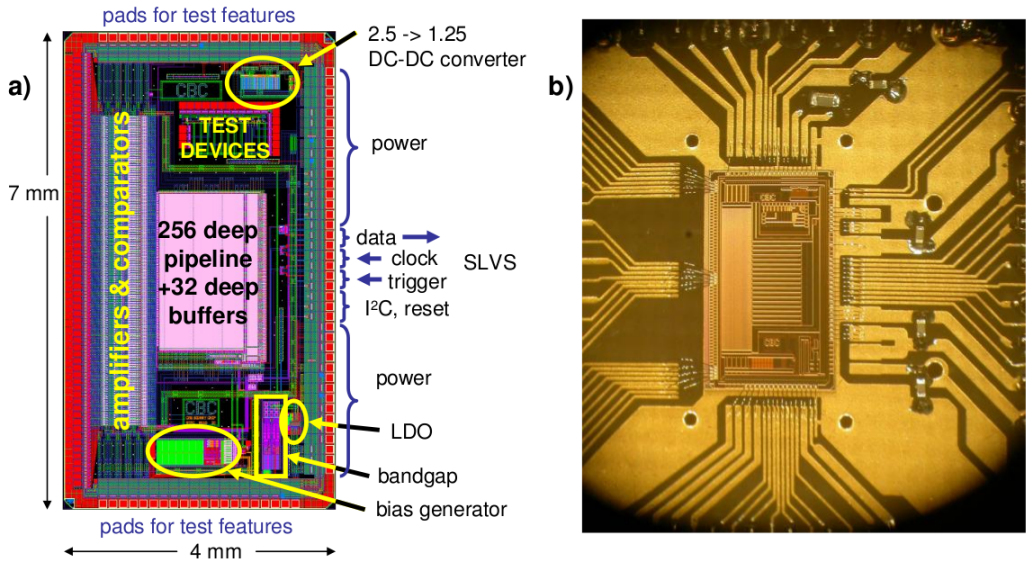

Figure 1. a) CBC layout with interfaces labeled. b) CBC chip mounted on test board.

2 Design and measured performance

Figure 1a shows the layout of the CBC, and 1b shows a chip glued and bonded on a test board. The 128 input pads on the left hand side are arranged as two staggered rows with an effective pitch of 50 microns. All other peripheral pads are on 150 μm pitch. The inputs feed the front end amplifier and comparator stages and the comparator outputs are sampled into a pipeline memory at 40 MHz. The depth of the pipeline is programmable up to 256 allowing a level 1 trigger latency of up to 6.4 μs. If a trigger occurs, the data from the triggered time-slice (the 128 bits of data that were stored in the pipeline a latency period before) are retrieved and stored in a readout buffer which can accommodate up to 32 triggered data sets awaiting readout. If the buffer was previously empty then the serial data output begins promptly at 40 Mbps.

Critical digital blocks have been designed for SEU resistance. The fast interface signals (output data, 40 MHz clock and trigger inputs) are implemented using the Scalable Low Voltage Signaling (SLVS) standard [2]. An on-chip bias generator provides currents and voltages required by the analogue stages, programmed via an I^2C slow control interface, which is also used to set up all other programmable features of the chip.

Power provision is a major concern for the central trackers at SLHC with existing cable cross sections imposing limits on deliverable currents. CMS has adopted a DC-DC powering solution as the baseline for SLHC, where higher voltages are locally translated to lower voltage levels required by on-detector electronics. The CBC incorporates features to allow possible powering implementations to be studied. A switched capacitor DC-DC circuit can convert a 2.5 V supply to the lower voltage needed by the core circuitry. A low dropout linear regulator is included which can be used to provide a clean power rail to the analogue front end.

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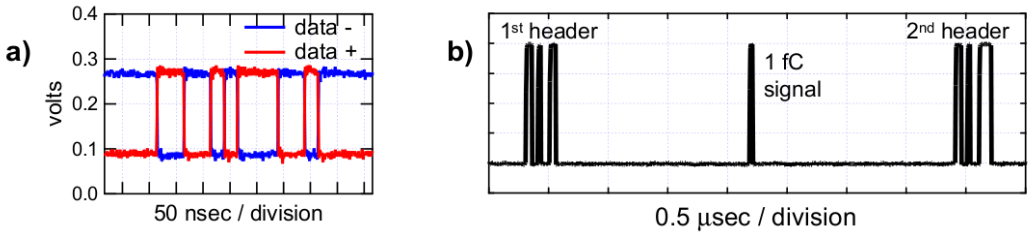

Figure 2. a) SLVS interface signals. b) CBC output data frame following two consecutive triggers.

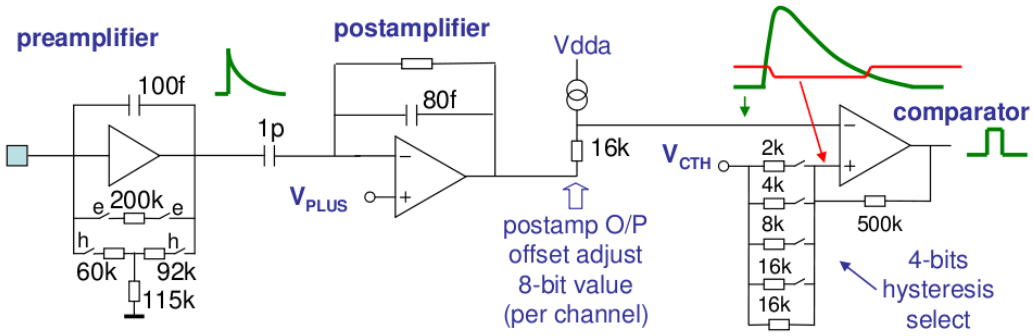

Figure 3. Front end circuitry.

2.1 Interfaces functionality

Figure 2a shows a scope measurement of the differential SLVS interface signals showing the voltage levels which are easily accommodated within the nominal 1.2 V power supply range of the 130 nm CMOS core transistors. The data in figure 2 are a sample of the chip output. SLVS signaling is also used for the 40 MHz clock and level 1 trigger inputs to the chip.

Figure 2b shows the CBC output data stream after triggering twice, where the first trigger follows the injection of a 1 fC signal into one of the inputs. The output data frame consists of a 12-bit digital header followed by the 128 bits of triggered data. The header comprises 2 start bits, 2 error bits (if on-chip circuitry has detected a malfunction of the digital circuitry) followed by the 8-bit address of the triggered pipeline time-slice.

2.2 Front end circuitry

Figure 3 shows a simplified schematic of the front end circuit of the CBC, consisting of preamplifier (preamp), postamplifier (postamp) and comparator stages.

2.2.1 Preamplifier

The preamp is designed to allow DC coupling to a sensor of either polarity, where leakage current is absorbed by the resistive feedback. For n-in-p type sensors (electrons flowing into the preamp) a switch network selects *electrons mode* where only the single 200kΩ feedback resistor is used. In the absence of leakage current the preamp input and output voltages sit at a nominal level of ∼200 mV. For a leakage current of 1 μA the preamp output DC level rises by 200 mV, easily accommodated within the linear dynamic range of the preamp. In *holes mode* (p-in-n sensors,

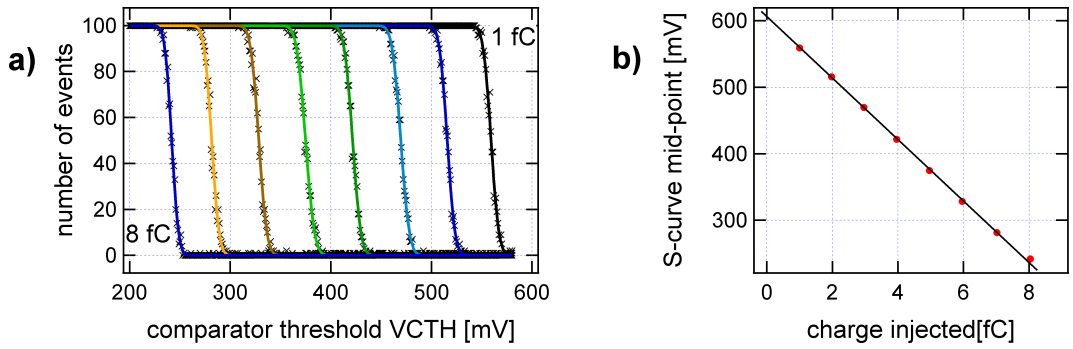

Figure 4. a) S-curves in electrons polarity mode. b) Resulting gain measurement.

holes flowing into the preamp) the output will move negative with increasing leakage and 1 μA will saturate the output, so the T-network of resistors must be selected. This produces a positive baseline shift at the output in the absence of leakage, so any negative shift produced by the leakage current can be accommodated.

The product of the preamp feedback capacitor and resistor results in a 20 ns decay time constant of the preamp output signal, which is beneficial for avoiding pile-up effects (note that in *holes mode* the choice of T-network resistor values produces an identical decay time constant).

2.2.2 Postamplifier

The preamp output is AC coupled to the postamp input, removing any DC component due to leakage current. The postamp, implemented by an operational amplifier, provides the necessary gain to interface to the comparator stage. The quiescent output voltage at the postamplifier is set by V_{PLUS}, a bias voltage common to all channels on the chip. The combination of high frequency bandwidth limiting in the preamp and postamp stages results in a postamp output pulse shape with a peaking time of approximately 20 ns.

2.2.3 Comparator

The postamp output feeds the comparator via a resistor. Each channel includes an 8-bit programmable (via I^2C) current source which flows in the resistor to produce a DC offset at the comparator input, which allows to correct for any channel-to-channel variations in comparator threshold across the chip. A global programmable threshold V_{CTH} is fed to all comparators. The comparators include a resistive hysteresis network, the level of which is also programmable.

2.3 Front end performance

2.3.1 S-curves and gain

In a binary system the analogue performance can be determined by varying the comparator threshold and the size of the signal injected, to generate a set of S-curves from which the front end gain and noise can be extracted. An S-curve is obtained by injecting a signal and sweeping the comparator threshold from a region where the comparator fires all the time, to where it does not fire at all. The resulting data are fitted with a complementary error function.

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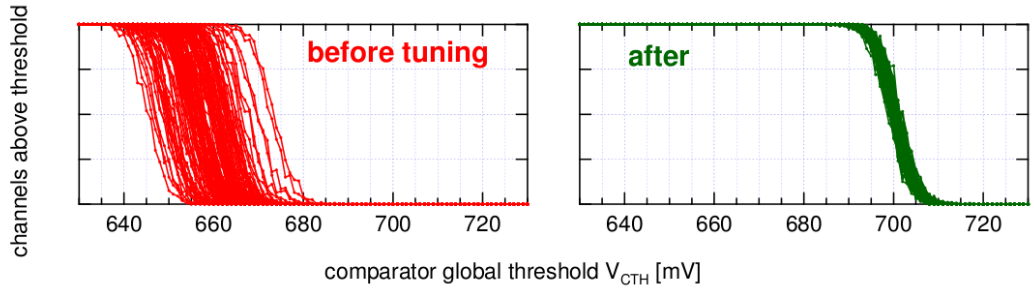

Figure 5. Comparator threshold uniformity before and after tuning.

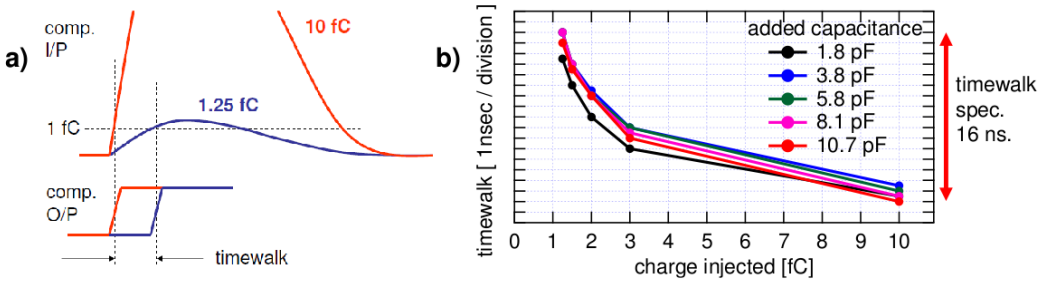

Figure 6. a) Comparator time-walk definition. b) Time-walk measurement.

Figure 4a shows a set of S-curves measured in electrons polarity mode, for signals in 1 fC steps between 1 and 8 fC. The measured response is similar for the holes polarity mode. The S-curve mid-points can be taken to represent the gain, shown in figure 4b. The gain is approximately 50 mV / fC, close to that expected from simulation. The response is quite linear to 8 fC, but for a binary system linearity is only important in the region where the normal operational comparator threshold will be set, in the region around 1 fC.

2.3.2 Comparator performance

Figure 5 shows a set of S-curves measured for all 128 channels on a chip, illustrating channel-to-channel spread in comparator thresholds before and after the individual channel tuning process. Before tuning the peak-to-peak threshold spread is approximately 30 mV, corresponding to 0.6 fC. After tuning this is reduced to the ∼mV level.

To ensure that hits are associated with the correct bunch crossing (25 ns bunch spacing), we require that the comparator time-walk be less than 16 ns for signals in the range 1.25 to 10 fC, for a threshold setting of 1 fC (figure 6a, specification analogous to that defined for the Atlas ABCD3Tchip [3]). The measurements in figure 6b show that the chip is performing just within specification. Figure 6b shows no significant degradation in time-walk for a range of preamp input capacitance values, which is achieved by varying the current in the input transistor to compensate for the effect of the preamp output rise-time (which would otherwise increase with input capacitance) on the overall pulse shape.

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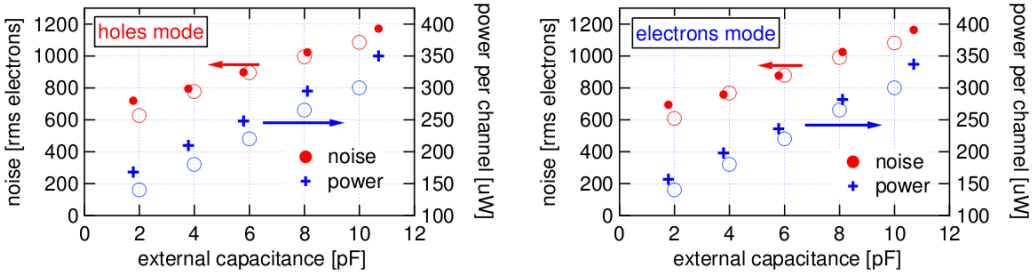

Figure 7. Noise and analogue power in holes and electrons mode. Solid symbols are measurements, open circles are simulations.

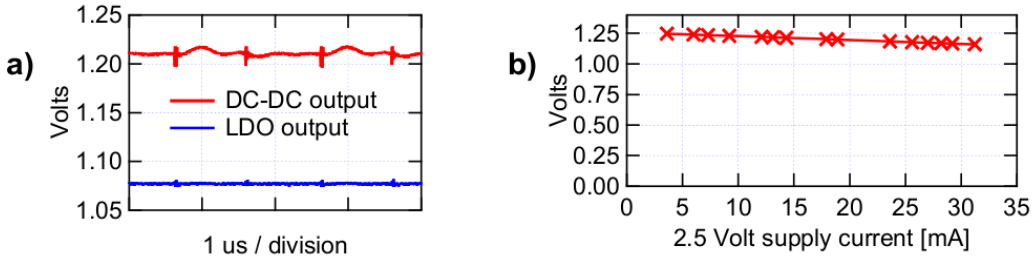

Figure 8. a) DC-DC and LDO outputs. b) DC-DC output dependence on load.

2.4 Noise and power

Figure 7 shows a measurement of the noise dependence on external capacitance added at the preamp input. There is no significant difference between holes and electrons modes of operation. The noise is determined from S-curve measurements. The preamplifier output rise-time increase with input capacitance is compensated for by increasing the current in the input device, so for this reason the analogue power can be seen to increase with capacitance in figure 7. Both noise and analogue power measurements are close to simulation expectations. The noise performance can be approximately described by noise [rms electrons] = 500 + 64/pF.

The overall power consumption of the chip has to include the digital power consumption which has been measured to be less than 50 μW/channel. Adding this to the analogue power, the total power can be approximately described by power/channel [μW] = 180 + 21/pF. So, for example, for a mid-range sensor strip capacitance of 5 pF a noise performance of approximately 820 electrons is achievable for a power consumption less than 300 μW/channel.

2.5 Powering circuitry

The switched capacitor DC-DC converter can be used to power the core transistors (1.2 Vs nominal) from a 2.5 V supply using higher voltage rated transistors (available on-chip) to implement the switches. The LDO regulator can be used to provide a clean 1.1 V supply rail to the front end analogue circuitry from a 1.2 V supply that could be noisy. To operate correctly an LDO circuit needs a voltage reference which is provided by a band-gap circuit.

Figure 8a shows the DC-DC circuit operating in conjunction with the LDO. The DC-DC circuit is provided with an external clock at the design frequency of 1 MHz. Figure 8b shows the variation

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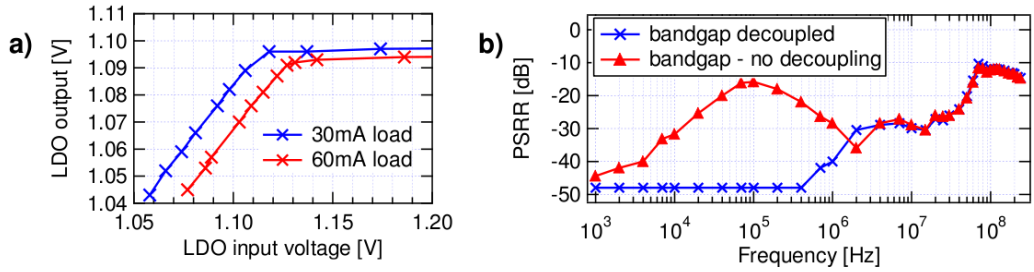

Figure 9. LDO performance measurements. a) Output voltage dependence on input. b) Power supply rejection, PSRR = 20log(Vout/Vin).

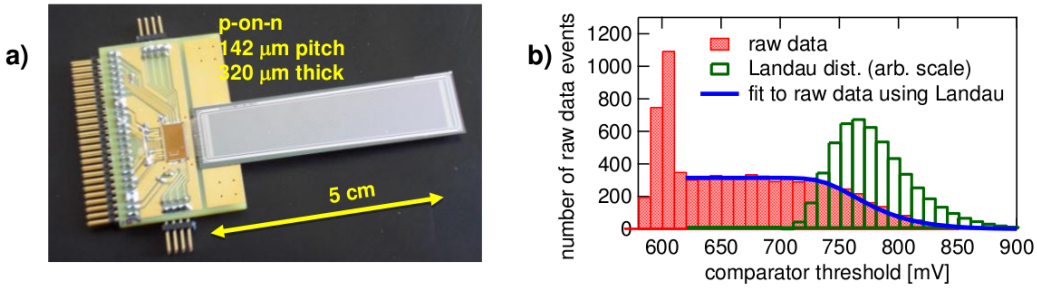

Figure 10. a) CBC + sensor module. b) Sr-90 beta source spectrum.

of the DC-DC output voltage with supply current as the load is varied. At a typical CBC supply current of ∼30 mA the efficiency of the DC-DC converter (power out / power in) has been measured to be 90%.

Figure 9a illustrates the LDO dropout performance where, for example, at 60 mA (approximately twice the 128 channel CBC load current) the dropout is ∼40 mV. Figure 9b shows the power supply rejection (PSRR) achieved with the LDO, measured by superimposing a swept frequency sinusoidal ripple on the input voltage. It is noticeable that the PSRR is degraded unless the band-gap reference is externally decoupled, because the band-gap circuit is fed by the LDO input voltage. It is proposed to provide on-chip filtering of the band-gap output in the next version of the chip. With the band-gap decoupled very good rejection is apparent at low frequencies, and approximately 30 dB is achieved up to 10 MHz.

3 Results with sensors

The CBC front end is designed to match sensor capacitances up to ∼10 pF, (strip lengths up to ∼7 cm), which is compatible with current plans for modules in the CMS outer tracker region where 5 cm strips are currently being considered. Figure 10a shows a single chip module with a single CBC used to read out a 5 cm p-on-n strip sensor (320 μm thick, 142 μm pitch). This module has been used to detect signals from a Sr-90 beta source, with scintillator triggered readout. The scintillator trigger is time-stamped with 1 ns precision to allow selection of events which are correctly timed with respect to the phase of the 40 MHz CBC clock.

Figure 10b shows a histogram of data acquired by counting hits in the CBC for a fixed number of scintillator triggers, sweeping the value of the global comparator threshold. The shape of the raw

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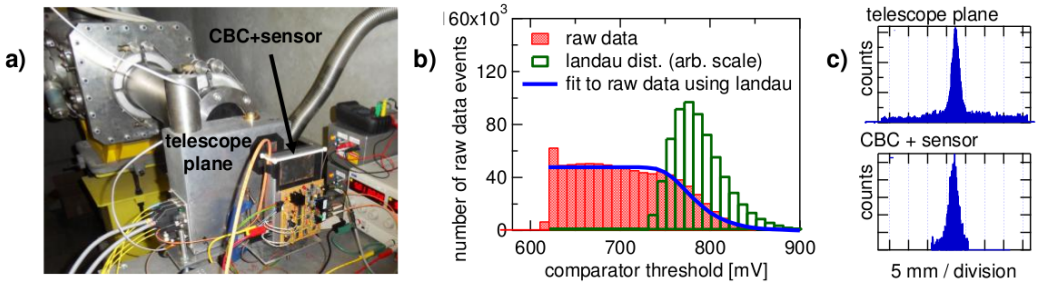

Figure 11. a) Beam test setup. b) Beam spectrum. c) Beam profile.

data is well fitted by a curve derived from a Landau distribution, and comparing the most probable value from the Landau with an electronic calibration the equivalent charge signal is 3.7 fC.

The CBC+sensor module of figure 10a has also been recently operated in a 400 GeV proton beam in the CERN H8 beam line. The arrangement is shown in Figure 11a, where the CBC module is positioned furthest downstream of a telescope [4]. Analysis is at a very early stage, but figure 11b shows a spectrum obtained in a similar way to that of figure 10b, with very similar characteristics, and figure 11c shows a beam profile measured in both CBC module and adjacent telescope plane. These early results show encouraging performance.

4 Conclusions, further work, and future developments

The prototype CBC is a 128 channel 130 nm CMOS chip designed for short strip readout at SLHC. The measured performance demonstrates that it works for both sensor polarities, sinking or sourcing leakage currents up to 1 μA. For a midrange sensor capacitance of 5pF a noise performance of $\sim$ 800 electrons is achieved for a power consumption of 300 μW/channel. Electronic measurements of chip performance have been confirmed in CBC+sensor module measurements, in the lab with a beta source and in a test beam.

Further measurements are planned, including more detailed studies of the powering options and temperature effects on performance. Radiation testing is required to confirm ionizing radiation hardness, and to study single event effects.

The next version of the chip is currently foreseen to have 256 channels and to be bump-bondable, so that routing of sensor signals to inputs and/or pitch adaptation can be implemented in an advanced hybrid technology. The CMS tracker is required to provide information to the level 1 trigger at SLHC, and the "2-in-1" approach [5] is currently considered to be the most promising technique to implement this in outer tracker modules. The logic circuitry required for this functionality will be included in the next version.

Acknowledgments

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References

[1] M. Raymond et al., *The CMS Tracker APV25 0.25 µm CMOS readout chip*, in the proceedings of the 6th *LEB Workshop*, September 11–15, Cracow, Poland (2000), CERN-LHCC-2000-041, see page 130.

[2] S. Bonacini et al., *E-link: a radiation-hard low-power electrical link for chip-to-chip communication*, in the proceedings of the *Topical Workshop on Electronics for Particle Physics (TWEPP2009)*, September 21–25, Paris, France (2009), CERN-2009-006, see page 422.

[3] W.Dabrowski et al., *Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS semiconductor tracker*, *IEEE Trans. Nucl. Sci.* **47** (2000) 1843.

[4] M. Pesaresi et al., *Design and performance of a high rate, high angular resolution beam telescope used for crystal channelling studies*, 2011 *JINST* **6** P04006.

[5] M. Raymond and G. Hall, *CMS tracker readout at the SLHC*, in the proceedings of the *Topical Workshop on Electronics for Particle Physics (TWEPP2008)*, September 15–19, Naxos, Greece (2008), CERN-2008-008, see page 354.

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