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Studies of the CBC3.1 readout ASIC for CMS 2S-modules

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ABSTRACT

The CBC3.1 is the final version of the CMS Binary Chip for readout of the outer radial region of the upgraded CMS Tracker at the High-Luminosity LHC. The CBC development was completed with an engineering run in 2018 and two pre-production lots delivered in 2019. Large scale manufacture began in May 2021. Issues were raised when some wafers were tested at low temperature (−30 °C) and probing was suspended for investigation. After studies, some additional tests were added to reject affected chips and we show that the impact of the low temperature issues is expected to be very small.

1. Introduction

The CBC3.1 [1] is a 254-channel, 130 nm CMOS ASIC designed to be bump-bonded to a hybrid substrate to which silicon microstrip sensors will be wire-bonded. The CBC provides front-end readout of "2S-modules" [2] which identify "stubs", or short track vectors made of hits in two closely spaced silicon sensor layers. The CBC transmits two kinds of data off-chip: hit data on receipt of a Level-1 trigger, and stub data at the 40 MHz beam crossing rate to contribute to the trigger decision. The performance has been proven in modules produced with CBCs from wafers in the engineering run in beams [3] and with TID [4] and SEU [5] tests. Deliveries are in "lots" of up to 25 wafers. We number lots incrementally, with the engineering run being lot 1. After two pre-production lots (2 & 3) were delivered in 2019, large scale manufacture began in May 2021. An automatic wafer probing system was developed for CBC quality control and adapted to allow measurements down to temperatures below −30 °C, believed to be the first time wafer scale tests at such temperatures have been attempted for HEP applications. Some unexpected issues were found and investigated, with the conclusion that the effects are most likely related to fabrication.

2. Wafer probing system and low temperature tests

The wafer probing system was developed to identify fully functional chips. It is based on a rigid mechanical station holding an electrical probe card at a fixed position and a movable vacuum chuck holding a wafer below the probes. A chip under test makes contact with the needles by raising the chuck, which is lowered and moved transversely to scan all the 478 CBC sites on the wafer. A PC controls the chuck position, operates the chips and stores data. The characteristics and functions tested are currents, I2C registers, 320 MHz serial data lines, pipeline and buffer memories, an LDO band-gap circuit and output voltage, offset tuning, S-curves, gain, DLL functionality, Fast Command Interface, stub logic, and channel masks.

The system was adapted for cold operation. It was challenging to achieve humidity control and good probe contact quality but tests were successfully undertaken for 32 wafers from the two pre-production lots and five production lots (4 to 8) at −30 °C to study yield issues and check performance at CMS operating temperatures. Generally the yield of good chips at −30 °C was found to be high but rare memory bit errors and occasional corruption of some I2C registers were observed in some lots, which became the subject of more detailed studies.

3. Study of issues at low temperature

Errors in hit data memory: The memories consist of a 512-deep pipeline and 32-deep intermediate storage buffer for binary hit data from the 254 channels. Memory errors have no effect on stub reconstruction and off-detector transmission, as those data are not stored in the memory. A check was done for 26 wafers from lot 3 to 8, counting the percentage of chips which exhibited more than a certain fraction (1%, 0.1%, 0.01%) of bit errors. Lots 3 and 5 behaved very differently from other lots, showing more frequent errors at the 0.01% level. Other lots show virtually no errors. Both poorly behaving lots have a lower overall yield of good chips, as shown in Fig. 1, and chips with this error are often distributed in circular patterns on wafers. It was also found that most chips with a memory error at low temperature also show corruption at room temperature of redundant debugging data sent with the hit data, and this check was added to the set of tests. Even without the additional test and in the worst case where all chips installed in CMS exhibit the bit errors at 0.01%, this would give rise to an excess occupancy (or a deficit) of 0.01%. Given that the expected occupancy

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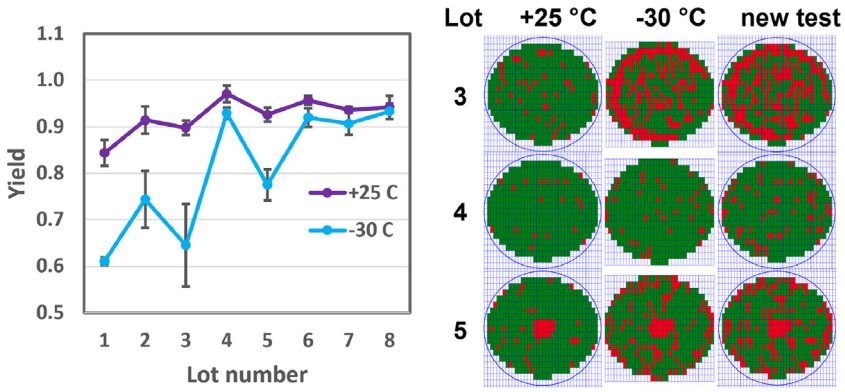

Fig. 1. Left : Yield from the original set of tests at room temperature and at −30 °C; Right : Yield patterns (red: bad chip, green: good chip) at +25 °C and −30 °C with the original set of tests, and the new set of tests at room temperature. One wafer is selected from each lot for lot 3, 4, and 5. The yield of the three wafers are (+25 °C, −30 °C, new test) = (92%, 61%, 57%), (99%, 92%, 87%), and (91%, 73%, 70%), for lot 3, 4, and 5 wafers, respectively. The new set of tests at room temperature finds most chips which failed the tests at −30 °C.

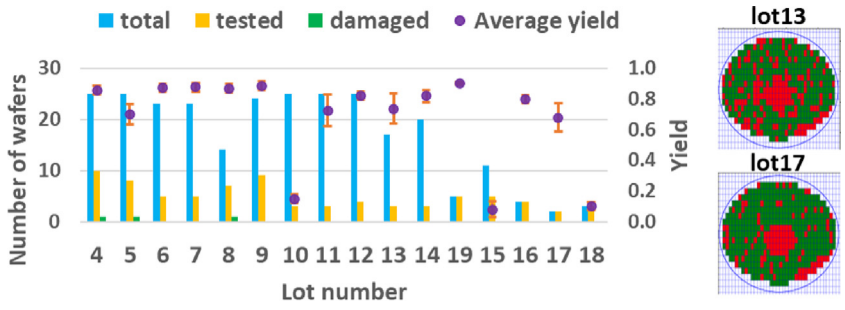

Fig. 2. Results for production lots using the new set of tests. Left: Total, tested, and damaged number of wafers, and the average and standard deviation of the yield per lot. The lot is in the order of production time; lot 19 was produced between lot 14 and lot 15. Right: Yield patterns (red: bad chip, green: good chip) of selected wafers from lot 13 and lot 17, whose yields are 64% and 74%, respectively.

in the region of the tracker where the CBCs will be used is 1–2%, this is not a serious problem, e.g. for track reconstruction.

I2C register errors: I2C registers are in two pages of 8-bit address space with a special register at address 0 (R0) which does not belong to either page 1 or 2. An address decoder which has an 8-bit address and a page bit as input is located next to each register. One bit of the R0 register is wired to the page bits of all the address decoders to control them. Corruption is sometimes observed when a write operation is conducted when the page is 2 or changing the page bit. A simplified summary of the I2C register corruption is:

- Only page 2 registers, containing individual channel pedestal offset tuning values, are affected and the number of those registers depends on temperature and supply voltage; VDDD = 1.2 V is the design value.
- The number of corrupted registers in a faulty chip is small, most commonly only one, and much less often two or more.
- The corrupted registers are not the same on every chip, which might be expected if the origin is in the design; each register affected also has a different error rate.
- There is a strong correlation between I2C failures at low supply voltage and the low temperature results. Most chips with the error can be rejected by a test at VDDD = 1.1 V with tolerable impact on the yield (> 75% is the target).
- The chips with this error are randomly distributed on wafers. They are otherwise fully functional.

Each offset register is located close to the analogue channel input port and the registers spread over the long side of the chip with the page bit and write lines close to each other. The long paths and the line alignment are suspected to be sensitive to manufacture quality. If a stress test at low VDDD is added, the undetected channels with an error at low temperature on good chips are fewer than 5 per wafer. Each wafer has 478 dies, and each chip has 254 channels. The estimated impact on occupancy would be very small, $< 10^{-4}$, i.e. the same level as the hit data memory.

4. Additional observations and remarks

The memory and I2C register errors which occur at low temperature could both be identified using the additional tests at room temperature. As shown in Fig. 1, those issues have a strong lot to lot variation and many wafers which have large yield drops at low temperature have circular patterns which hint at a possible fabrication issue which has been observed for APV25 production in the past [6]. The new set of tests has been used for 79 production wafers in 16 lots as shown in Fig. 2. As is in the original tests at low temperature, the average yields for lots 4, 6, 7, and 8 are high, above 85%, while it is about 70% for lot 5. Further tests on sampled wafers from lot 9 to 19 also show lot variations but mostly with yields above 70%. Circular patterns are observed in some production lots with similar yield to lot 5, as shown in Fig. 2 (right).

5. Summary

During CBC3.1 wafer probing some operational faults were found to occur more frequently at low temperature. The fraction of defective

chips has a strong lot to lot variation and suggests non-optimal manufacture as the origin. The impact on CMS performance is expected to be negligible following optimisation of the selection tests.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

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References

[1] K. Uchida, et al., The CBC3 readout ASIC for CMS 2S-modules, Nucl. Instr. Meths. A 924 (2019) 175, http://dx.doi.org/10.1016/j.nima.2018.09.051.
[2] CMS Tracker Group, The Phase-2 Upgrade of the CMS Tracker, CERN-LHCC-2017-009.
[3] W. Adam, et al., Test beam demonstration of silicon microstrip modules with transverse momentum discrimination for the future CMS tracking detector, JINST 13 (2018) P03003, http://dx.doi.org/10.1088/1748-0221/13/03/P03003.
[4] S. Seif El Nasr-Storey, Recent developments in the CBC3, a CMS microstrip readout ASIC for track-trigger modules at the HL-LHC, Nucl. Instr. Meths. A 936 (2019) 278, http://dx.doi.org/10.1016/j.nima.2018.11.005.
[5] G. Hall, et al., Single event upset rates in the CBC in CMS, Nucl. Instr. Meths. A 978 (2020) 164416, http://dx.doi.org/10.1016/j.nima.2020.164416.
[6] R. Bainbridge, et al., Production testing and quality assurance of CMS silicon microstrip tracker readout chips, Nucl. Instr. Meths. A 543 (2005) 619–644, http://dx.doi.org/10.1016/j.nima.2004.11.050.