CBC3 Architecture & Plans

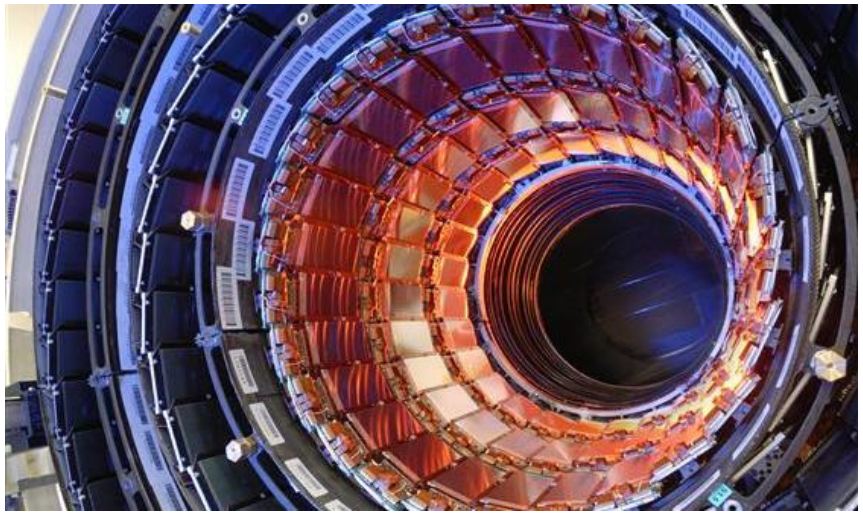
STFC RAL: Mark Prydderch, D. Braga, L. Jones, M. Key-Charrier

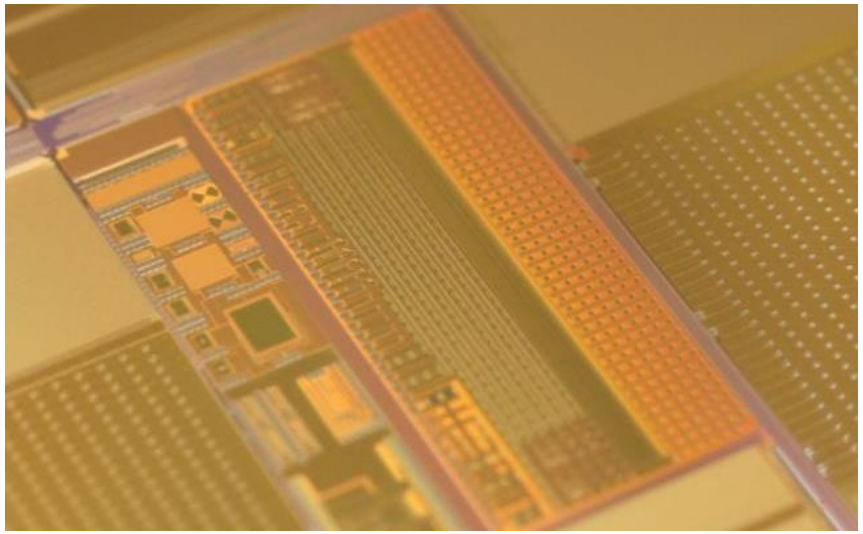
Imperial College: G. Hall, M. Raymond, M. Pesaresi

Imperial College London

Science & Technology Facilities Council

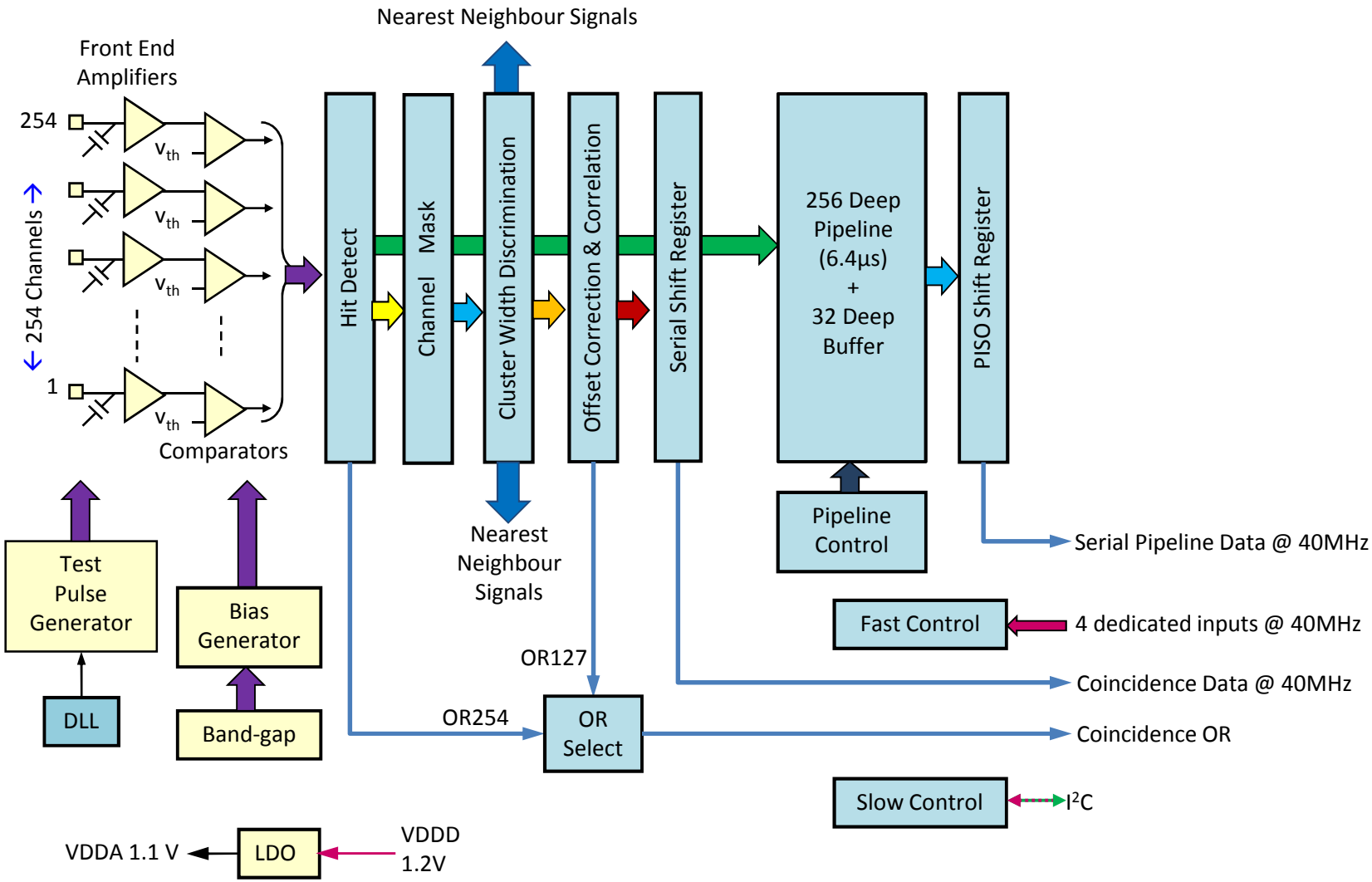
Outline



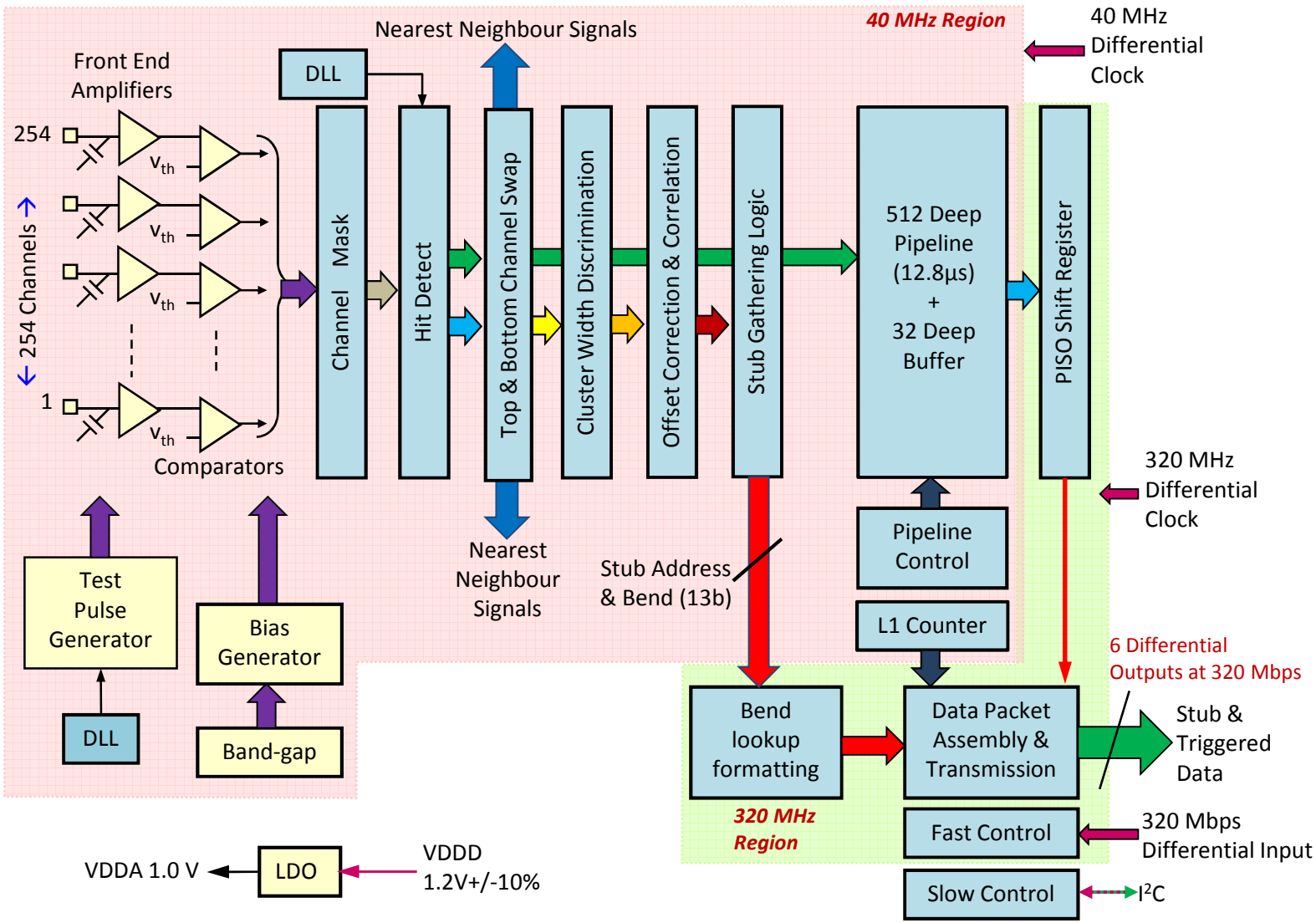


- **CBC2 Architecture: Reminder**
- **CBC3 Architecture: What's new**
- **Plans**

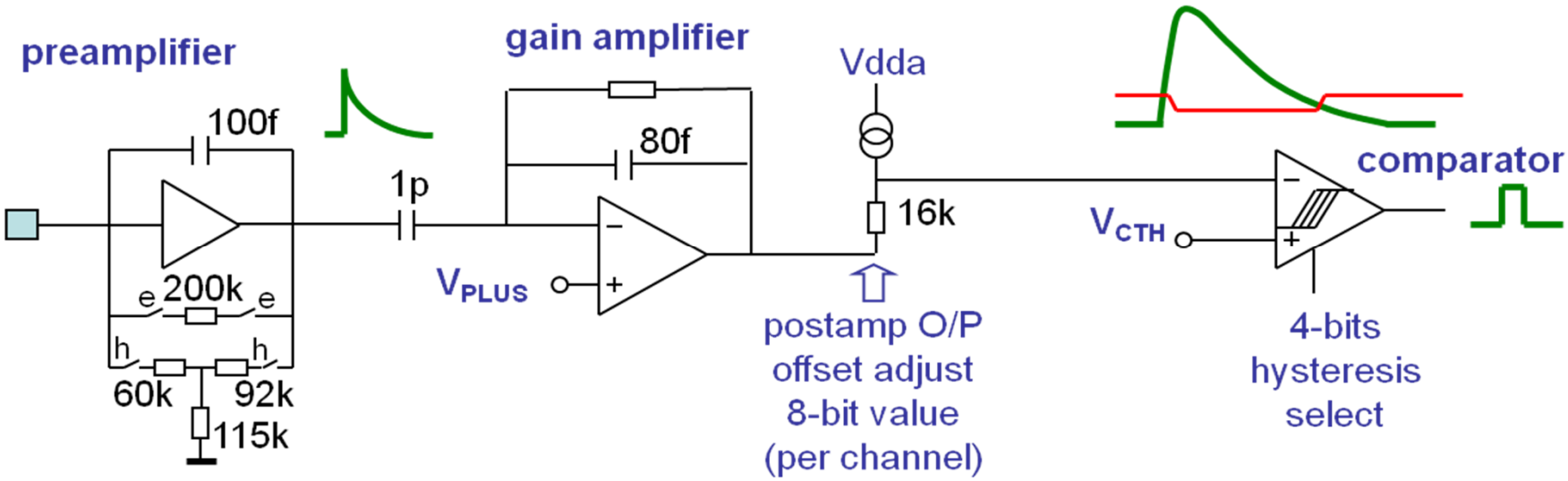
CBC2 Architecture



CBC3 Architecture



CBC3 Front End



Pre-Amplifier:

- Single polarity
- Return to baseline within 50 ns
- 1V operation
- Larger Detector Capacitance

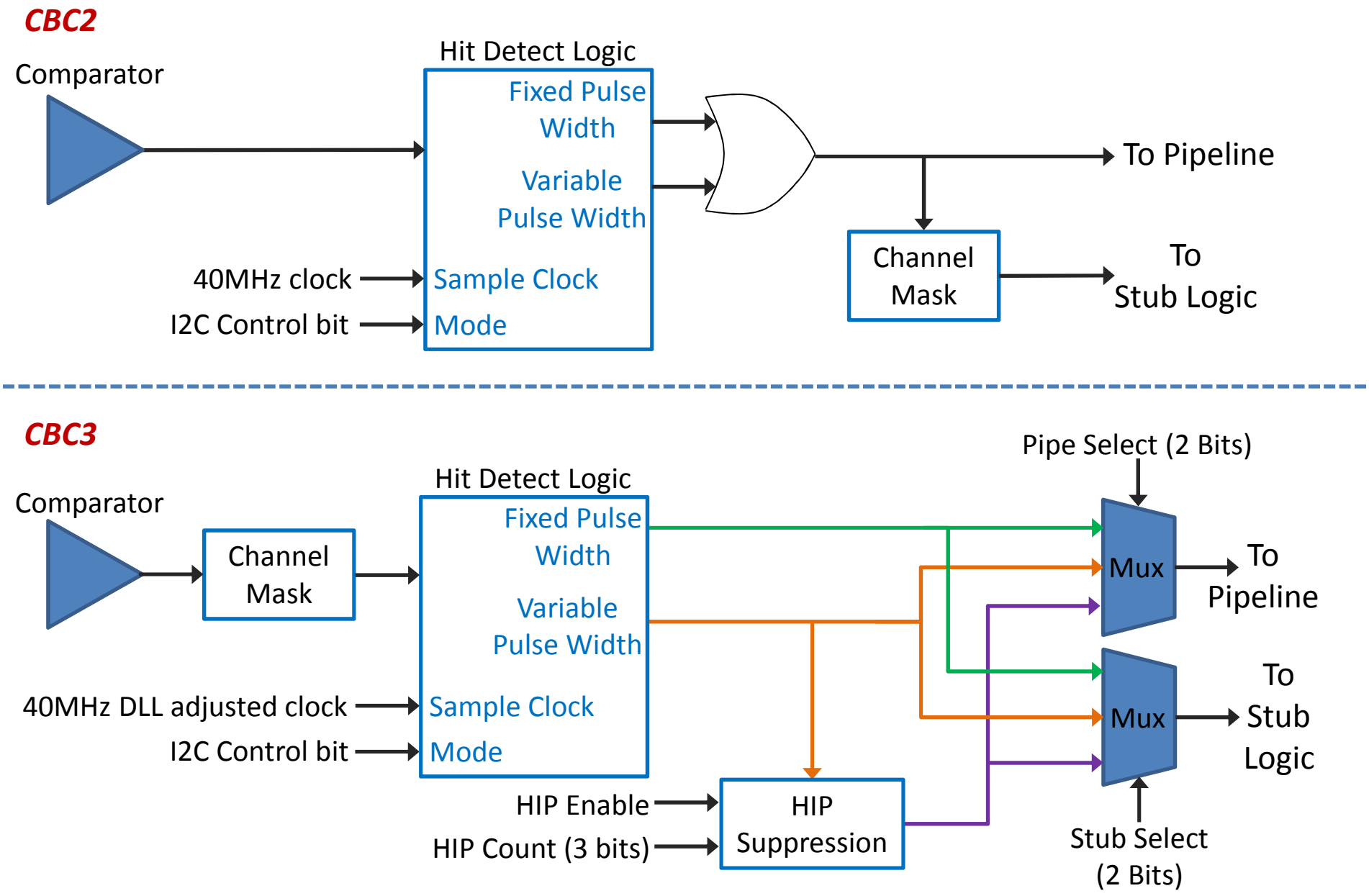
Gain Amplifier:

- Single polarity
- 1V operation

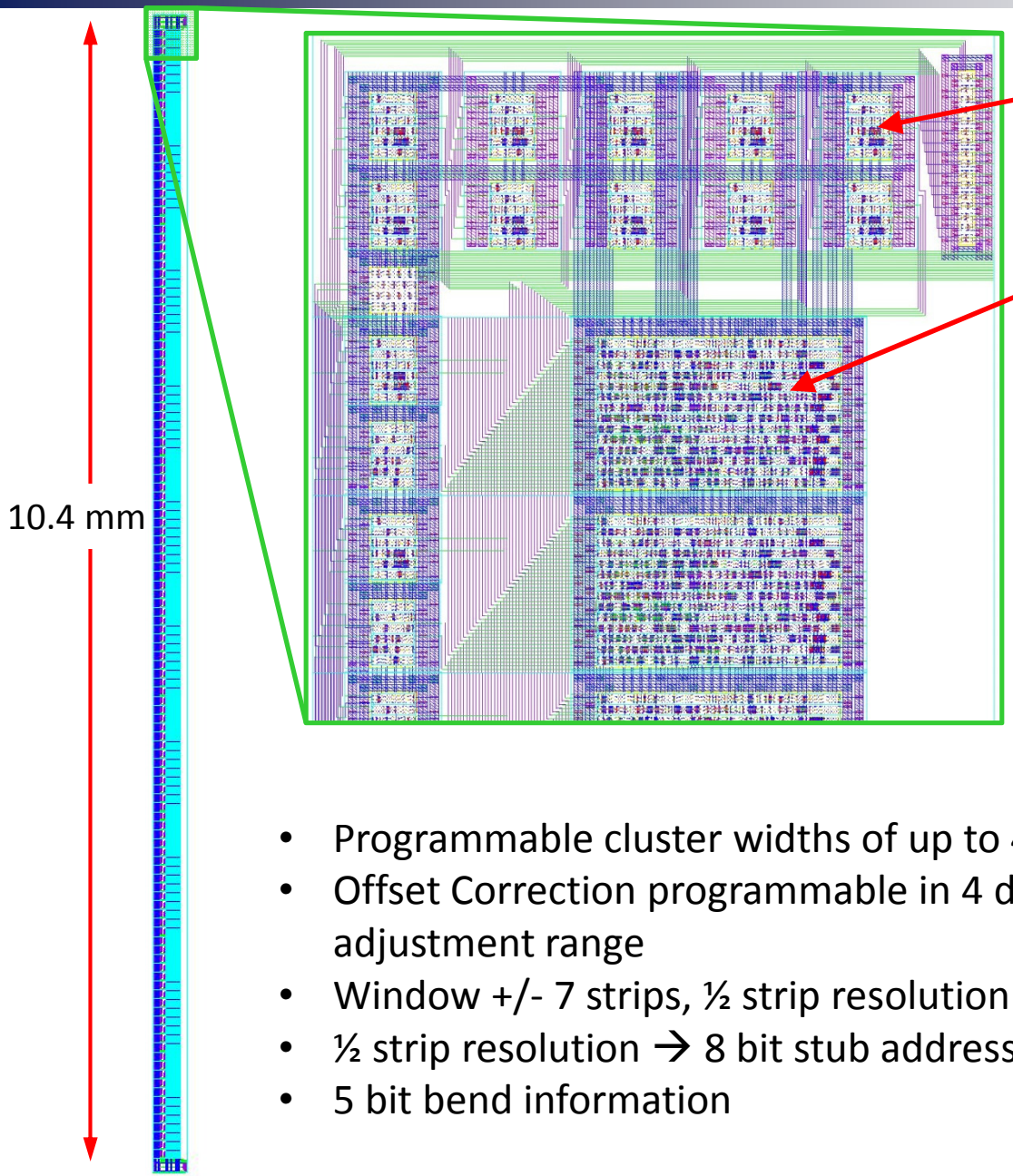
Comparator:

- Balance current load
- 1V operation

Hit Detect

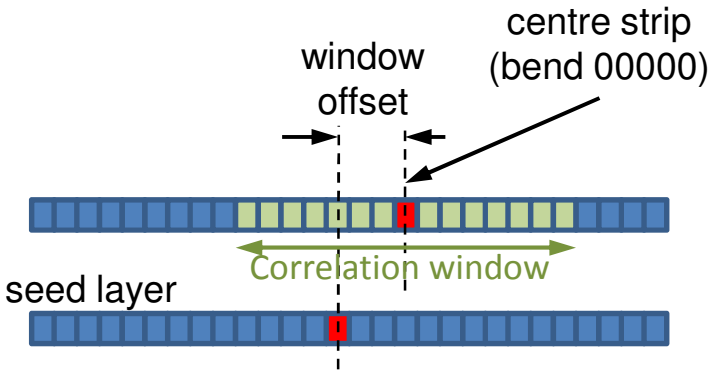

CBC2
Comparator
Hit Detect Logic
Fixed Pulse Width
Variable Pulse Width
Sample Clock
Mode
40MHz clock
I2C Control bit
To Pipeline
Channel Mask
To Stub Logic
CBC3
Comparator
Channel Mask
Hit Detect Logic
Fixed Pulse Width
Variable Pulse Width
Sample Clock
Mode
40MHz DLL adjusted clock
I2C Control bit
HIP Enable
HIP Count (3 bits)
HIP Suppression
Pipe Select (2 Bits)
Mux
To Pipeline
Mux
To Stub Logic
Stub Select (2 Bits)

Stub Logic



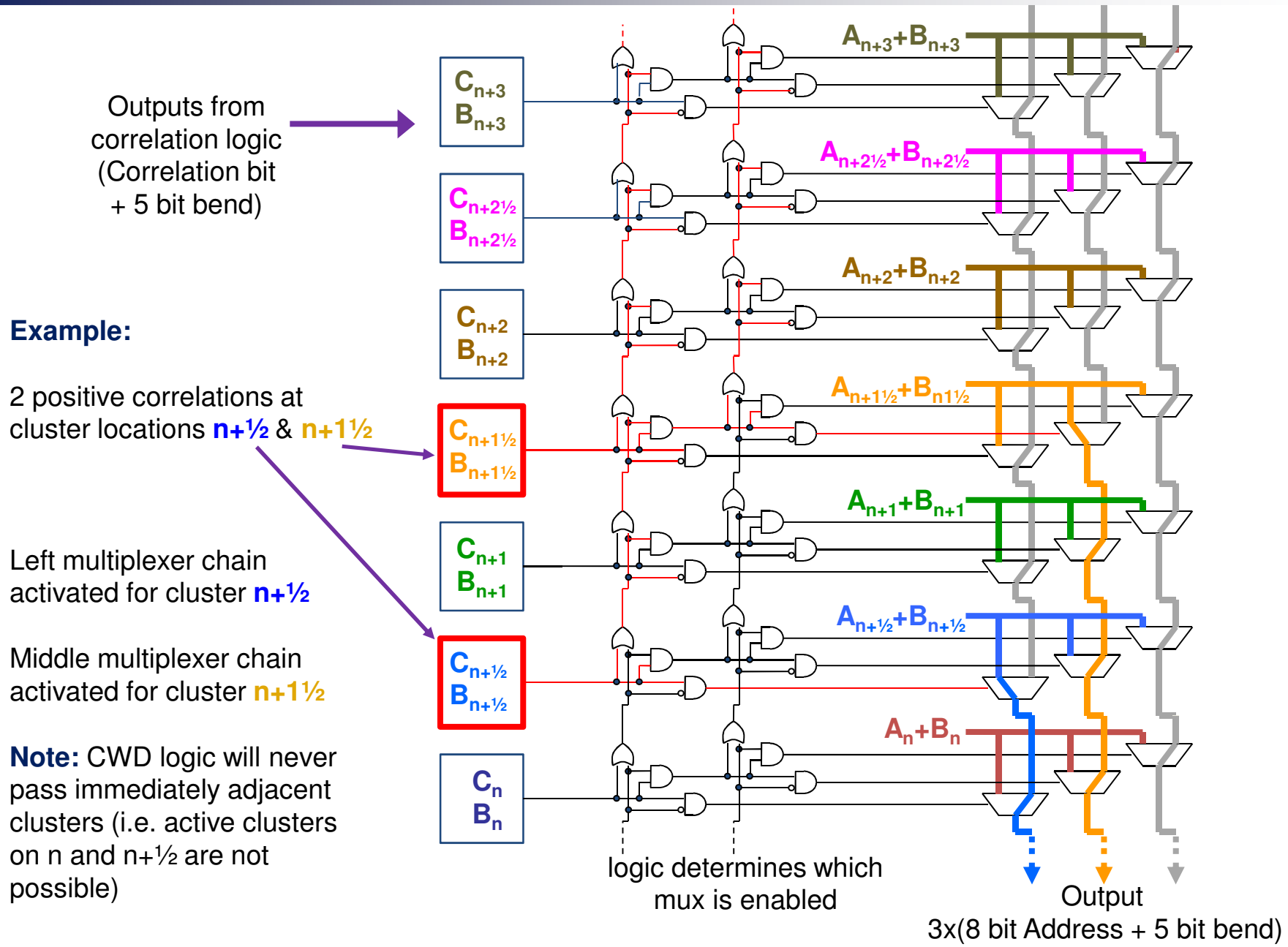
CWD Logic for off chip Neighbours

Offset Correction, Correlation and Bend Logic

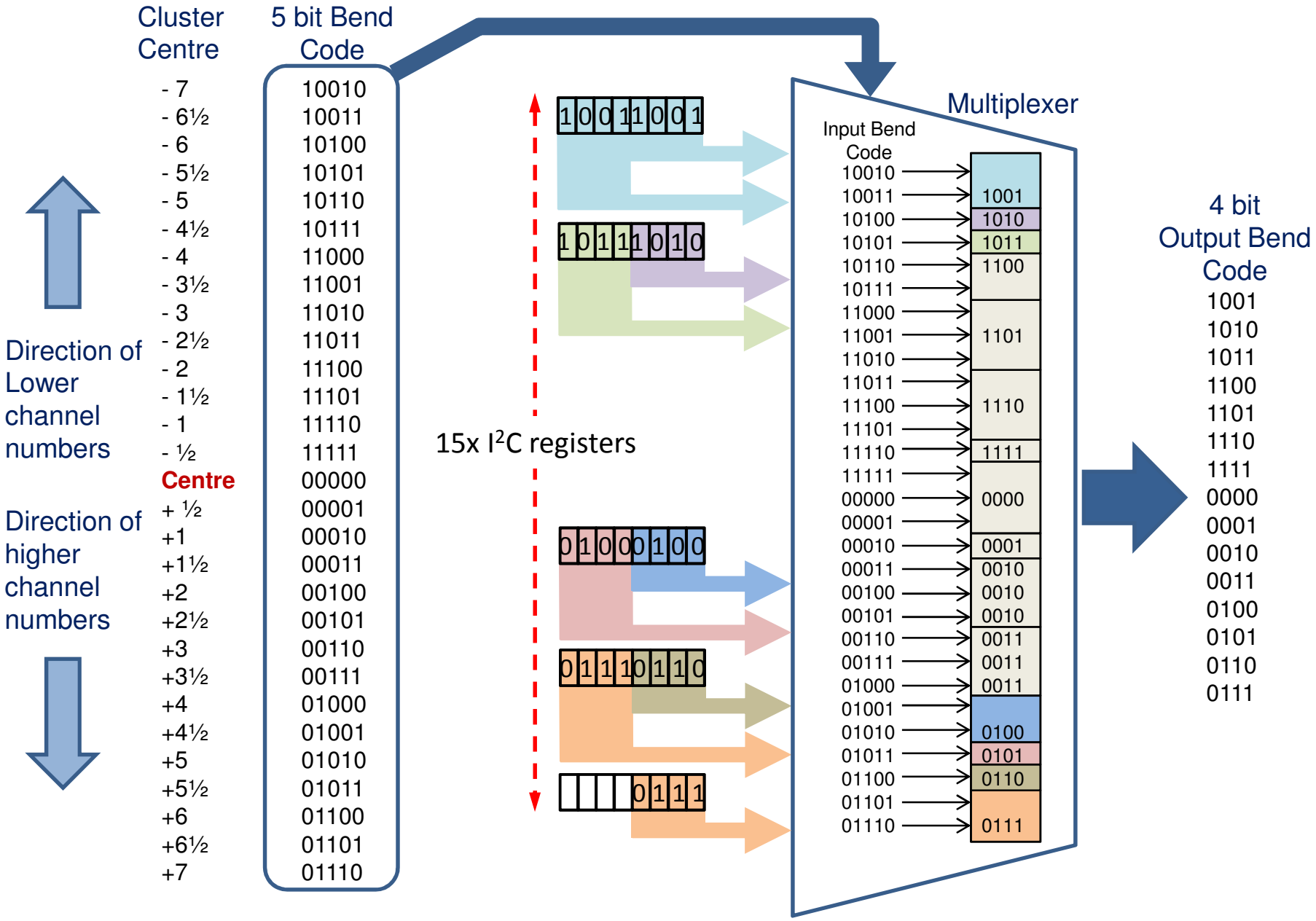


- Programmable cluster widths of up to 4 (>4 are rejected)
- Offset Correction programmable in 4 domains across chip with +/- 3 strips adjustment range
- Window +/- 7 strips, ½ strip resolution. 1 Stub/window (highest Pt)
- ½ strip resolution → 8 bit stub address
- 5 bit bend information

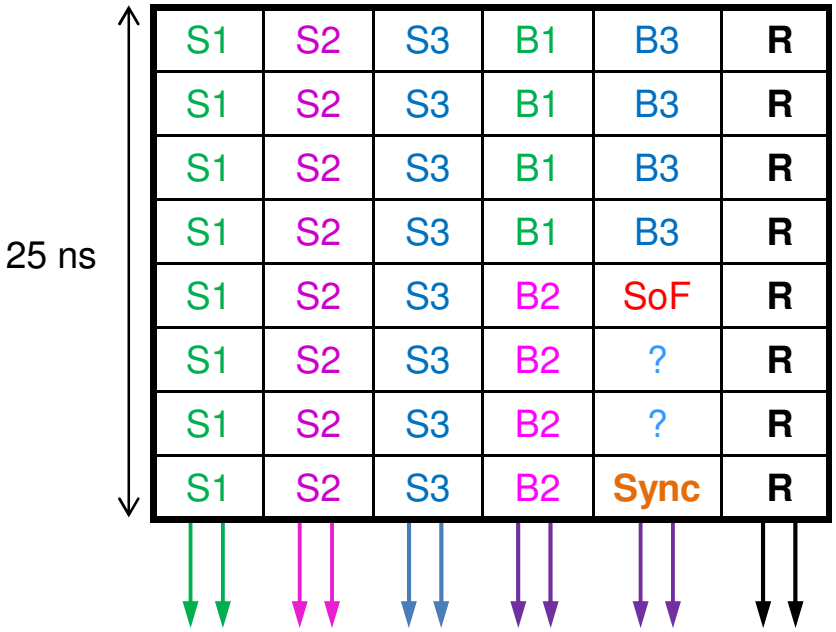
CBC3 Stub Gathering Logic



CBC3 Bend Look-Up Table



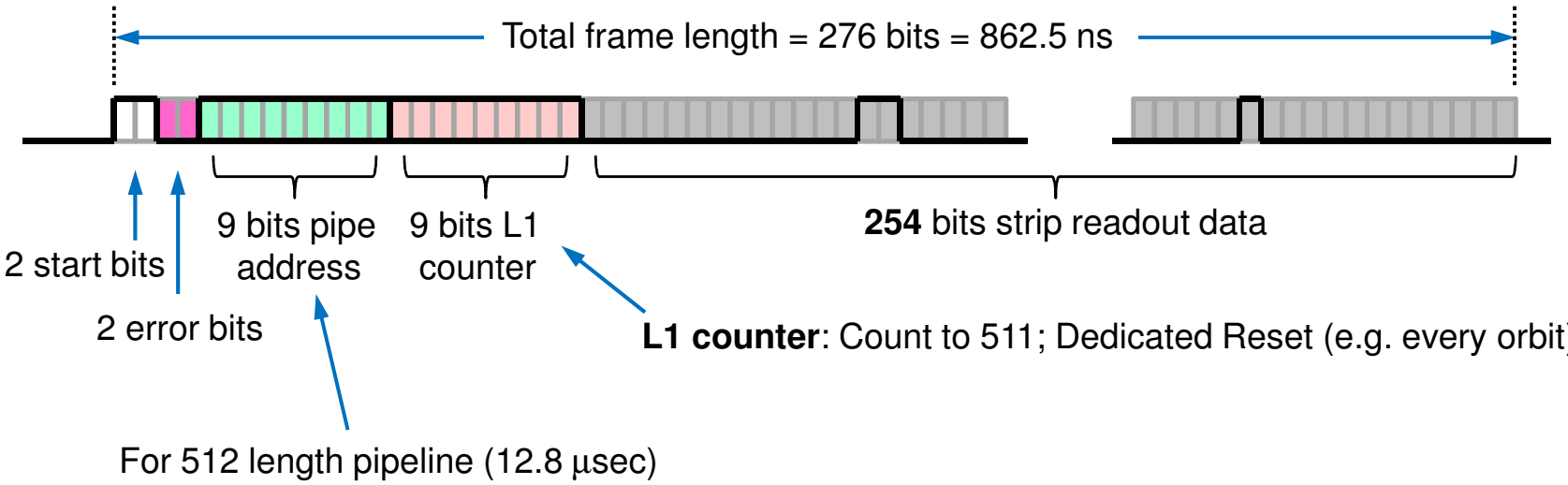
CBC3 Data Readout



S = Cluster address (½ strip resolution)
B = Bend data
SoF = Stub Overflow (>3 Stubs)
? = Spare/To be defined
Sync = For synchronisation with CC
R = Triggered readout data
(remains unsparsified)

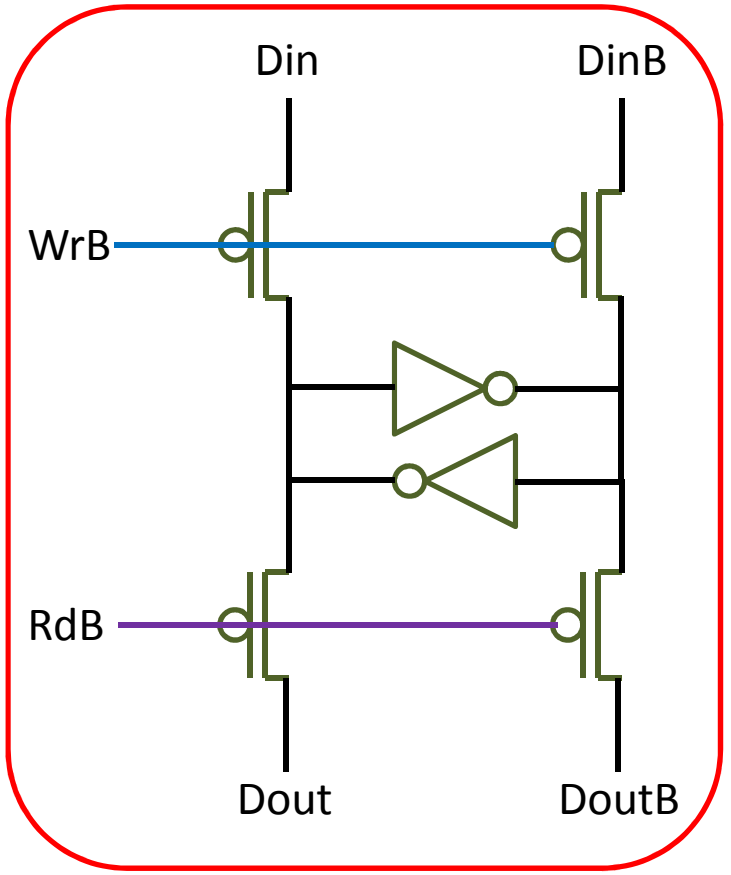
Six differential (SLVS) outputs running at 320 Mbps

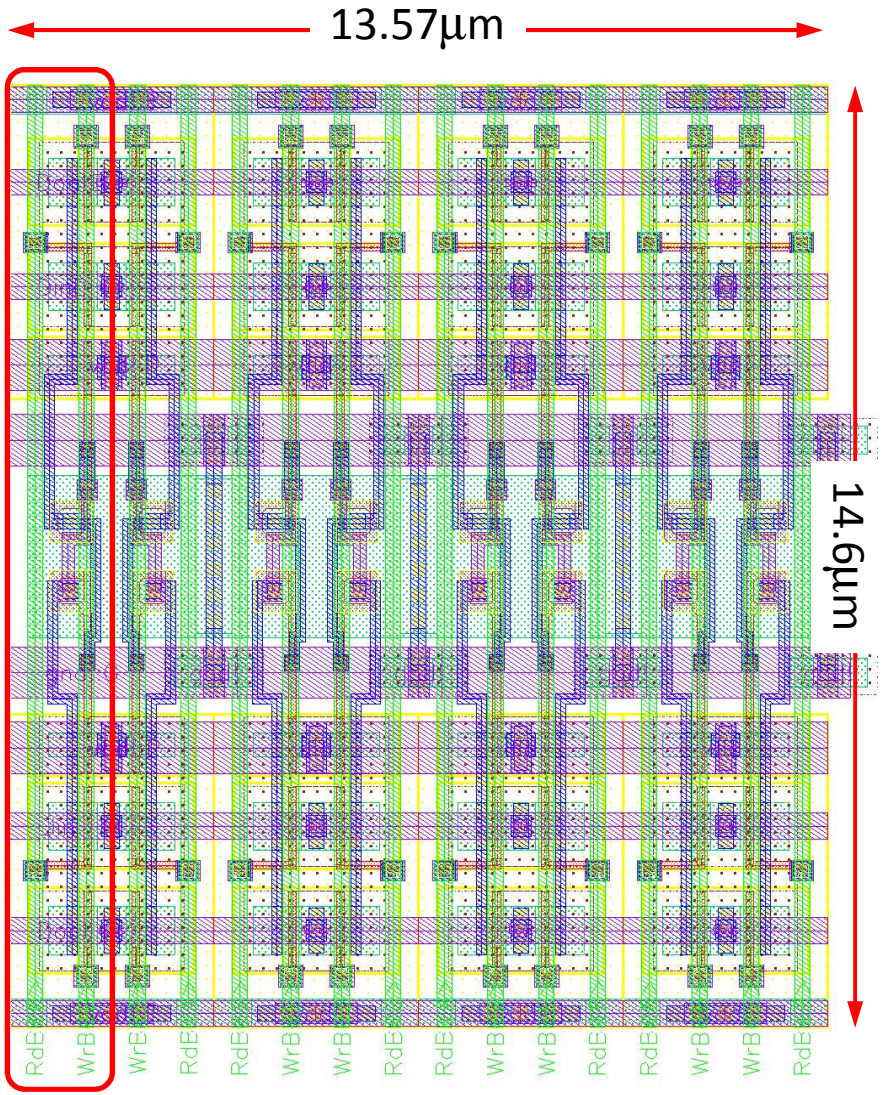
CBC3 Triggered Data Format



NOTE: Existing buffer length of 32 is sufficient for very low inefficiency at 1 MHz rate

CBC3 SRAM





Layout of 8 SRAM cells

Miscellaneous

Fast Command Interface: Fast Reset, Trigger, Test Pulse Trigger, L1 Counter Reset

Biases: VCTH to be monotonic & 1 mV resolution (10 bit); Modify IREF so that Ibias is related to GND rather than VDDA.

I2C register SEU immunity: Modify registers to improve immunity

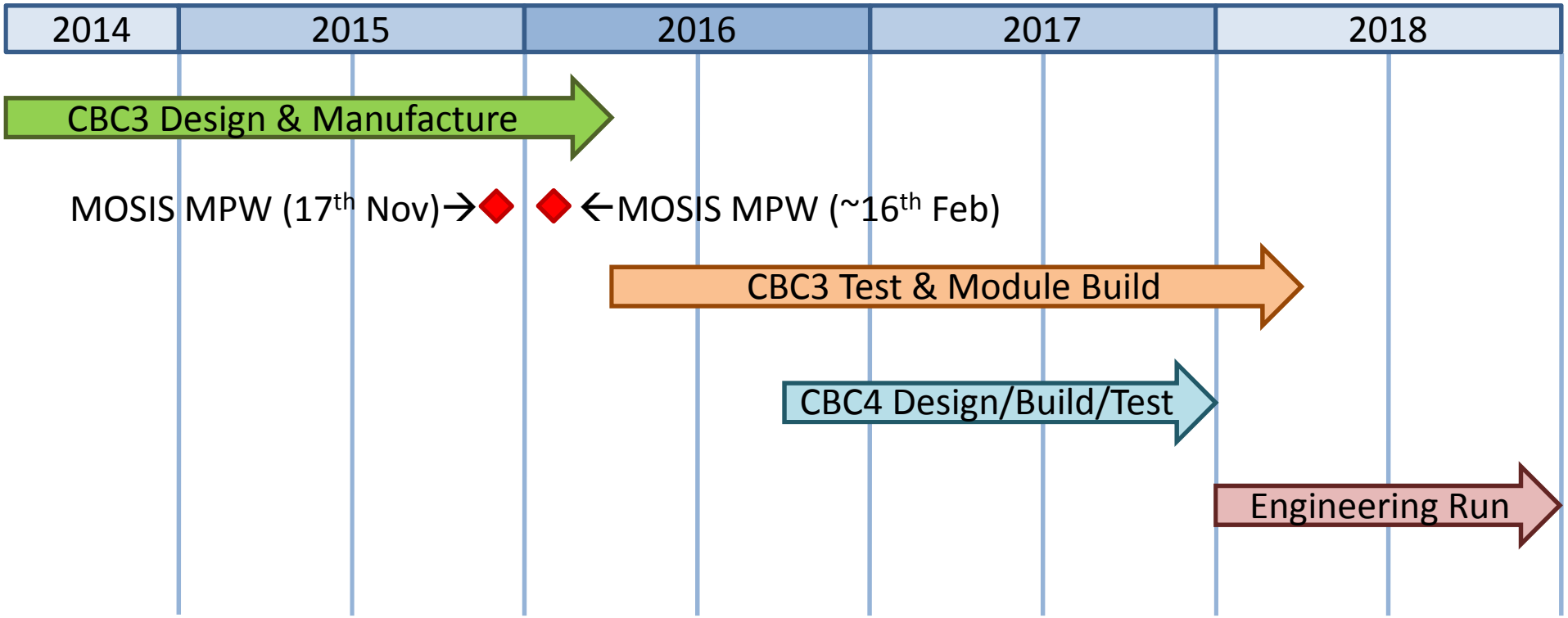
Clock domains: DLL with programmable tap off for all of 40 MHz domain

Powering: 1.2V VDDD +/- 10%; no switched cap DC-DC; LDO modified to cope with minimum VDD

40MHz Test Mode: To allow testing at 40MHz on Wafer Prober

Pad Pitch: As for CBC2

CBC3 schedule



- Manufacture on MOSIS MPW
- Aim to have CBC3 in hand ~1st half 2016
- CBC4 is an 'insurance iteration' in case something needs fixing

END