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Recent developments in the CBC3, a CMS micro-strip readout ASIC for track-trigger modules at the HL-LHC

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ABSTRACT

The CMS Binary Chip (CBC) is the front-end readout ASIC planned for the outermost layers of the CMS Phase 2 silicon outer tracker. Results from an extensive irradiation campaign carried out on the CBC3, the first version of the ASIC to include the full trigger logic circuitry, have demonstrated that the chip is capable of withstanding the levels of radiation expected at the HL-LHC, with only a slight ($< 1\%$) increase in power consumption. Results from the irradiation campaign, and details of the novel damage model developed to describe the measurements and extrapolate to the final operating conditions, will be presented. Additionally, results from tests at the Fermilab test beam facility will be shown that demonstrate the full functionality of the trigger logic.

Contents

1. Introduction

The Phase-2 CMS silicon tracker upgrade [1] will have to provide high-quality physics data while operating at the extreme beam intensities and particle collision rates foreseen at the high-luminosity upgrade of the Large Hadron Collider (HL-LHC). The outer tracker (OT) will be built from double-layered modules, those in the three outermost layers each consisting of two strip (2S) silicon sensors.

The trajectory of charged particles in the CMS magnetic field forms a circle in the transverse plane, with a radius of curvature proportional to the transverse momentum p_T. A single module can therefore identify high p_T particles by looking for a pair of coincident hits (a stub) in nearby channels in the two closely separated sensors. Stubs from different layers can then be combined into tracks in off-detector electronics. The CMS Binary Chip (CBC) is a 254-channel front-end ASIC manufactured in 130 nm CMOS technology for the readout of the 2S modules (shown in Fig. 1). The CBC3 [2] is the final prototype of the ASIC and the first to include the full logic circuitry required for stub finding (see Fig. 2).

Total ionizing dose (TID) tests performed on the previous prototype [3] of the CBC showed a large, but temporary, increase in digital current, and a pipeline sensitivity to occupancy. Both effects were attributed to radiation-induced leakage in the SRAM elements of the pipeline which motivated the decision to modify the SRAM block in the CBC3.

In this report the results of an X-ray irradiation campaign measuring the radiation tolerance of the CBC3 are reported. A radiation damage model, developed to extrapolate the results to HL-LHC operating conditions, will also be described.

2. Experimental procedure

Nine CBC3 chips were irradiated, using the CERN Seifert RP149 X-ray machine, at a variety of dose rates (0.11 ± 0.02 to 23.0 ± 4.6 kGy/h) and temperatures (−20 to 5 °C). The temperature of the chips was controlled and monitored throughout the irradiation, and the dose rates

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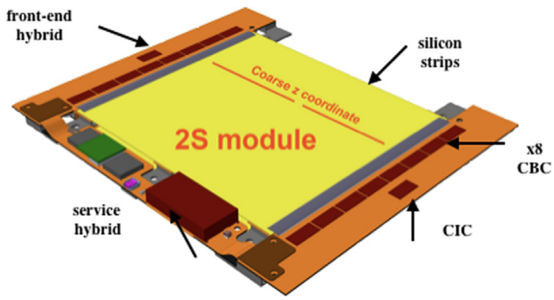

Fig. 1. An OT 2S module with two front-end hybrids containing sixteen CBC3s to read out the full module. A service hybrid will provide power and data connectivity.

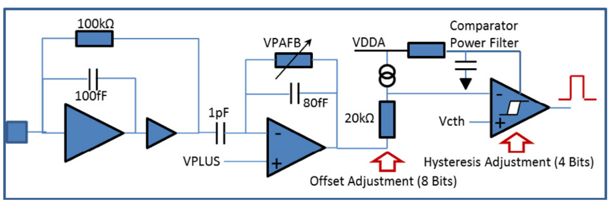

Fig. 2. A schematic of the CBC3 analogue front-end.

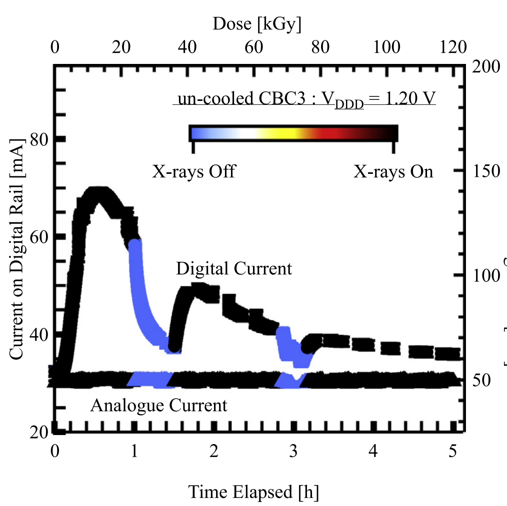

Fig. 3. Measured CBC3 digital (left axis) and analogue (right axis) currents during exposure to X-rays at the CERN X-ray irradiation facility. The colour of the marker indicates the state of the X-ray machine during the measurement.

were measured, with an uncertainty of 20%, using a calibrated PIN diode.

To replicate realistic operating conditions, a prototype DAQ system was used to provide the 320 MHz system clock, slow-control I2C commands, and clock-synchronous fast commands such as triggers and resets. The chips were wire-bonded to carrier boards plugged into an interface card, which provided the low voltage (1.25 V) and level translation to interface to the DAQ. The interface card also provided monitoring of the digital and analogue currents, and the on-chip analogue bias signals.

3. Results

3.1. Current consumption

The current consumption of the digital and analogue circuits recorded during the irradiation of a CBC3 at 23 kGy/h is shown in Fig. 3.

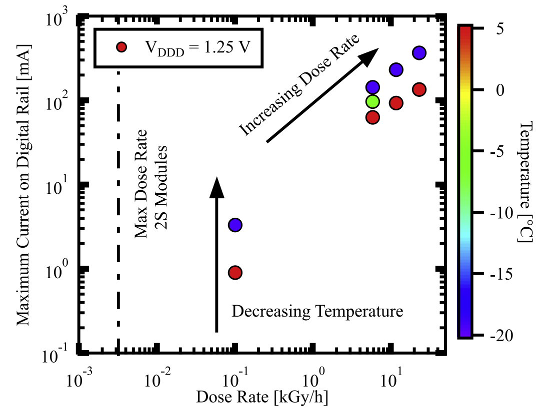

Fig. 4. The (maximum) measured current consumption on the CBC3 digital rail as a function of dose rate. The colour of the markers indicates the temperature at which the irradiation took place. All measurements used a supply voltage of 1.25 V.

As with the previous version of the chip, a radiation-induced leakage current is observed. The current consumed begins to increase after a few kGy of dose and continues to increase up to a dose of approximately 15 kGy, beyond which it decreases exponentially towards the initial value.

The initial irradiation was performed at a dose rate 10^4 times higher than that expected for the 2S modules closest to the interaction point, and with chips 47 °C warmer than expected in the Phase-2 OT. Determining the magnitude of the current increase under realistic HL-LHC operating conditions therefore requires an understanding of the effect of temperature and dose rate on the radiation induced leakage current. This motivated the undertaking of a series of measurements at different temperatures and dose rates summarized in Fig. 4.

The measured increase in current rises for decreasing temperatures and increasing dose rates. The temperature of the CBCs when deployed in the Phase-2 OT will range from −17 °C to −9 °C; the expected dose rate, indicated by a dashed line in Fig. 4, is approximately 2% of the lowest dose rate reached in the X-ray irradiations.

3.2. Analogue front-end performance

To verify robustness of the CBC3 analogue front-end against damage from ionizing radiation, all critical parameters were monitored throughout. This included checking the behaviour of analogue bias registers, verification of the on-chip pipeline by measuring the response to the internal test pulse, and continuous monitoring of the pedestal and the noise.

The two most important analogue biases are the band-gap reference V_{BG} (the reference for all on-chip analogue biases), and the global comparator threshold voltage V_{cth}. The resolution of V_{cth}, provided by a 10 bit digital to analogue converter (DAC) with reference voltages provided by the analogue supply rail (V_{DDA}) and the on-chip ground (GND), is given by

$$V_{cth}\left[\frac{\text{mV}}{\text{DAC units}}\right] = \frac{V_{DDA} - GND}{1024} = \frac{2V_{BG} - GND}{1024}, \qquad (1)$$

where V_{DDA} is twice V_{BG}.

The evolution of the band-gap reference voltage during irradiation, and the corresponding change in V_{cth}, for a chip irradiated at 2.3 kGy/h and a temperature of −5 °C is shown in Fig. 5. The measured 10 mV increase (∼ 2%) in the band-gap reference voltage of the chip is within the expected range (±12 mV) [4], and the increase in threshold voltage is as expected from Eq. (1).

The noise and pedestal must be inferred from an S-curve, which shows the fraction of events in which a hit is detected as a function

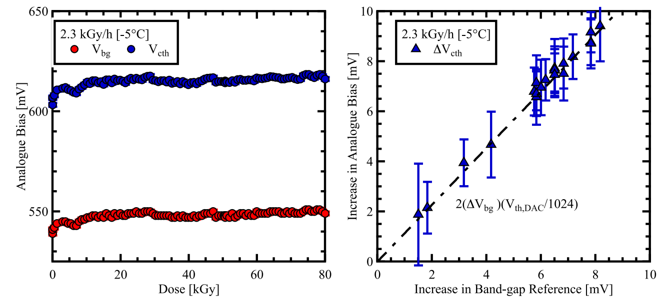

Fig. 5. V_{BG} and V_{cth} during irradiation; the comparator threshold corresponds to the output of the bias DAC at the nominal threshold setting of ≈580 DAC units.

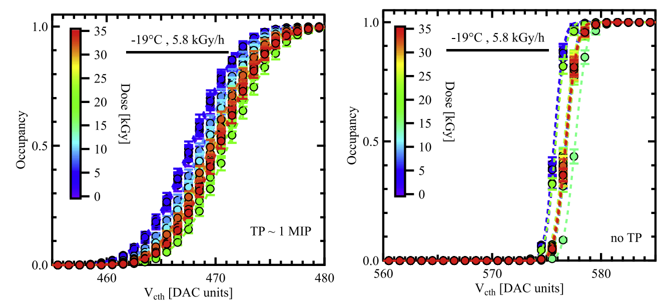

Fig. 6. S-curves measured during the irradiation period: (left) using the on-chip test pulse to inject charge equivalent to 1 MIP, and (right) with no charge injected. The colour of the markers indicates the dose received at the time of measurement, and the dashed lines the result of the fit using Eq. (2).

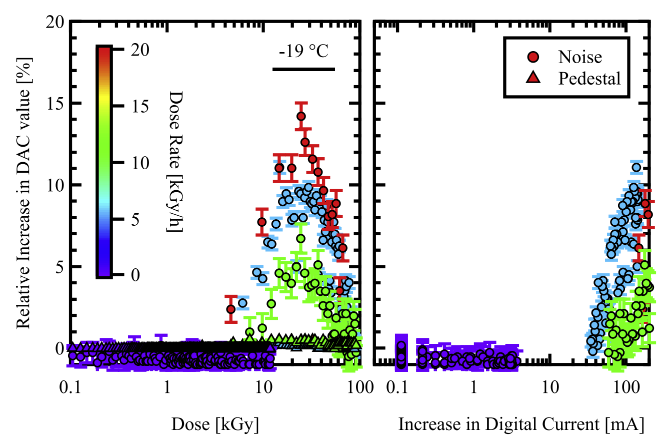

Fig. 7. Noise and pedestal as a function of dose (left), and correlation between noise and increase in digital current (right). The colour of the markers indicates the dose rate at which the irradiation took place.

of V_{cth}. Examples of S-curves collected during an irradiation are shown in Fig. 6. Fitting the S-curve with a sigmoid of the form

$$f(x,\mu,\sigma) = \frac{1}{2}\left[1+\mathrm{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right], \qquad (2)$$

returns the pedestal μ and noise σ. As Fig. 6 shows, the CBC3 also remains responsive to the on-chip test pulse in the presence of a large leakage current (≈200 mA). This indicates that enclosed pipeline transistors have mitigated the effects observed in previous versions of the CBC. The noise and pedestals measured for different dose rates are shown in Fig. 7. The increase in noise observed during irradiation at high dose rate is correlated with the radiation-induced leakage current; no change in noise is observed as long as the increase in current remains below 10 mA.

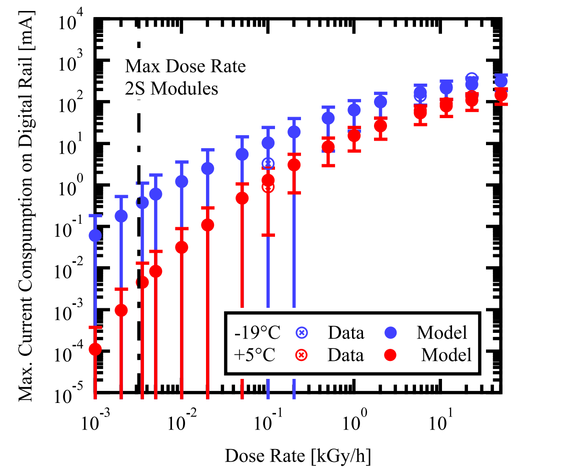

Fig. 8. Predicted and measured increase in the CBC3's current consumption as a function of dose rate. Measurements in open markers, predictions in solid.

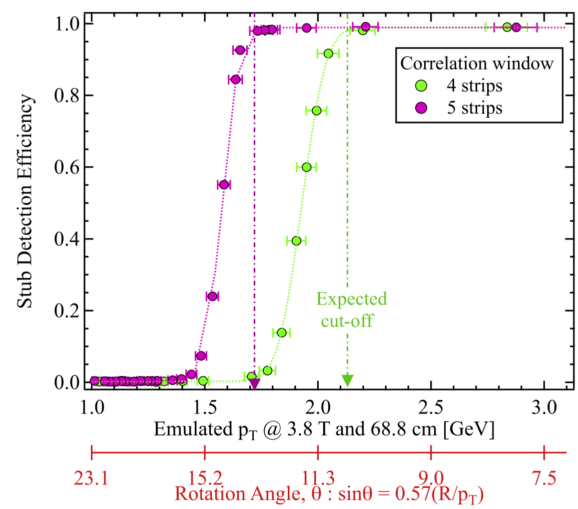

Fig. 9. Stub detection efficiency as a function of emulated p_T; the expected p_T cut-off estimated from the strip pitch (90 μm) and the sensor spacing 1.8 mm is also shown. The device was rotated with respect the beam to emulate the incident angle of charged particles on an OT module at $R = 68.8$ cm (radius of the innermost 2S layer in the OT).

4. Radiation damage model

The data collected with the CERN X-ray source (Fig. 4) was used to develop a model to predict an upper limit for the expected current increase in a 2S module under HL-LHC operating conditions. The model extends that proposed by Backhaus et al. [5], where the leakage current is attributed to the creation of leakage paths between source and drain via the inversion layer. The leakage paths are described as parasitic transistors, each with a transfer characteristic given by

$$I_D \approx 0 \;:\; N_{\mathrm{eff}} < N_{\mathrm{thr}} \qquad (3)$$

$$I_D \approx K_0\,(N_{\mathrm{eff}} - N_{\mathrm{thr}})^2 \;:\; N_{\mathrm{eff}} \geq N_{\mathrm{thr}}\;, \qquad (4)$$

where N_{eff} is the effective number of charges located in the inversion layer created by the build-up of positive charge in the oxide, N_{thr} is the threshold number of charges required to activate the transistor, and K_0 is a proportionality constant.

The effective number of charges in the transistor can be expressed [6] as

$$N_{\mathrm{eff}} = N_{\mathrm{OT}} - N_{\mathrm{IT}}. \qquad (5)$$

where N_{OT} and N_{IT} are the number of positive trapped charges and interface traps respectively, created when electron–hole pairs (ehps) generated by ionization interact with existing defects and impurities in the oxide. Some holes that survive initial prompt recombination may be trapped by deep traps as they move through the oxide, others interact with hydrogen-containing defects introduced in the oxide during its growth. The simplest of these interactions releases a proton from the defect site. Interface traps are created when such a proton reaches the Si-SiO$_2$ interface and forms a hydrogen molecule by removing a proton from a dangling Si-H bond.

An analytical description for the number of fixed positive charges N_{OT} and interface traps N_{IT} created during an irradiation can be found by solving the system of coupled differential equations describing the formation of holes and their trapping. The solution for the case where the irradiation starts at $t = 0$ is given by

$$N_{IT} = N_{SiH}\,[1 - e^{-f(t)}] \tag{6}$$

$$f = f_I\,N_p[1 - e^{-f_p k_0\,\dot{D}\,t + f_p\,N_{OT}}] \tag{7}$$

$$N_{OT} = N_{OT,max}\,\frac{f_{OT}k_0\dot{D}}{f_{OT}k_0\dot{D} + r_{OT}}\,[1 - e^{-(f_{OT}k_0\dot{D}+r_{OT})t}], \tag{8}$$

where:

- N_{SiH} and N_p are the number of hydrogen-passivated dangling bonds and hydrogen-containing defects present in the un-irradiated oxide respectively,
- f_I is the fraction of freed protons captured by dangling Si-H bonds,
- f_p and f_{OT} are the fractions of holes trapped by hydrogen and oxygen containing defects respectively,
- r_{OT} is the de-trapping rate of holes from deep traps,
- and finally k_0 is a constant related to the number of ehps initially created in the oxide by ionizing radiation.

A simultaneous fit of the parametrized damage model to the data collected for each set of four chips irradiated at −19 °C and 5 °C was used to extract the dose-rate dependence of the model parameters. The predicted current increase at the expected HL-LHC dose rate and −19 °C of 2.3 mA, shown in Fig. 8, is believed to be a conservative upper limit on the current increase expected in 2S modules due to radiation induced leakage in the CBC3s. This increase in current corresponds to less than a 1% increase in the total power consumption of a 2S module.

5. Stub finding in the CBC3

A 2S module prototype, constructed with two sensors separated by 1.8 mm and a double-sided rigid hybrid with two bump-bonded CBC3 chips, was used to test the full stub finding logic using the 120 GeV proton beam at the Fermilab Test Beam Facility. The chip can be configured to use different-sized correlation windows (the maximum transverse distance between the two clusters forming a stub), effectively setting a lower limit on p_T.

Fig. 9 shows the measured stub-detection efficiency, defined as the fraction of single track events in which a stub is found within 1 strip of the projected track impact point on the prototype, for two different correlation windows. The measurement shows that the stub efficiency is high (>99%) and that the p_T cut-off is in agreement with that expected for the sensor strip pitch and spacing.

6. Conclusion

An extensive irradiation campaign at CERN and tests at the Fermilab test beam facility have verified the functionality of the CBC3, the final prototype ASIC for the CMS OT 2S modules. The measurements have shown the CBC3 to be capable of withstanding HL-LHC radiation levels, and have demonstrated the CBC3's ability to identify high p_T tracks with high efficiency.

A radiation damage model has been developed, using data collected during the irradiations, to predict the expected increase in power consumption for HL-LHC operation. The maximum expected current increase in the CBCs would increase power consumption of a 2S module with 16 CBCs by approximately 20 mW, which corresponds to less than a 1% increase in the total power consumption of a module.

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