Results from the CBC3 readout ASIC for CMS 2S-modules

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ABSTRACT

The CBC3 is the latest version of the CMS Binary Chip for readout of the outer radial region of the upgraded CMS Tracker at the High Luminosity LHC. This 254-channel, $130\,\text{nm}$ CMOS ASIC is designed to be bump-bonded to a substrate to which sensors will be wire-bonded. It will instrument double-layer 2S-modules, containing two overlaid silicon microstrip sensors, aligned with a parallel orientation. On-chip logic identifies Level-1 trigger primitives from high transverse-momentum tracks by selecting correlated clusters in the two sensors. The CBC3 was delivered in late 2016; wafer probing and performance tests have been carried out. Several prototype modules using the CBC3 have been produced and tested in the lab and in different beams. The results show that the CBC3 satisfies CMS requirements and only small corrections are needed for the final version of the chip for production.

Contents

1. Introduction

The High Luminosity LHC (HL-LHC) sets stringent requirements for a new CMS silicon tracker [1], such as finer granularity, new power distribution, and capabilities to keep event rates in the Level-1 trigger under control. New trigger functionality will be achieved by providing outer tracker data to the trigger, using sensor modules constructed with two silicon microstrip planes separated (radially in the barrel region) by a few mm and on-chip logic in the readout chip selecting correlated hit clusters in the two sensors to identify trigger primitives from high transverse-momentum tracks. These so-called "stubs" are then formed into tracks by processors outside the detector. Stubs which are consistent with a track of transverse momentum $p_T \gtrsim 2\,\text{GeV}/c$ are passed to the track-finding processors. The outer tracker consists of an inner part containing modules with pixel–strip sensor pairs (PS-modules) and an outer part containing modules with strip–strip sensor pairs (2S-modules) [1]. The CBC is a binary readout ASIC designed in $130\,\text{nm}$ CMOS technology for the 2S-modules.

2. CBC development

A series of prototypes (CBC1, CBC2, and CBC3) has been developed as the system design and requirements evolved, gradually incorporating the functionality required by CMS. The basic functionality implemented in the wire-bondable CBC1 [2] includes 128-channels with analogue front-end preamplifier, shaper and comparator, followed by a binary pipeline memory, for sensors of either n-on-p or p-on-n polarity. The CBC2 [3] was bump-bondable and added coincidence logic for identifying potential stubs, along with programmable cluster-width discrimination and geometric-offset correction. It was designed with 254 channels,

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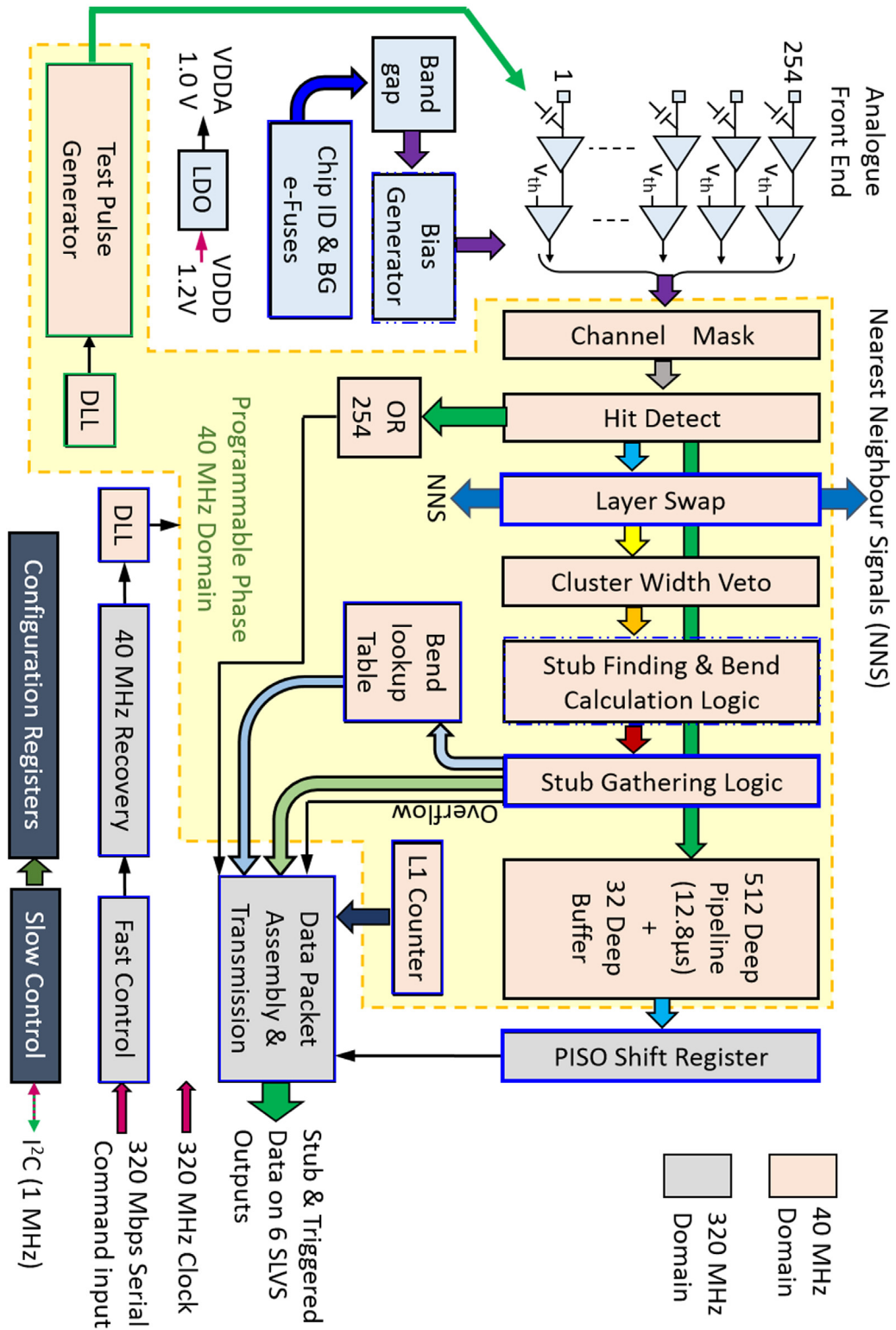
Fig. 1. CBC3 architecture.

so that adjacent channels could handle pairs of input signals from the two sensors.

The CBC3 [4] is intended to meet the final specifications; it is a 254-channel chip designed for the n-on-p sensors chosen by CMS and includes all the logic necessary to identify stubs and transmit them from the module. Following the amplifier stage, comparator outputs are stored in a 512-deep digital pipeline to accommodate trigger latencies of up to 12.8 μs. Several other new features are included in the design: the

CBC3 increased the resolution from single to half pitch for the cluster location and additional logic is provided to assemble a trigger data packet containing status flags and up to three stubs per bunch-crossing, each of which consist of an 8-bit address and 4-bit bend information. This data packet is divided into five bytes and transmitted from the ASIC via five differential SLVS output drivers operating at 320 Mb/s, thus allowing the complete data packet to be sent in one 25 ns bunch crossing interval. The control interface was designed to accept serial
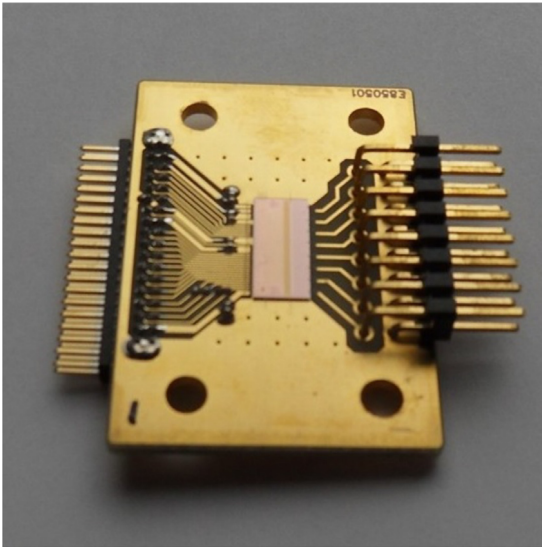
Fig. 2. A CBC3 chip prepared for evaluation on a PCB using wire-bonded connections. The left-side pads are intended for probe-testing on a wafer and provide power, and control data connections. On the right-hand side, 8 signal input pads designed for bump-bonding can be connected to different load capacitances.
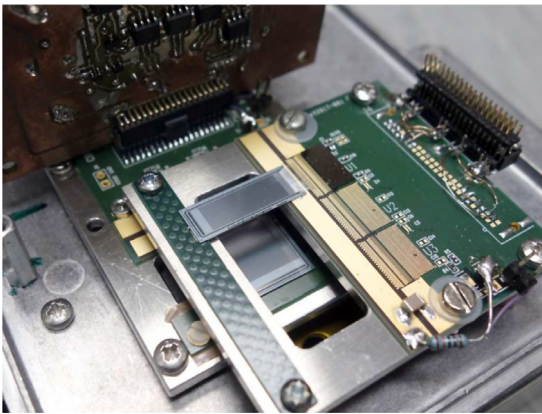

Fig. 3. A CBC3 bump-bonded to a PCB, and wire-bonded to a sensor, ready for insertion in a test beam.

8-bit differential SLVS command words at 320 Mb/s. An on-chip 40 MHz clock is derived from a pattern coded in the command word, the phase of which is adjusted to match signals from collisions using a programmable Delay-Locked Loop (DLL). The pipeline and I2C registers have also been redesigned to increase the radiation tolerance compared with the CBC2. In the CBC3, logic is implemented to curtail long duration (multi-clock cycle) hits resulting from HIP (highly ionising particle) [5] events which causes long duration signals from nuclear recoils in the sensor. The maximum number of clock cycles allowed for these long duration hits is configurable. The CBC3 architecture is summarised in Fig. 1.

Eight wafers were delivered, before solder-bump metallisation, in a shared multi-project submission, with 186 CBC3 chips on each wafer. Chips diced from one untested wafer were used to quickly assemble several simple one-chip modules using wire bonding (Fig. 2) instead of bumping. These enabled the injection of test signals of a precisely known size, and the addition of external capacitances for evaluating performance with different loads. Five further wafers were metallised with solder bumps and diced after good die had been identified by testing each one in detail on a wafer prober instrumented with a dedicated data acquisition system. CBC3s from these wafers were bump-bonded onto suitable PCBs by heating the chips on a solder-reflow station, before assembling the modules with sensors (Fig. 3).

3. CBC3 functionality test

The analogue front-end performance was evaluated with the single-chip wire-bonded modules. The parameters can be set by means of values stored in I2C registers. In this way the parameters of a band-gap circuit, bias currents, a global comparator threshold (VCTH), and channel offsets are tuned to define the correct pulse shape and optimise performance.

The band-gap voltage is used by a low dropout (LDO) circuit to create a reference voltage (VDDA) which is twice the band-gap value and this is fixed individually for each chip by 6 electrically programmable polysilicon resistors (e-fuses) at wafer probing time. The tuning resolution is ~1.7 mV and the target value chosen to be 520 mV.

The analogue front-end operates with a set of bias currents consistent with simulations, and a total analogue current of ~80 mA per chip. VCTH is generated by a 10-bit resistor ladder DAC and excellent linearity (~0.6 LSB non-linearity) is achieved over the full range from 0 to 1 V.

The pedestal level of each channel is adjusted by means of an offset. First VCTH is scanned over a wide range, producing a set of Gaussian error functions (s-curves), to establish for each channel the value at which it fires 50 % of the time. Then the offset for each channel is adjusted to match its central VCTH value to the average value for all channels. The tuned VCTH values have an rms variation of ~0.3 mV (~50 e) as shown in Fig. 4. The rms noise values corresponding to the s-curve width were measured for several load values at room temperature, as shown in Fig. 5, together with results from simulations. From the measurements made at room temperature, we conclude that the CBC3 satisfies the requirement that the Equivalent Noise Charge (ENC) should be ~1000 e up to 10 pF at the expected operating temperature in CMS (typically −20 °C).

The signal shape can be obtained by measuring the threshold level which fires the comparator while scanning the signal timing. Fig. 6 shows the pulse shape for an internal test pulse charge of ~1 fC with added external capacitance in the range 7 to 12 pF, where only small effects on the pulse shapes and peaking times are visible. The peaking time and the pulse width are measured to be ~20 ns and less than 50 ns respectively. The gain has been measured to be ~48 mV/fC which is consistent with simulation. A channel to channel variation of around 5 % in the gain (peak height) has been measured for the 8 externally accessible channels of the chip visible in Fig. 7. The signal shapes for externally injected charges up to 10 fC using a small external capacitor (overall input capacitance < 1 pF) in Fig. 8 are also consistent with simulation, and show that for normal amplitude signals the pulse shape duration remains acceptably short.

The effect of HIPs and the suppression logic were also tested by injecting a large signal charge into one channel. The effect was confined within 7 channels, where only nearest neighbour strips were found to have tails extending more than 1 μs after the HIP signal. The logic successfully suppresses the long duration hits observed in the central three channels and almost no dead time is observed for the remaining channels.

4. CBC3 wafer test

The test system was developed initially using single-chip wire-bonded modules and later adapted for the wafer probing system. The tests implemented are for I2C functionality, power consumption, pipeline, stub logic and DLL operation, and for channel uniformity. Correct I2C register operation is required for a chip to be useful. During the test, a chip ID is defined by programming a register via a set of e-fuses. The stub data were checked by comparing them in software with the equivalent correlation logic operating on recorded triggered data. The stub logic was also checked with different settings of the programmable cluster-width discrimination and geometric-offset correction, and creating various hit patterns by adjusting VCTH and channel mask settings. A small number of inconsistent stub addresses
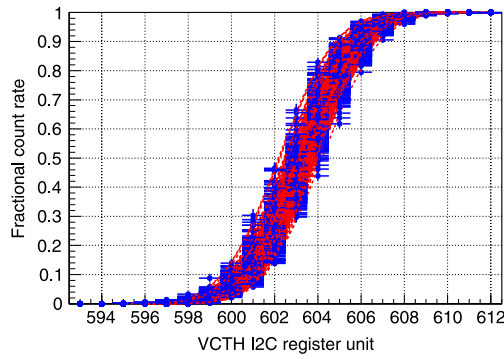
Fig. 4. Pedestal s-curves for all 254 channels of one CBC3 after offset tuning. Data are the blue points, with errors and fit functions in red. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)
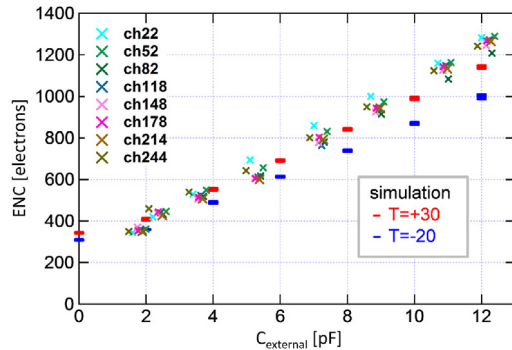

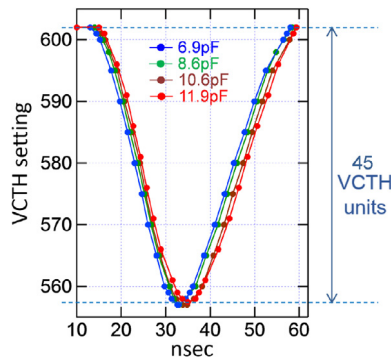**Fig. 5.** ENC values vs external capacitance load, compared with simulations at two temperatures.

Fig. 6. Pulse shapes for internal test pulse charge of ∼1 fC with added external capacitance. 1 VCTH unit = 1.07 mV for this chip.
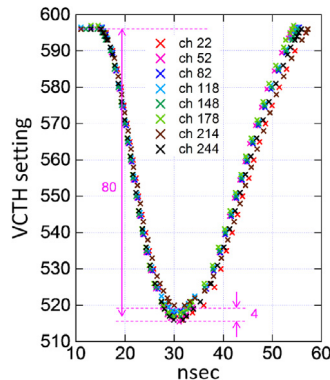

Fig. 7. Pulse shapes produced by injecting a charge of 1.8 fC into the 8 externally accessible channels.
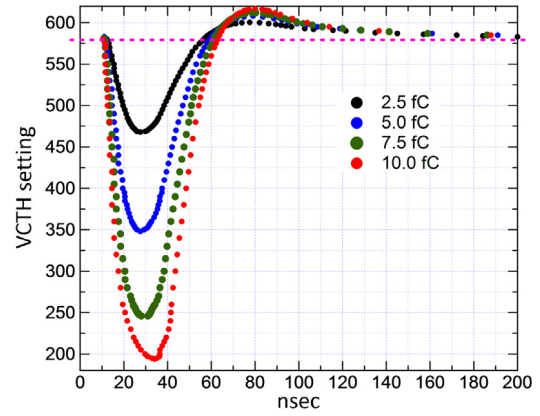

Fig. 8. Pulse shapes for different values of externally injected charge. An input charge of ∼2.5 fC corresponds to the MIP signal expected for a silicon thickness of 200 μm.

and bend information were found due to typographical errors in the stub logic circuit description in the HDL code which were not identified at the simulation stage.

Wafer probing was carried out at the full 320 MHz clock frequency on 8 wafers with an average yield of ∼85 %. The largest failure category was due to channel non-uniformity where a gain variation of more than ±10 % or the existence of defective channels leads to rejection.

5. Radiation tests

Total Ionising Dose (TID) tolerance of the pipeline in the CBC3 was enhanced compared to the CBC2 by a design change to use PMOS and enclosed NMOS transistors. The effect of TID appears as a leakage current increase in the digital circuitry, from a pre-irradiation value of ∼30 mA, and was studied using a CERN X-ray irradiation facility. The results are being prepared for separate publication. In summary, the digital current was observed to increase up to ∼10 kGy and then decline. The pedestals, noise, and gains were observed to be stable during irradiation; the performance is insensitive to TID.

To estimate the maximum digital current increase in HL-LHC conditions, chips were irradiated at dose rates from 0.1 to 20 kGy/h and several temperatures between −20° and +20 °C; extrapolations were then made to HL-LHC conditions (<0.01 kGy/h for 2S-modules) using an extension of the ATLAS FeI4 radiation damage model [6]. The estimated maximum digital current increase on a chip in the worst case location at HL-LHC is 3.5 mA which corresponds to ∼1.3 % increase in total power consumption. The small temporary current increase is not a concern so this and other results demonstrate that CBC3 performance is sufficiently insensitive to TID.

I2C registers and pipeline logic must be corrected at suitable intervals following Single Event Upsets (SEU) and the SEU rate should be low enough to allow sufficiently long periods of operation before resets. The SEU tolerance of the I2C registers implemented with triplicated logic cells in the CBC2 was lower than expected, owing to limited spatial separation of the cells, so in the CBC3 these were replaced by Whitaker cells [7], which is also used in the pipeline logic since CBC2; a sufficient SEU tolerance of the Whitaker cells in pipeline logic was observed and the tolerance was also estimated to be better than that of triplicated logic cells in the I2C registers.

SEU tolerance was tested in a proton beam at the Light Ion Facility in the Cyclotron Resource Centre of Louvain. The energy of the beam was 62 MeV and the flux was 2.3×10^8 cm^{-2}s^{-1}. The SEU cross section at this proton energy can be used as the average value in the outer tracker region at HL-LHC [8]. The HL-LHC rate was estimated by scaling the beam to the flux of 7×10^6 cm^{-2}s^{-1}, estimated from FLUKA simulations, at a radius of 68 cm, which corresponds to the innermost layer of 2S-modules.
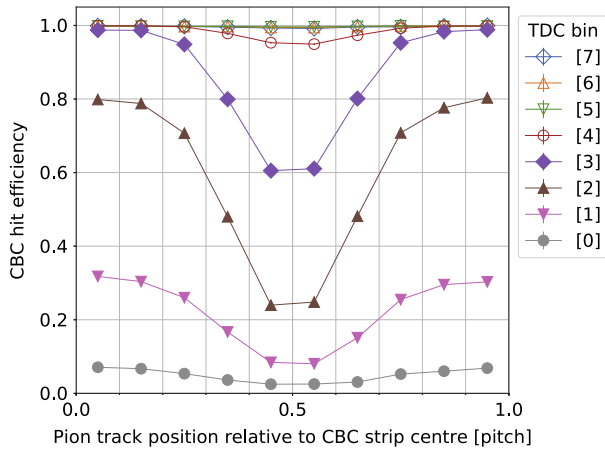
Fig. 9. Hit efficiency with respect to the incident beam position relative to CBC3 strip centres, which are located at 0 and 1. Each set of data points refers to a different delay with respect to the Hit Detect signal as described in the text. The data are grouped into $3.125\,\mathrm{ns}$ TDC bins. Efficiency falls as events are delayed with respect to the trigger.

Fig. 10. Hit efficiency with respect to telescope coordinate x and y, where strips are aligned parallel to y. A hit is a CBC3 cluster within $200\,\mu\mathrm{m}$ of the track reconstructed by the telescope. Event selection used TDC information, and events were required to be in bins 5, 6 and 7 of Fig. 9.

Fig. 11. A 2D histogram which displays the average evolution in time of highly ionising events generated by xenon ions. The contents of the bins, normalised to the most frequently populated, is colour-coded as indicated.

For the pipeline logic, an upper limit on the error rate of $1.2 \times 10^{-5}\,\mathrm{s}^{-1}$/chip was obtained, which is easily acceptable with the expected fast system resets, which take only a couple of clock cycles. SEU bit-flips were observed in the I2C registers, whose source was identified to be in inverters in write and reset logic. However, the rate was improved by an order of magnitude compared to the CBC2 and estimated to be 1.5 bit-flip per chip per day for the CBC3, which is low enough for operation and only a few % of these registers are the global chip configurations. Continuous monitoring of the registers with reconfiguration upon error detection is also practical.
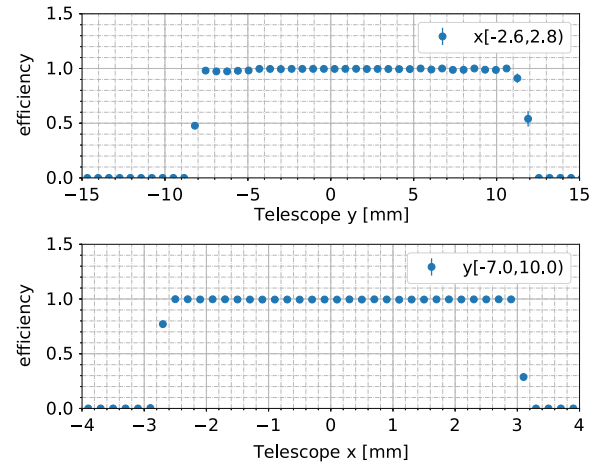
6. Beam tests with sensors

Single-sensor modules have been tested in the CERN H8 beam line parasitically with studies for the UA9 experiment where a precise telescope is available [9]. A module with a single Hamamatsu Photonics K.K. (HPK) n-on-p sensor of $2.0\,\mathrm{cm}$ length, $300\,\mu\mathrm{m}$ thickness, and $90\,\mu\mathrm{m}$ pitch microstrips was placed in a pion beam at 180 GeV and a xenon ion beam at 150 AGeV.

In the pion beam, the pedestals were stable, with typical noise $\sim 800\,\mathrm{e}$; the resolution was measured to be $25\,\mu\mathrm{m}$, very close to expectation. The hit efficiency was checked using straight tracks reconstructed by the UA9 telescope for different signal timings of the $40\,\mathrm{MHz}$ system clock with respect to the asynchronous pion beam.

When a scintillator trigger occurs it is transmitted to the CBC3 but synchronised to the $40\,\mathrm{MHz}$ master clock, so the CBC3 trigger can have up to $25\,\mathrm{ns}$ delay relative to the beam particle (once time of flight adjustments have been made). A TDC with a resolution of $3.125\,\mathrm{ns}$ recorded the delay of the CBC3 trigger relative to the scintillator. Fig. 9 shows the results of dividing the delay into eight intervals labelled 0 to 7. The earliest signal with respect to the trigger goes into bin 7, and the latest signal to bin 0. With a threshold set to $\sim 6\,\sigma$, the efficiency for signals with good timing with respect to the Hit Detect signal is more than 99 % and gradually drops, especially in the region between strips, for late-arriving signals as can be seen in Fig. 9. Uniform hit efficiency over the sensor for well timed signals is also demonstrated in Fig. 10.

Using a xenon beam [10], data resembling HIP events could be taken, allowing confirmation of measurements made in the lab by injecting electrical signals. Fig. 11 shows a summary of events, without the CBC3 HIP logic enabled, from which signal evolution in xenon beam events can be inferred. As expected, only a small number of strips near to the one where the ion was incident are affected by the large signals, and suppressing long duration events should be effective in reducing the already small dead time. A check was also made using the pion beam
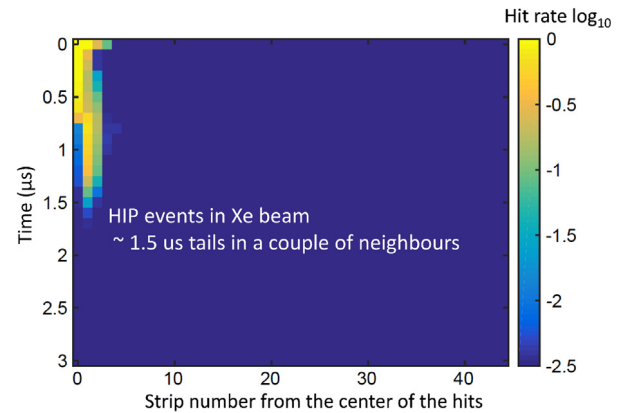
data for possible HIP events; with very small statistics, the fraction of events with similar long tails was of order 10^{-4}.

7. Conclusions

Test results demonstrate that the CBC3 will meet CMS requirements, once minor corrections are made. Further tests of the CBC3 and 2S-modules are ongoing and will continue in the coming year.

Acknowledgements

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