CBC3 Irradiation Tests Summary

Sarah Seif El Nasr-Storey
……on behalf of the UK Phase-2 tracker upgrade team

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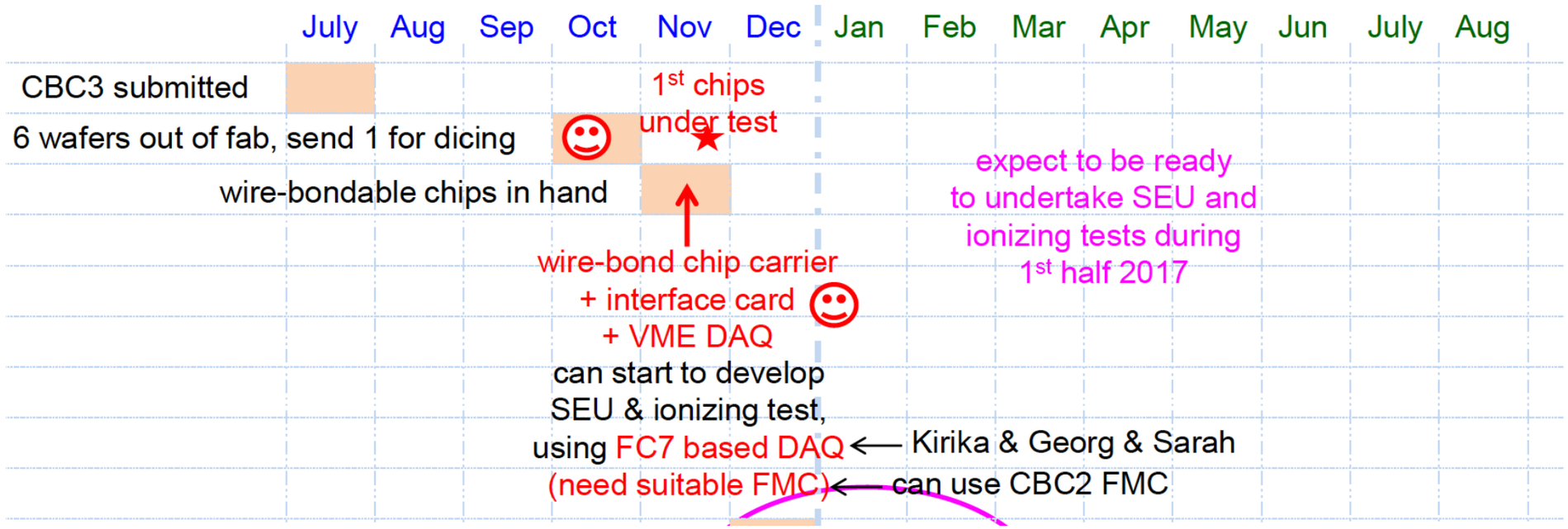
CBC3 Irradiation Tests Summary

Characterization of the CBC3 chip

- Final prototype front-end chip for the 2S module for the Ph2 Outer Tracker in CMS
- First CBC3 chips received in October of 2016 (6 wafers)
  - one wafer immediately sent out for dicing, so first chips in hand since November 2016
    - first report on performance during March tracker week
  - goal was to complete radiation testing on the CBC3 during the first half of 2017

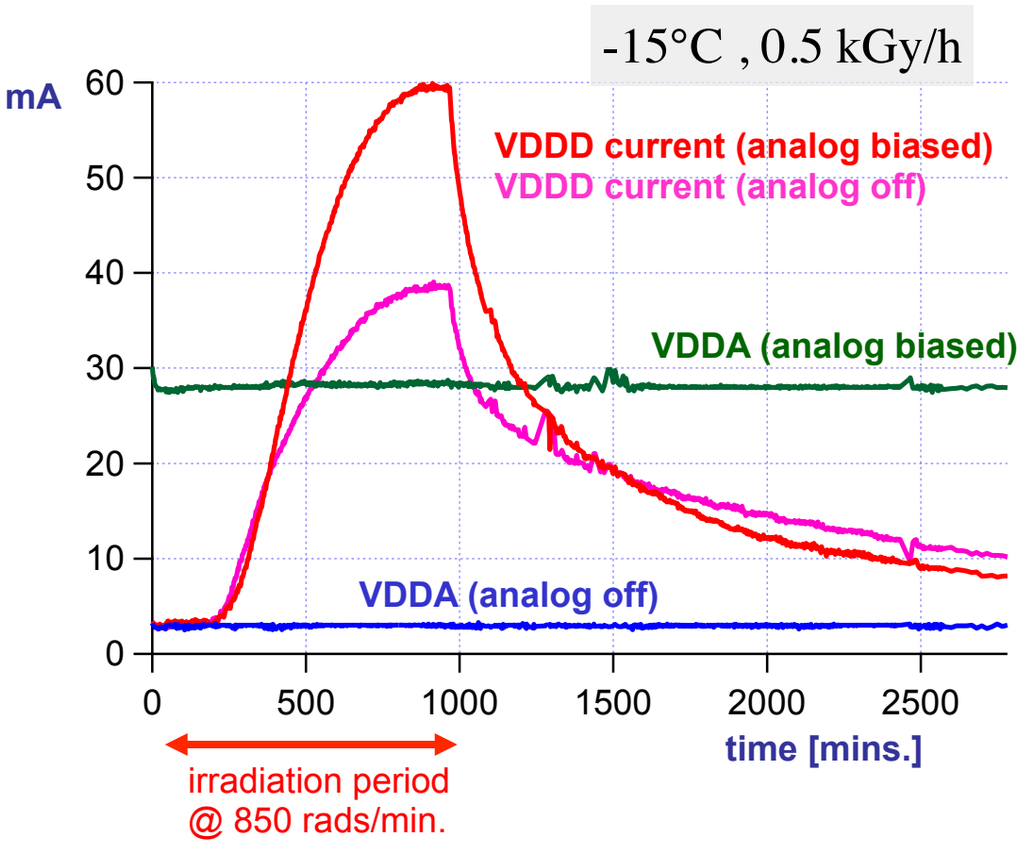


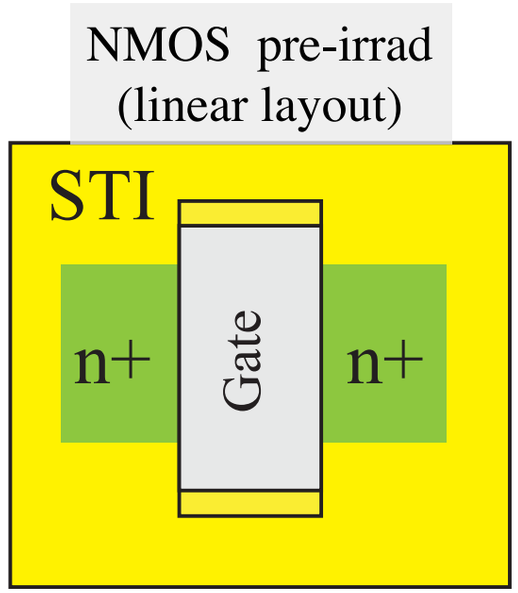
Schedule for CBC3 from Mark Raymond's status report November 2016 electronics meeting.

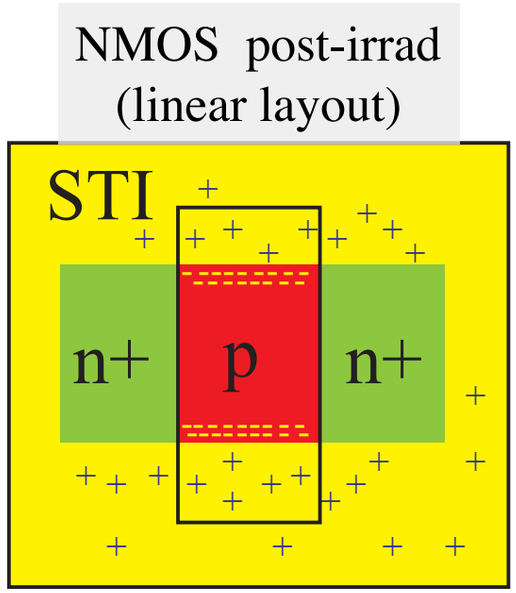
CBC3 Irradiation Tests Summary

Lessons learned from the CBC2 Irradiations : Radiation induced leakage

- Ionizing dose tests on CBC2 showed an initial spike in the current consumption of the chip :
  - identified as radiation induced leakage in the pipeline logic
    - non-enclosed NMOS transistors in pipeline suspected
  - effect also manifests as failure of some channels to respond to the test pulse







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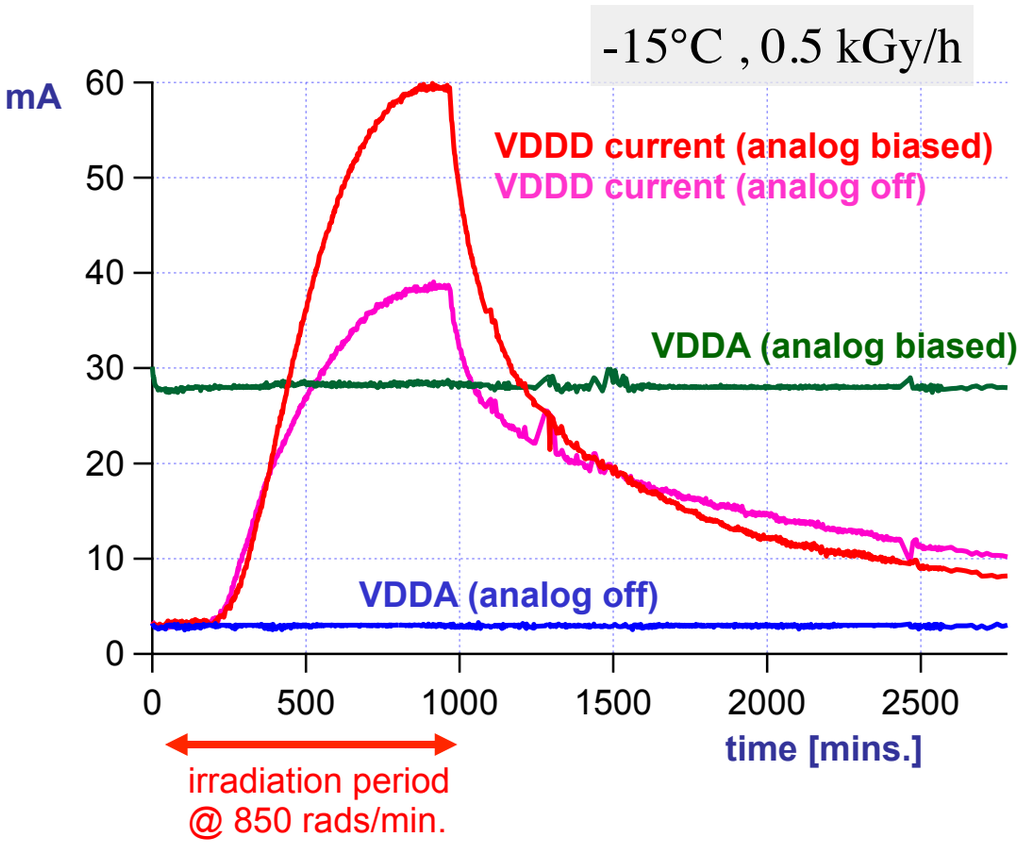
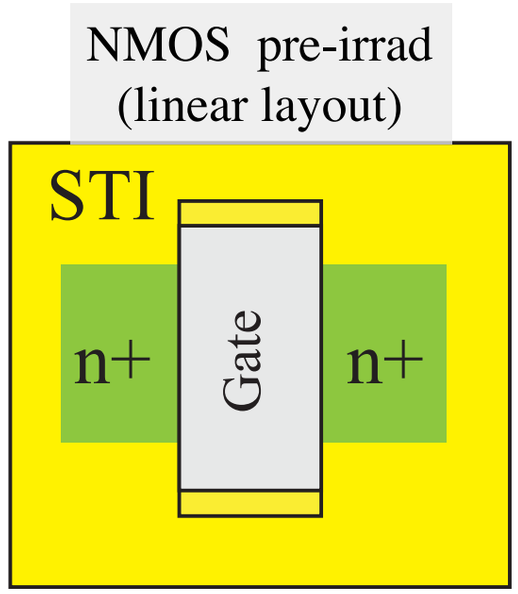
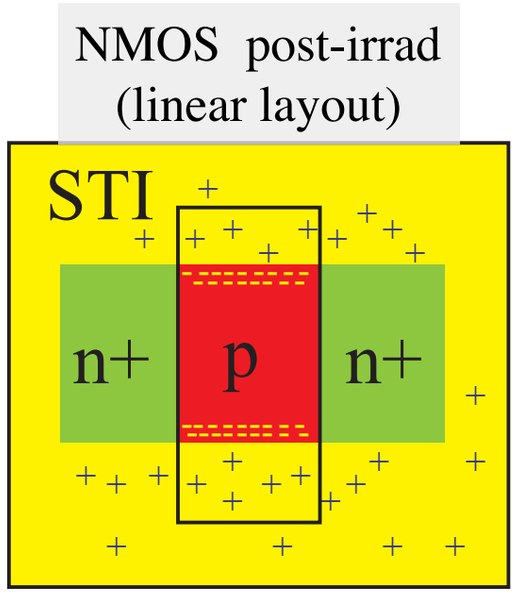






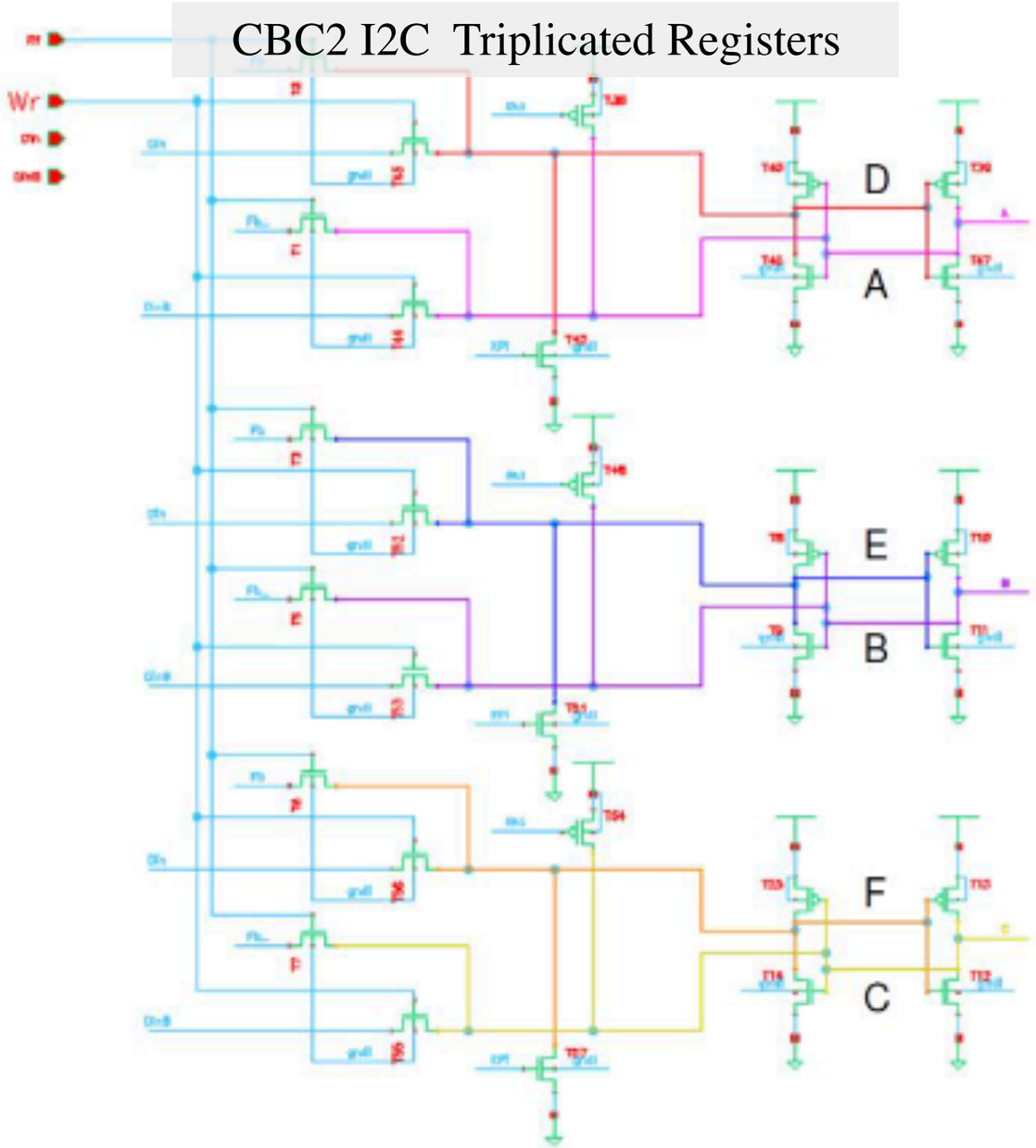
- Radiation hardness of pipeline SRAM block in the CBC3 improved by :
  - replacing NMOS read and write access transistors by more rad hard PMOS devices
  - replacing NMOS pull-down transistors with enclosed NMOS devices

CBC3 Irradiation Tests Summary

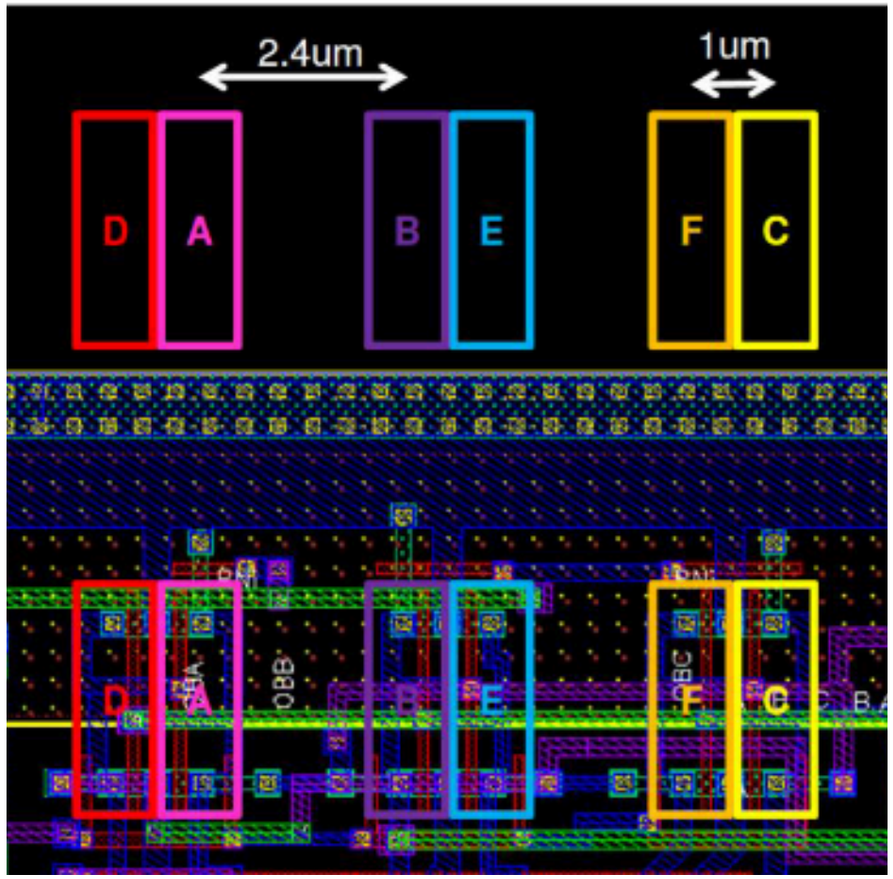
Lessons learned from the CBC2 Irradiations : SEU sensitivity

- Single Event Upset tests on the CBC2 showed that the I2C registers were susceptible to SEUs :
  - triplicated I2C registers used in the CBC2
    - but with insufficient separation (2.4 μm) between the three nodes of the cell
      - cells susceptible to simultaneous upsets in multiple nodes

CBC2 I2C Triplicated Registers



Triplicated Logic Layout



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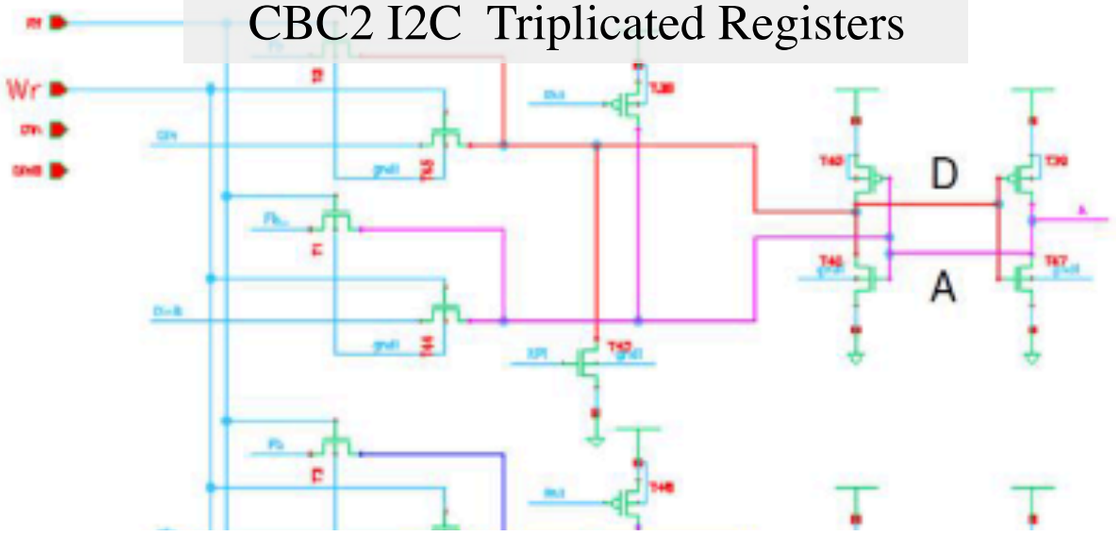
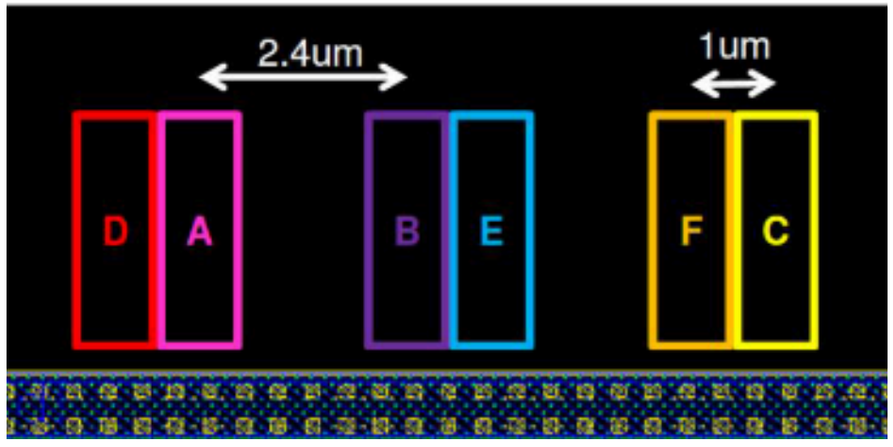
CBC2 I2C Triplicated Registers



Triplicated Logic Layout



- Sensitivity of the CBC3 to SEUs improved by :
  - replacing triplicated I2C registers with Whitaker latches
    - n+ diffusions used to store 0's (an SEU can only change their state from 1→ 0)
    - p+ diffusions used to store 1's (an SEU can only change their state from 0 → 1)

CBC3 Irradiation Tests Summary

Radiation Testing of the CBC3 chip

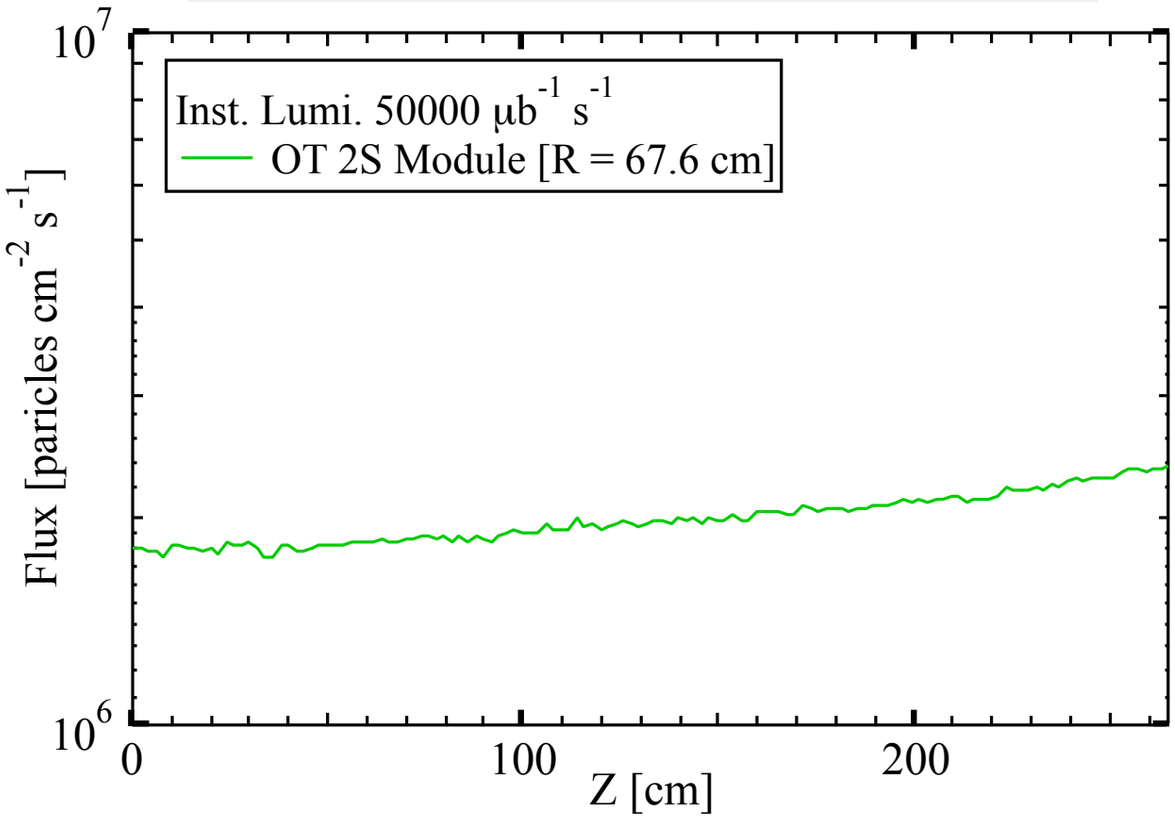
- Two test campaigns carried out in the first half of 2017 :
  - Total Ionizing Dose Tests using the CERN X-ray irradiation facility (EP-ESE-MIC)
  - Single Event Upsets Tests using the Light Ion Facility (LIF) at the Cyclotron Resource Centre in Louvain-La-Neuve, Belgium.
  - Special thanks to Federico Faccio and Davide Porret for their help with the X-ray machine, and Christophe Delaere and Martin Delcourt for their assistance in Louvain.
- Simple and portable FC7 based system used for all radiation tests :
  - Single-chip wire bonded carrier board to house CBC3
  - Firmware developed by Kirika
  - 1xCBC2 FMCs per CBC3 used to interface to the back-end

CBC3 Irradiation Tests Summary

A quick word on estimating particle flux and dose rate for 2S Modules

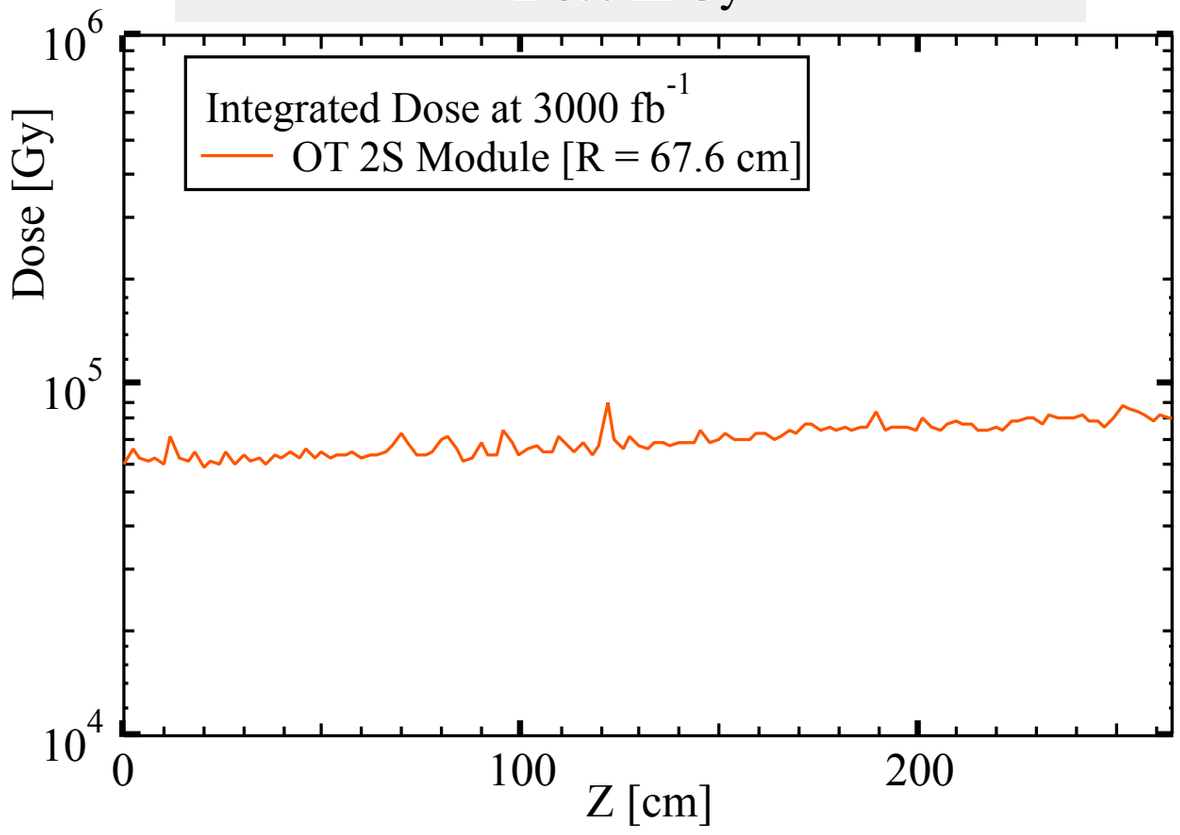
- BRIL Radiation Simulation and outer tracker layout from TDR used to estimate expected radiation levels for the innermost 2S module [R ~ 68 cm] :
  - Safety factor of (x3) applied to expected flux [particles cm^2 s^{-1}] and dose [1 Gy = 100 rad]

CMSphase2_pp_7TeV_v3.7.0.0_FLUKA :
Flux of Hadrons E > 20 MeV



Expected Flux : 7×10^6 particles cm^2 s^{-1}

CMSphase2_pp_7TeV_v3.7.0.0_FLUKA :
Dose in Gy

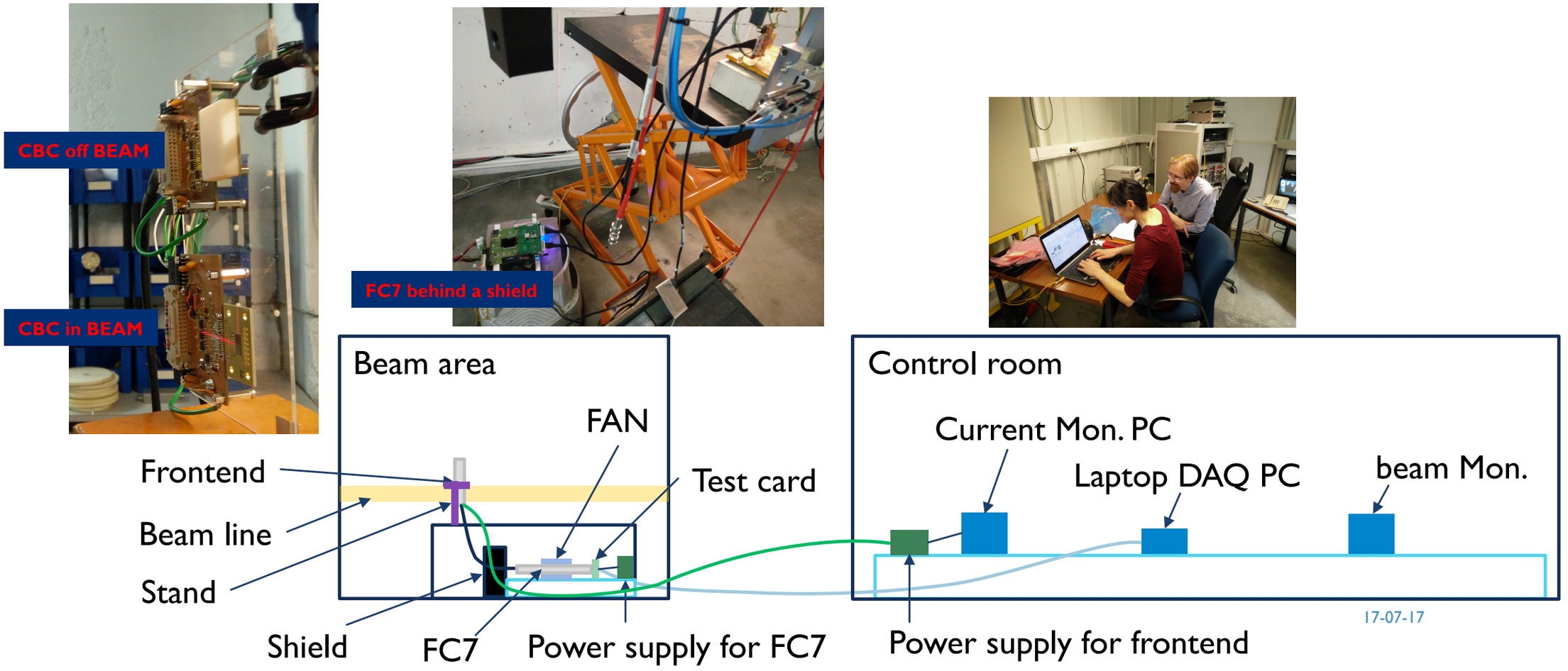


Expected Dose Rate : 9 Gy/h
[assuming 2800 hours of operation/year]

CBC3 Irradiation Tests Summary

SEU Testing of the CBC3 : Test Set-Up

- 14.6 hours of beam at the LIF (more details available in May's tracker week presentation) :
  - Proton beam from cyclotron with max. energy at 62 MeV and flux ~2.3x10^8 cm^{-2} s^{-1}
  - Data taken with 1 kHz trigger, latency set to 12.8 μs, no fast reset



- Measured SEU sensitivity of :
  - Pipeline memory cell of the CBC3 (pipeline data)
  - Pipeline logic cell of the CBC3 (pipeline logic)
  - I2C control registers

$$\sigma_{\mathrm{SEU}} = \frac{\mathrm{ER}\ [\mathrm{bit\ flips/s}]}{\phi\ [\mathrm{cm}^{-2}\mathrm{s}^{-1}]}$$

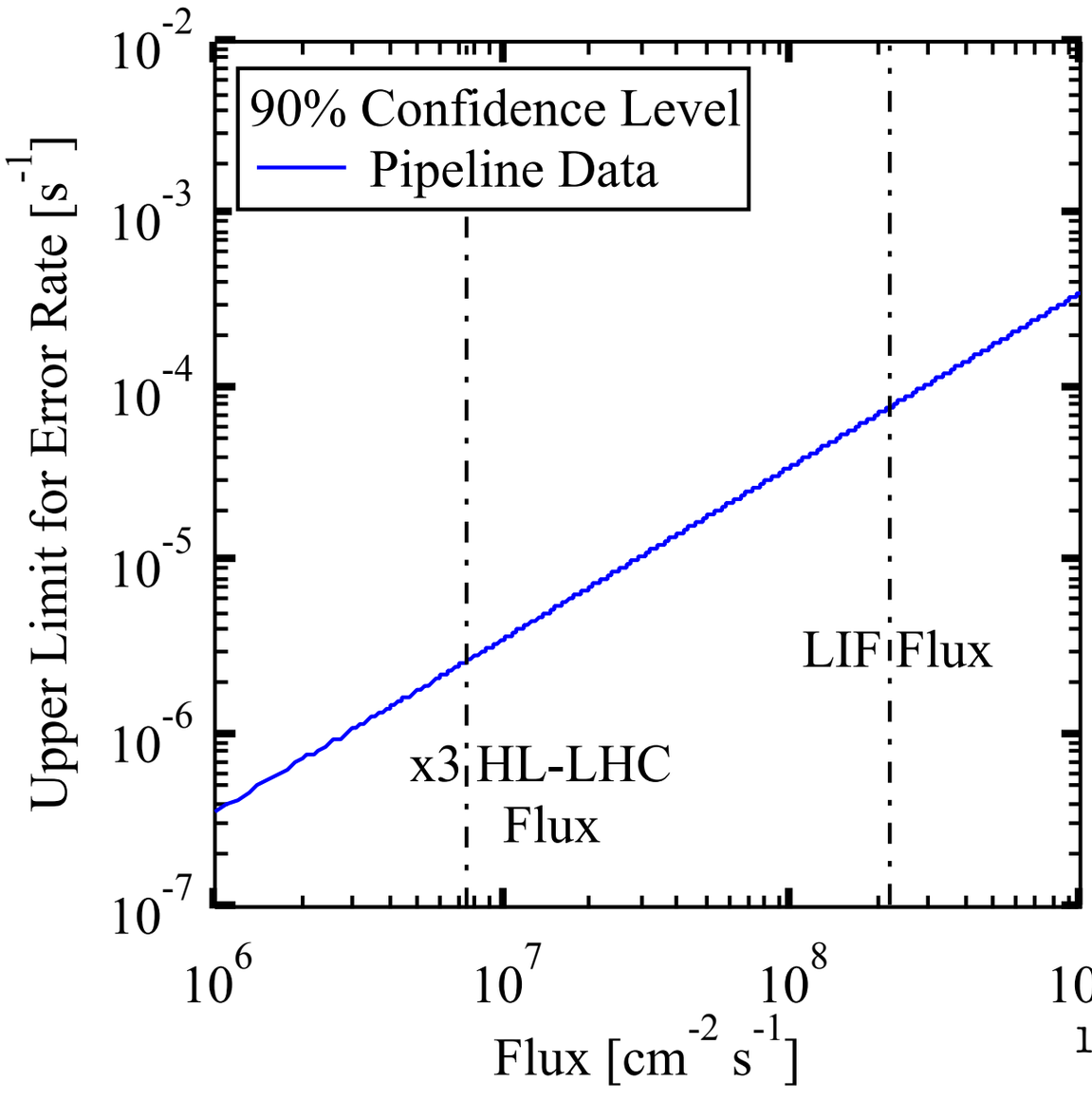
CBC3 Irradiation Tests Summary

SEU Testing of the CBC3 : SEU Rates in Pipeline Data

- 10.7 hours of beam time dedicated to measuring the SEU rate in the data stored in the CBC3's pipeline.
  - no errors which can be attributed un-ambiguously to SEUs
    - all errors observed in CBC3 in the beam were also seen in the shielded CBC3
  - ***upper limit*** placed on expected SEU cross-section using LIF data : **2.7×10^{-13} cm^2**
    - ***upper limit*** placed on error rate expected at HL-LHC : **1.9×10^{-6} s^{-1} per chip → 0.2 errors per day**

$$\text{ER [bit flips/s]}_{\text{Upper Limit}} = \frac{-ln(1-\text{CL})}{t_{\text{no errors}}}$$

$$\sigma_{\text{SEU}} = \frac{\text{ER [bit flips/s]}}{\phi\ [\text{cm}^{-2}\text{s}^{-1}]}$$



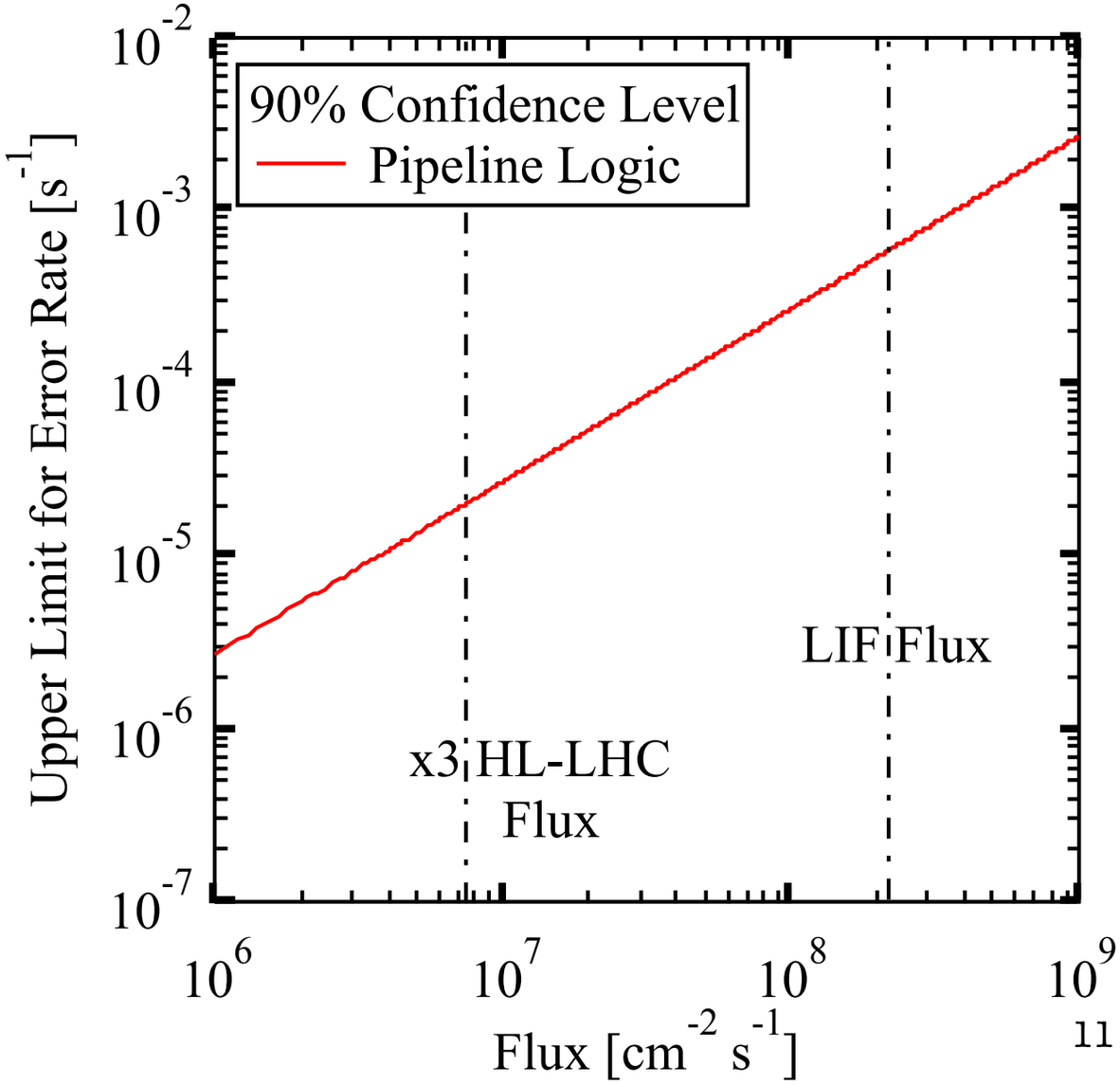
CBC3 Irradiation Tests Summary

SEU Testing of the CBC3 : SEU Rates in Pipeline Logic

- 1.4 hours of beam time dedicated to measuring the SEU rate in the data stored in the CBC3's pipeline.
  - no errors which can be attributed to SEUs
  - ***upper limit*** placed on expected SEU cross-section using LIF data : **2.1×10^{-12} cm^2**
    - ***upper limit*** placed on error rate expected at HL-LHC : **1.5×10^{-5} s^{-1} per chip → 1.3 errors per day**

$$\text{ER [bit flips/s]}_{\text{Upper Limit}} = \frac{-ln(1-\text{CL})}{t_{\text{no errors}}}$$

$$\sigma_{\text{SEU}} = \frac{\text{ER [bit flips/s]}}{\phi\ [\text{cm}^{-2}\text{s}^{-1}]}$$

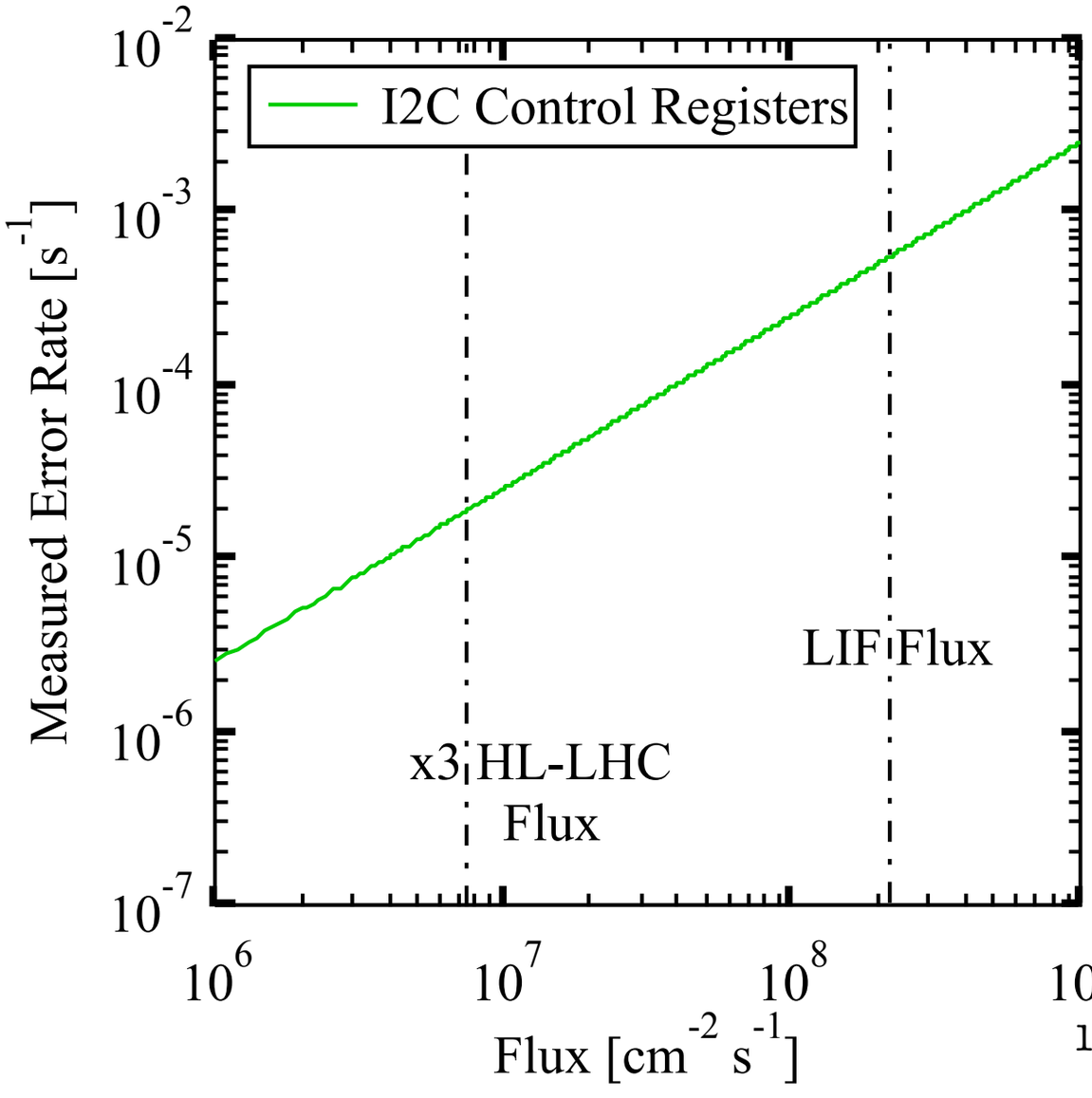


CBC3 Irradiation Tests Summary

SEU Testing of the CBC3 : SEU Rates in I2C Registers

- 12.4 hours of beam time dedicated to measuring the SEU rate in the configuration bits stored in the CBC3's I2C registers.
  - 25 bit flips observed in CBC3 in the beam
  - ***measured*** SEU cross-section using LIF data : **2.6×10^{-12} cm^2**
    - error rate expected at HL-LHC : **1.8×10^{-5} s^{-1} per chip → 1.5 errors per day per chip**

$$\sigma_{\mathrm{SEU}} = \frac{\mathrm{ER\ [bit\ flips/s]}}{\phi\ [\mathrm{cm}^{-2}\mathrm{s}^{-1}]}$$



CBC3 Irradiation Tests Summary

SEU Rates in I2C Registers : CBC2 vs. CBC3

- SEU tolerance in CBC3 improved compared to the CBC2 :
  - compare number of bit flips measured in a 10 minute interval (with no fast reset) from both tests
  - error rate at HL-LHC estimated for innermost layer in the outer tracker [R ~ 68 cm]

CBC version	# I2C bits	ϕ_{LiF} [$cm^{-2}\ s^{-1}$]	# bit flips [LIF]	σ_{SEU} [x $10^{-11}\ cm^{-2}$]	$ER_{HL\text{-}LHC}$ [bit flips/h]
3	2640	2.2E+08	0.36 ± 0.07	**0.27 ± 0.05**	0.069 ± 0.013
2	2456	2.5E+08	2.8 ± 0.5	**1.9 ± 0.3**	0.47 ± 0.084

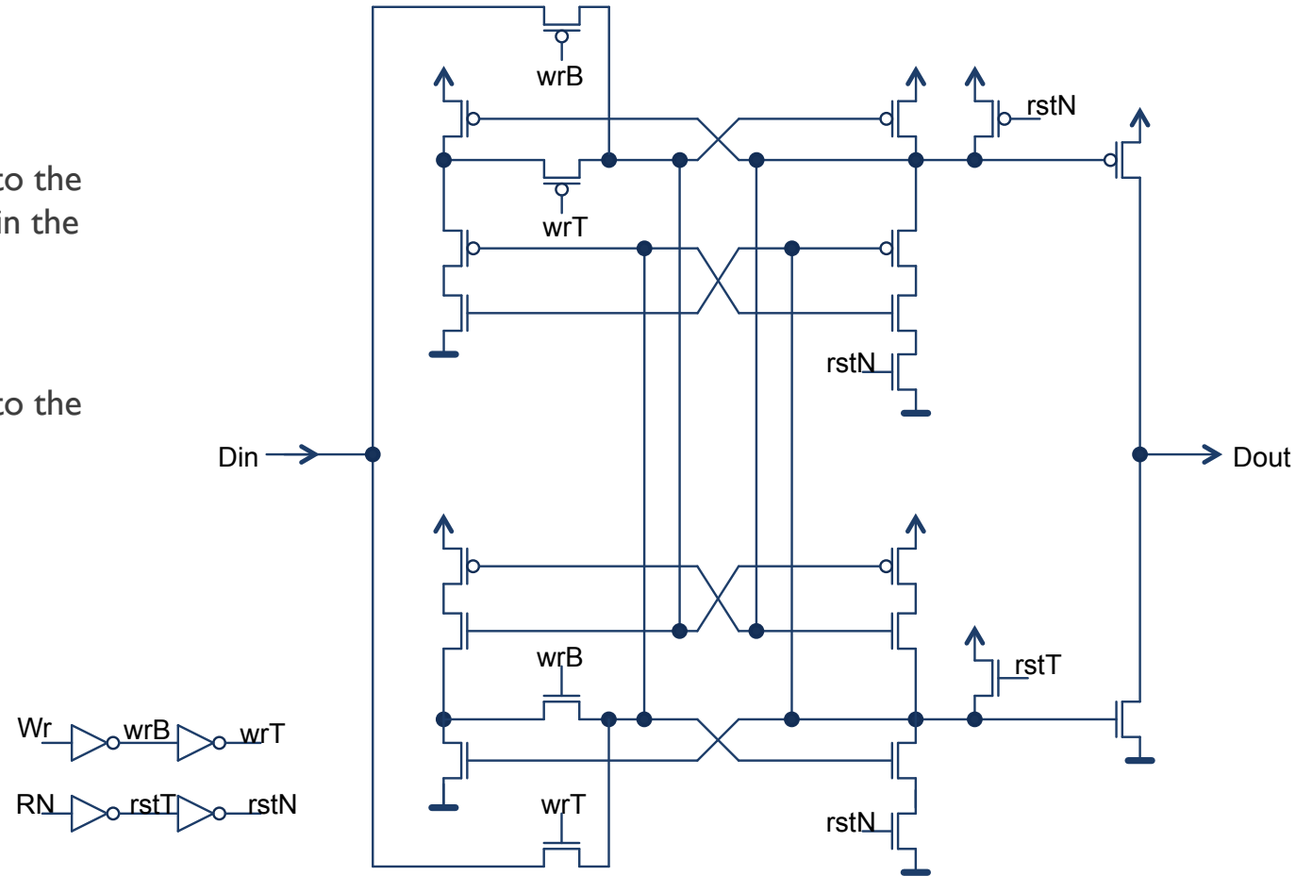
- I2C control registers implemented as Whitaker latches
  - should not be possible to corrupt the latch with an SEU
  - so why are we still seeing SEUs in the I2C registers?

CBC3 Irradiation Tests Summary

SEU Rates in I2C Registers : CBC3

- Why are we still seeing SEUs in the I2C registers?
  - RAL identified some nodes of the I2C registers that might still be sensitive to SEUs
    - Write and Reset nodes of the I2C registers

- Write (Wr)
  - Causes the storage cell to flip to the last write transaction data left in the bus
- Reset (RN)
  - Causes the storage cell to flip to the default.

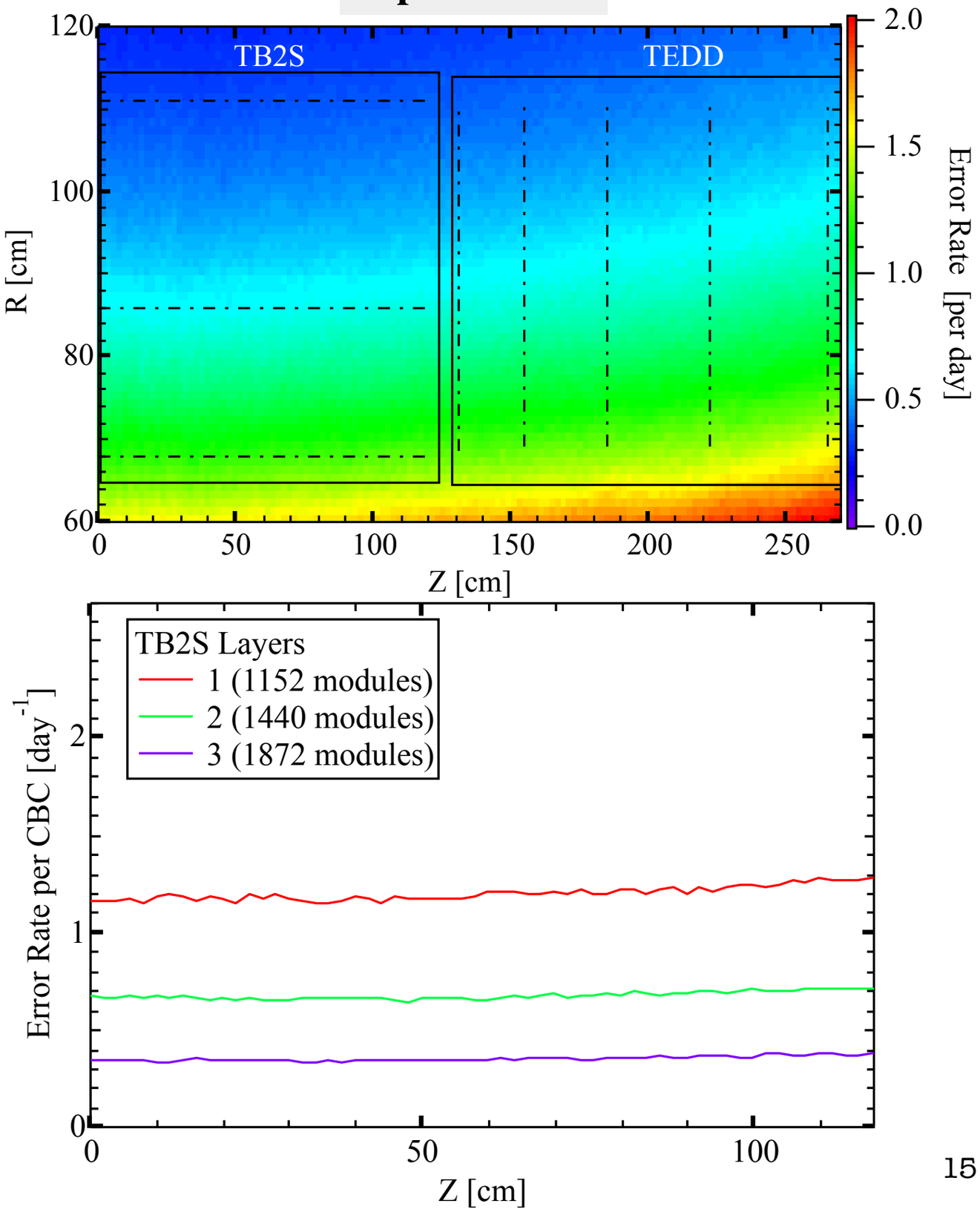


CBC3 Irradiation Tests Summary

Total SEU rate estimate for Phase-2 Outer Tracker

- Estimating SEU rate (per CBC) in the tracker barrel (TB2S) using :
  - outer tracker layout from the TDR
  - expected flux [x3] from BRIL sim.
  - measured SEU rate in I2C registers

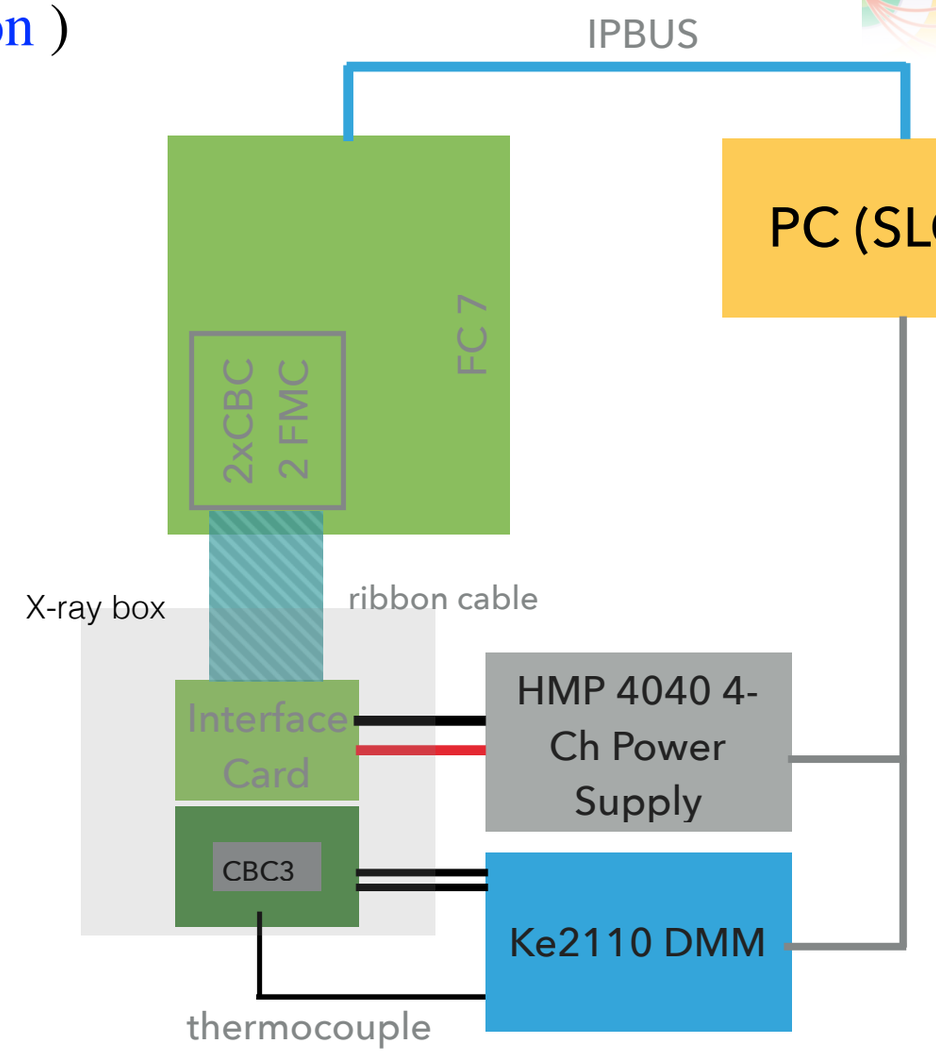
Expected number of bit flips in TB2S (1.9×10^8 I2C registers) : 2.1×10^3 per hour [error in 1.1×10^{-3} % of I2C registers per hour]

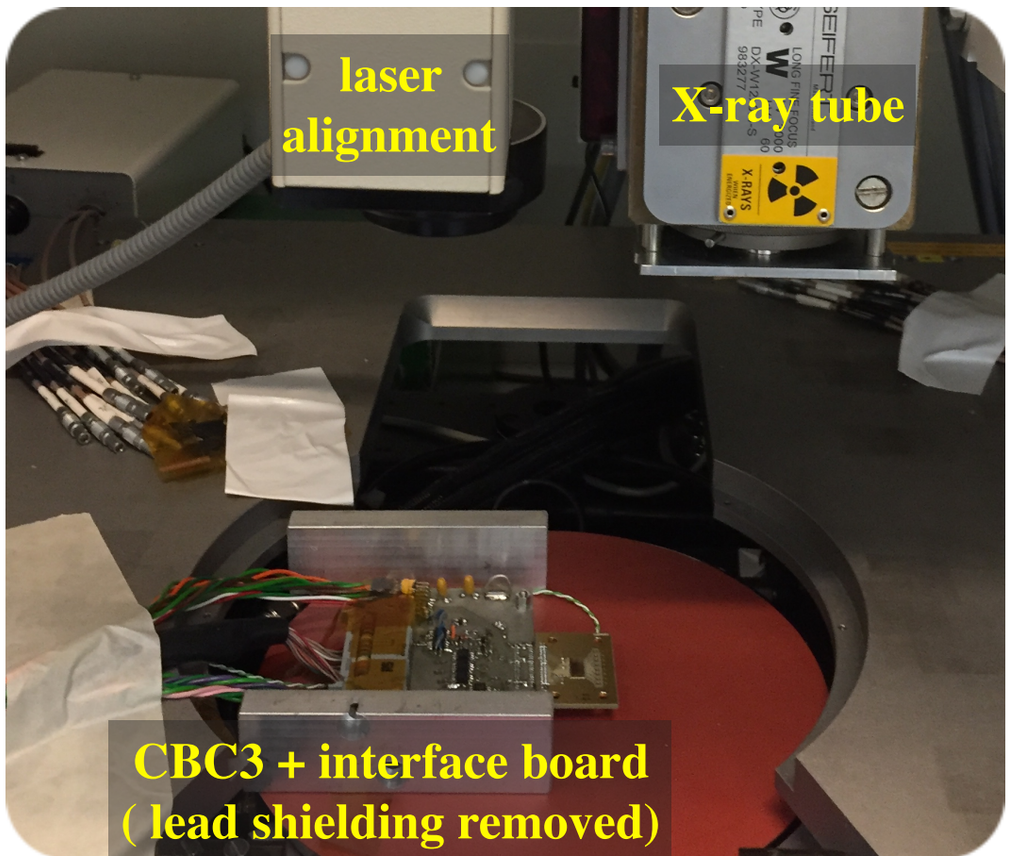


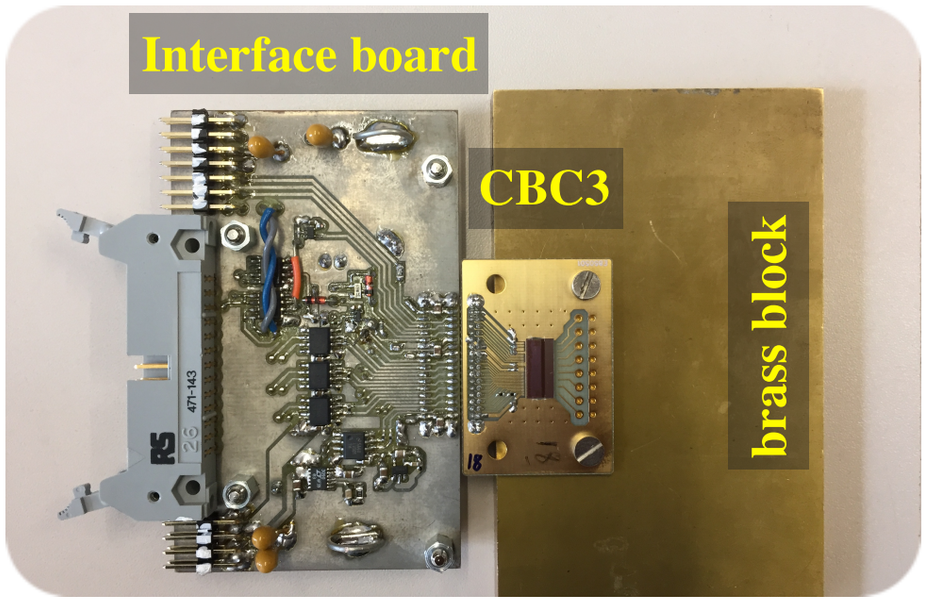
CBC3 Irradiation Tests Summary

Total Ionizing Dose Tests on the CBC3 : Test Set-Up

- More details available in May's tracker week presentation)
  - Ph2_ACF as DAQ software
  - 1.5m shielded ribbon cable allows to place FC7 outside of X-ray box
  - USB based monitoring:
    - HMP4040 4-Ch power supply for current monitoring
    - Ke2110 DMM for bias measurements & temperature monitoring





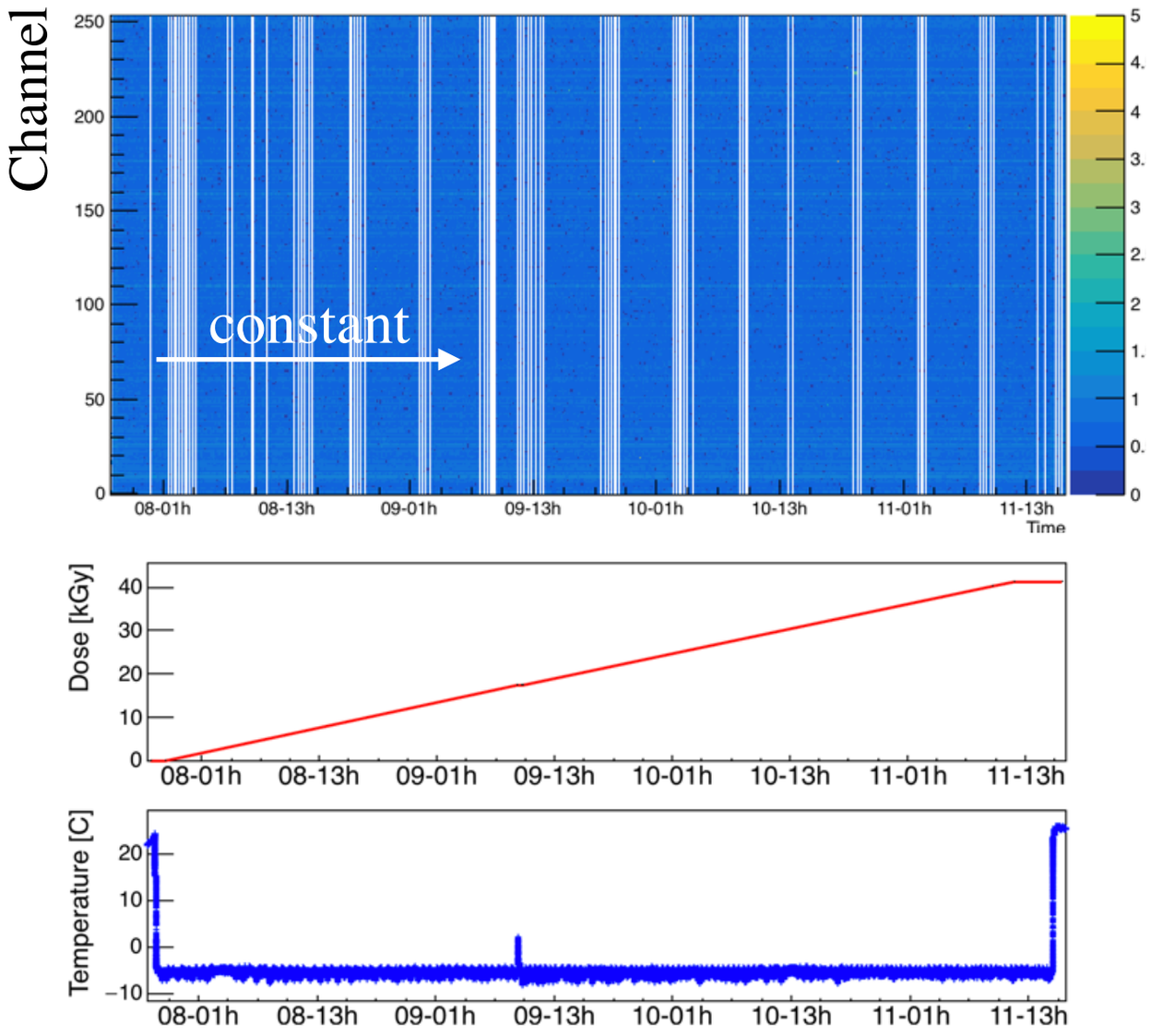


CBC3 Irradiation Tests Summary

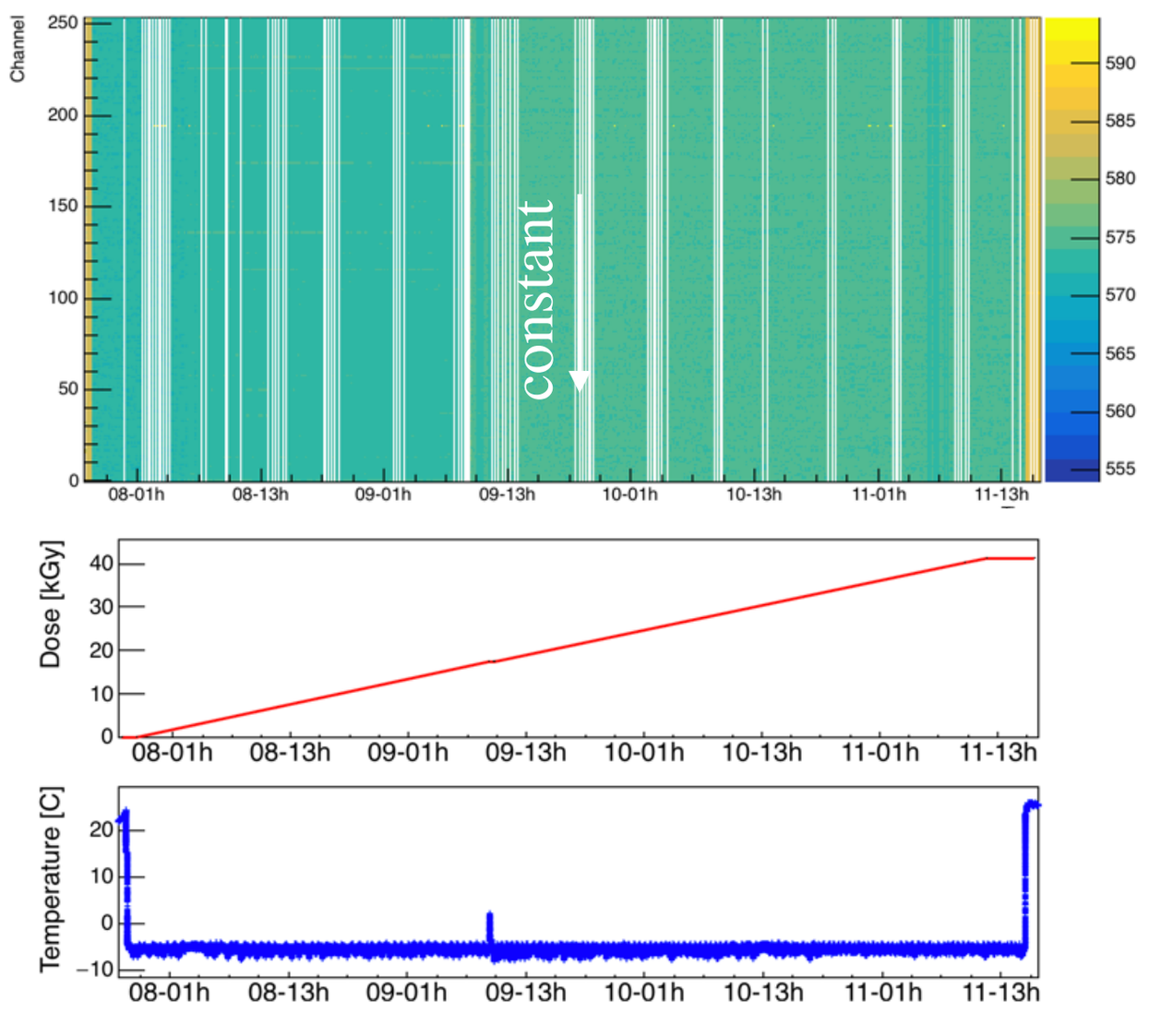
Pedestal S-curves after offset tuning : 0.1 kGy/h , -5°C , 42 kGy received dose

- Pedestal & noise not dose dependent
  - noise is constant over time and pedestals are the same across channels

Noise (V_{cth} units)



Pedestal (V_{cth} units)

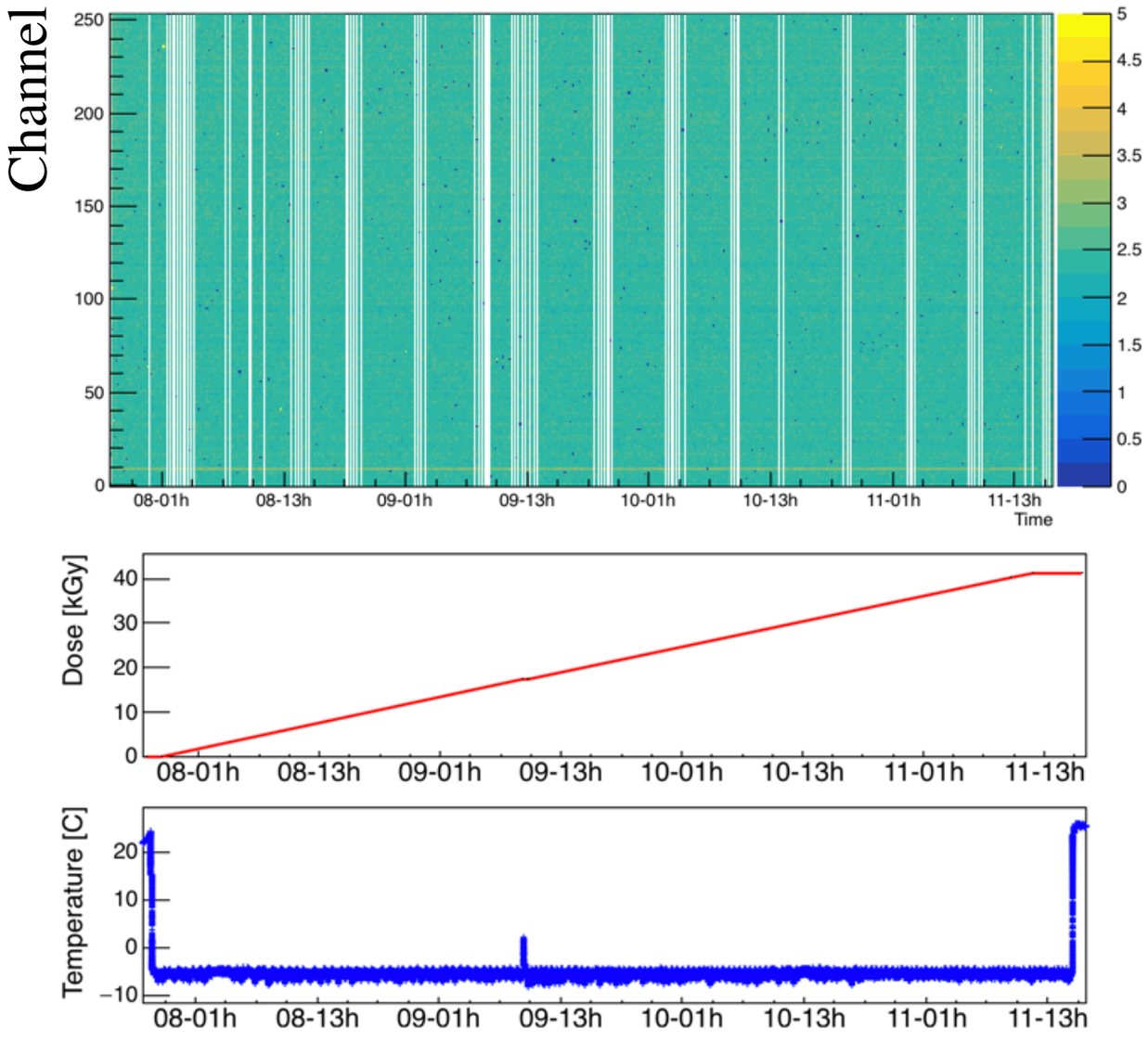


CBC3 Irradiation Tests Summary

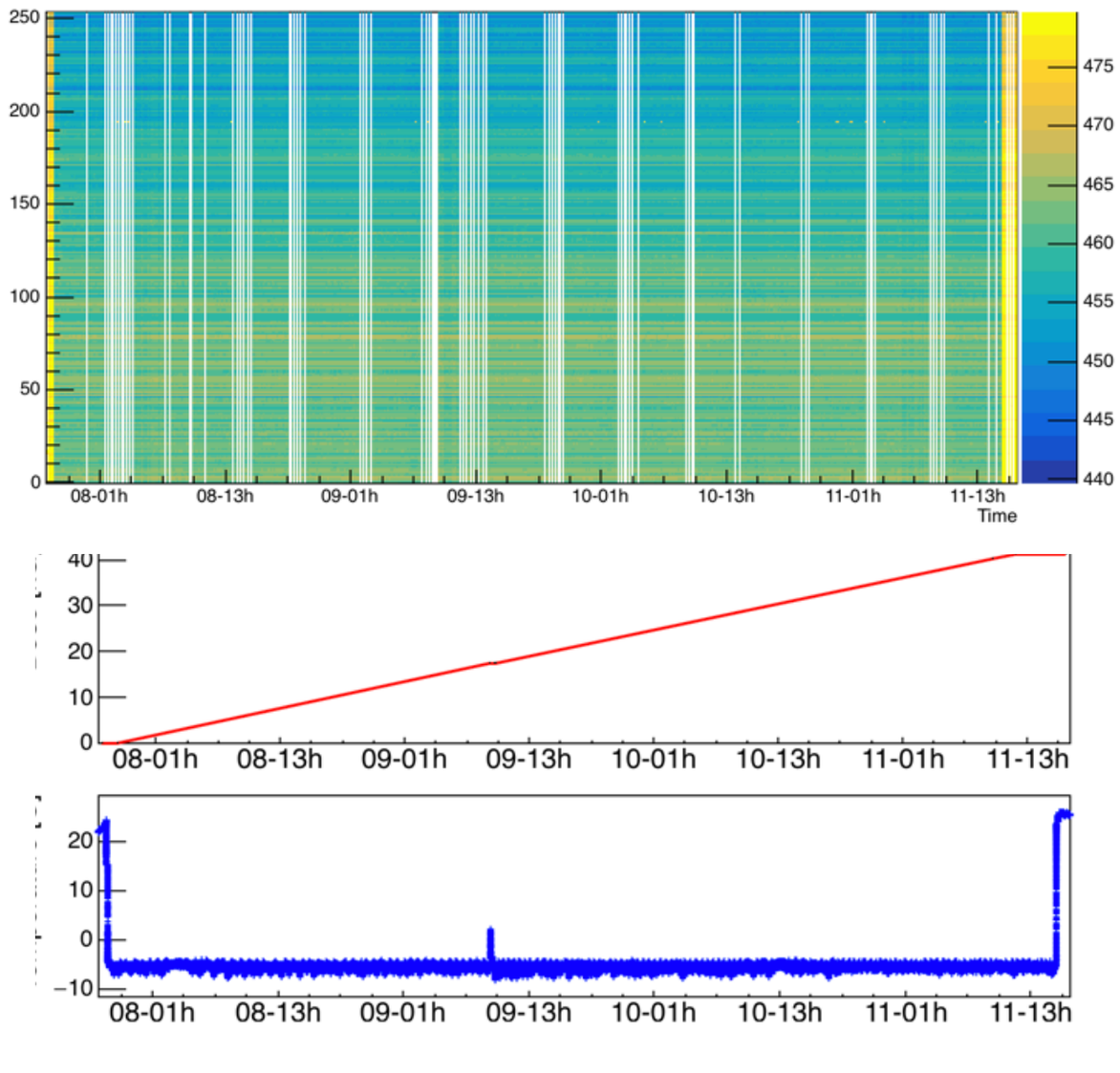
S-curves with TP amplitude of 30 DAC units : 0.1 kGy/h , -5°C , 42 kGy received dose

- Midpoint & width of S-curves not dose dependent
  - width of S-curves is pretty constant over time
  - channel to channel variations in S-curve midpoint due to channel-to-channel variations in TP

S-curve width (V_{cth} units)



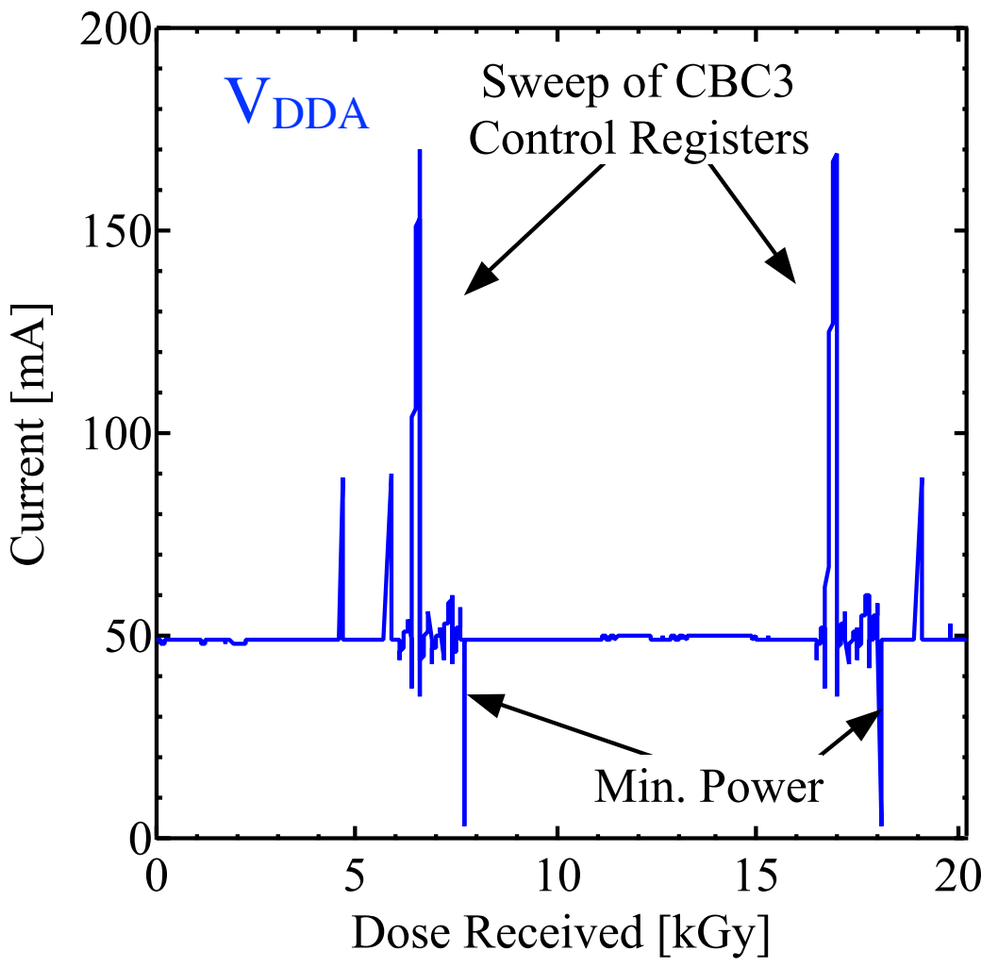
S-curve Midpoint (V_{cth} units)

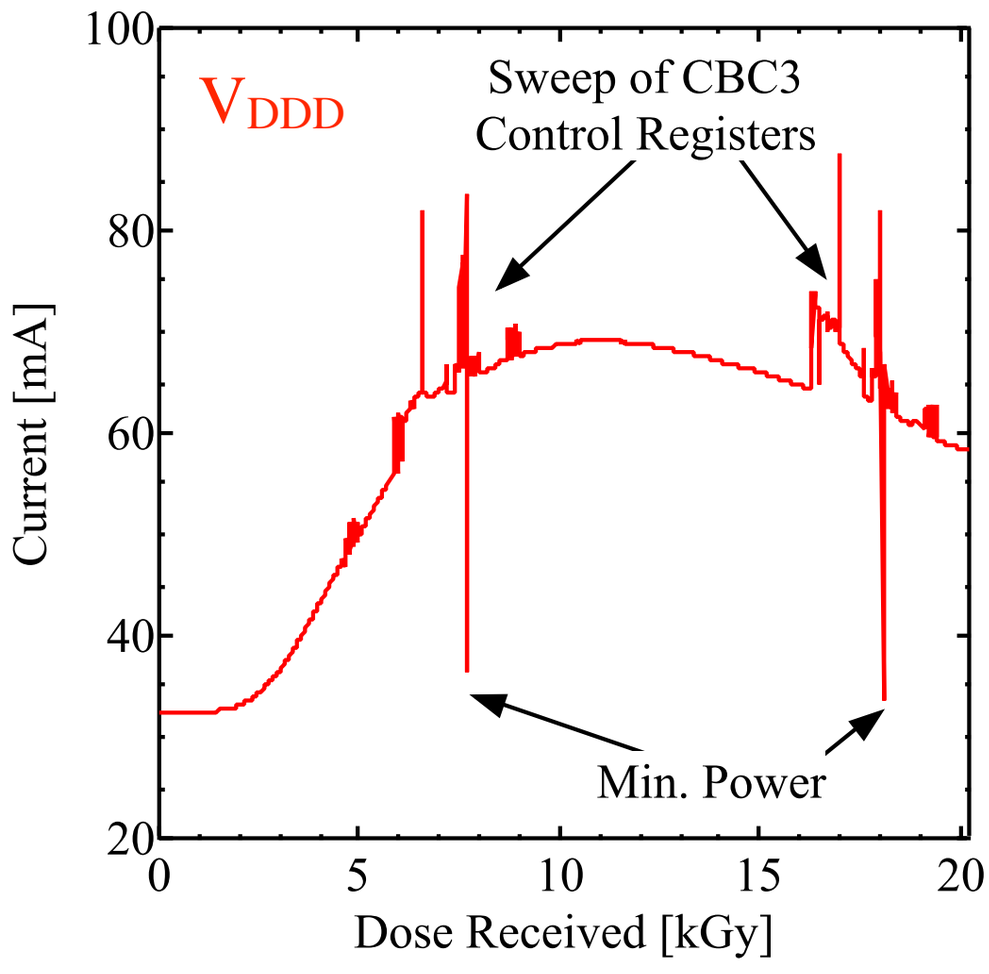


CBC3 X-ray Irradiation :

Digital Current, Un-cooled, 20 kGy/hr , max. dose of 350 kGy

- Similar effect to that observed in the CBC2 :
  - increase only present on the digital side
  - increase in the digital current observed near the start of the irradiation (dose of ~ 2.3 kGy)
  - increase saturates after about 12 kGy of TID, and begins to decrease after that





- Changes implemented in the CBC3 have improved the radiation tolerance, however :
  - radiation induced leakage still present in the ASIC

CBC3 Irradiation Tests Summary

Total Ionizing Dose Tests on the CBC3

- Dedicated effort to understand dose rate and temperature dependence of current increase to understand impact on the power consumption of a 2S module in an HL-LHC like environment
  - -15°C lowest expected temperature on CBCs
  - expected dose rate 9 Gy

thanks to Andreas Mussgiller, module WG

- first (03/2017) @ 1.20 V.
- remaining measurements @ 1.25 V.

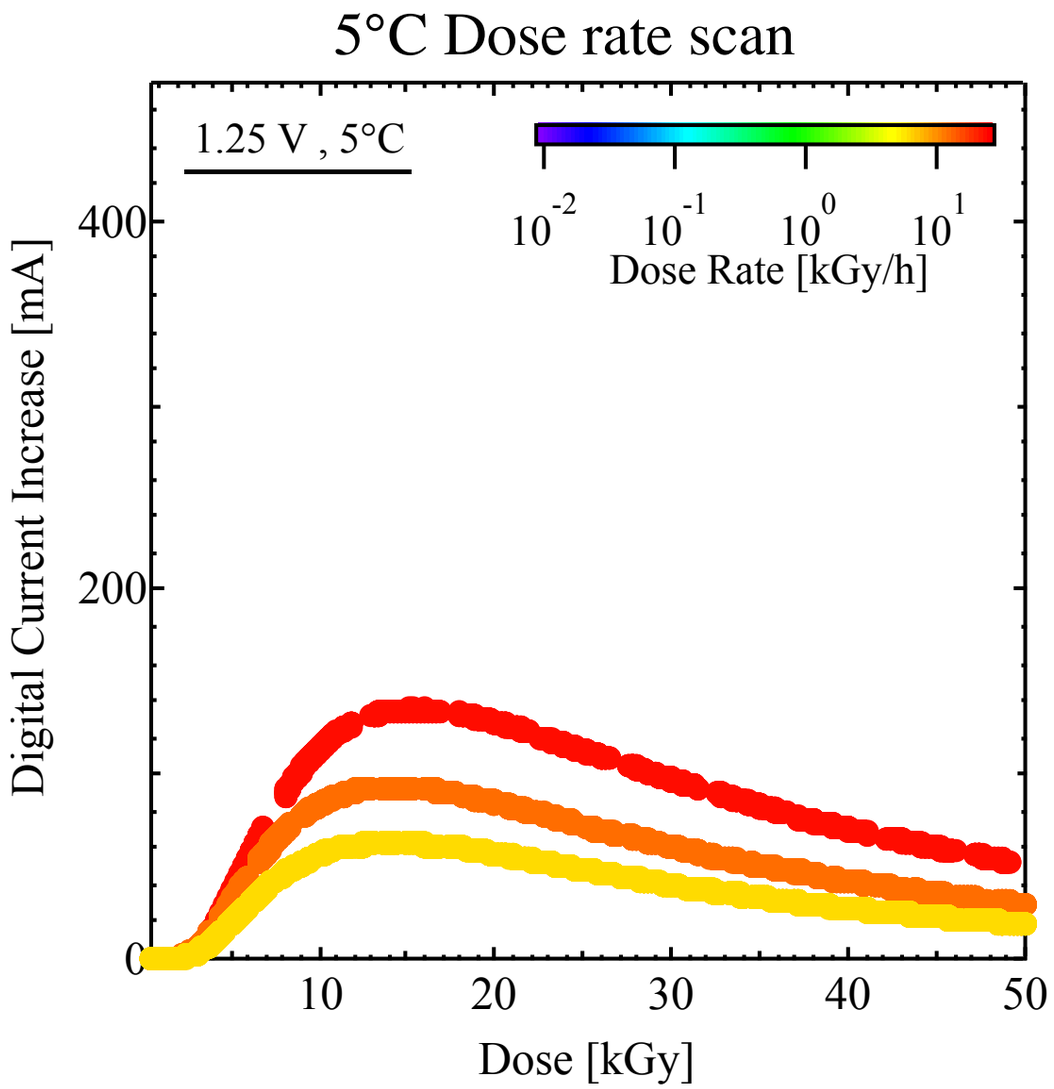
Complete list of irradiations 2017

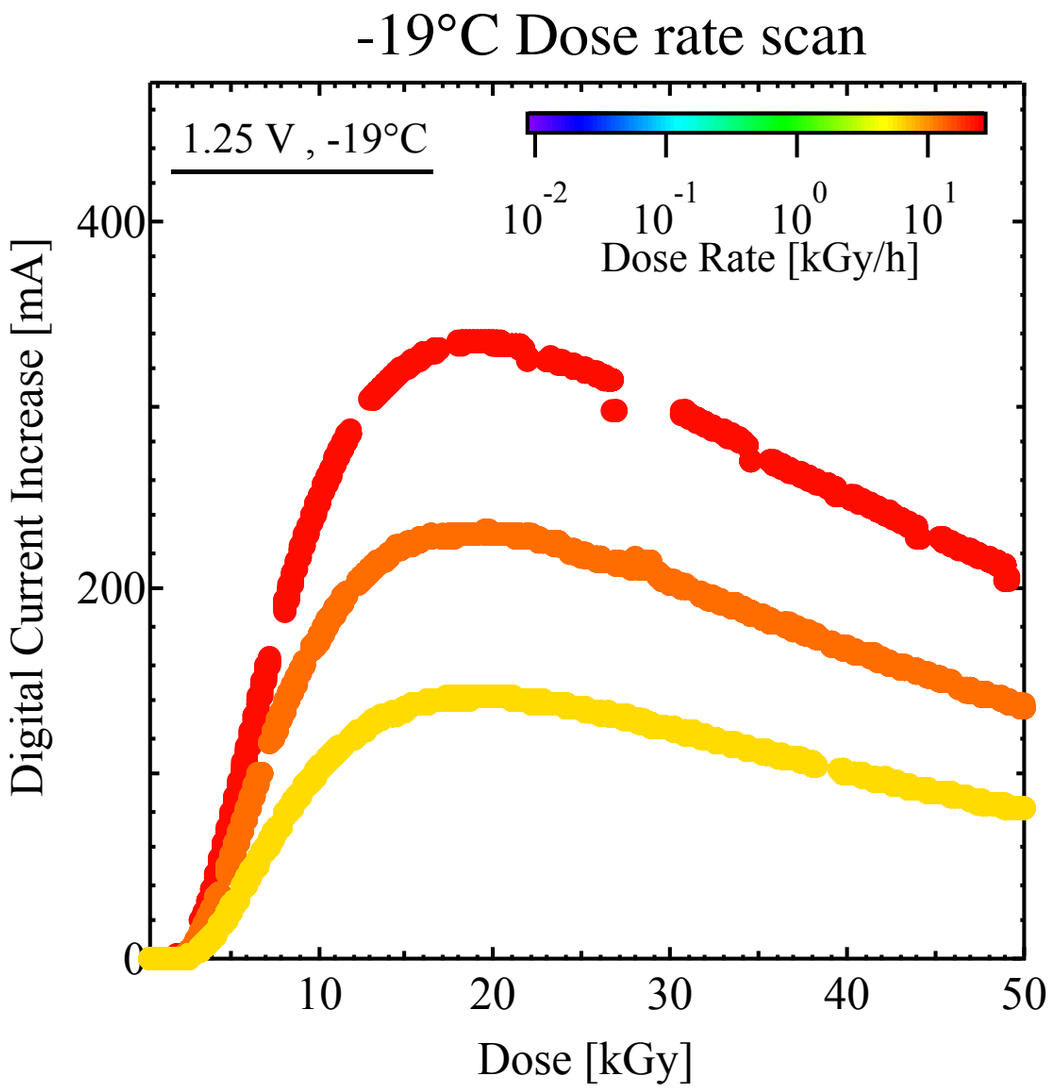
	20 [kGy/h]	10 [kGy/h]	2 [kGy/h]	5 [kGy/h]	0.1 [kGy/h]
20°	03/2017				
5°	05/2017	05/2017		05/2017	05/2017
0°				04/2017	
-5	03/2017		03/2017	04/2017	03/2017**
-20°	04/2017	04/2017		04/2017	04/2017

CBC3 Irradiation Tests Summary

Temperature and dose-rate dependence of radiation induced leakage current

- Increase in digital current at three different dose rates for two temperatures [1.25 V]



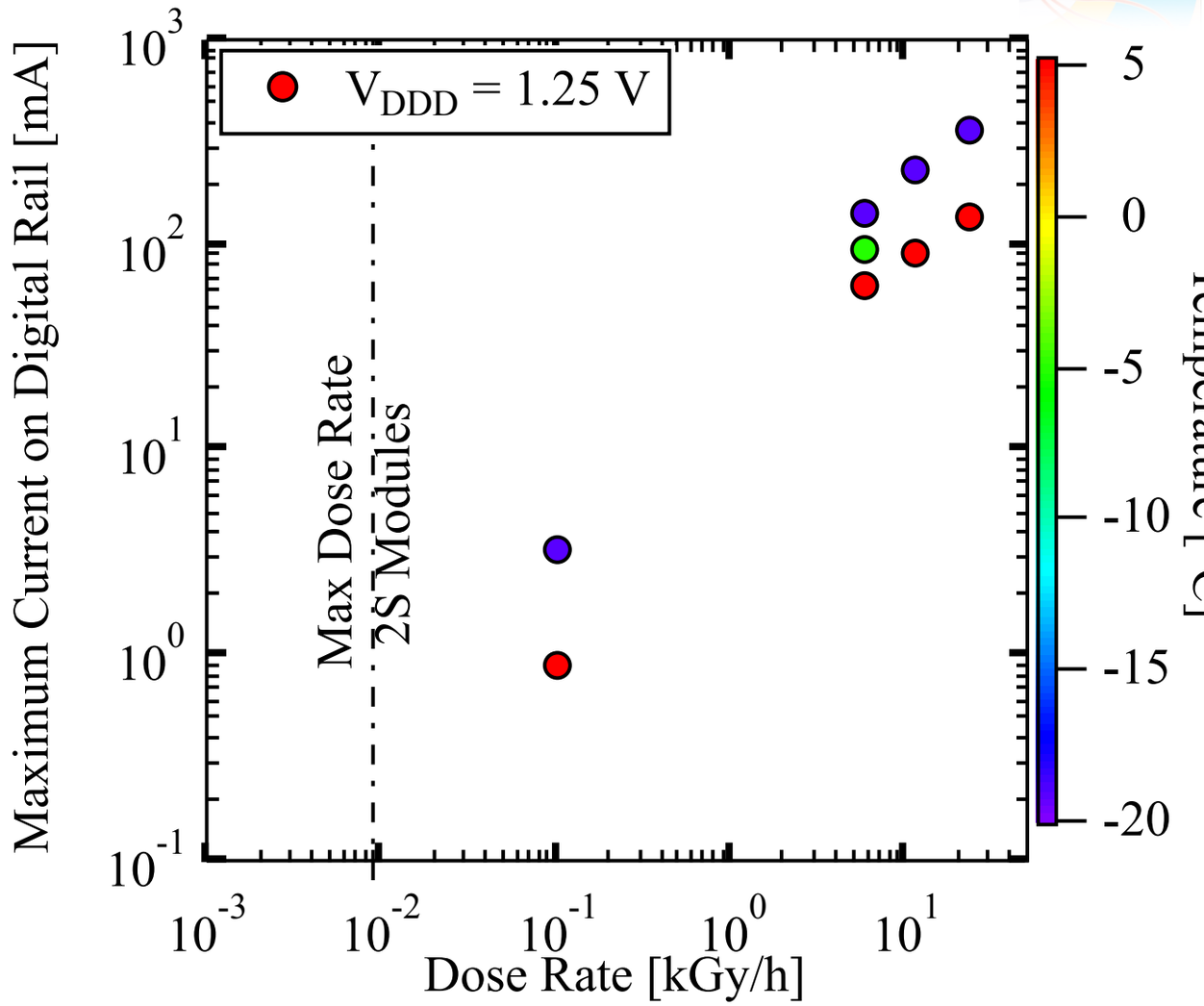


- Dose rate and temperature dependence as expected :
  - current drawn by the digital circuitry increases as the temperature decreases
  - current drawn by the digital circuitry decrease as the dose rate decreases

CBC3 Irradiation Tests Summary

Summary of CBC3 irradiation @ 1.25 V using CERN X-ray facility

- Measured (maximum) increase in current consumption on the power rail supplying V_{DDD} to the CBC3 during exposure to X-rays at :
  - maximum expected CBC3 bias
  - 4 dose rates at two temperatures
  - 3 temperatures at fixed dose rate

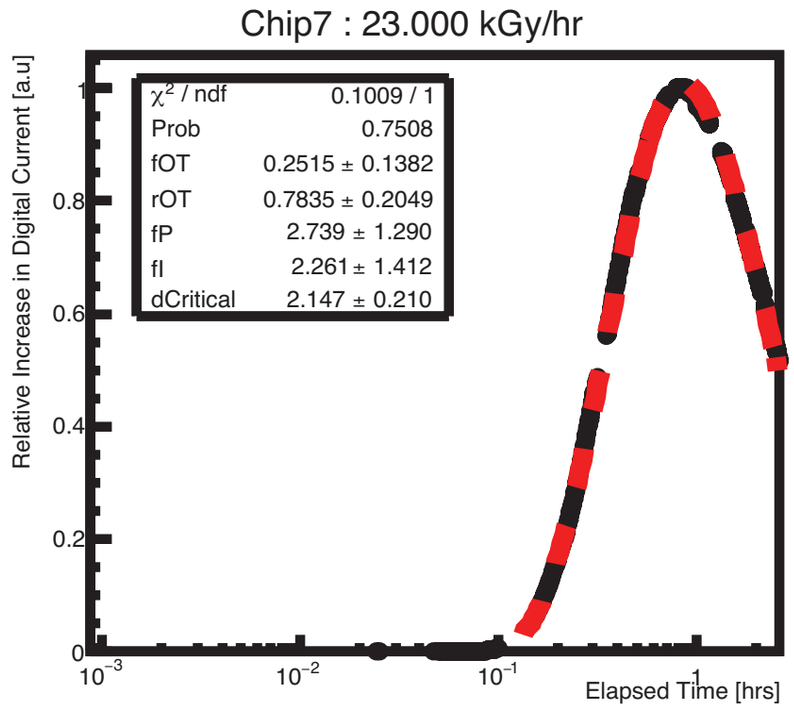


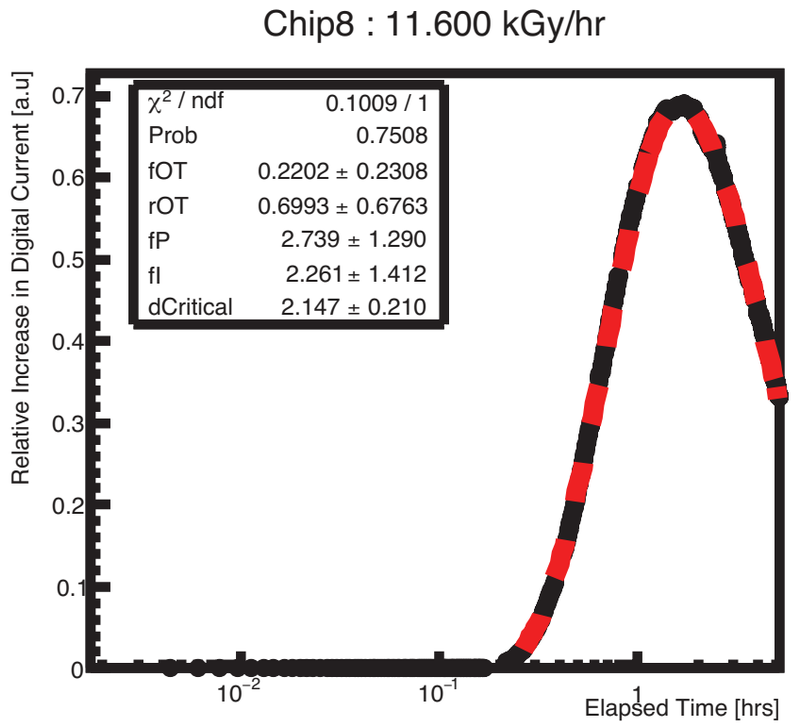
- Enough information collected to place a (conservative) upper limit on the expected magnitude of the current increase in a 2S module under HL-LHC operating conditions.
  - accomplished by fitting a mathematical model to the measured increase in current
  - model based on known radiation damage effects in CMOS (build up of fixed positive charge in the STI + creation of interface traps along the Si-SiO2 interface)
    - extension of ATLAS FeI4 damage model

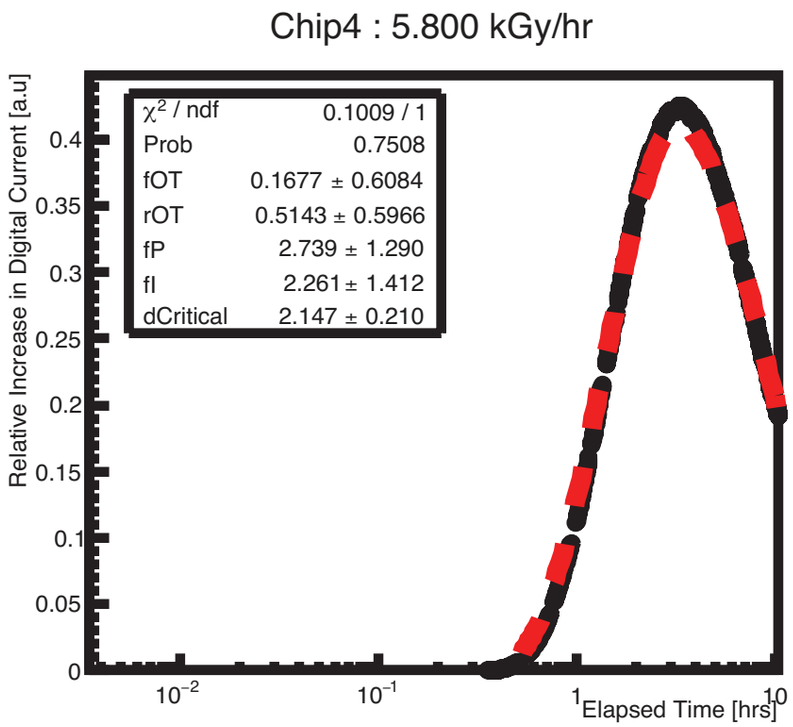
CBC3 Irradiation Tests Summary

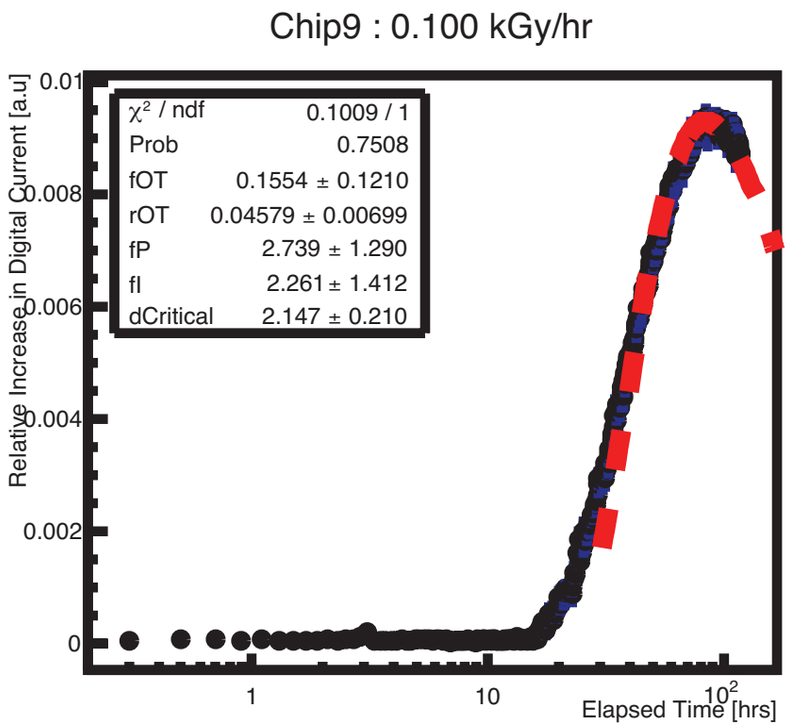
Results of combined fit to CBC3 data (-19°C)

- Simultaneously fit of current increase in all chips irradiated at -19°C





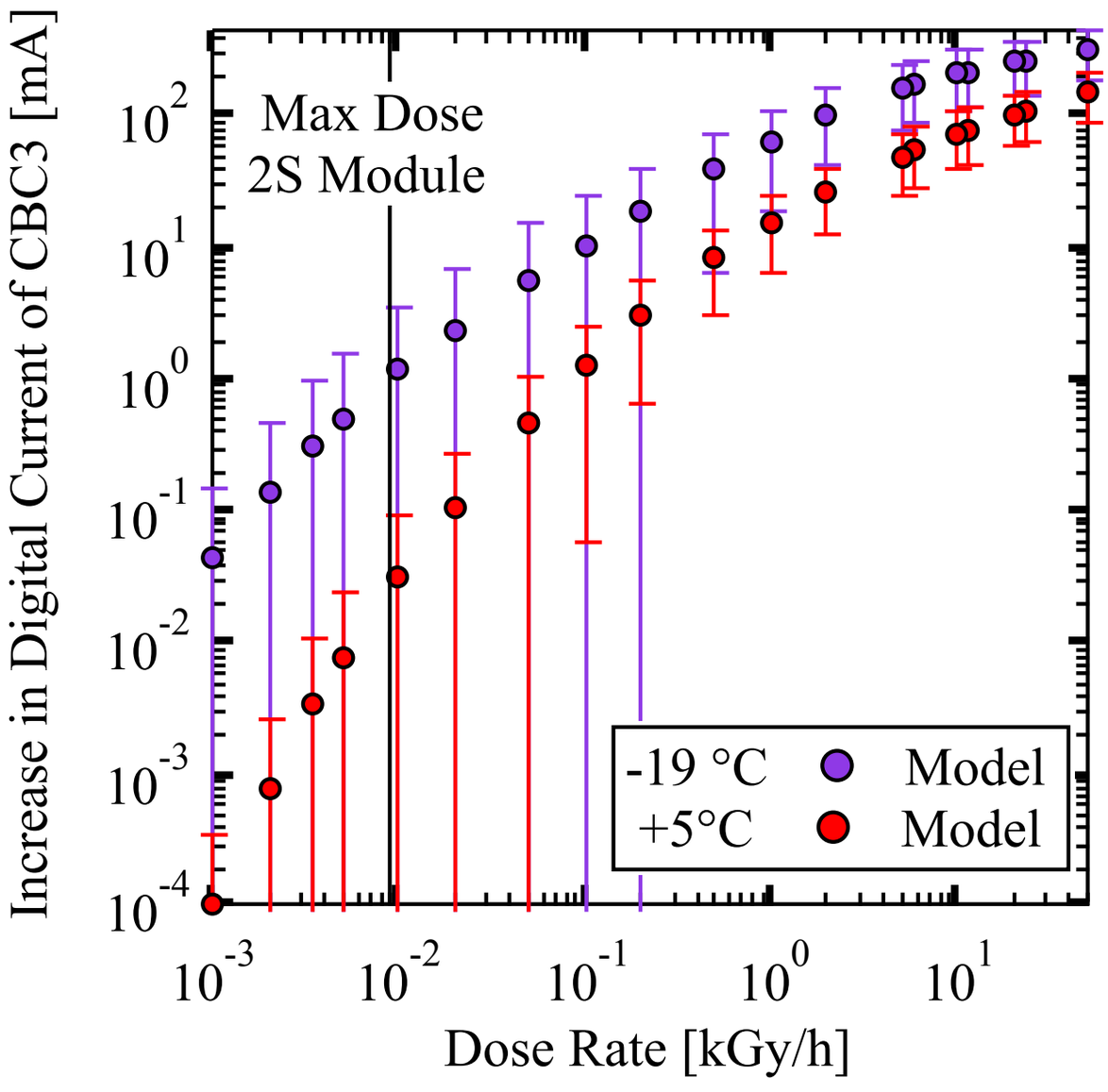




CBC3 Irradiation Tests Summary

Predicted increase in current consumption of CBC3

- Know that lowest expected temperature on the 2S modules is ~ -15°C
  - measured that the current increases with decreasing temperature
  - can use results from irradiations at -19°C and 5°C to set bounds on the expected increase per CBC for a 2S module



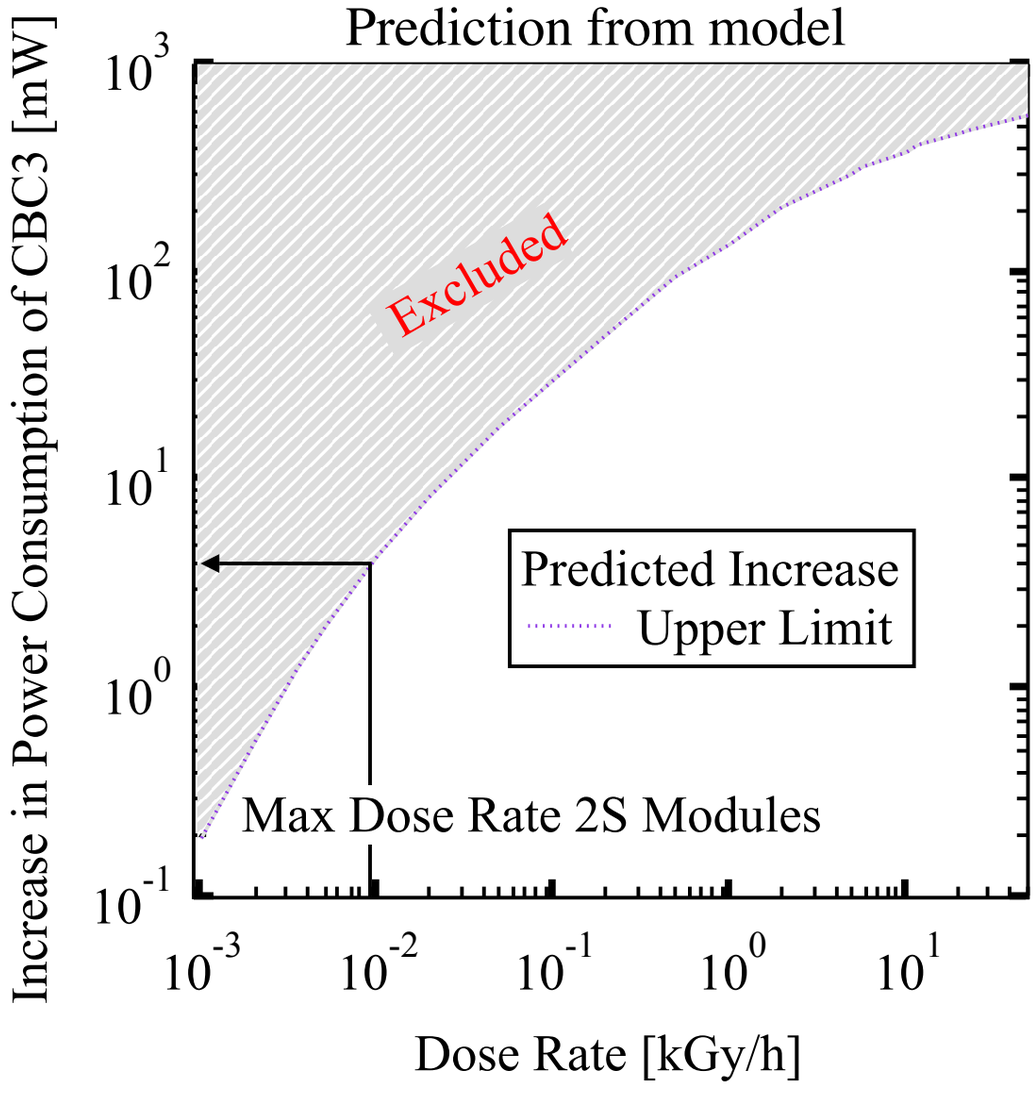
$$\Delta I_{+5°} < \Delta I_{expected} < \Delta I_{-19°}$$

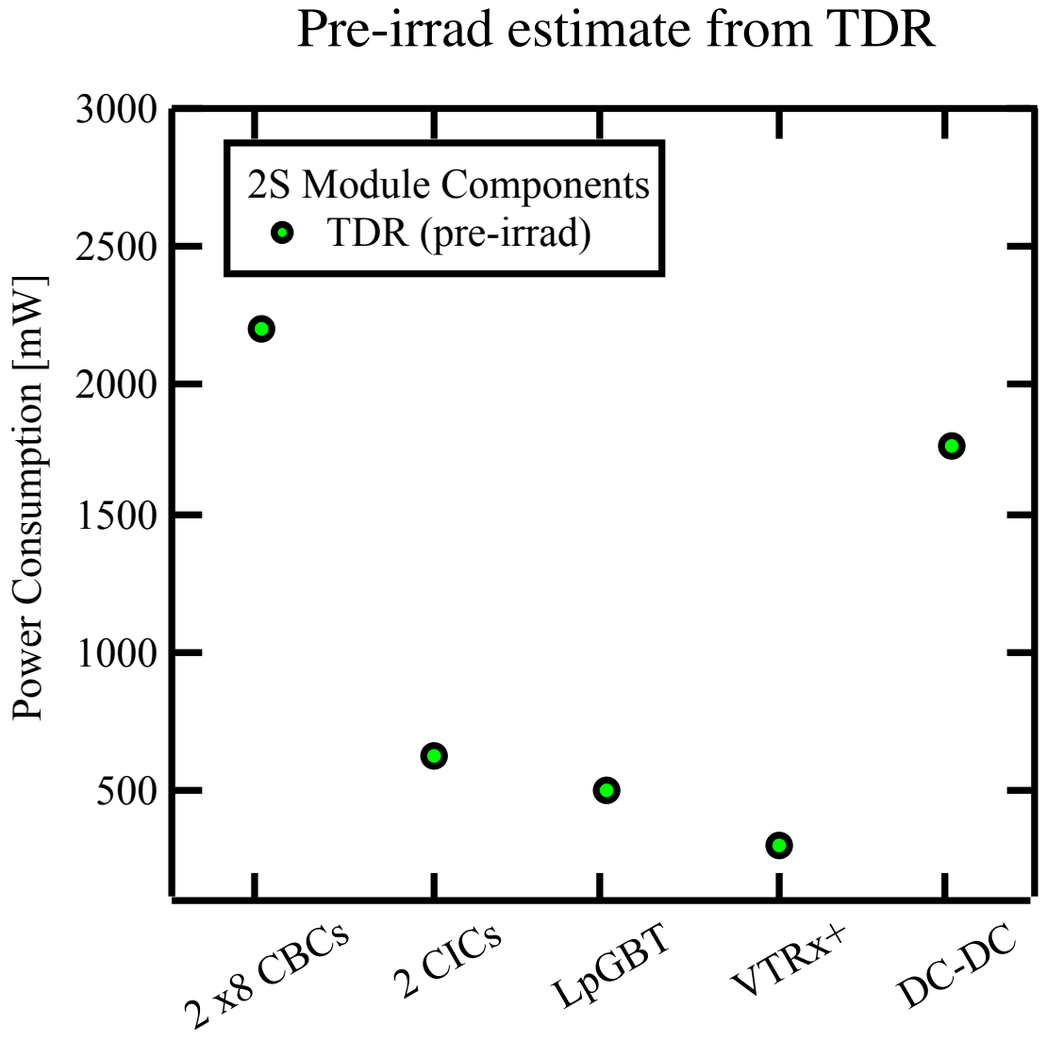
$$0.09\ mA < \Delta I_{expected} < 3.5\ mA$$

CBC3 Irradiation Tests Summary

Impact on power consumption of 2S Modules

- Want to understand the effect the expected current increase due to damage from ionizing radiation will have on the power consumption of a single 2S module
  - max. expected current increase in CBCs would increase power consumption of a 2S module by ***approximately 70 mW*** (x16 CBCs per 2S module)
    - corresponds to a ***1.3 % increase in power consumption per module***
      - 1.9 % increase if DC-DC converter is not considered



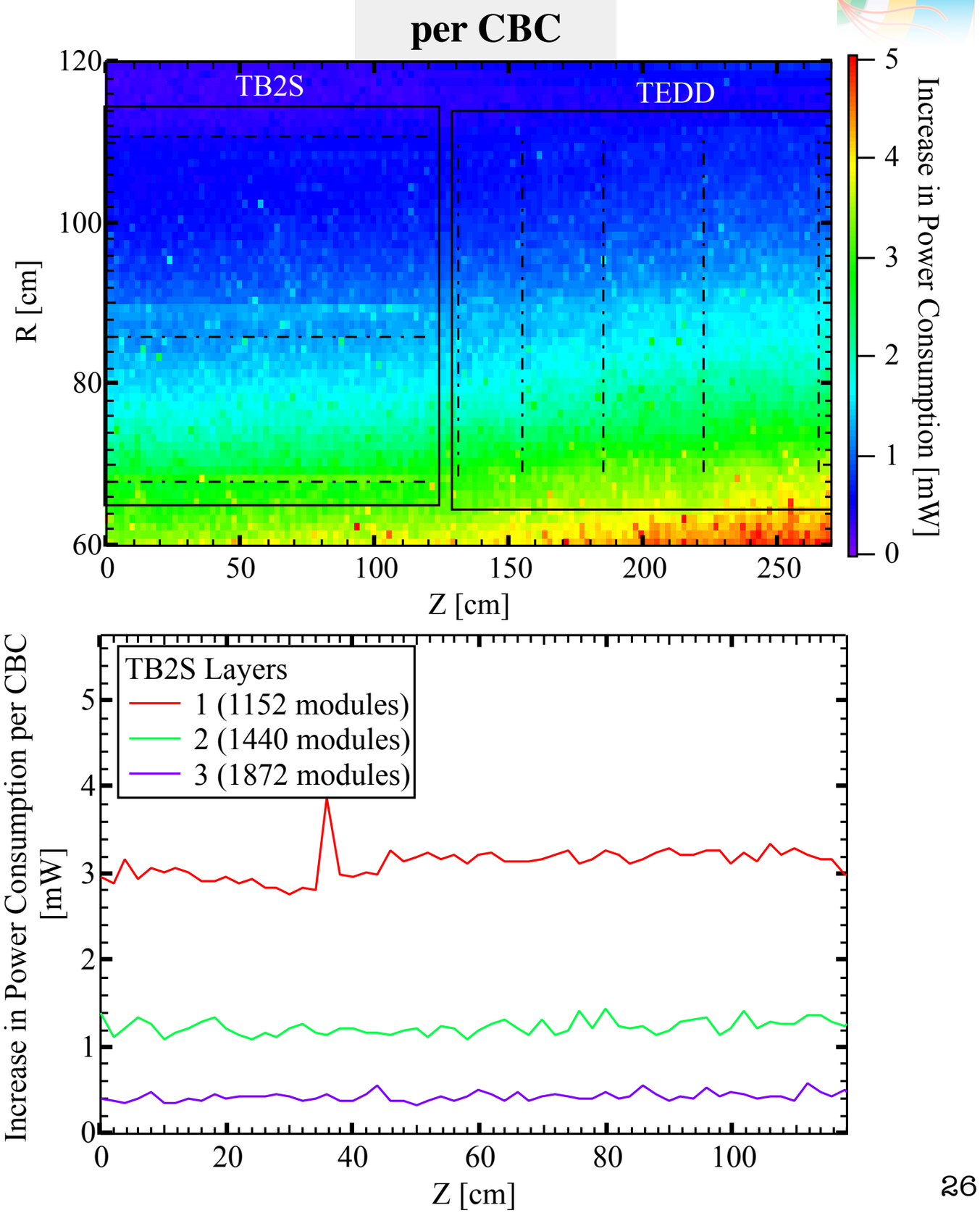


CBC3 Irradiation Tests Summary

Total Increase in power consumption for Phase-2 Outer Tracker

- Estimating increase in power consumption (per CBC) in the tracker barrel (TB2S) using :
  - outer tracker layout from the TDR
  - expected dose [x3] from BRIL sim.
  - predicted upper limit for increase from damage model

Upper limit for total increase in TB2S (consumption ~ 24 kW) :
104 W
[0.4 % increase]



CBC3 Irradiation Tests Summary

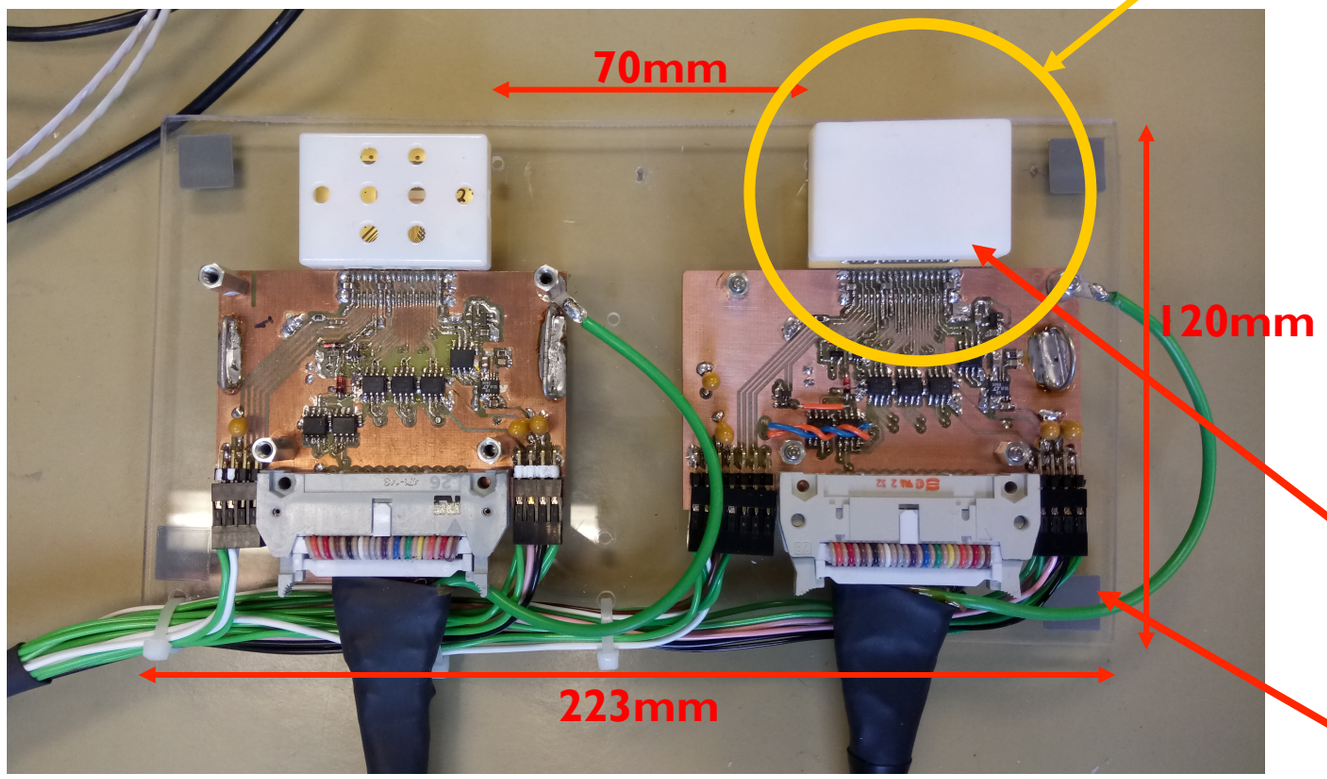
- Qualification of CBC3 (TID) for HL-LHC levels completed in first half of 2017
- Design changes (rel. to CBC2) improved the radiation hardness of the CBC3
  - parts of I2C registers still sensitive to SEUs : $\sigma_{SEU} = 2.6 \times 10^{-12}$ cm^2
    - can consider the reconfiguration of registers regularly during a run to handle error rate
    - minor modifications to CBC3 also under study if reloading the registers is not an option
  - confident that current increase measured in accelerated conditions using the CERN X-ray irradiation facility represents a worst-case scenario for the ASICs
  - expected increase on power consumption of a single 2S module due to leakage in CBC3 expected to be < 2%
    - N.B : safety factor of (x3) applied to expected dose and flux!

Back-up Slides

CBC3 Irradiation Tests Summary

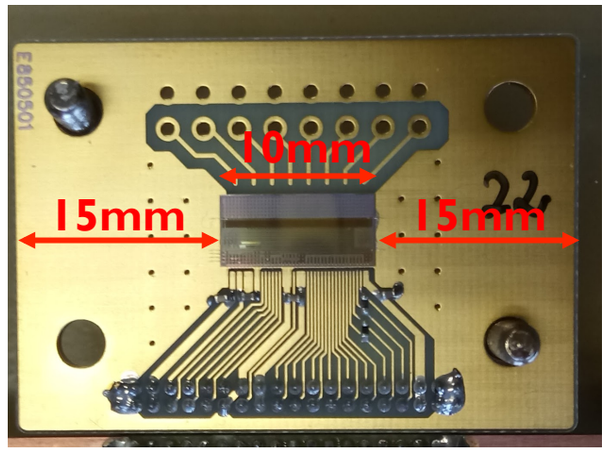
SEU Testing of the CBC3 : Test Set-Up

- 14.6 hours of beam at the LIF (more details available in May's tracker week presentation)



2 CBC3s : one centred in the beam spot, the other placed well outside

CBC3 single carrier board



These white plastic covers will be taken away during the test

3mm thick acrylic plate : 223mm x 120mm

17-07-17 4

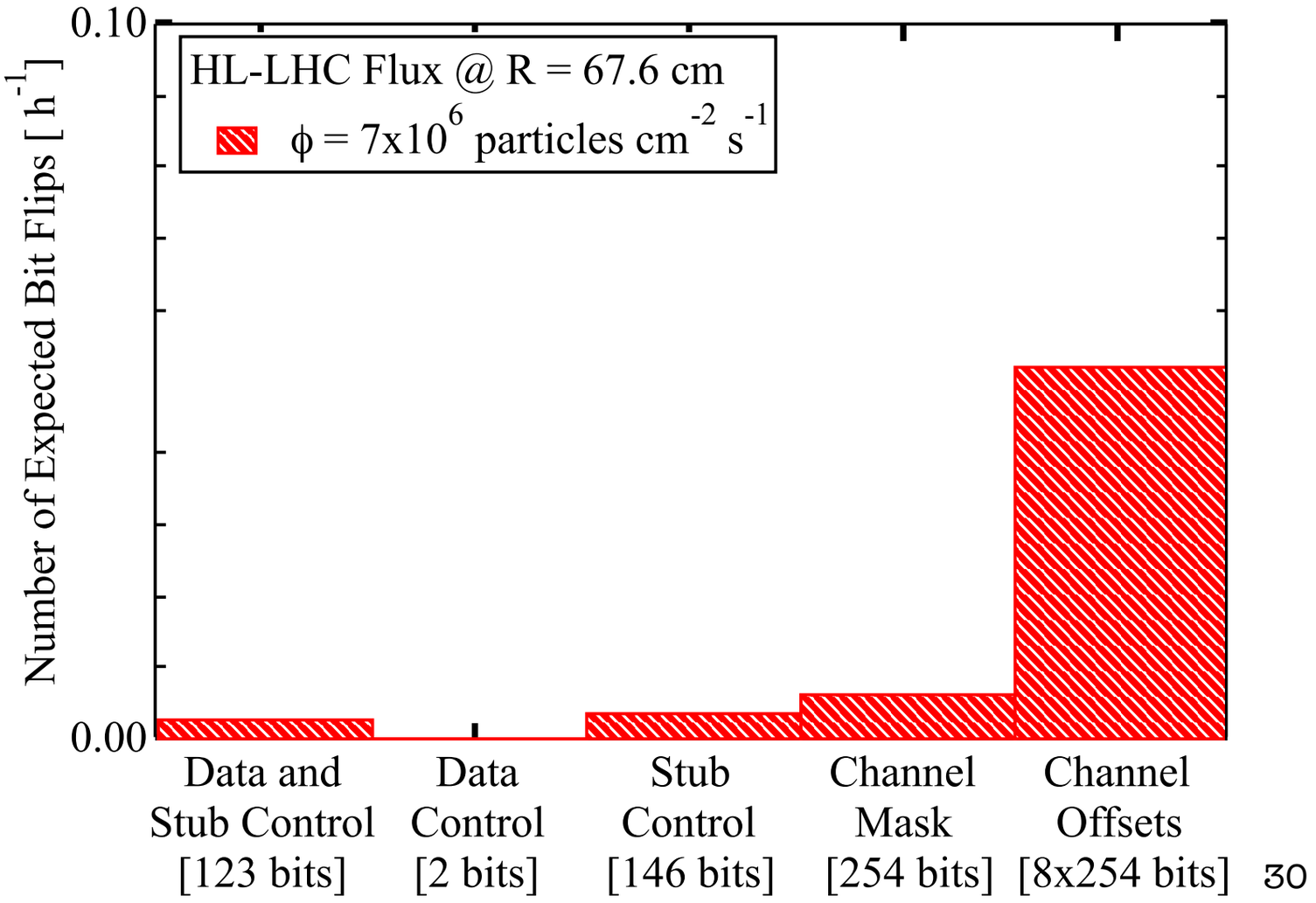
CBC3 Irradiation Tests Summary

SEU Rates in I2C Registers : Impact on HL-LHC performance

- ***Measured*** SEU cross-section using LIF data (data from one 10 minute interval) : **2.7×10^{-12} cm^2**
  - error rate expected at HL-LHC : **1.9×10^{-5} s^{-1} per chip → 0.069 h^{-1} per chip**
  - error rate expected at HL-LHC : **7.2×10^{-9} s^{-1} per I2C bit → 2.6×10^{-5} h^{-1} per I2C bit**

CBC version	# I2C bits	ϕ_{LiF} [cm^{-2} s^{-1}]	# bit flips [LIF]	σ_{SEU} [x 10^{-11} cm^{-2}]	$ER_{HL\text{-}LHC}$ [x10^{-2} bit flips/h]
3	2640	2.2E+08	0.36 ± 0.07	**0.27 ± 0.05**	6.9 ± 1.3

- Impact of error rate on data taking depends on the number of bits used to control different parts of the CBC3

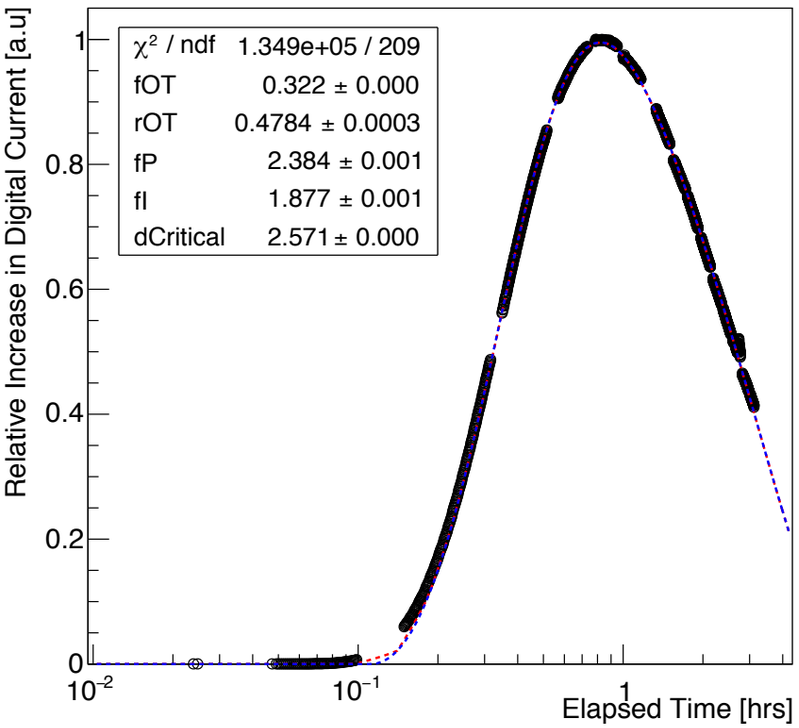


CBC3 Irradiation Tests Summary

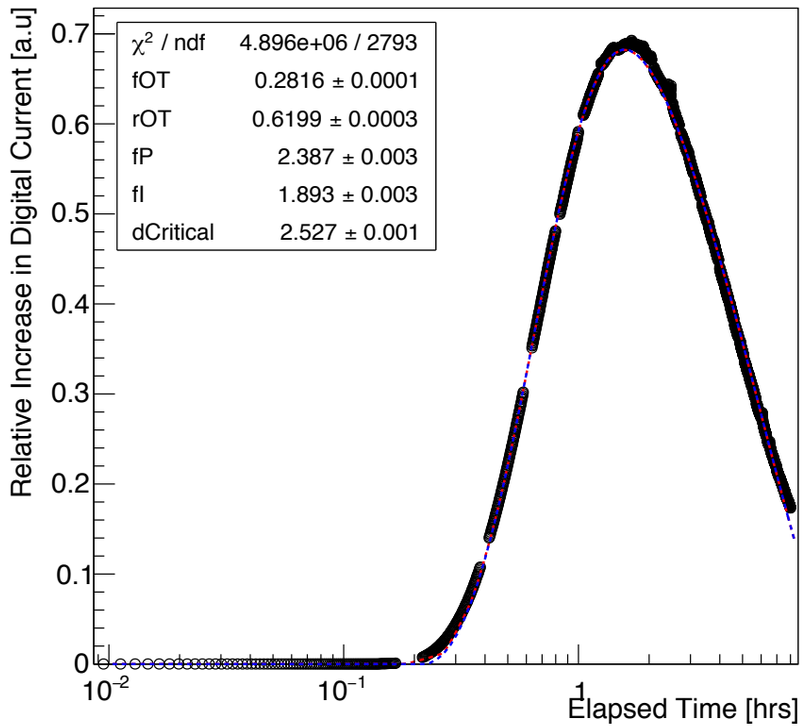
Results of fit to individual chips (-19°C)

- Modified damage model used to fit current increase for all chips irradiated at -19°C
  - can see that already with the individual fits that parameters related to the production of interface traps are not dependent on dose rate (consistent across all chips)

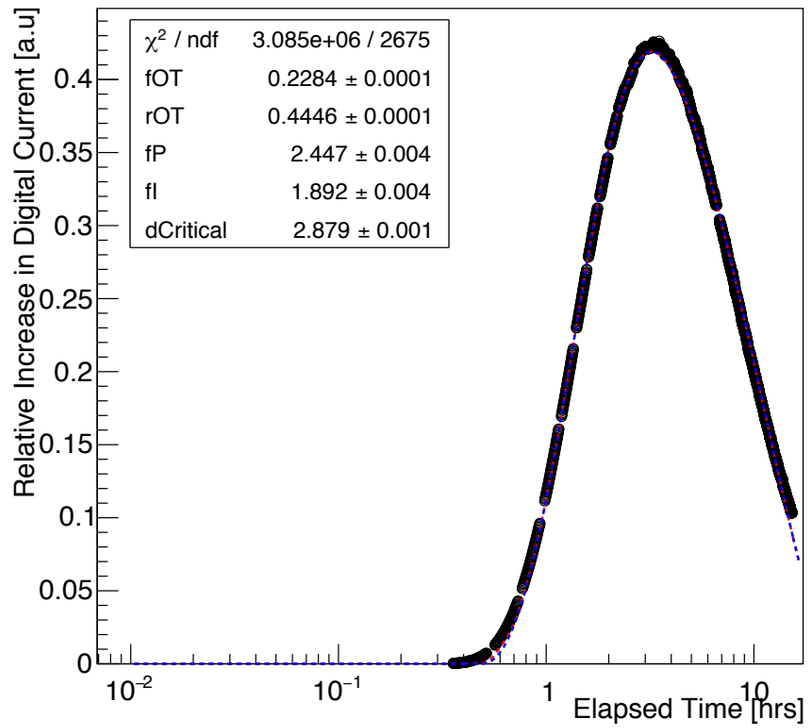
Chip7 : 23.000 kGy/hr



Chip8 : 11.600 kGy/hr



Chip4 : 5.800 kGy/hr



- Next step is to try and fit all chips simultaneously, keeping parameters related to interface trap production fixed.

CBC3 Irradiation Tests Summary

Fitting increase in current/CBC3

- Want to achieve the best possible fit for 4 curves with very different amplitudes
  - default function to minimize would be the sum of the Chi2 for the 4 curves

$$g = \sum_i \chi_i^2 \qquad \chi_i^2 = \sum_j \frac{(y_j - f(x_j))^2}{\sigma_j^2}$$

  - error (on the measured current) is the same for all 4 data sets, so can see that the value of g would be dominated by the curves with large amplitudes
  - expect the minimizing algorithm to be pretty insensitive to what is going on with the curve at the lowest dose rate.
- So instead chose to minimize the sum of the residuals of the individual curves

$$G = \sum_i R_i \qquad R_i = \sum_j \frac{|y_j - f(x_j)|}{y_j}$$

- effectively a normalization.

Bit flip details

Setting type	Page	Address	Set value	Value after bit-flip	Flipped bit	Default value	Type	Flip direction	Flipped to default	Flipped to the last write	Last write value	Last transaction
A	2	0x17	0xFF	0xFB	2	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x2D	0xFF	0xDF	5	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xC4	0xFF	0xFD	1	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x5D	0xFF	0xFD	1	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xD3	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x4F	0xFF	0xBF	6	0x80	Offset	1->0	Yes	No	0x41	Status reg. read
A	2	0x97	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x01	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x08	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xAB	0xFF	0xDF	5	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	1	0x29	0xFF	0xFD	1	0xFF	Mask channel	1->0	No	Yes	0x41	Status reg. read
A	2	0x6D	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xA6	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xAB	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
B	1	0x1B	0x04	0x00	2	0x00	Layer swap & CW	1->0	Yes	Yes	0x41	Status reg. read
B	2	0x37	0x00	0x80	7	0x80	Offset	0->1	Yes	No	0x41	Status reg. read
C	2	0xC8	0x0F	0x0E	0	0x80	Offset	1->0	Yes	No	0x41	Status reg. read
C	2	0xEF	0x0F	0x0B	2	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
C	2	0xDC	0x0F	0x0D	1	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
C	2	0xFA	0x0F	0x07	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0x99	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0xDA	0x7F	0x3F	6	0x80	Offset	1->0	Yes	No	0x41	Status reg. read
D	2	0xE6	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0xA0	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0xA4	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
Total									24	21		

The last written value is 0x41 to the front end control register to read the status register (this was checked periodically in the test).

SOLUTIONS TO THE SEU RATE @ HL-LHC IN I2C REGISTERS

- No design change

  Reconfiguration of I2C registers regularly during a run. I2C register reconfiguration could be done without disturbing the data taking.
  It takes 158 ms to reconfigure all registers in a module (330 registers / chip x 16 chips x 30us = 158ms)

  - All modules could be reconfigured in ~158 ms, if all done at the same time.
    Once per hour with pausing the run is even realistic.
  - All modules could be reconfigured in 20 mins, if do one at a time (7500 modules).
    Without pausing the run. Even if the reconfiguration disturbs the data taking, ~0.013 % of data are affected.

- Minor modifications under study if reloading the registers is not an option
  - RAL has identified some nodes that are vulnerable to SEU.

ERRORS ON DATA FOR 10.7 HOURS (1.4 FOR PIPELINE LOGIC TEST)

Data taken with 1 kHz trigger to check pipeline logic, synchronization of the two chips, chip error, stub & hit information.

- Errors on CBC in beam
  - 1 hit (0 expected) at 17:03 (15/05)
  - 1 hit (0 expected) at 18:01 (15/05)
  - Stubs are found (0 expected) at 23:00 (15/05) until the end of the run at 23:25 (15/05)
    (*bit flip on the cluster width setting on i2c register happened during 22:58 to 23:03 (15/05)*)
  - Error on slvs5 at 09:38 (16/05)
- Errors on CBC out of beam
  - Error on slvs5 at 08:56 (16/05) L1A counter did not match with the other CBC after this.
  - 6 hits were found (0 expected) at 12:11 (16/05)
  - sync lost bit was set in i2c register at 15:52 (16/05). Fixed by a fast reset at 15:56 (16/05)

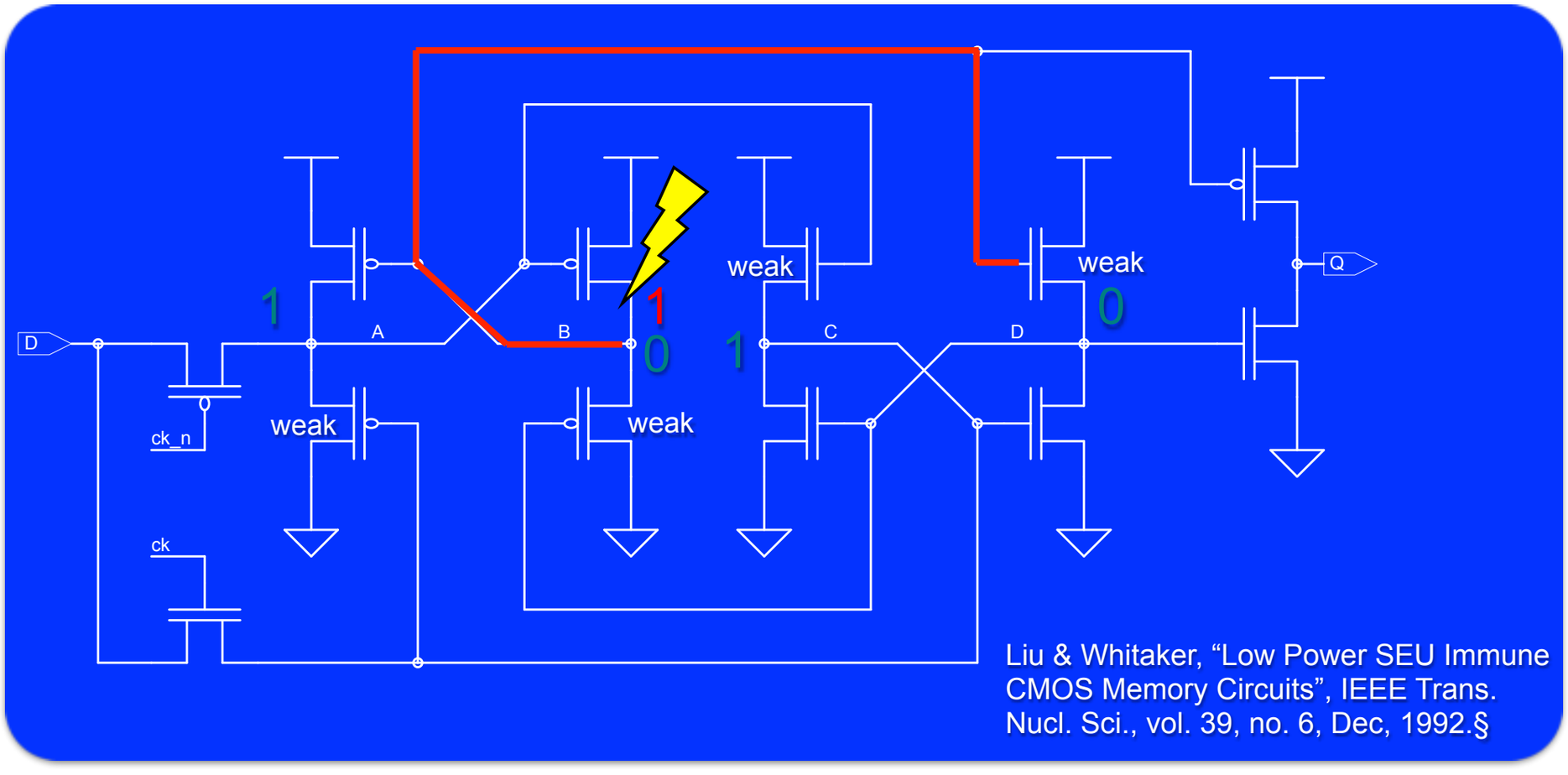
All the observed errors on CBC in beam were also seen on CBC off beam except for the stub error due to I2C register bit flip.

Pipeline logic error upper limit at HL-LHC : 5.9×10^{-6} sec^{-1}/chip

CBC3 Irradiation Tests Summary

Whitaker Latch

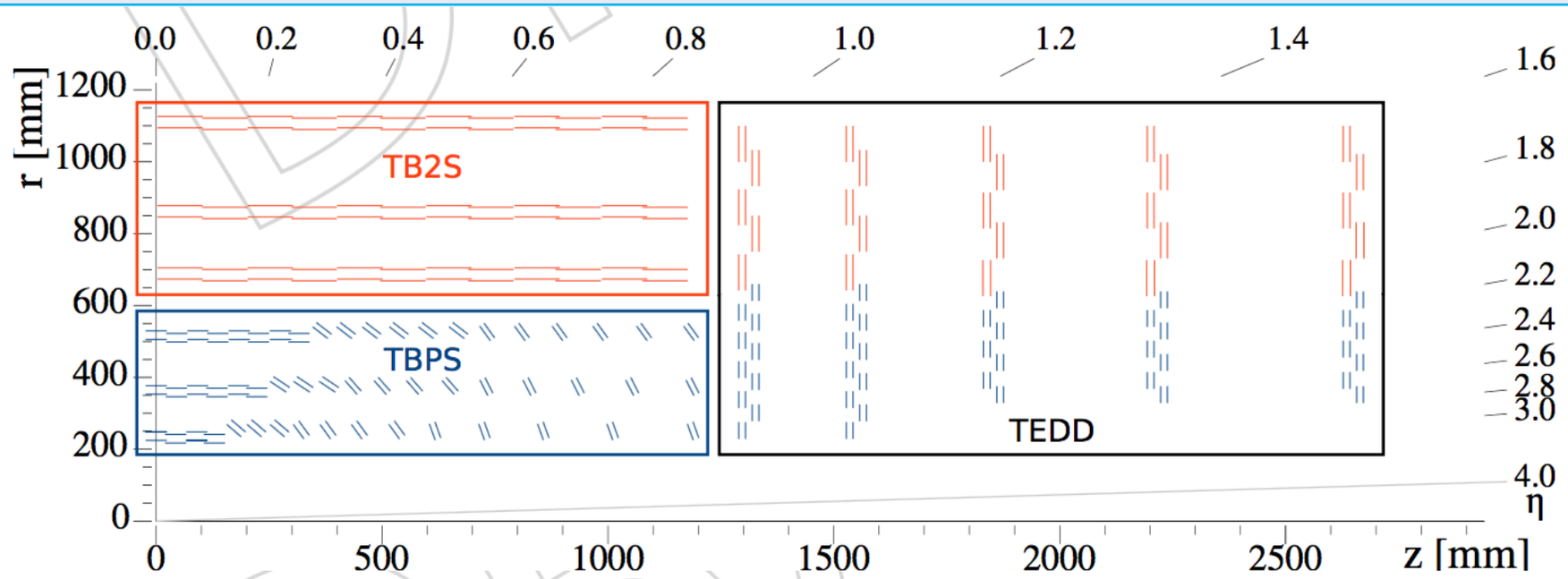
- Whitaker latches
  - n+ diffusions used to store 0's (since an SEU can only change their state from 1→ 0)
  - p+ diffusions used to store 1's (since an SEU can only change their state from 0 → 1)



Liu & Whitaker, "Low Power SEU Immune CMOS Memory Circuits", IEEE Trans. Nucl. Sci., vol. 39, no. 6, Dec, 1992.§

CBC3 Irradiation Tests Summary

Information on tracker layout from TDR



TBPS						
Layer	1	2	3			
Average radius [mm]	248.1	371.7	522.7			
z coverage [mm]	±1203.1	±1203.5	±1201.8	**Total**		
N_{planks}	18	26	36	**TBPS**		
N_{modules}	558	910	1 404	**2 872**		
TB2S						
Layer	1	2	3			
Average radius [mm]	687.0	860.0	1108.0			
z coverage [mm]	±1176.6	±1176.6	±1176.6	**Total**		
N_{ladders}	48	60	78	**TB2S**		
N_{modules}	1 152	1 440	1 872	**4 464**		
TEDD						
Double-disc	1	2	3	4	5	
Average z position [mm]	±1311.8	±1550.0	±1853.4	±2216.2	±2650.0	**Total**
N_{rings}	15	15	12	12	12	**TEDD**
N_{modules} (per z side)	644	644	564	564	564	**5 960**