CBC3 design review

RAL – June 2016

analogue front end
LDO

history(1)

CBC(1)

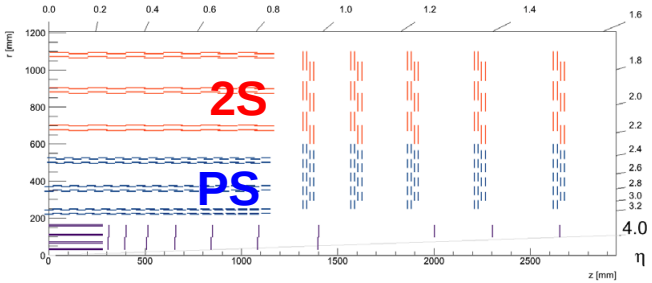
128 channels, wirebond, no triggering features, originally expected to be used for 2.5cm strips
wafers received January 2010
worked ok, a few issues
- VPAFB needed external decoupling to achieve CM stability
  - done differently for CBC2
- VCTH affected by comparator with external hysteresis
  - CBC2 comparator uses internal hysteresis
- bandgap output susceptible to VDDD noise
  - big RC filter added for CBC2

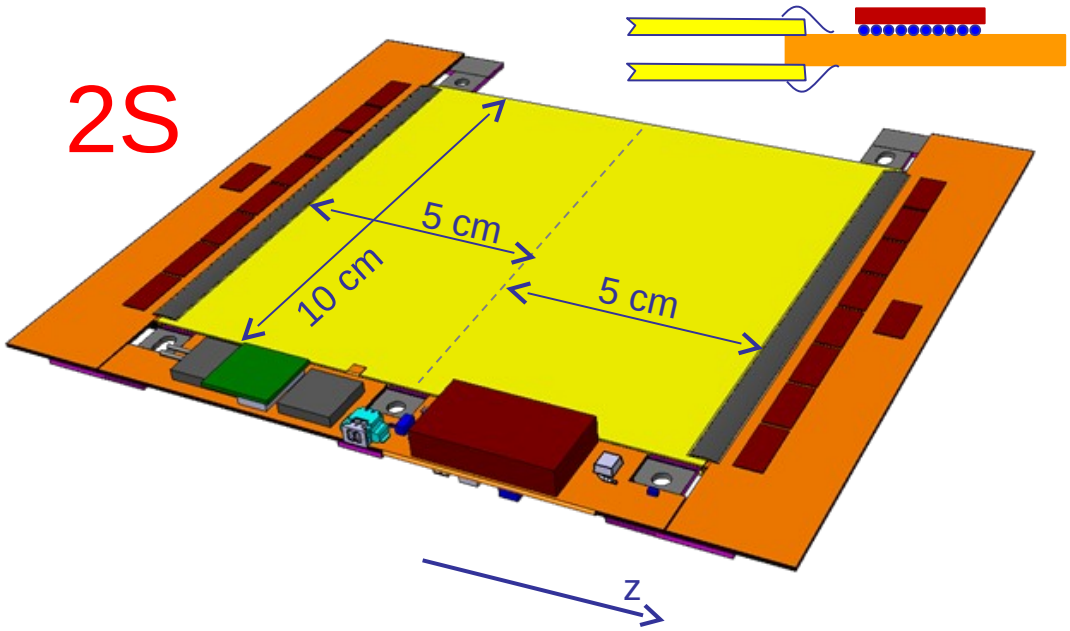
CBC2

254 channels, bump-bond
simple triggering features
- channel mask, CWD, offset correction and correlation
- single output indicates presence of positive correlation

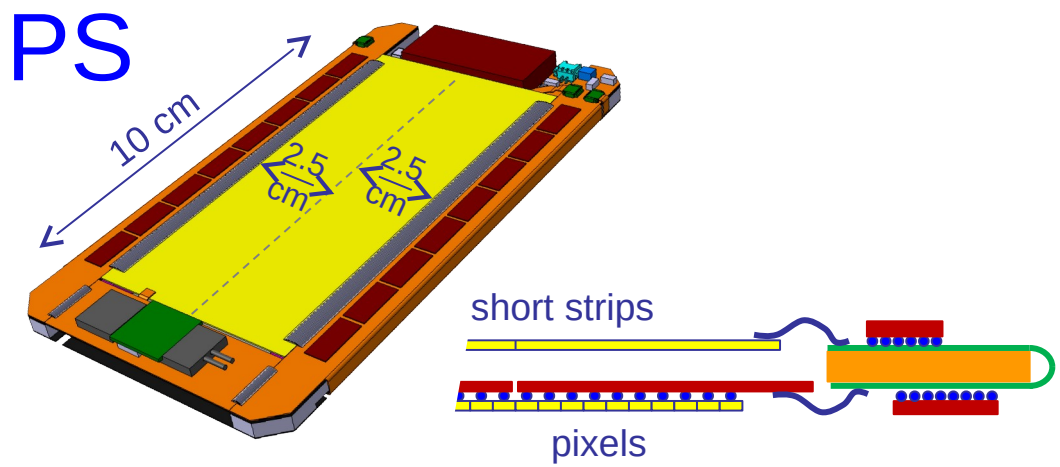
single-ended external signals (nothing faster than 40 MHz)
wafers received January 2013

Outer tracker region: p_T modules



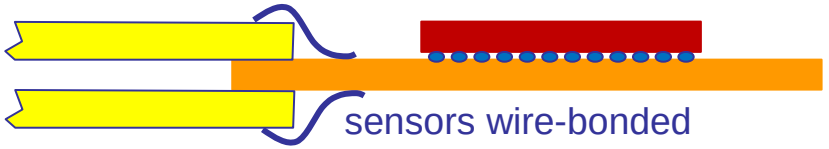


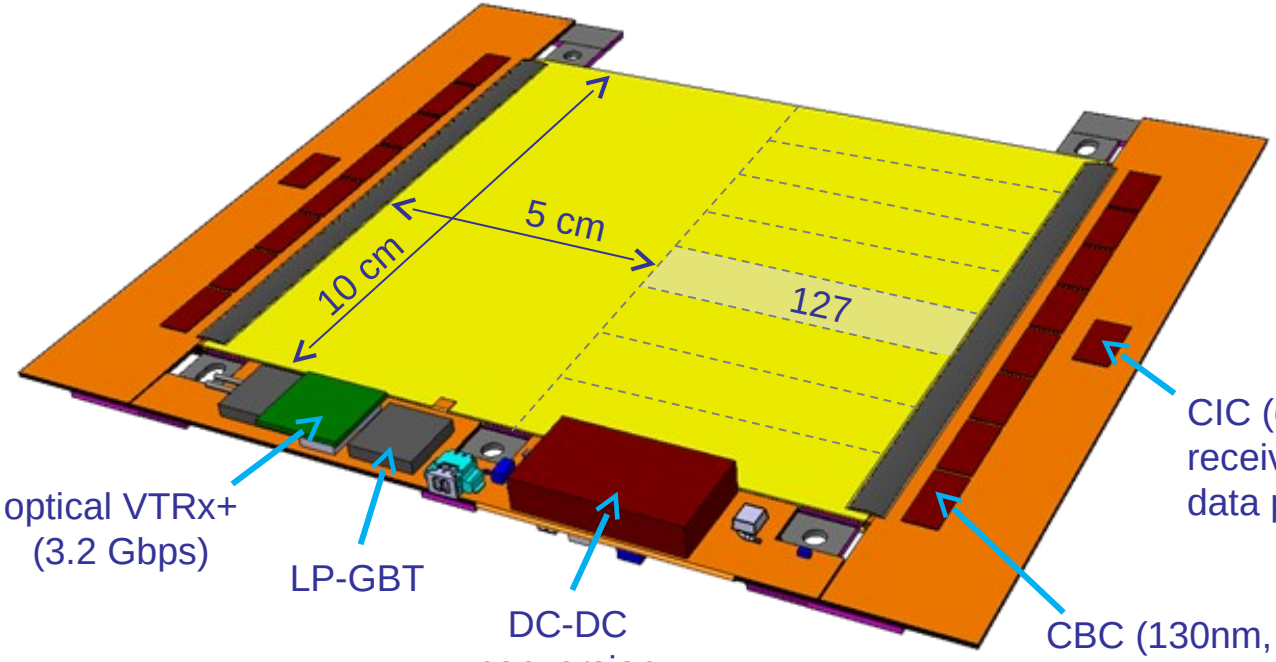
2 Strip sensor layers
for r > 60 cm
2 (hybrids) x 2 (layers) x 1016 strips
5cm long, 90 um pitch
coarse z information



Pixel + **S**trip sensors
for r > 20 cm
2 (hybrids) x 960 strips
2.5 cm long, 100 um pitch
2 (hybrids) x 16 x 960 pixels
1.5 mm x 100 um
accurate z information

2S p_T module





CIC (data concentrator - 65 nm)
receives data from CBCs, assembles
data packet and sends to LP-GBT

CBC (130nm, 16 altogether) each reads out
127 strips from upper layer, 127 from lower

1 module type, ~10 x 10 cm^2 active sensor area for whole of r > 60 cm region (endcaps too)

self-contained single, testable object; only needs power (~ 12 V) and optical connection to function

CBC2 stub-finding logic

cluster width discrimination (CWD)

exclude clusters with hits in >3 neighbouring channels
wide clusters not consistent with high pT track

offset correction & correlation

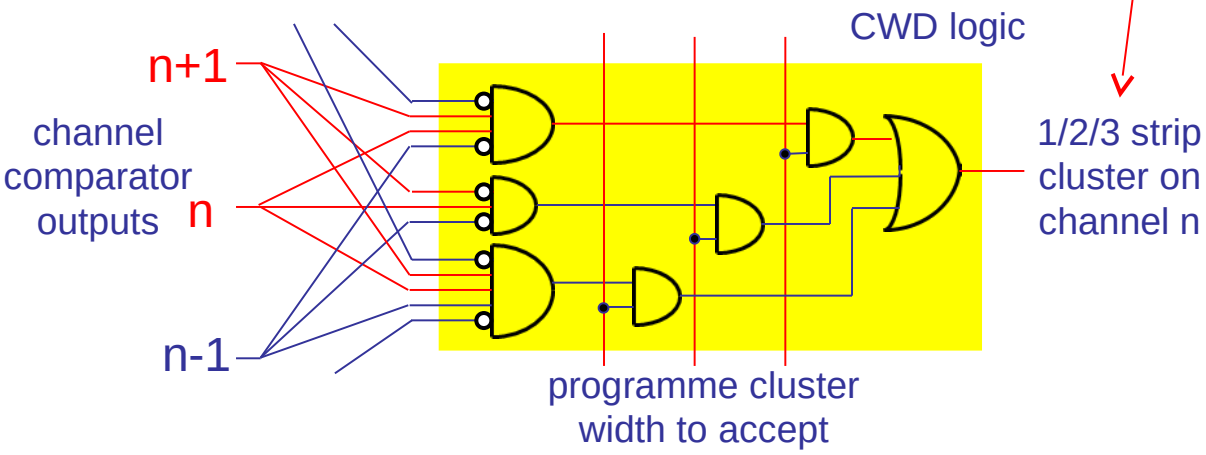
for a cluster in bottom layer, look for correlating cluster occurring in window in top layer

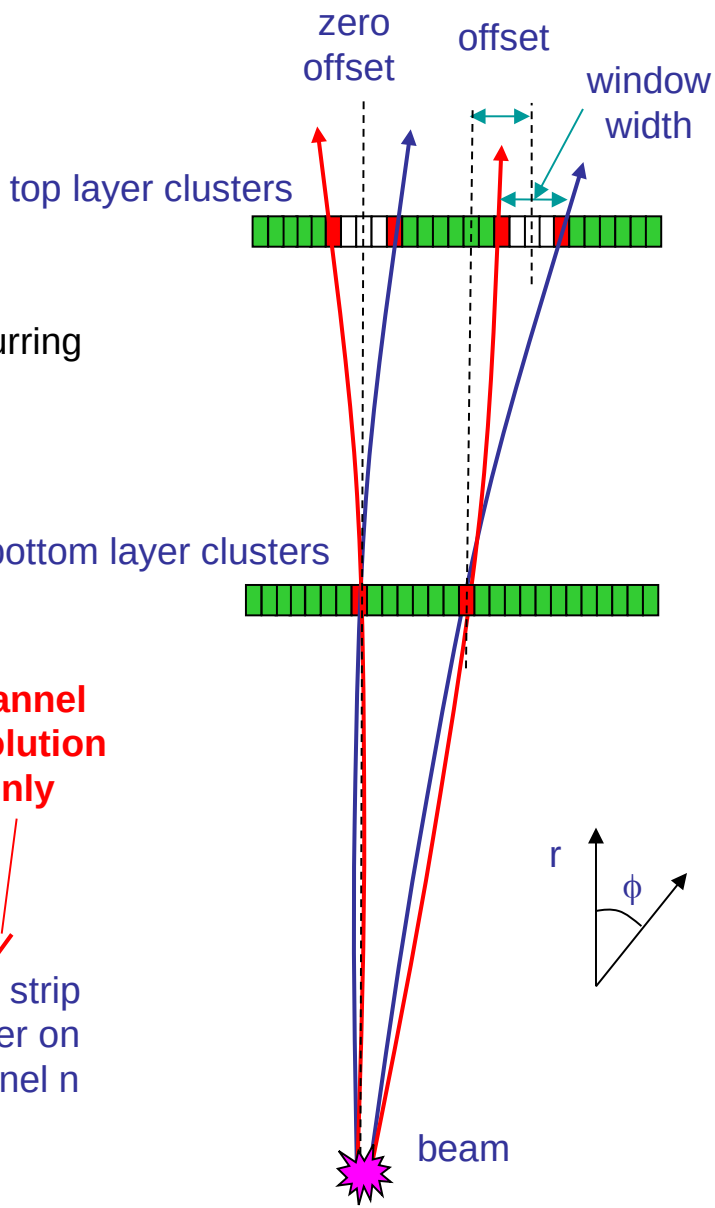
window width controls pT cut

stub found if cluster in bottom layer corresponds to cluster within window in top layer
window width programmable up to **+/- 8 channels**

offset defines lateral displacement of window across chip
programmable up to **+/- 3 channels**

channel resolution only





history(2)

CBC2 worked well enough to achieve major objectives

development of challenging hybrid technologies
proof of pT module concept

main issues

- CM effect when low threshold and many channels firing
  - evidence points to supply current fluctuations when many channels firing coupling to postamp feedback FET biasing
  - a new method for biasing the feedback FET has been implemented for CBC3
  - comparator has been modified to draw same current - fired or not
- so-called “shadow effect”
  - when signal injected into many channels, other channels fire, but ~50 nsec later
  - traced to coupling through preamp cascode bias node
  - can be solved by regulated cascode circuit for the preamp (other benefits)
- leakage current in pipeline at low ionizing doses
  - so-called RINCE effect for normal layout NMOS devices
  - enclosed NMOS devices now implemented
- SEU immunitity for I2C registers could be better
  - now using Whitaker cells for I2C registers

CBC3 specifications

analogue front end

n-on-p sensor polarity - signal current flows out of chip - electrons mode only
AC coupled - no specified leakage current tolerance
strip length 5cm (possibly up to 8cm)
    => may need to run with high currents in input FET
pulse shaping
    peaking time <20 nsec
    return to baseline within 50 nsec for signals in normal range (1 - 5 mips)
gain: ~50 mV / fC (mip signal for 200 um thick sensor 2.5 fC before irradiation)
overload recovery
    individual channel (and neighbours) should respond to normal size
    signal < 2.5 usec following hip signal up to 4 pC
noise target < 1000e

power

aim for overall analogue power of ~ 350 uW /channel

overall chip power ~ 450 uW / channel

CBC3 specifications

comparator

(individual channel offset trim implemented at postamp output)

10-bit resolution (~1mV) for comparator global threshold VCTH

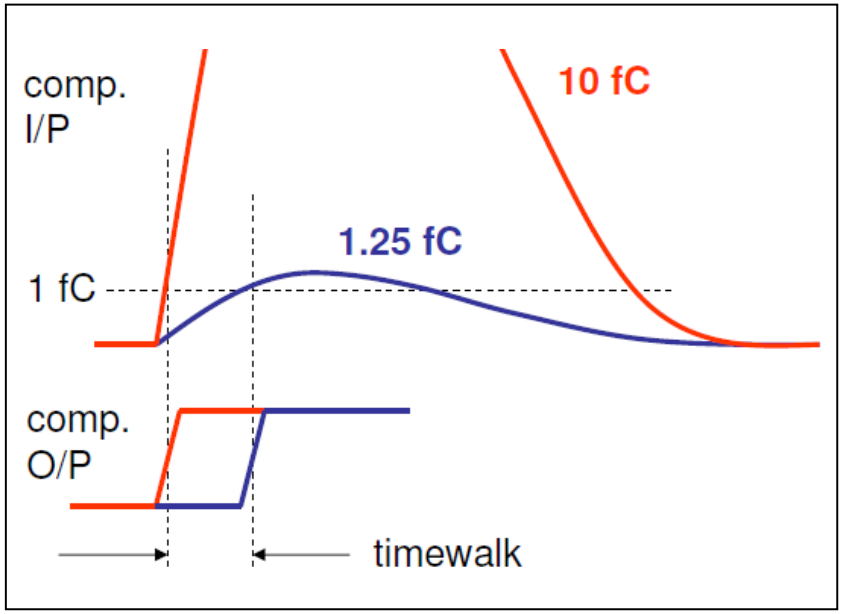
timewalk

originally specified for 300um sensors

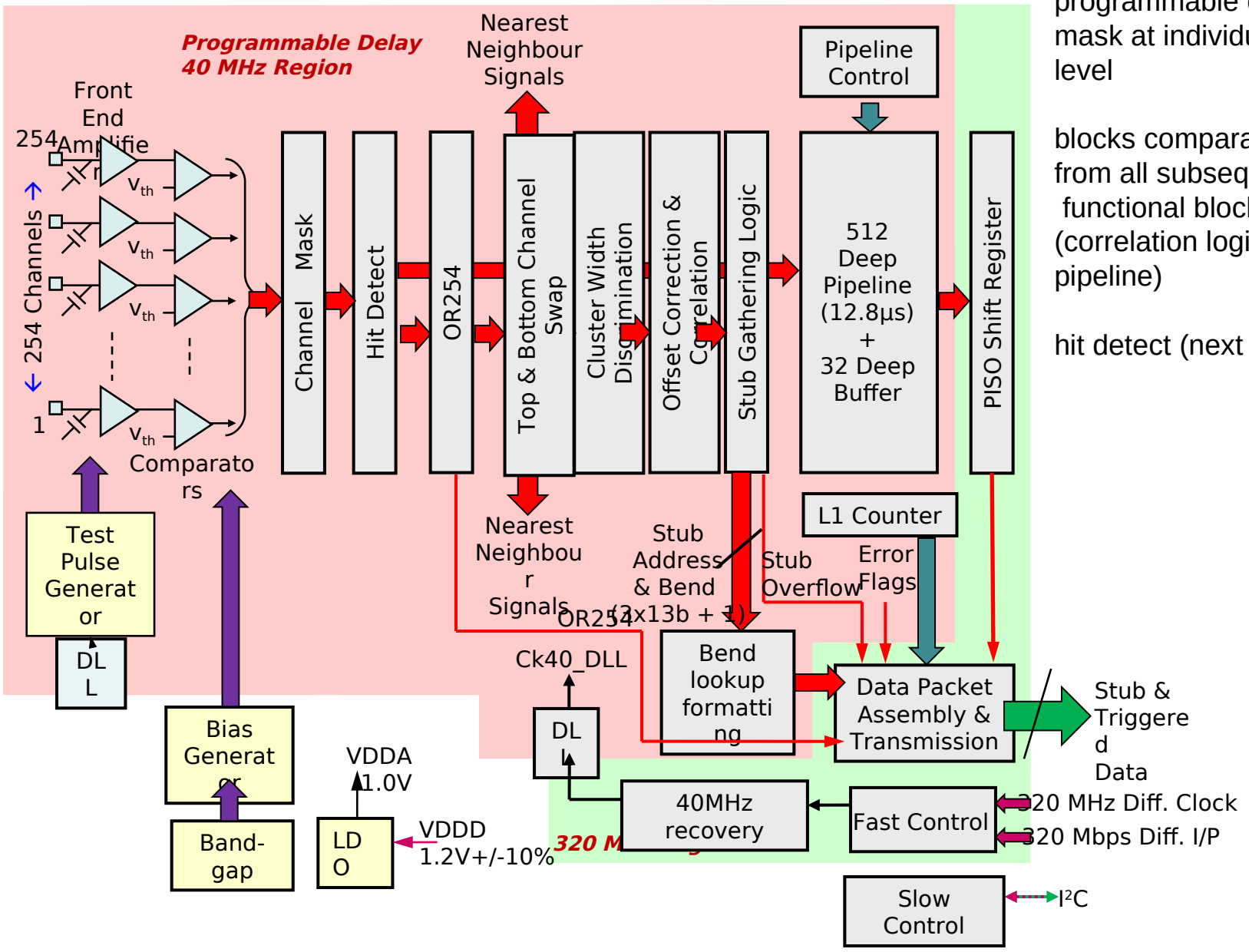
<16 nsec time difference between comp. output edges

for input signals of 1.25 (0.83) fC and 10 (6.7) fC for threshold of 1 (0.67) fC

(numbers in red adjusted for 200 um sensor)



CBC3: other blocks functionalities



programmable channel mask at individual channel level

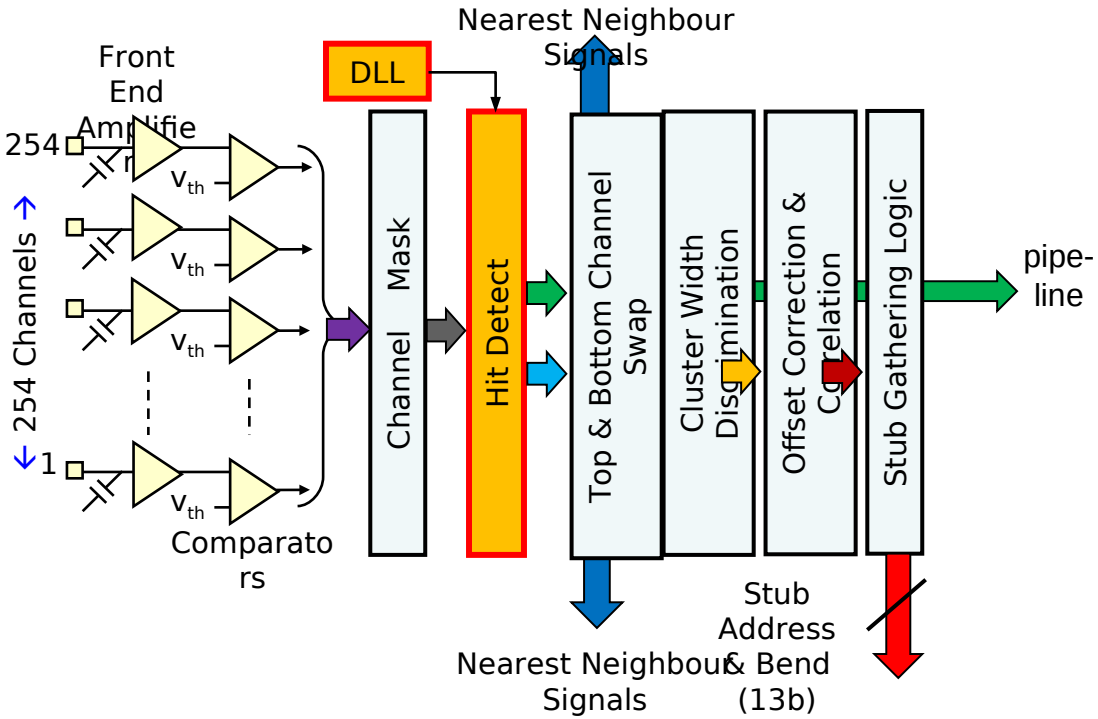
blocks comparator outputs from all subsequent functional blocks (correlation logic and pipeline)

hit detect (next slide)

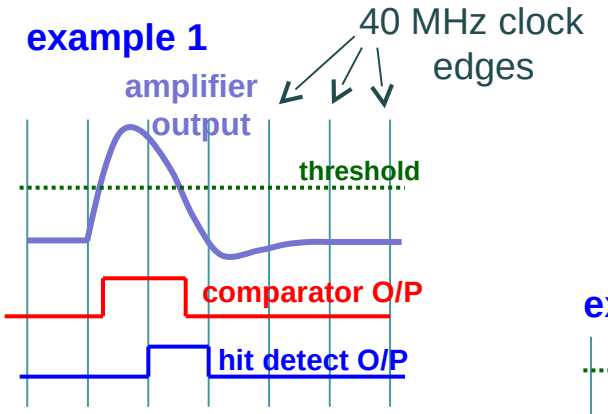
hit detect

samples output from comparator using programmable phase 40 MHz clock from DLL (1 nsec resolution)

needs to be sensitive to variety of input conditions

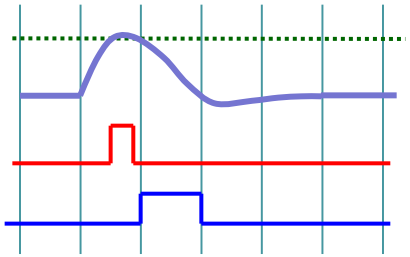


example 1



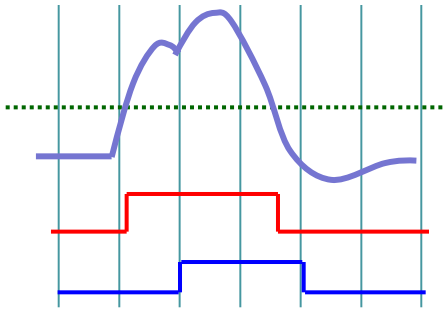
single pulse at amp. O/P. Comparator O/P fires. Hit detect produces output at next 40 MHz clock edge

example 2



single pulse only just exceeds threshold. Comp O/P rises and falls between clock edges, but hit detect still “detects” and produces an output

example 3



two consecutive pulses piled up. Comp O/P stays high for 2 clock edges. => hit detect output stays high for two clock cycles

top & bottom channel swap

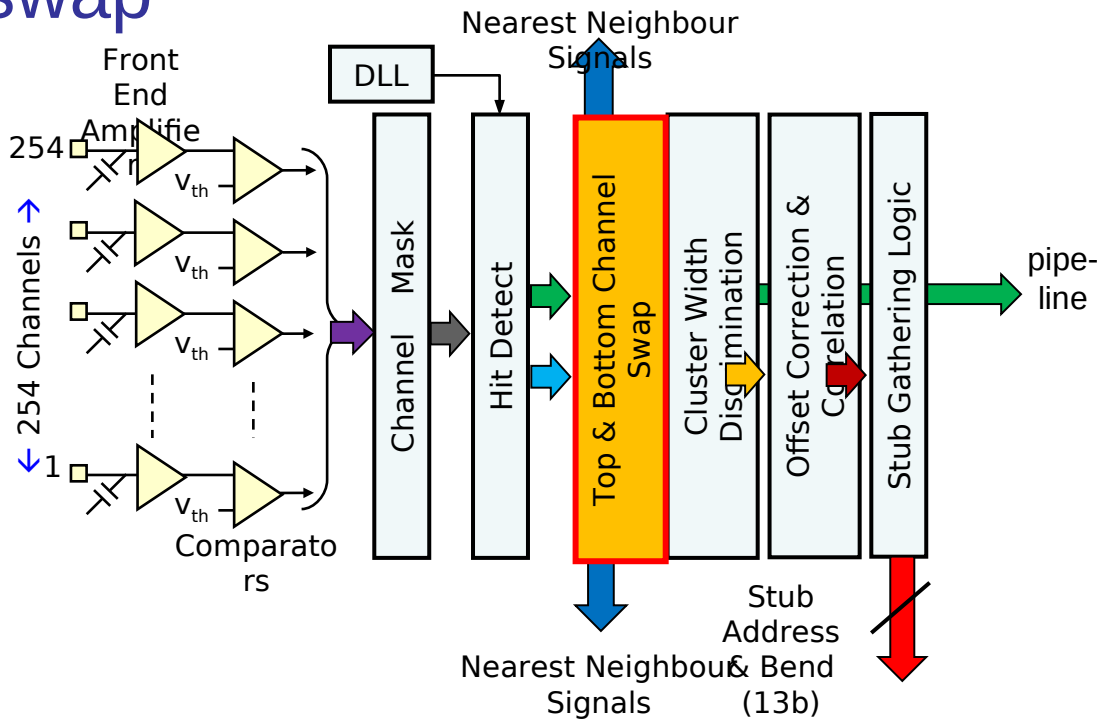
modules mounted above and below support structure will be flipped (probably)

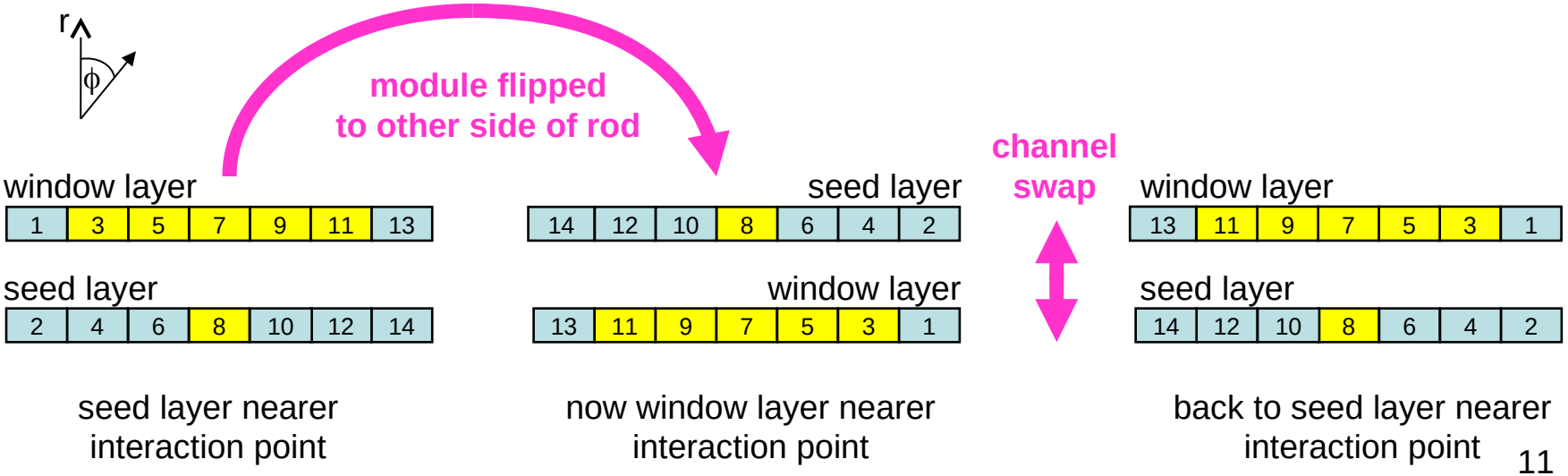
=> seed and window layers will also be flipped unless do something about it

(expect lower efficiency when seeding from outer layer because of scattering and conversions -> more hits in outer layer which don't correspond to valid stub)

simplest thing is to swap channels on chip

1<->2, 3<->4, 5<->6,.....





cluster width discrimination

CBC2: clusters ≤ **3** strips accepted

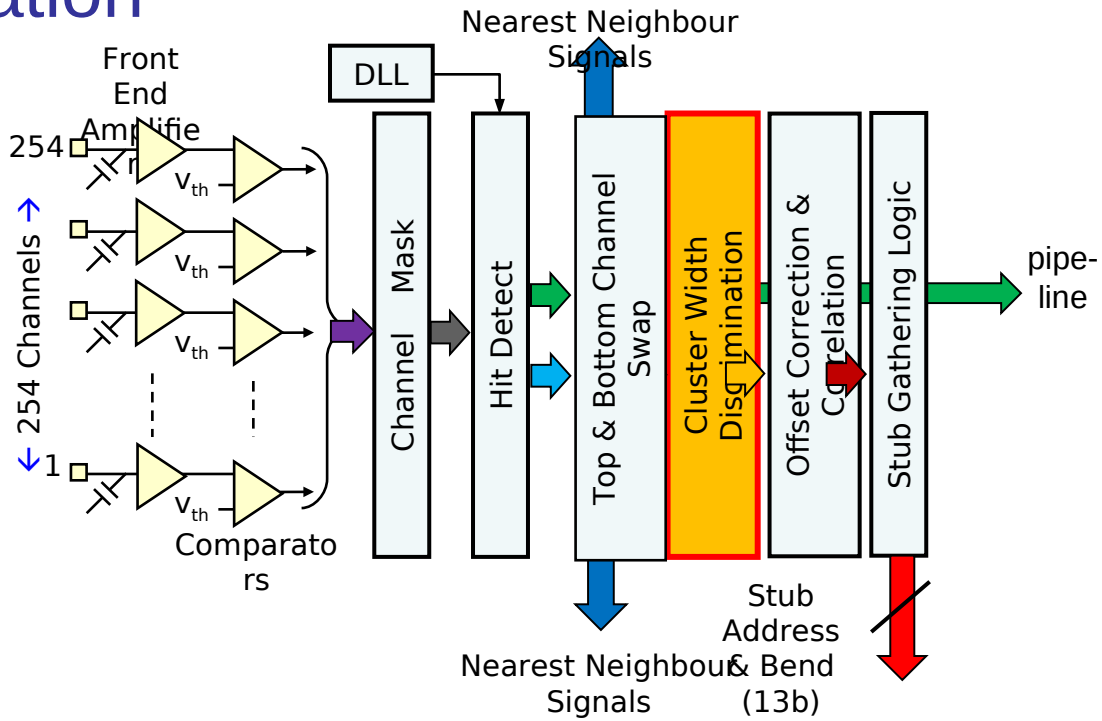
2 strip cluster assigned to one of the strips involved

CBC3: clusters ≤ **4** strips accepted

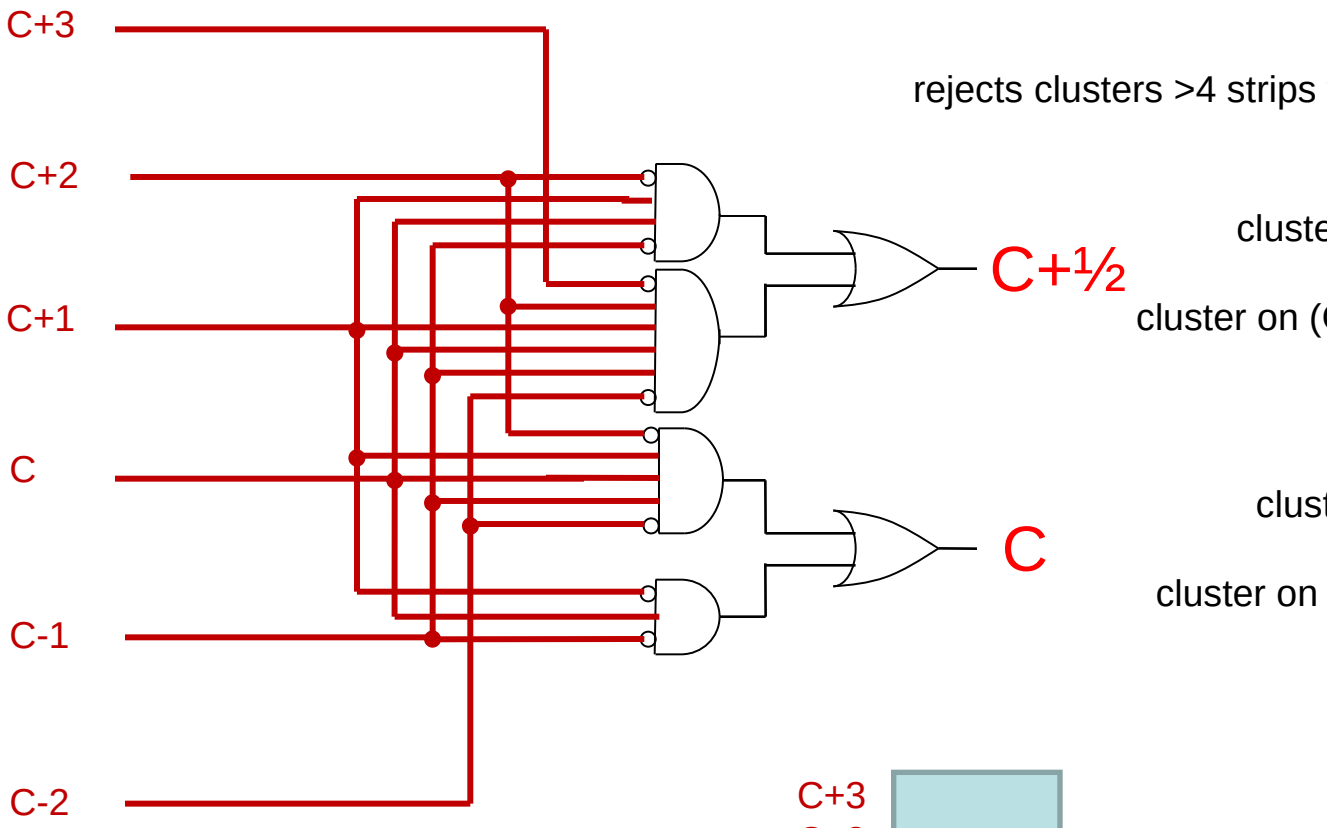
2 & 4 strip clusters assigned to mid-position

=> ½ strip cluster position resolution

=> 8-bit cluster address



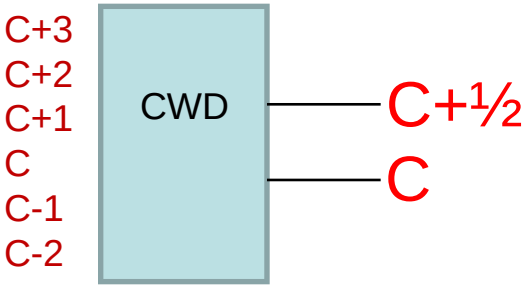
cluster width discrimination - logical representation



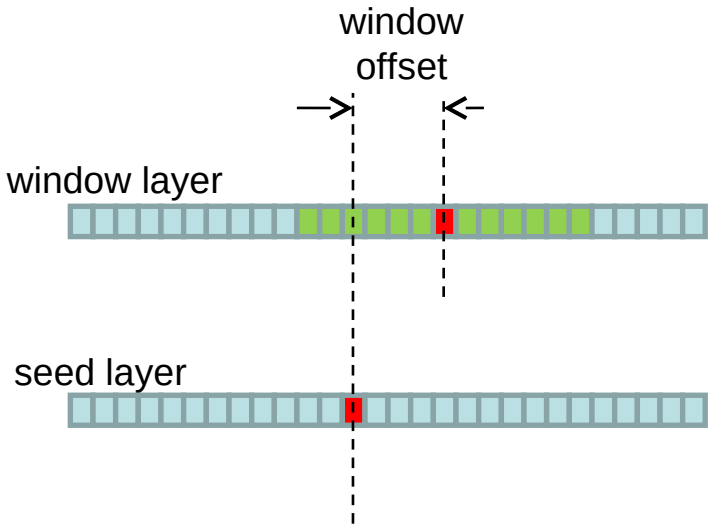
rejects clusters >4 strips wide

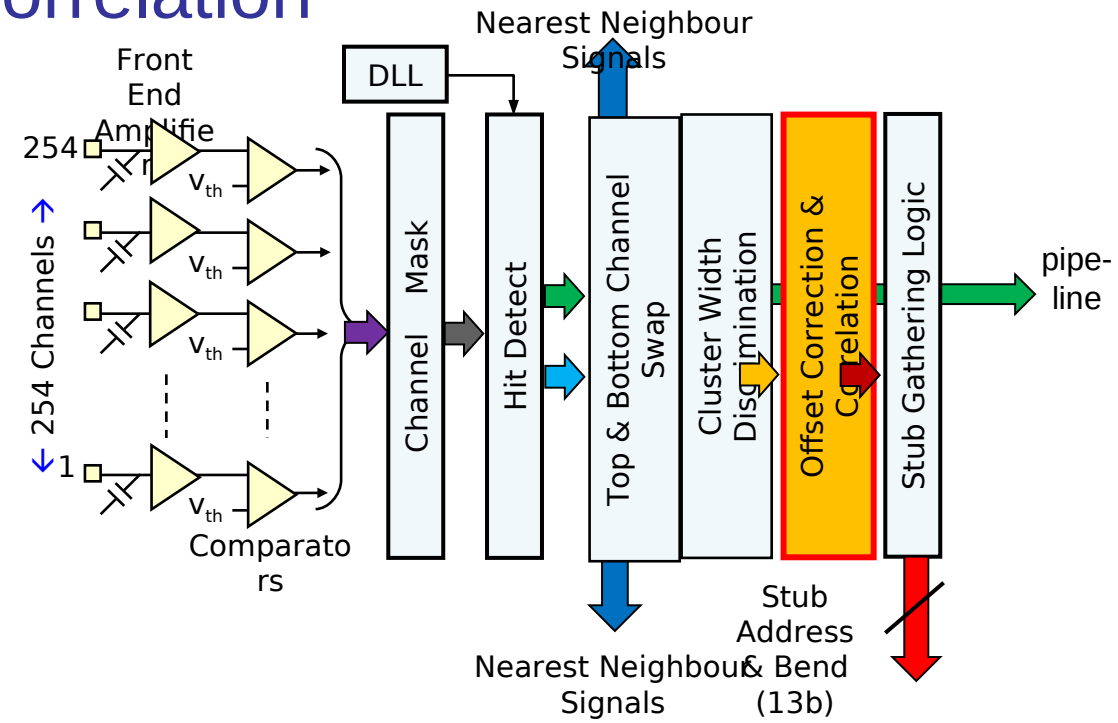
cluster on C/(C+1)
OR
cluster on (C-1)/C/(C+1)/(C+2)

cluster on C
OR
cluster on (C-1)/C/(C+1)



offset correction and correlation





CBC3 stub generated if cluster in seed layer corresponds to cluster found within window in other layer

window width programmable up to ± 7 strips (± 14 half strips)

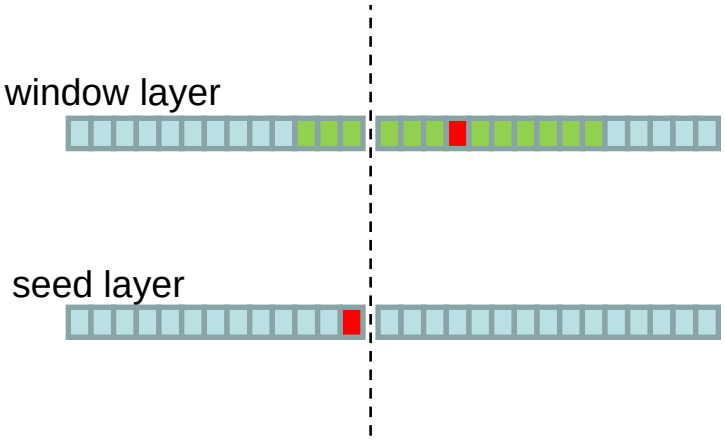
window can be offset, 4 domains / chip (=> 32 across module)

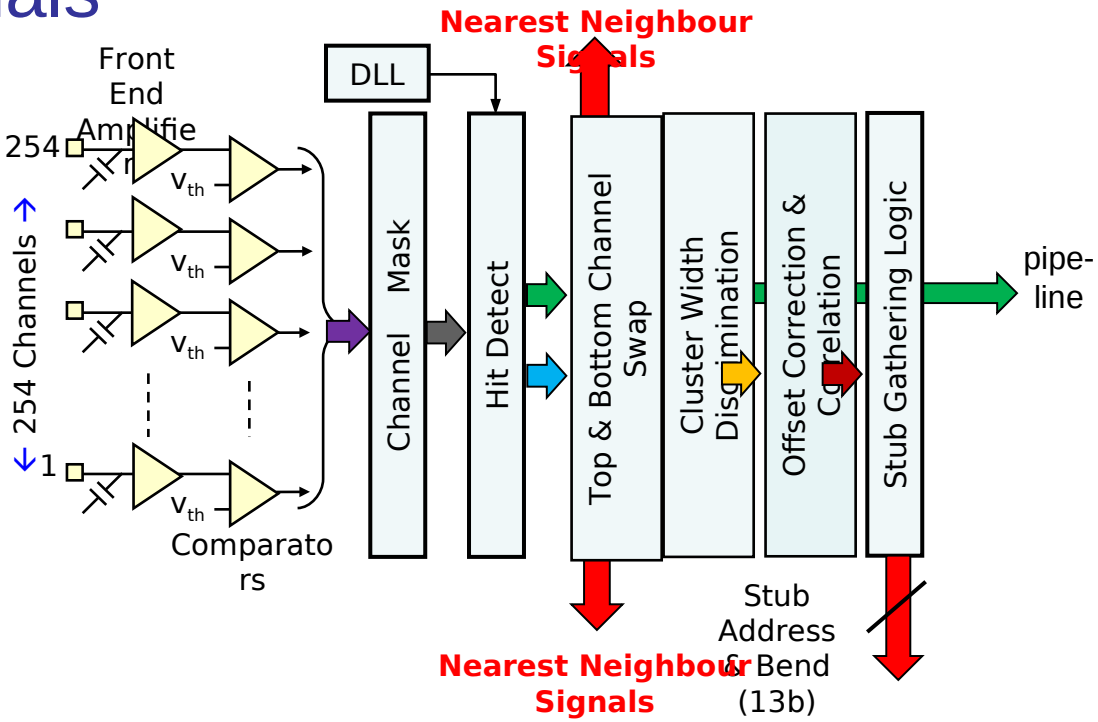
offset programmable up to ± 3 strips (± 6 half strips)

position of cluster in window indicates direction of stub -> this is the **bend** information

5 bits bend info locates cluster to individual ½ strip position if widest window selected

nearest neighbour signals



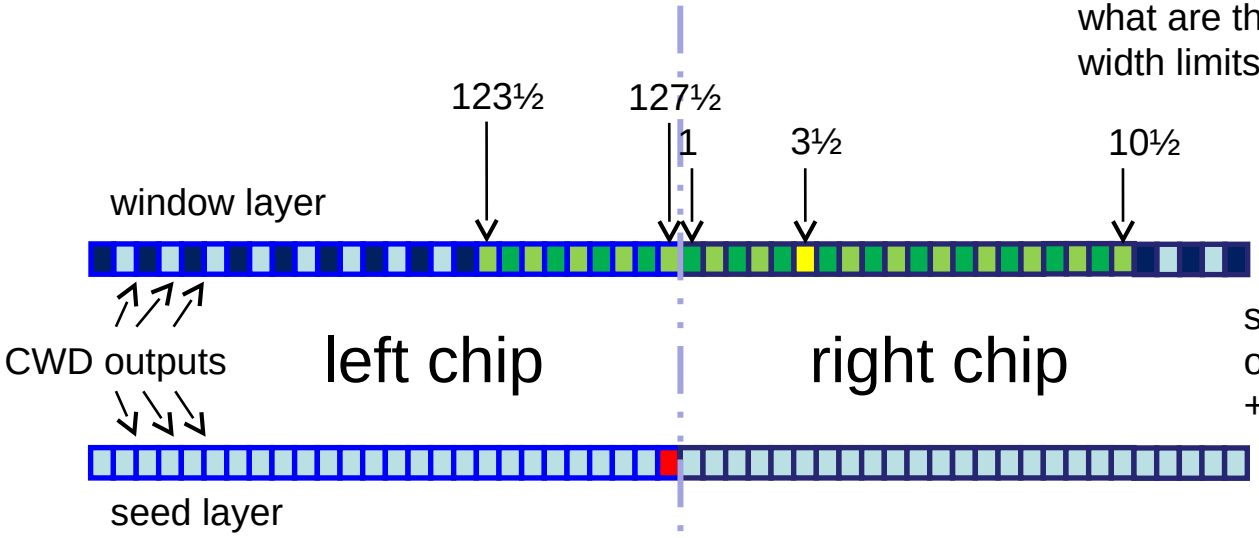


need to transfer signals between chips to ensure continuity across module

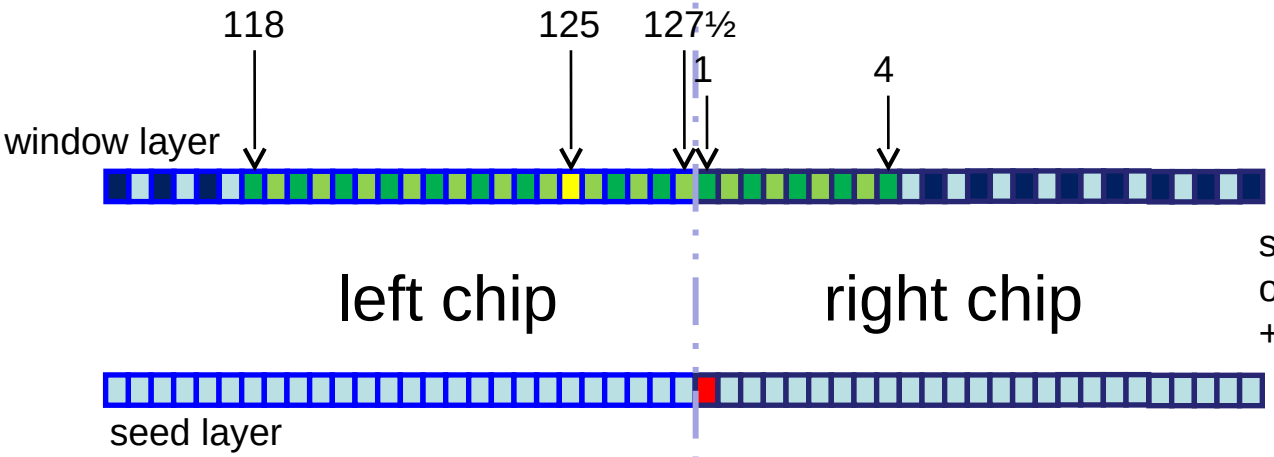
minimum no. to transfer achieved by transferring before CWD and duplicating logic on each chip

chip overlap regions

assume chip with seed performs correlation
what are the maximum offset and window width limits?



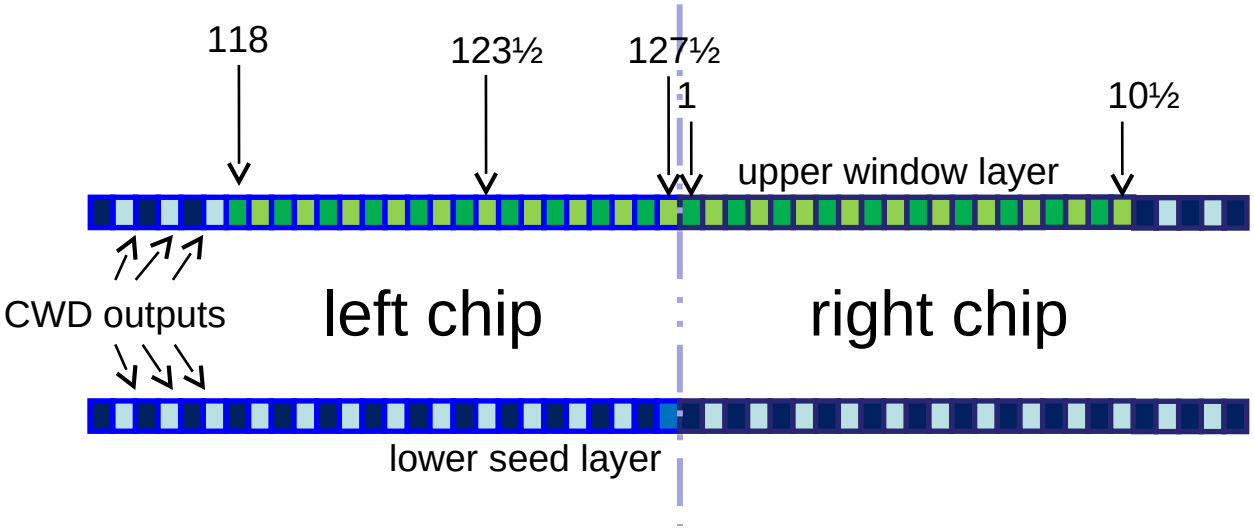
seed on rightmost edge of left chip
offset max +3 strips to right
+/- 7 strips window

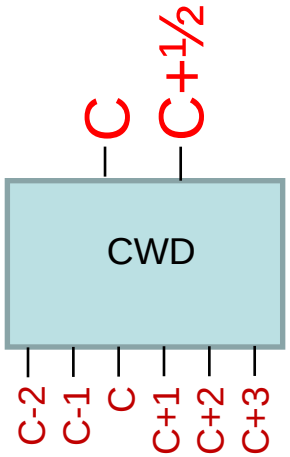


seed on leftmost edge of right chip
offset max -3 strips to left
+/- 7 strips window

use this picture to determine how many interchip signals there will be

interchip signal numbers





upper window layer

CWD logic for cluster on strip 118 requires inputs from strips 117 and 116
CWD logic for cluster on strip 10½ requires inputs from strips 11, 12, & 13

so hit detect outputs of 13 strips must be passed from right to left
1,2,3,4,5,6,7,8,9,10,11,12,13
and 12 from left to right
116,117,118,119,120,121,122,123,124,125,126,127

25

lower seed layer

seed on 127½ in left chip on seed layer requires 3 strips from right chip (1,2 & 3)
seed on 1 on right chip in seed layer requires 2 strips from left to right (126 & 127)

5

so total interchip signals requires 25 + 5 = **30 signals**

skip to slide 27

now look at interchip signal issue from viewpoint of CBC channel numbers (1 … 254)

channels 1,3,5,7,…249,251,253 read out 1 layer
channels 2,4,6,8,…248,250,252,254 read out the other

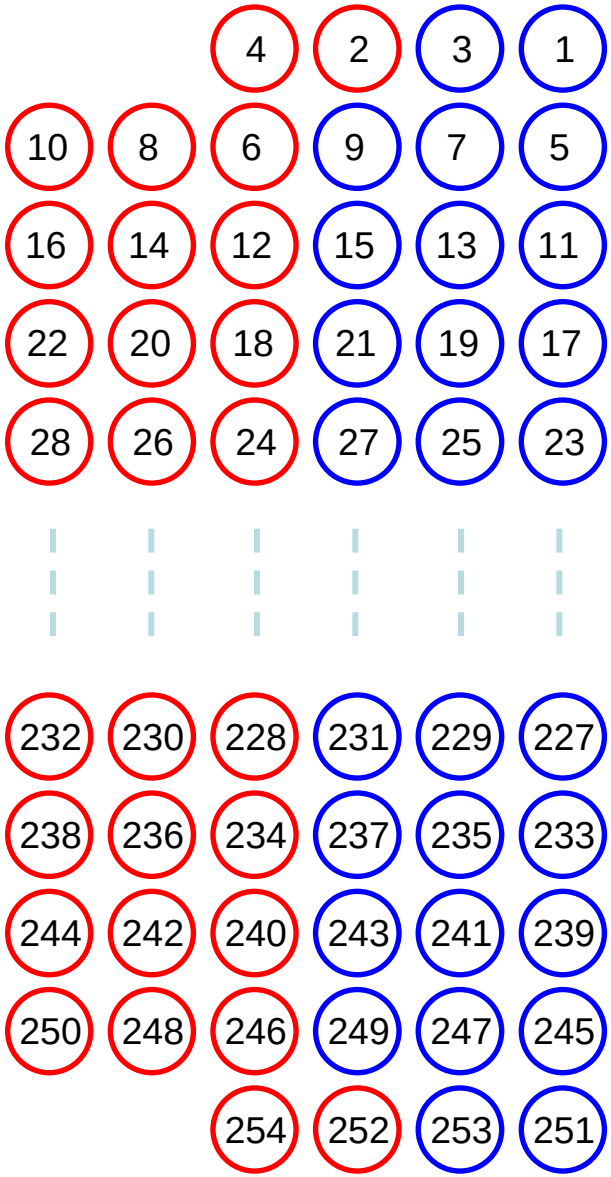
explore what happens when flip module on other side of support structure
want seed layer to still be the layer nearest the beam, so swap channels in CBC

1<->2, 3<->4, 5<->6, 7<->8, …. 249<->250, 251<->252, 253<->254

for CBC2 (2CBC2 and 8CBC2flex hybrids) odd channels (1,3,5,…) correspond to seed layer nearest to beam, and even channels (2,4,6,8,…) correspond to window layer

in the following pictures sensor channels are arbitrarily numbered 1 to 1016

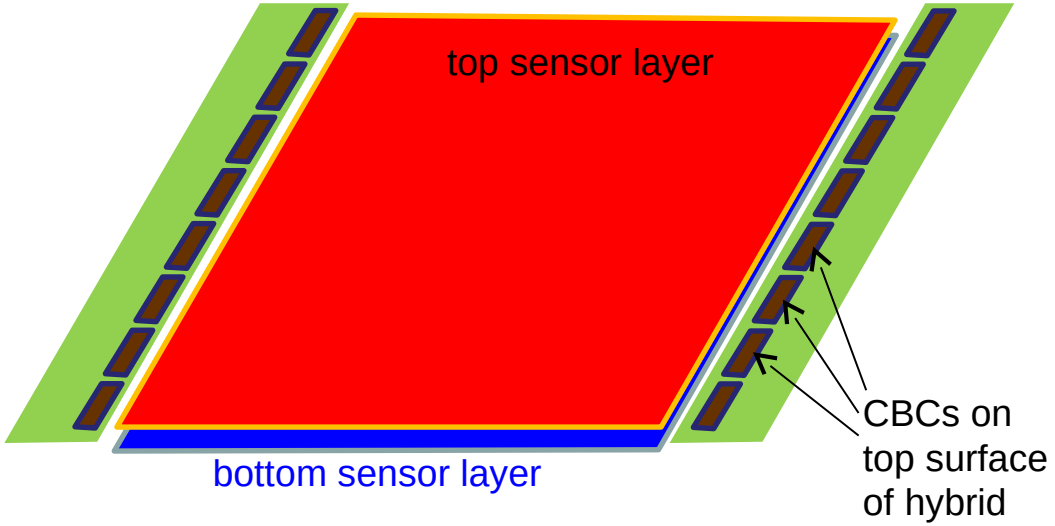
reminder of CBC channel numbering



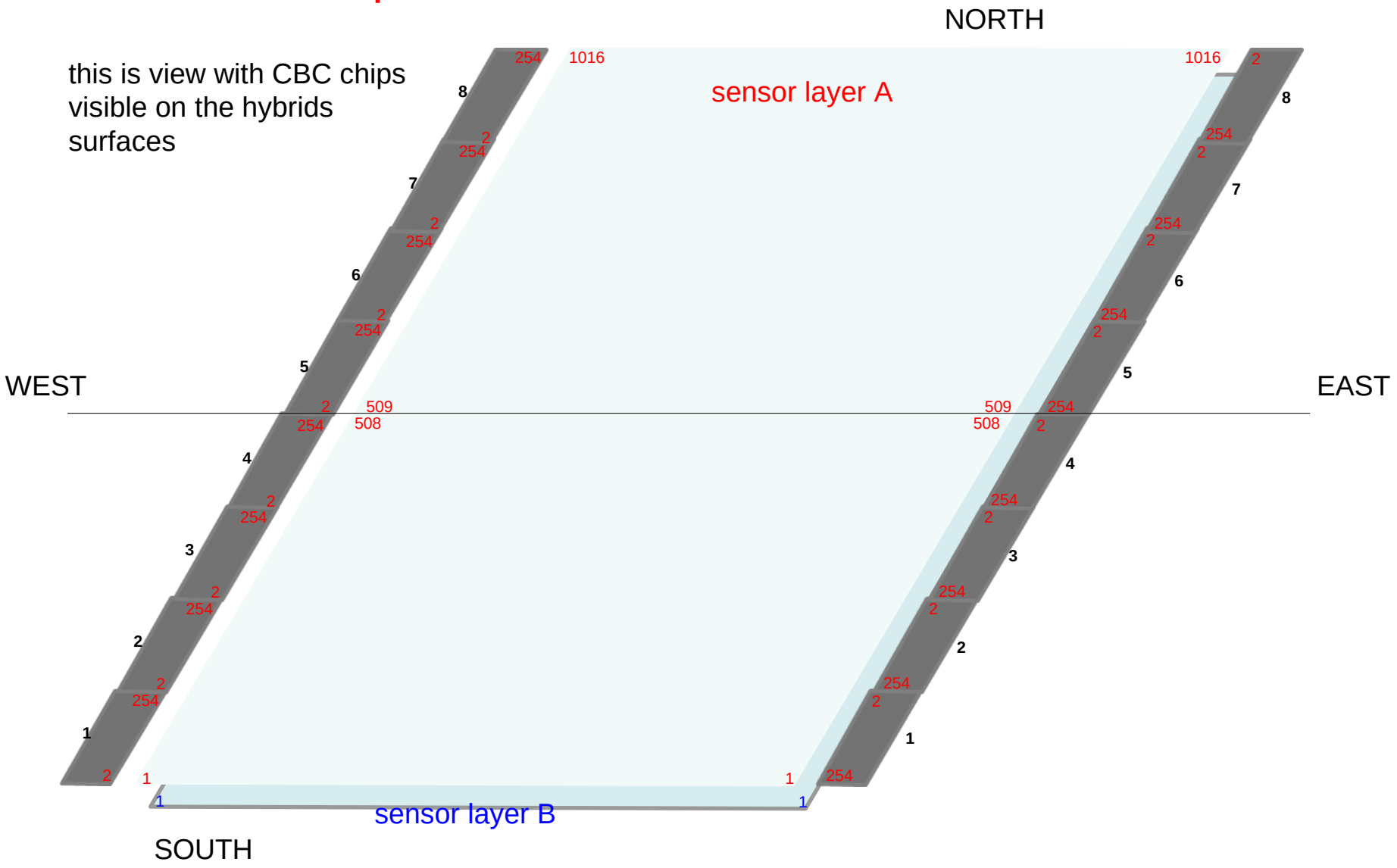
CBC channels number as if viewed through the CBC back surface, so this is the pad layout that would be visible on the hybrid

red channels route to the top sensor layer

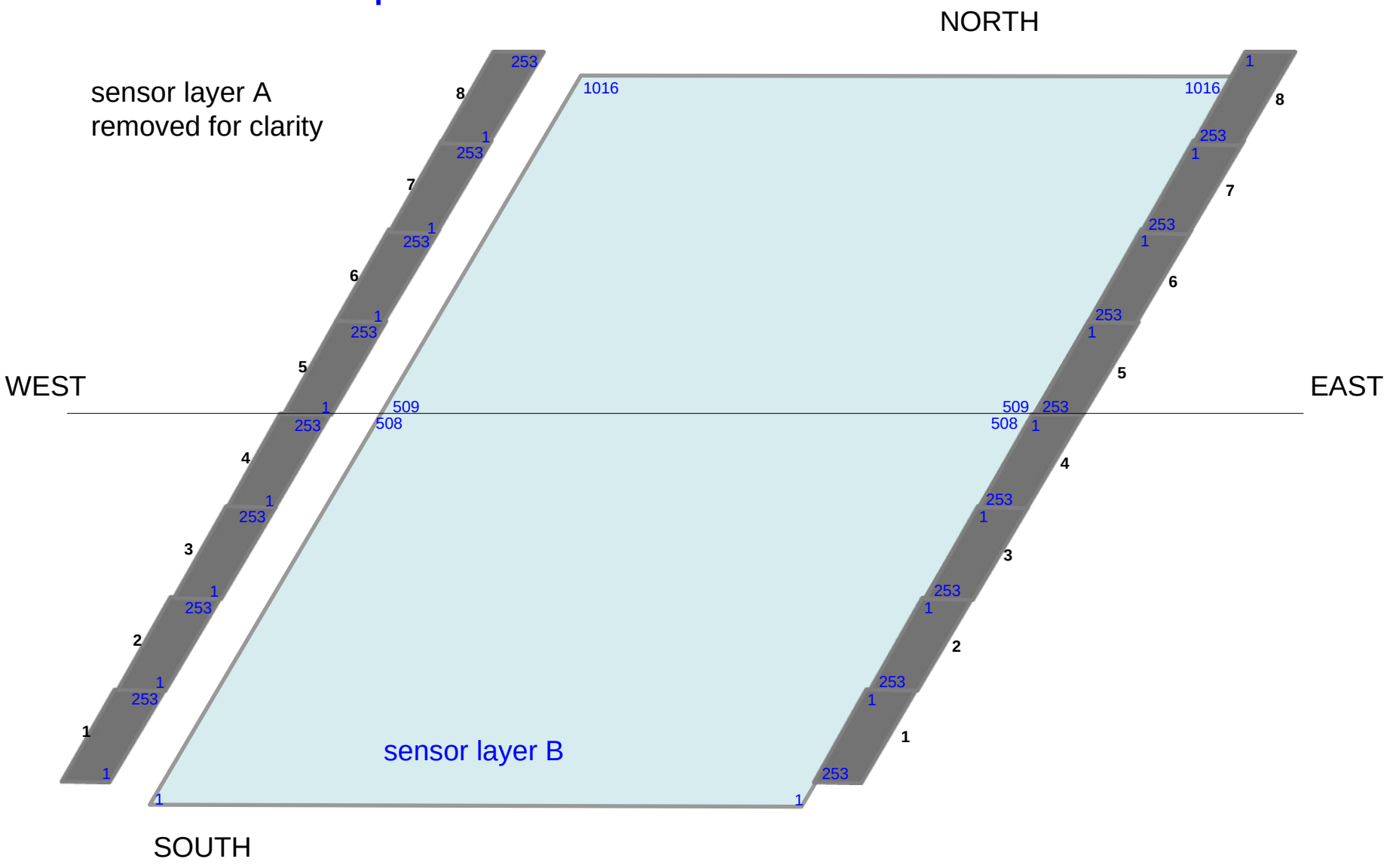
blue channels are via'd through the hybrid to the bottom sensor layer



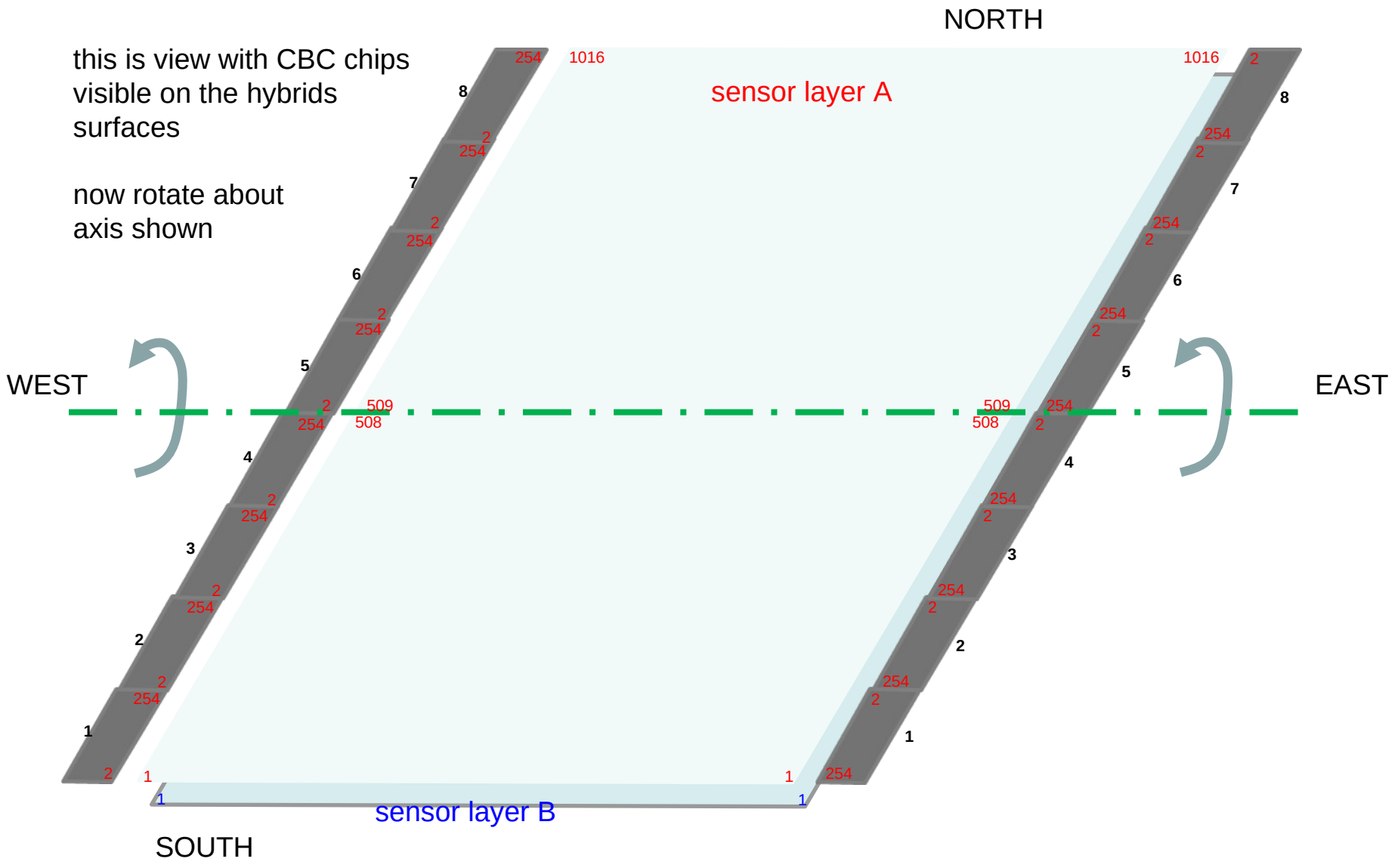
CBC channel/sensor layer A numbering convention before module flip



CBC channel/sensor layer B numbering convention before module flip

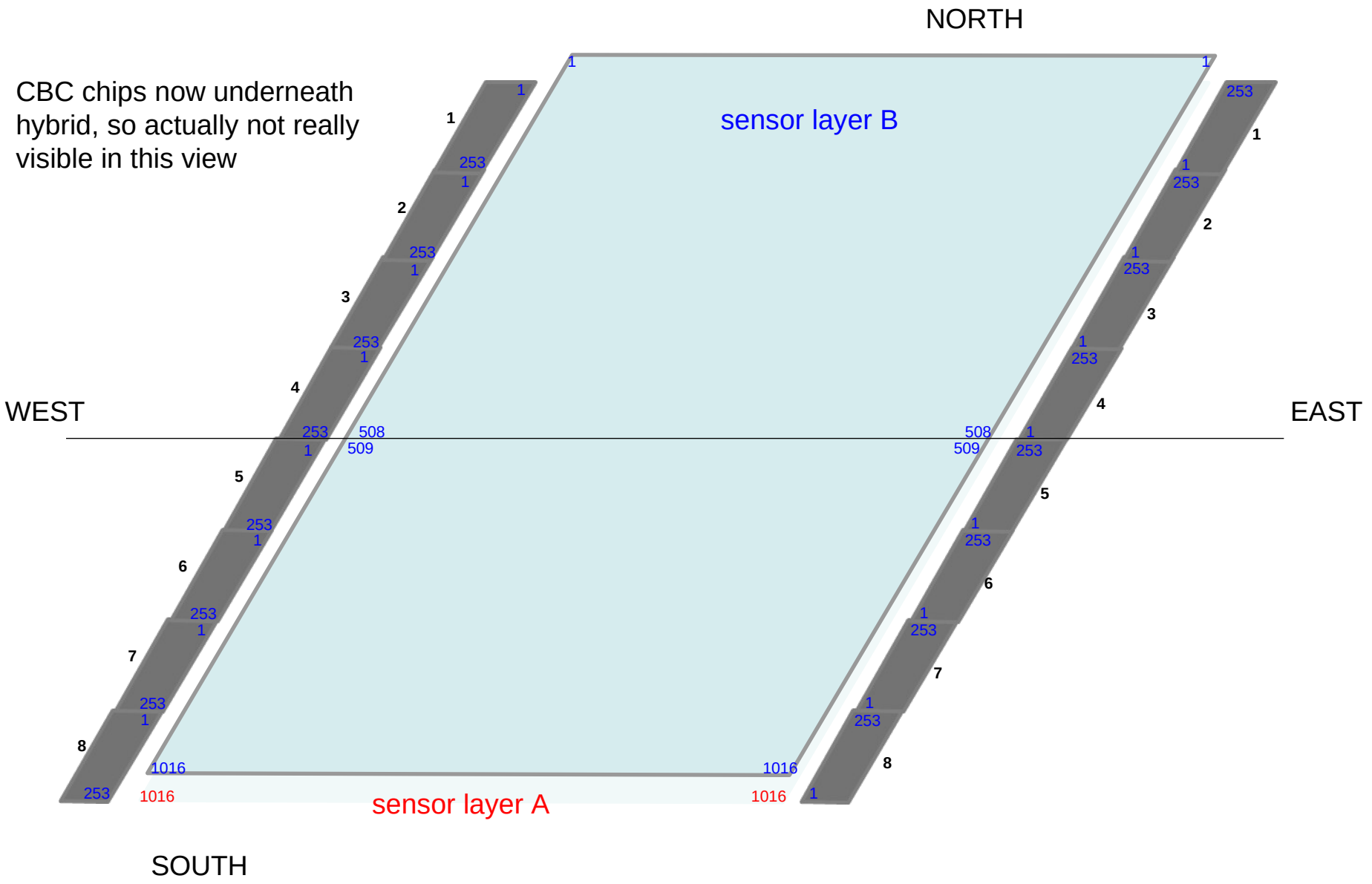


back to picture before module flip

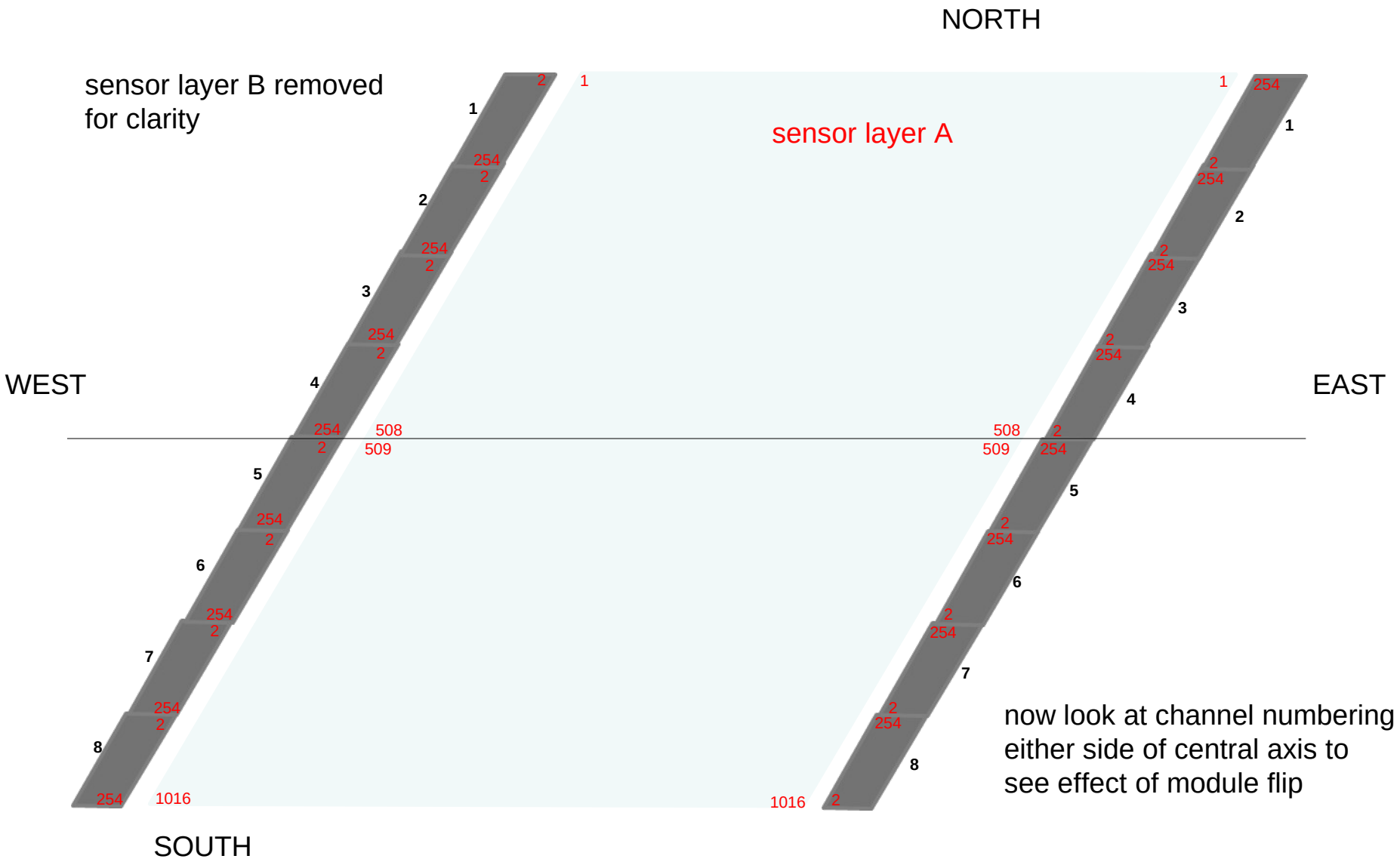


after module flip

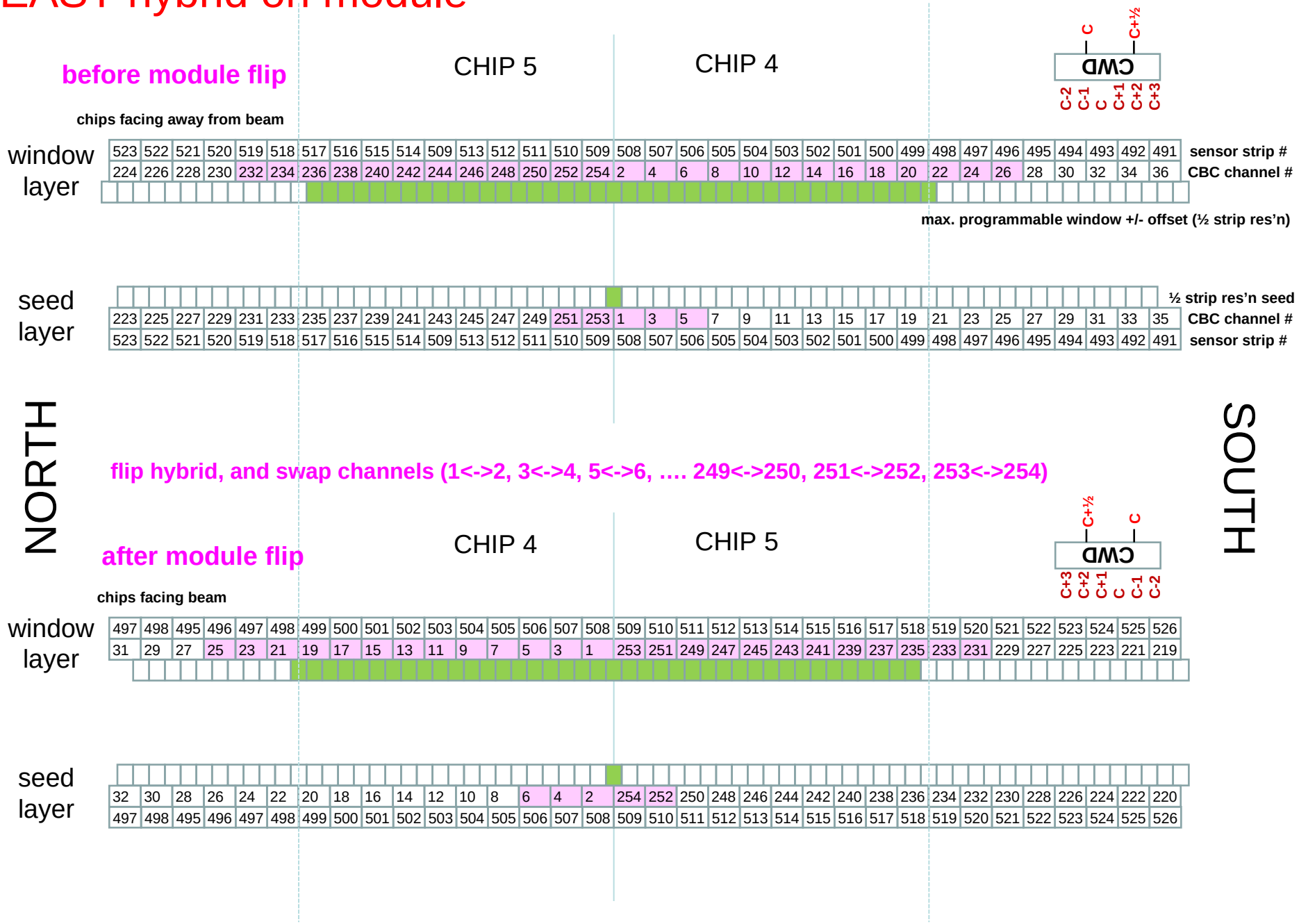
CBC chips now underneath hybrid, so actually not really visible in this view



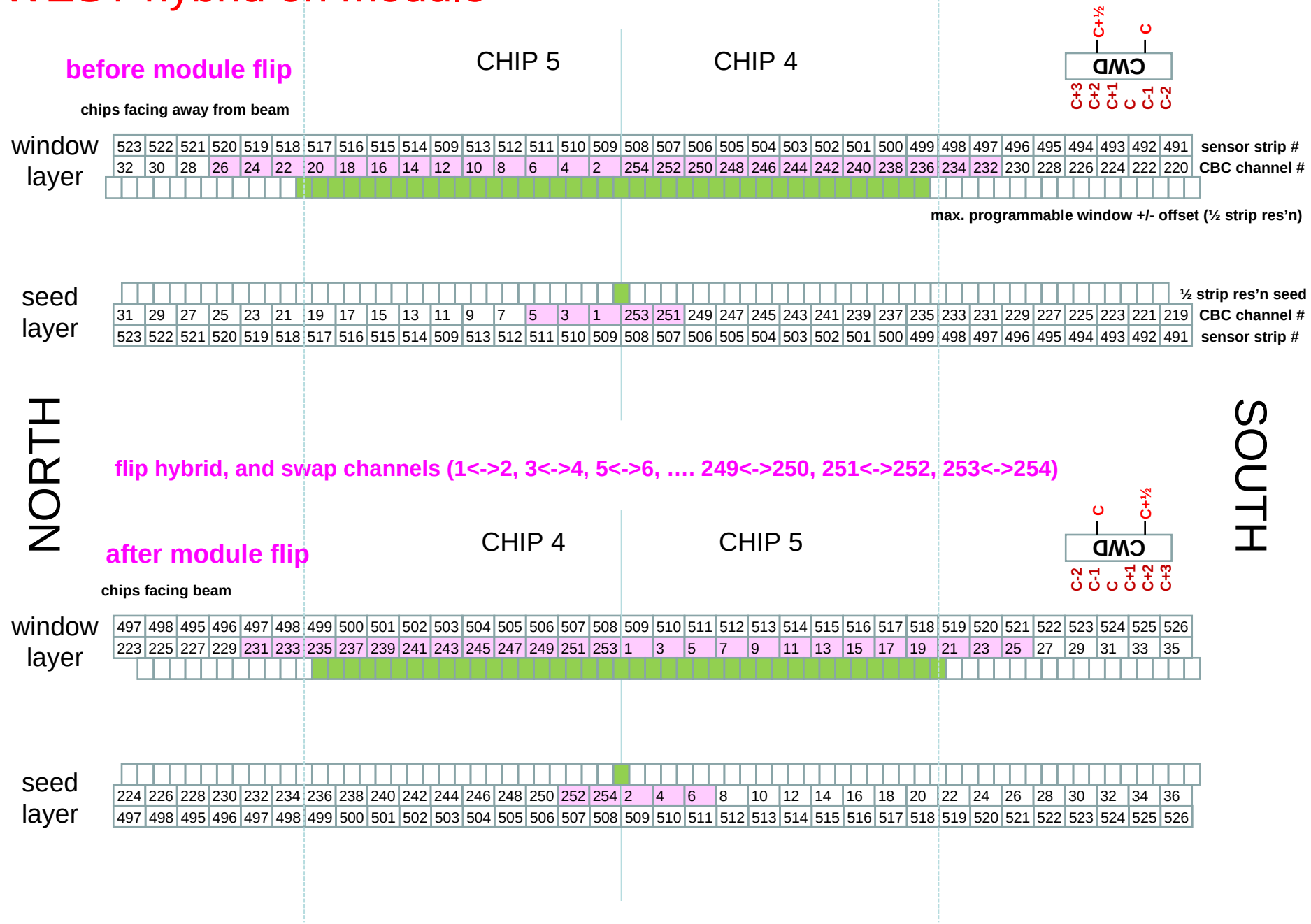
after module flip



EAST hybrid on module



WEST hybrid on module



stub gathering logic + bend lookup formatting

up to 3 stub addresses (8 bits) + associated bend info (5 bits) passed to **bend lookup formatting** block every BX

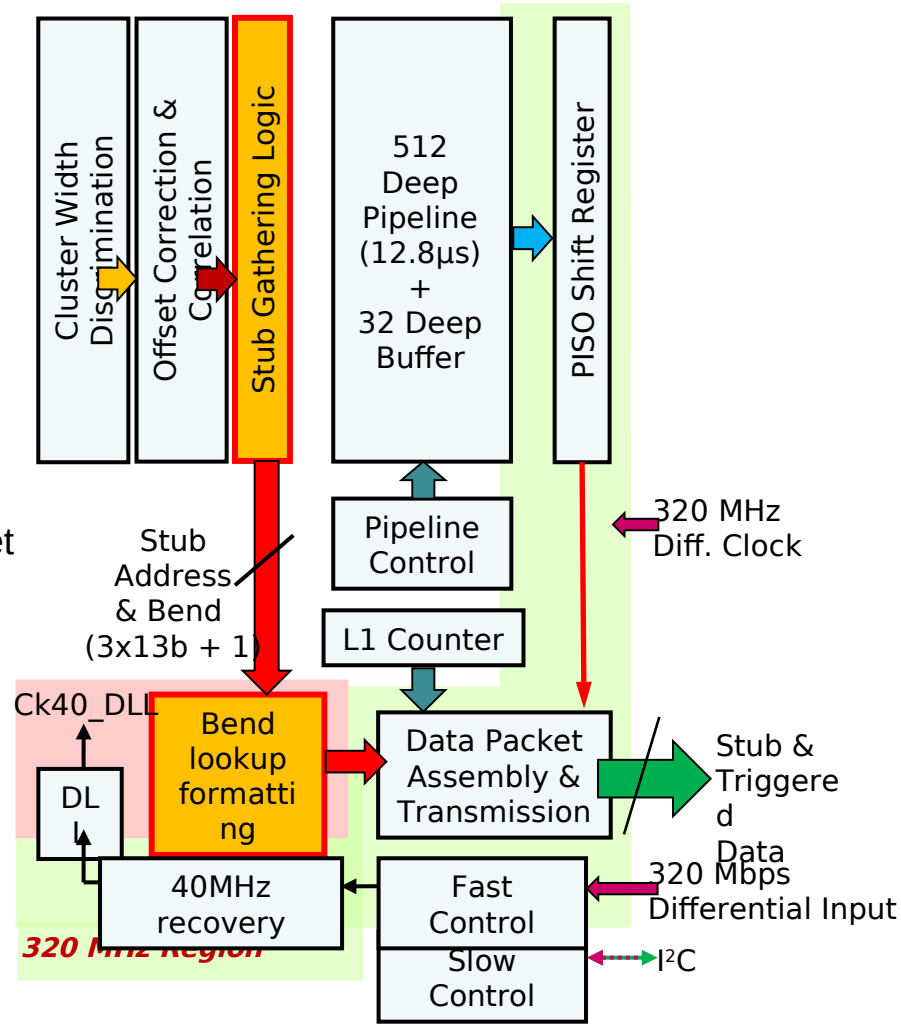
no priority logic - 1st 3 stubs only

more than 3 -> stubs overflow bit set in O/P data packet

13 bits / stub => 39 bits total

5 bits bend info reduced to 4 bits using programmable lookup table

(mapping will depend on module location in tracker)



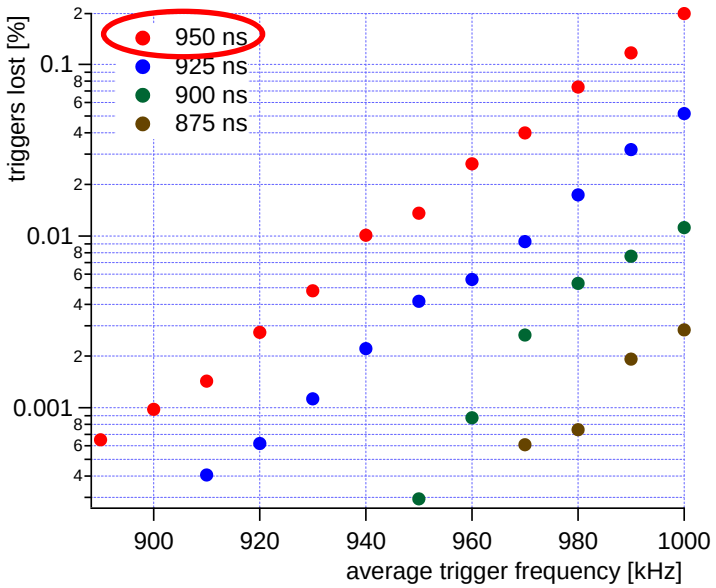
pipeline + buffer & PISO shift register

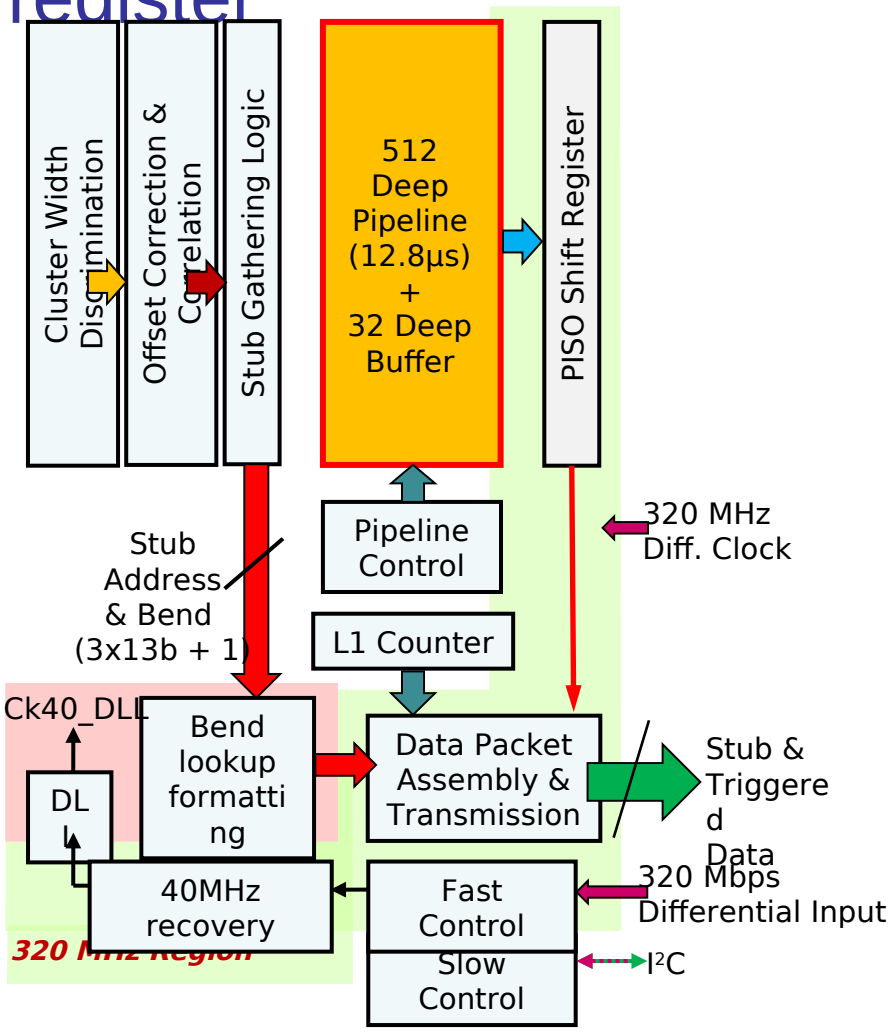
512 deep pipeline => up to 12.8 usec latency

32 deep buffer for triggered events awaiting readout

=> low inefficiency for trigger rate up to 1MHz

triggers rejected to avoid buffer overflow vs. trigger rate





data packet assembly & transmission

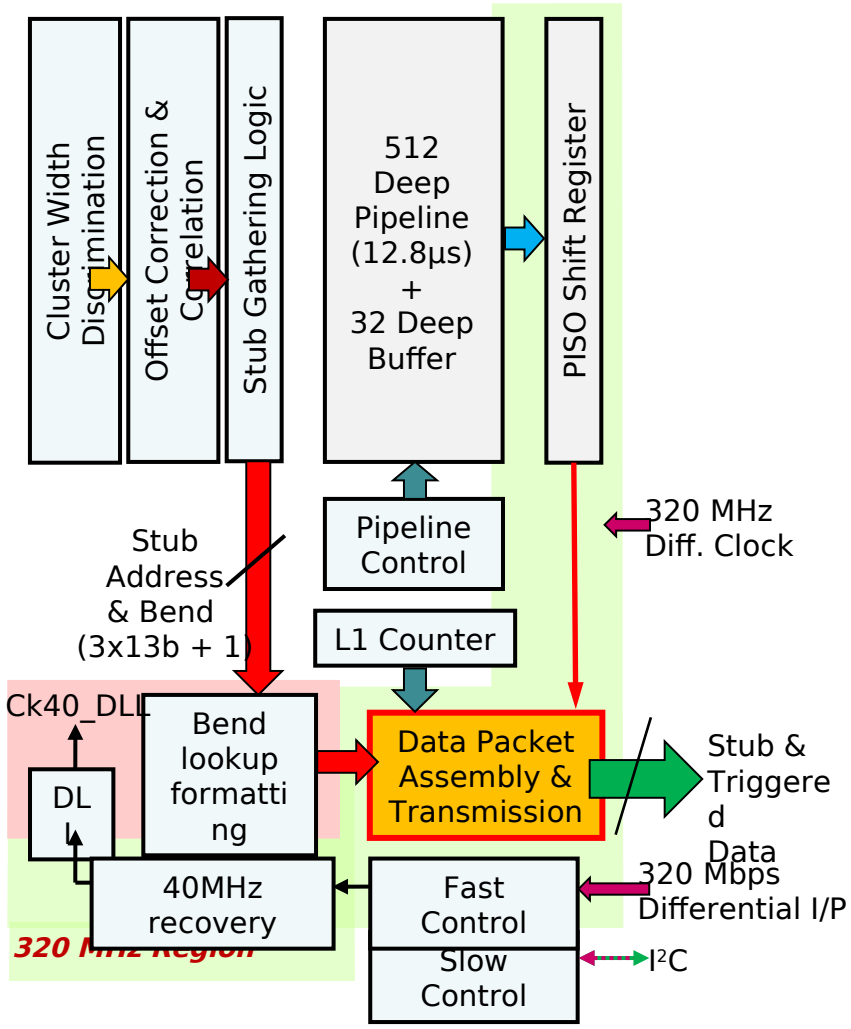
6 differential outputs running at 320 Mbps

output data block

SLVS<1>	SLVS<2>	SLVS<3>	SLVS<4>	SLVS<5>	SLVS<6>
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**

25 ns

R = L1 triggered readout data
time flow **bottom** to **top** (e.g. **S1<7> output first**)



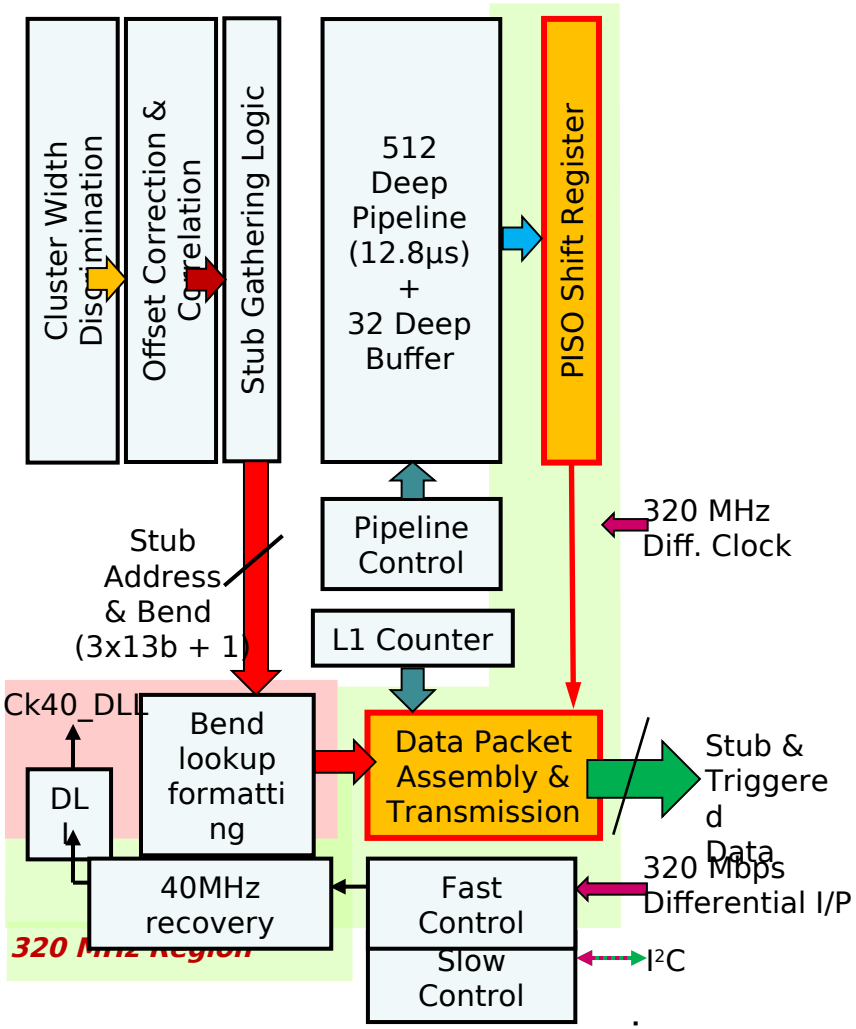
S = Cluster address, B = Bend data
SoF = Stub Overflow (>3 Stubs)
OR254 = any unmasked channel over threshold
Error = latency OR FIFO overflow error
Sync = For synchronisation with CIC
R = Triggered readout data (remains unsparsified)

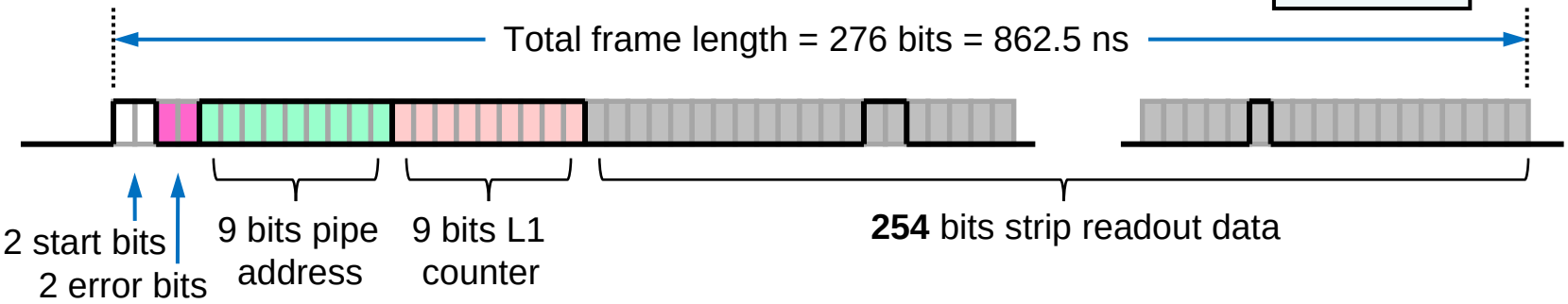
data packet assembly & transmission

trigger rate capability to 1 MHz

data frame comprises

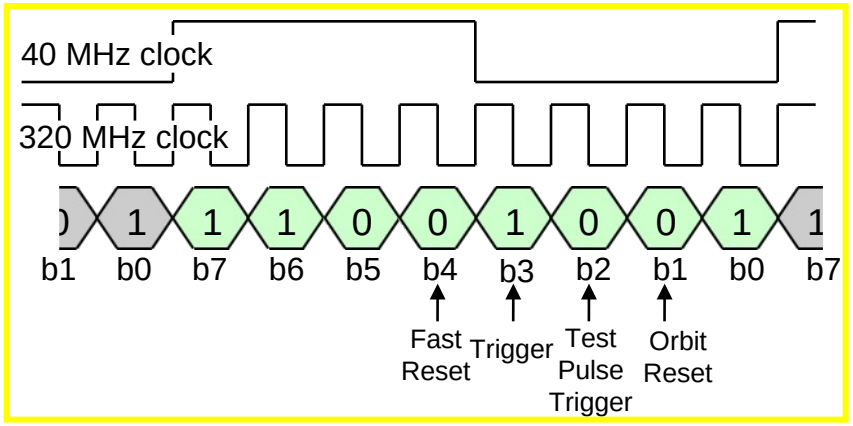
- 2 start bits
- 2 error bits (latency & FIFO overflow)
- 9 bits pipe address (triggered pipeline location)
- 9 bits L1 counter
  - reset by fast reset OR dedicated reset
    - e.g. every orbit
- 254 bits strip readout data
  - channel order 254, 253, … 3, 2, 1





fast and slow control

fast control

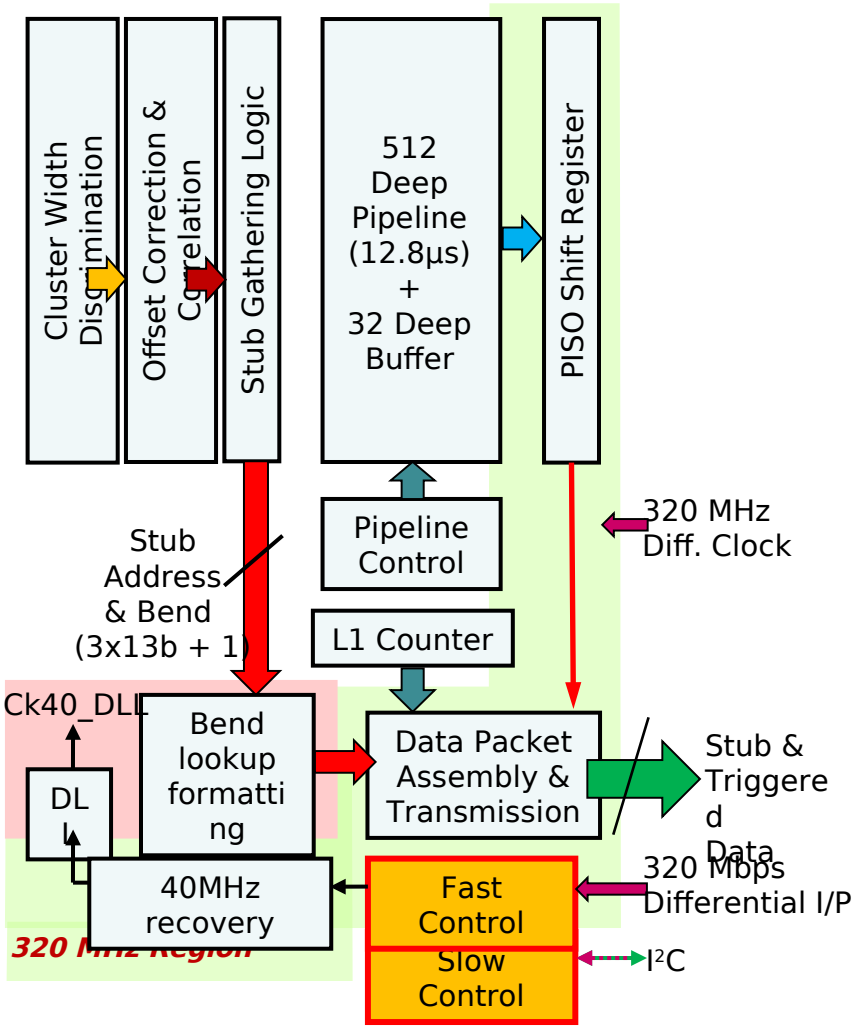


320 Mbps differential stream

40 MHz clock generated from fixed pattern in fast control data

commands are:

- fast reset
- trigger
- test pulse trigger
- L1 counter reset



slow control

I2C @ 1 MHz

CBC3 miscellaneous

clocks

320 MHz differential

test pulse feature

same as CBC2

SEU immunity

I2C register immunity to be improved by using Whitaker cells

for results see http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_SEU_Kirika_Nov_14.pdf

ionizing radiation tolerance

pipeline cell design to be modified to eliminate leakage effect at low doses

for results see http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_TID_Davide_Nov_14.pdf

power

originally 1.2 V ± 10% **(but more likely to be 1.25 ± 0.05 in the final system)**

on-chip LDO to generate analogue power rail

on-chip DC-DC conversion abandoned

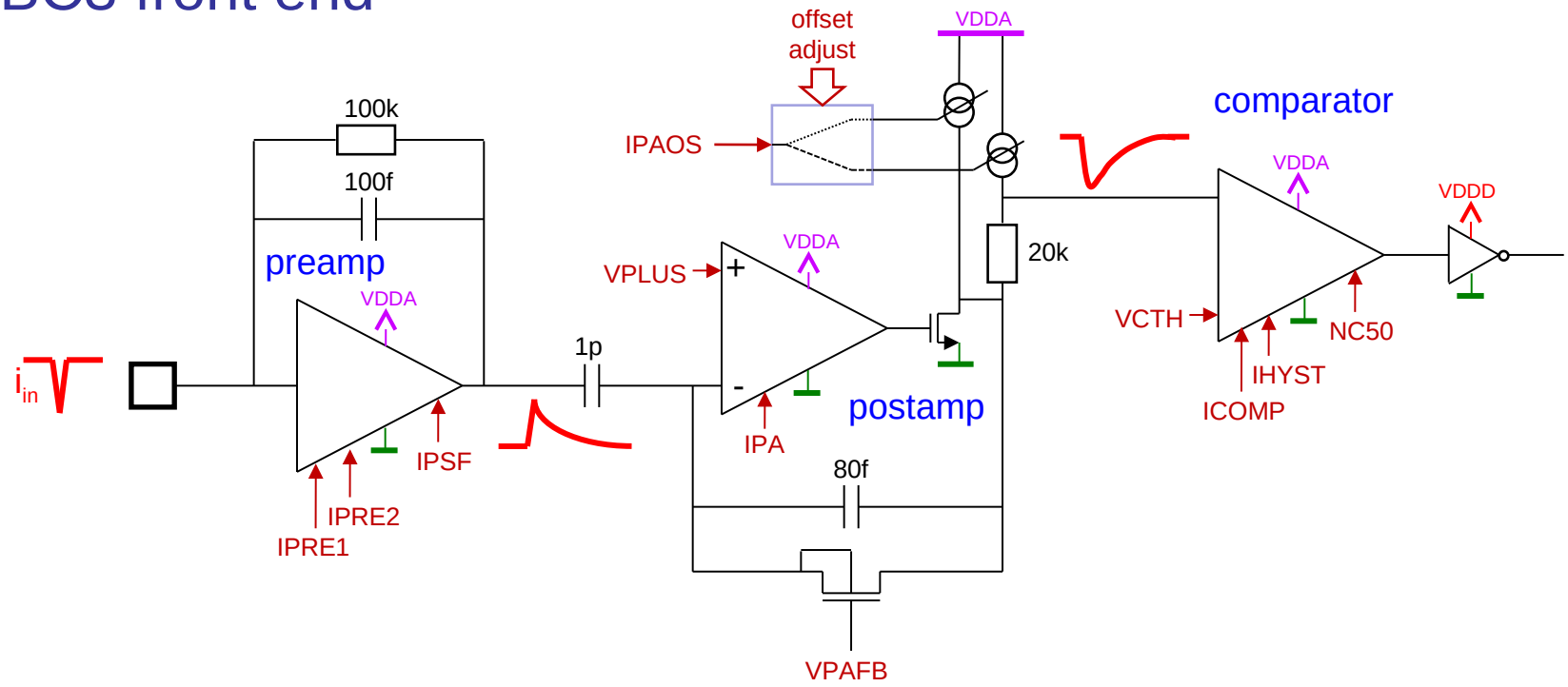
target power consumption for 5 cm strips 450 uW/channel

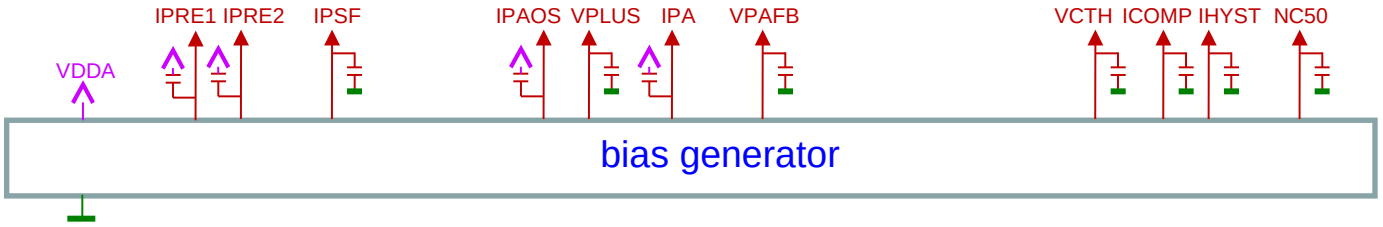
pads

250 um pitch, same as CBC2

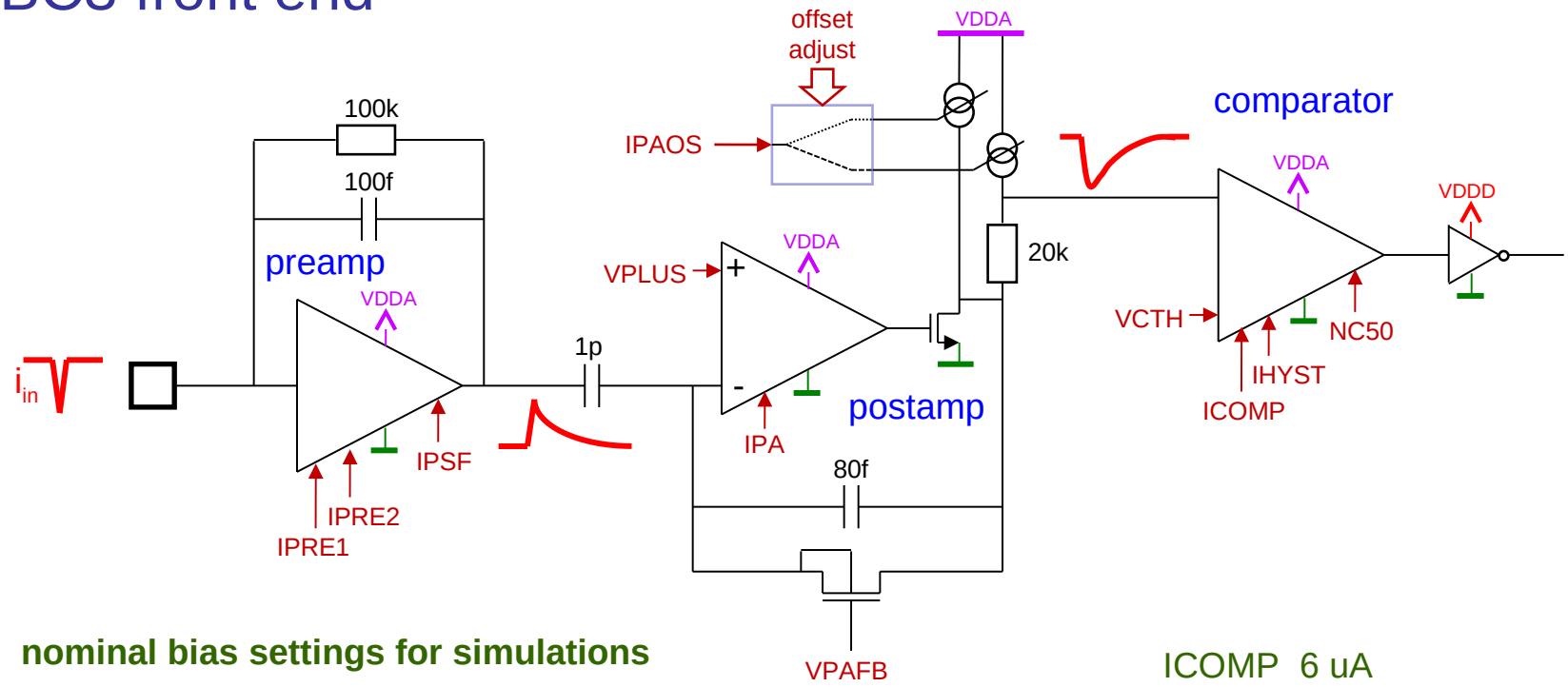
wire-bondable column for probing and other tests

CBC3 front end





CBC3 front end



nominal bias settings for simulations

IPRE1 35 uA
(current in preamp I/P device = IPRE1 x 6)
IPRE2 20 uA
IPSF 20 uA

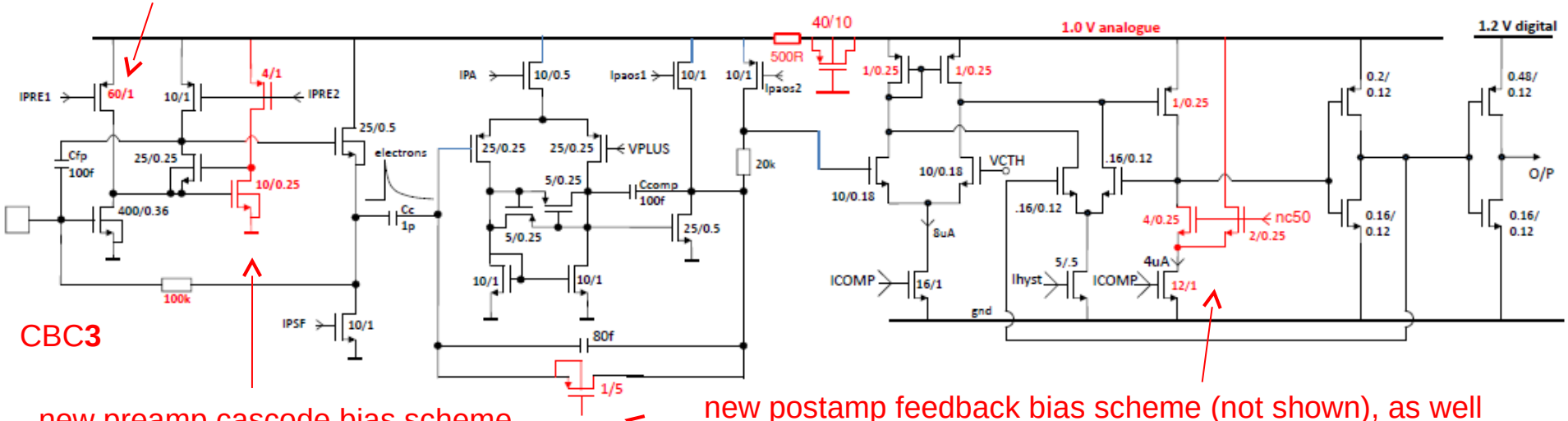
IPA 20 uA
IPAOS 6 uA
VPLUS (VPLUS2) 0.5V
VPAFB, 4 bit value, decimal 7
offset adj., 8 bit val., decimal 128

ICOMP 6 uA
(NC50 derived from ICOMP)
IHYST, 4 bit value, decimal 0
VCTH, as required

unless otherwise stated, these are the values used for the simulations here

CBC2 vs. CBC3

increase in bias FET
allows higher currents

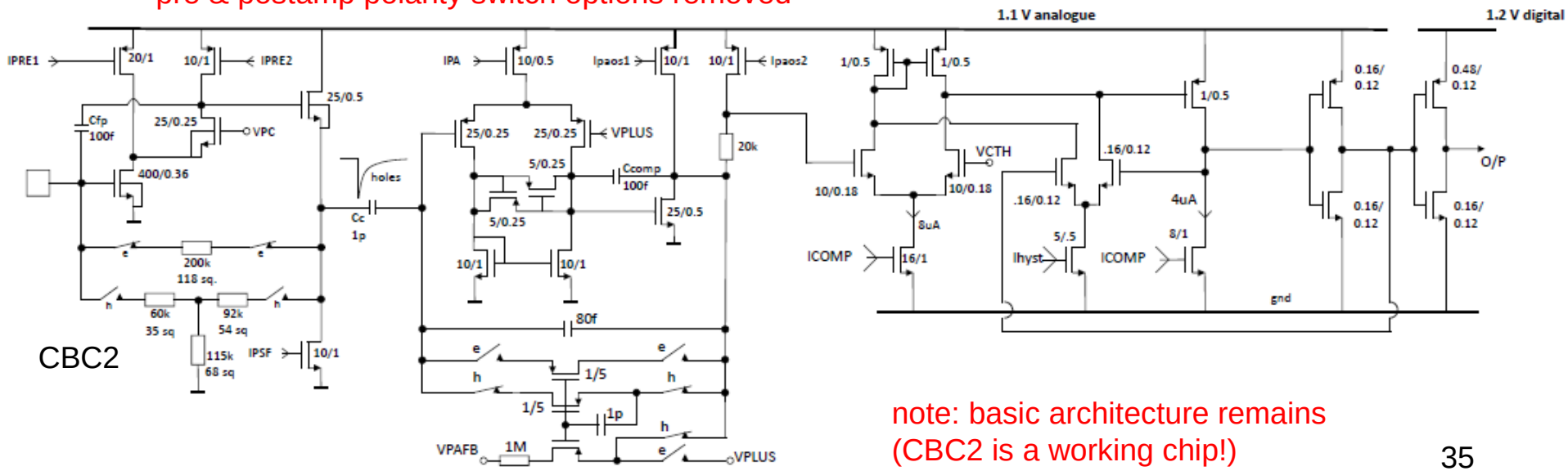


CBC3

new preamp cascode bias scheme
to eliminate “shadow effect”

new postamp feedback bias scheme (not shown), as well as current neutral comparator, addresses CM effects observed when many channels fire

pre & postamp polarity switch options removed



CBC2

note: basic architecture remains
(CBC2 is a working chip!)

simulation conditions and corners

VDDA = 1.0 V

this is worst case (least headroom for operation)
in practice (in experiment) will probably tweak bandgap to be slightly higher than 0.5 so that VDDA will be slightly higher than 1.0 (perhaps 1.05)
note: for CBC1 and 2 VDDA was expected to be 1.1, so some small changes have been made to ensure operation at 1.0

temperature = -20, +30

nominal operating temperature will be around 0
will want to test at room temperature

process corners

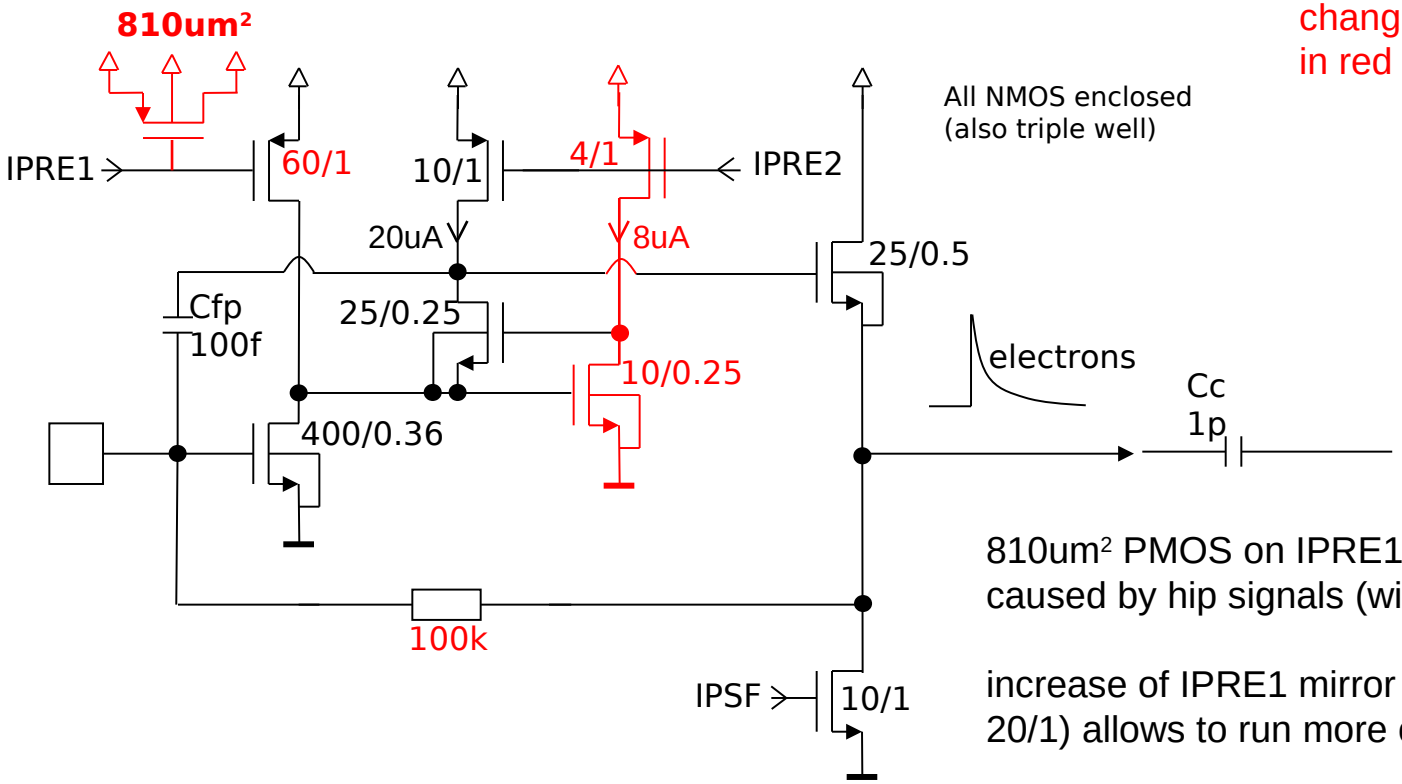
tt, ff, ss, sf, fs (not pushing to extreme ffc, ssc)

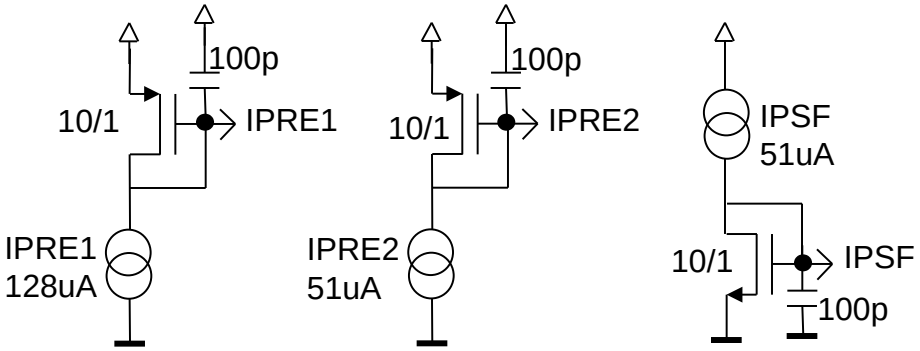
all simulations use extracted circuit files unless otherwise indicated

CBC3 preamplifier

CBC3 preamp

changes from CBC2 highlighted in red





810um² PMOS on IPRE1 decouples disturbance caused by hip signals (will discuss in hips sect'n)

increase of IPRE1 mirror device to 60/1 (from 20/1) allows to run more current in input device

regulated cascode gives higher open loop gain, while simultaneously providing self-biasing of cascode (cures shadow effect)

feedback resistor reduced to 100k (from 200k) to get faster pulse shape

(T network for holes polarity signals removed)

input device choice

CBC2 I/P device = 400/0.36 (C_{GS} ~ 1pF)

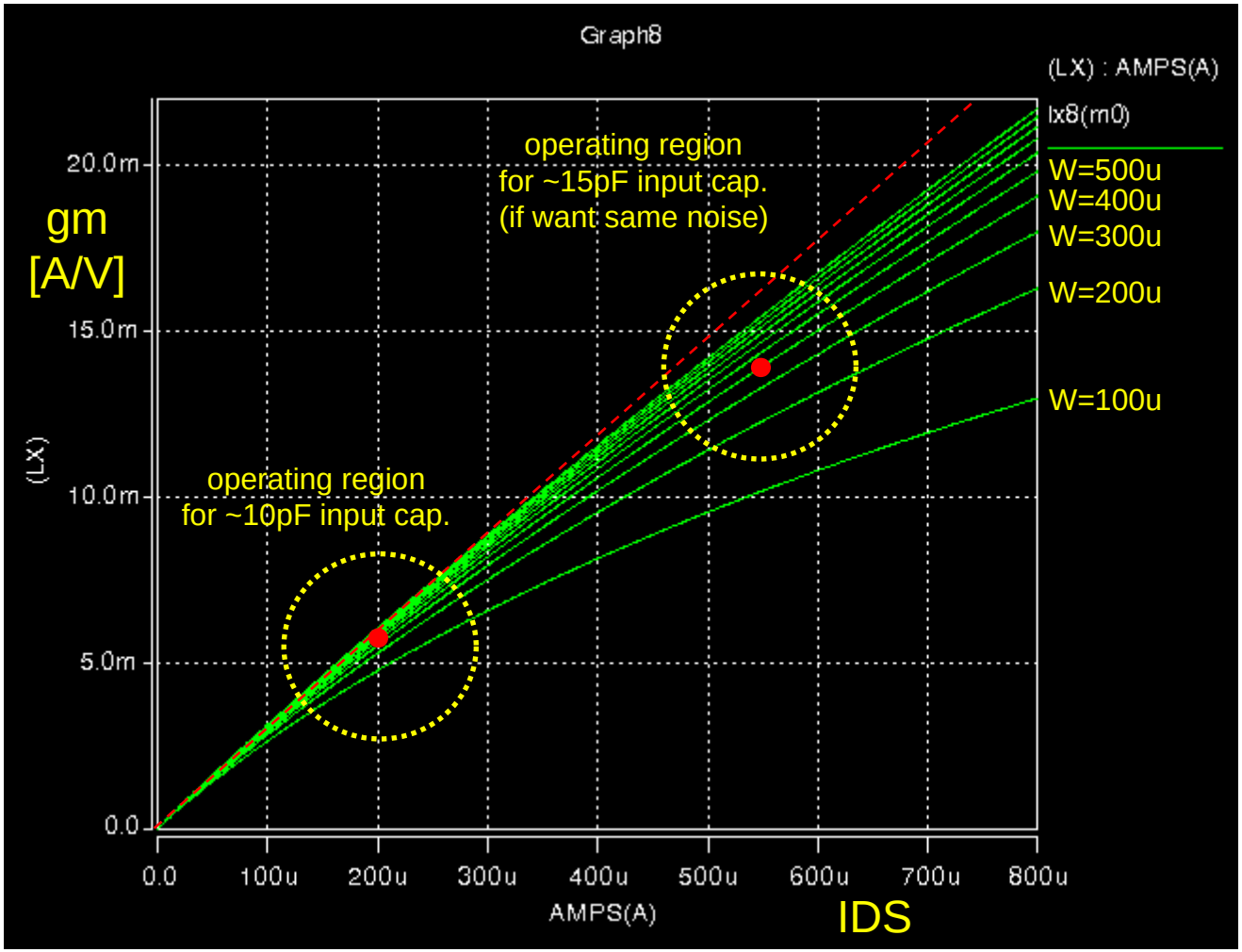
(length chosen to avoid 1/f corner penalty - see CBC1 design review)

do we need to increase width if need to run at higher IDS to cope with higher sensor capacitance?

- plot says not much to be gained - still in weak inversion for higher currents
- most likely to be operating in 150 - 300 uA range
- increasing width significantly will only give C_{GS} penalty with no g_m enhancement

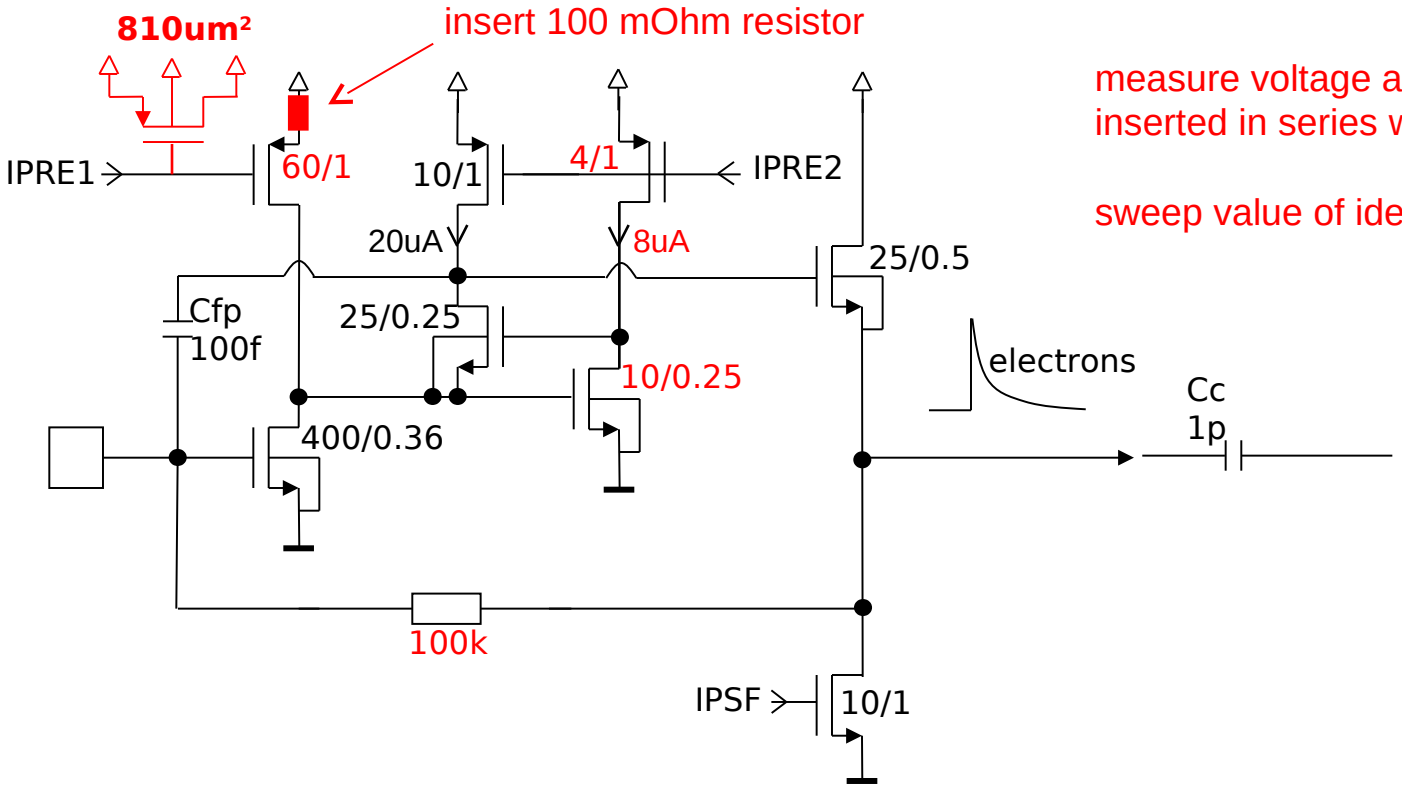
noise α $C/\sqrt{I_{DS}}$

(g_m α I_{DS})



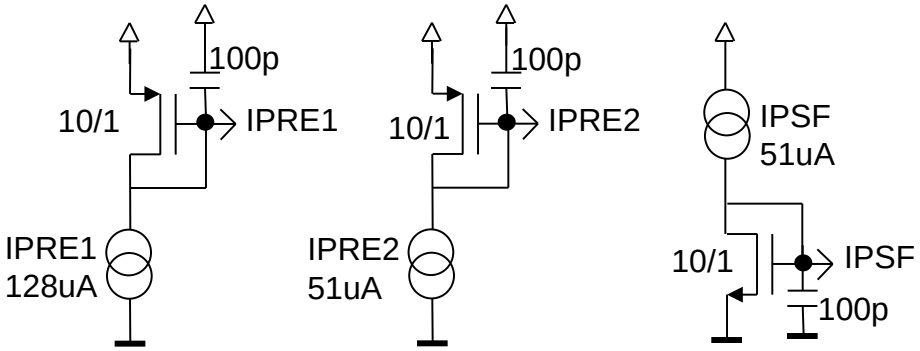
stick with W/L = 400/0.36

CBC3 preamp: check IPRE1 mirroring



measure voltage across small resistor inserted in series with 60/1 source

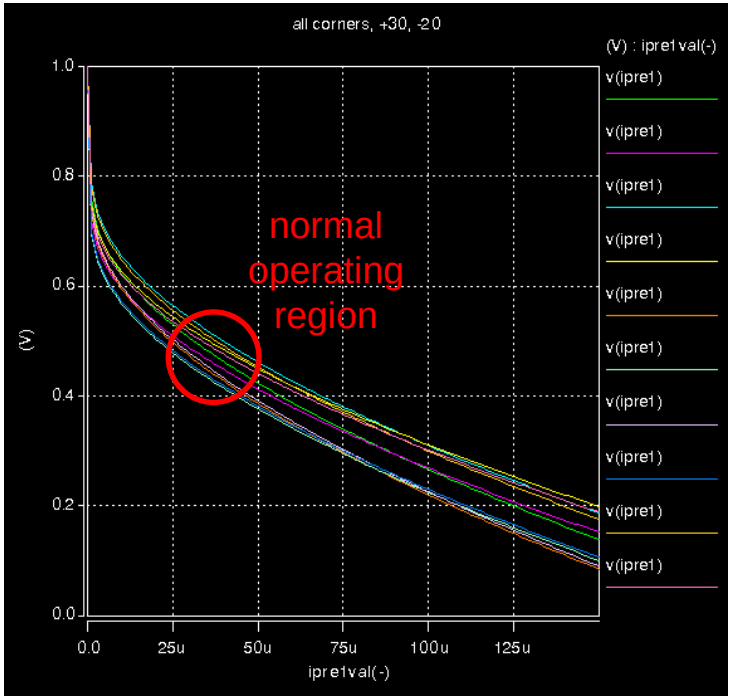
sweep value of ideal current source IPRE1

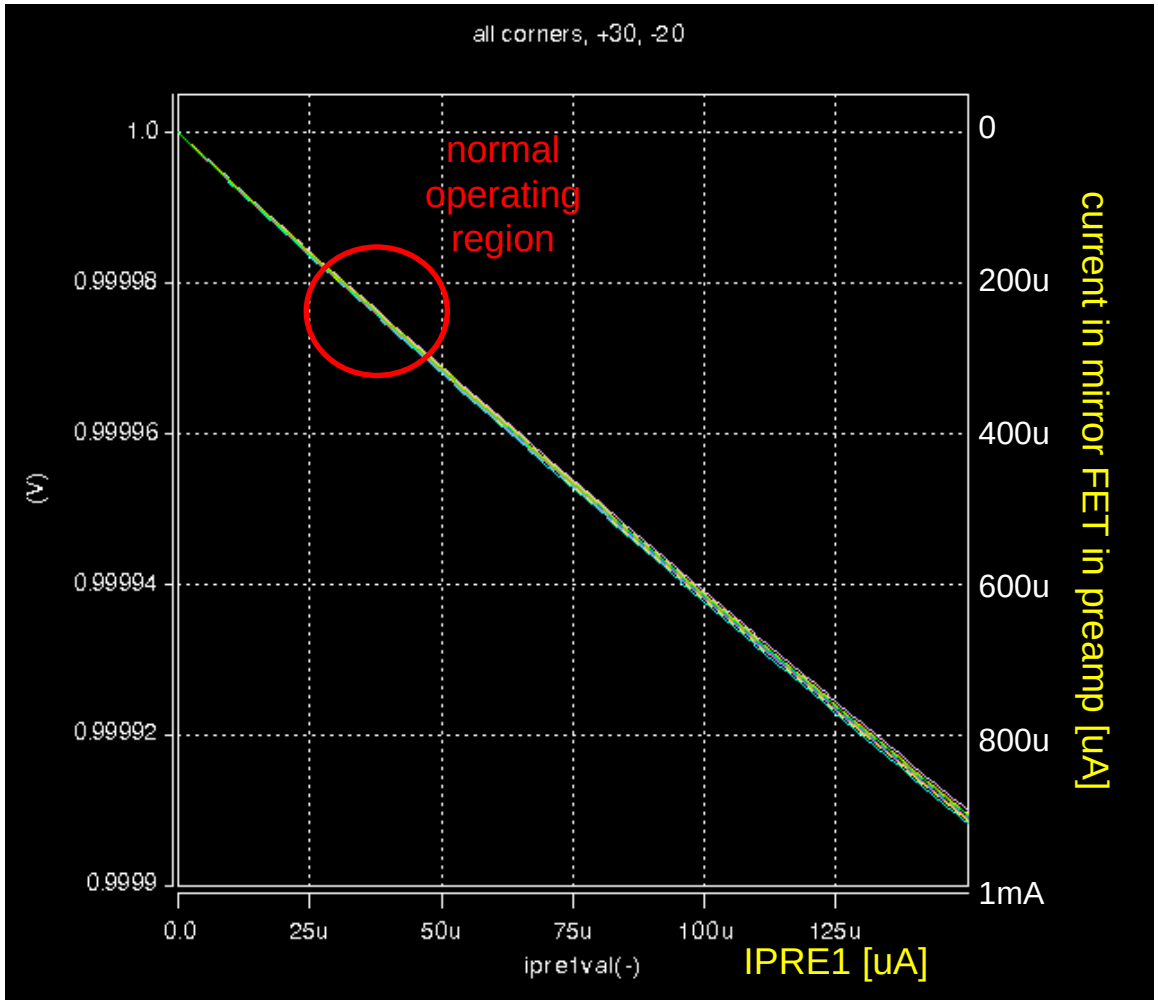


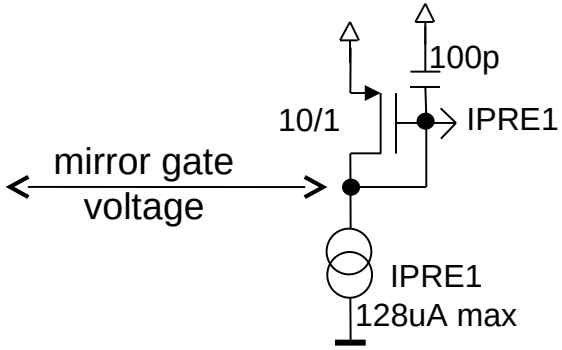
IPRE1 mirroring

current mirrors well if IPRE1 produced by ideal current source

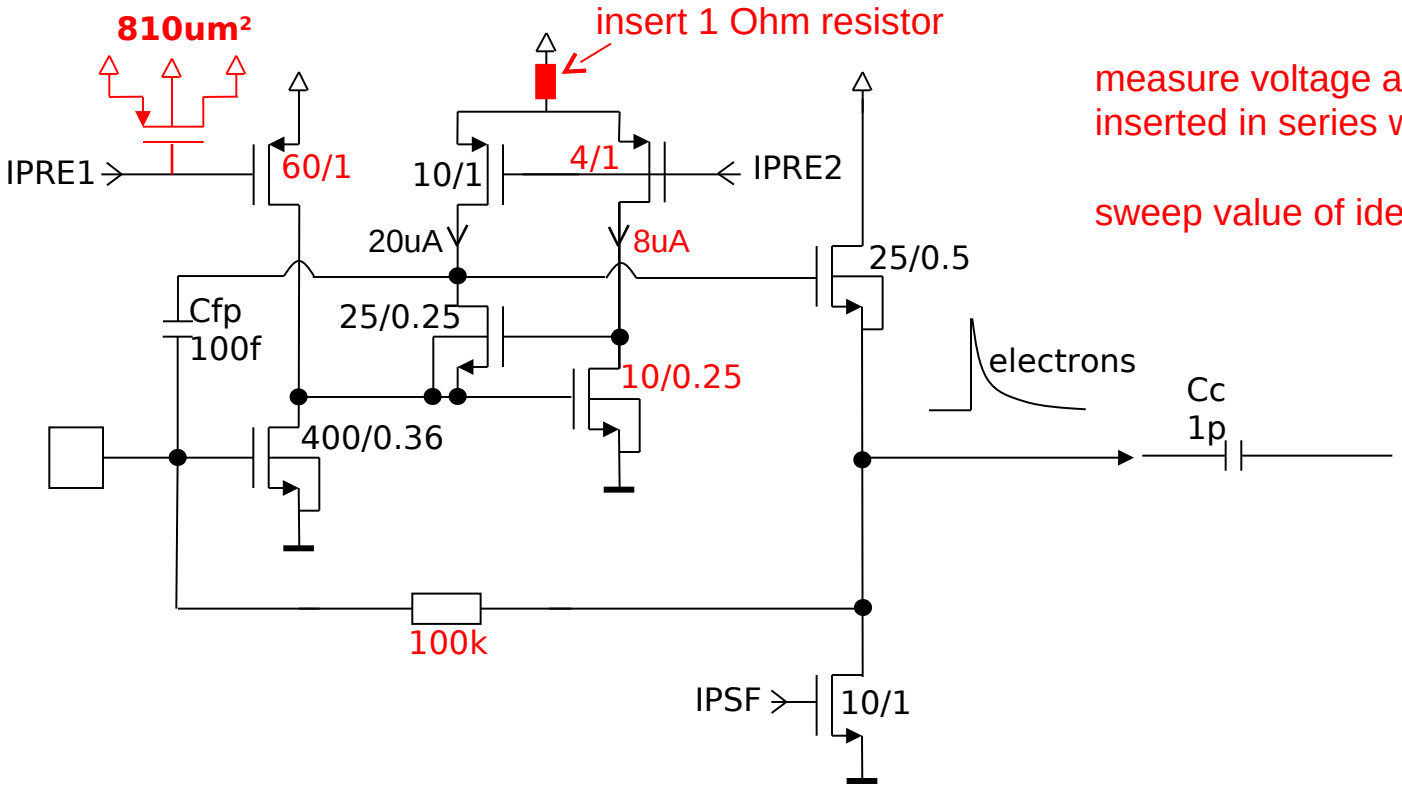
current in mirror device ~ 6 x IPRE1

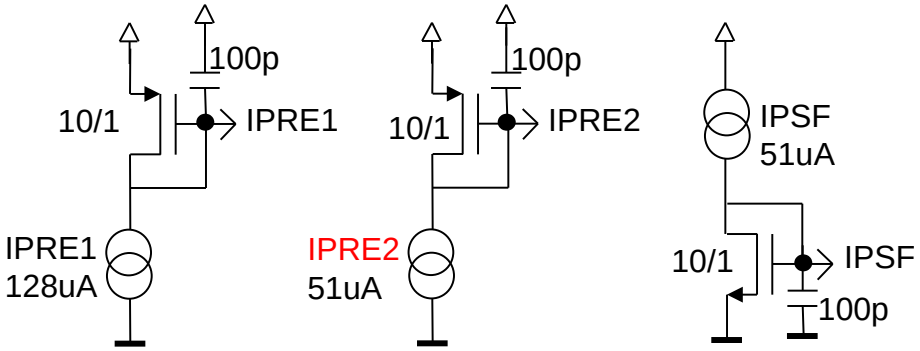






CBC3 preamp: check IPRE2 mirroring





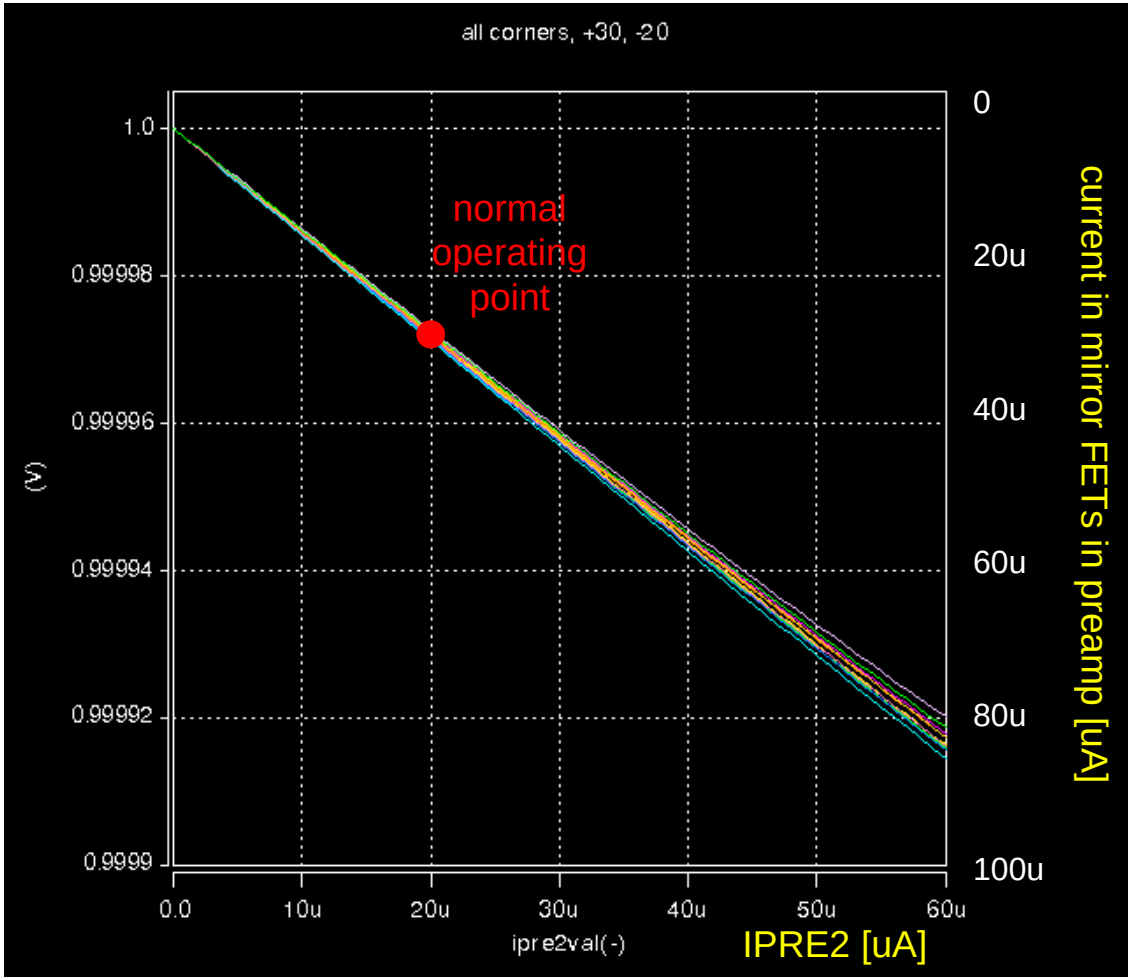
measure voltage across small resistor inserted in series with IPRE2 mirror devices

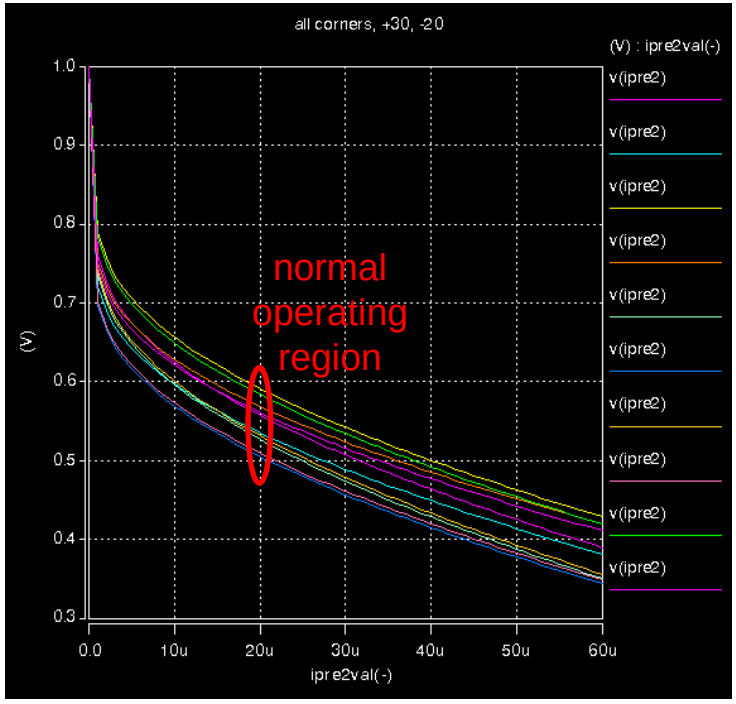
sweep value of ideal current source IPRE2

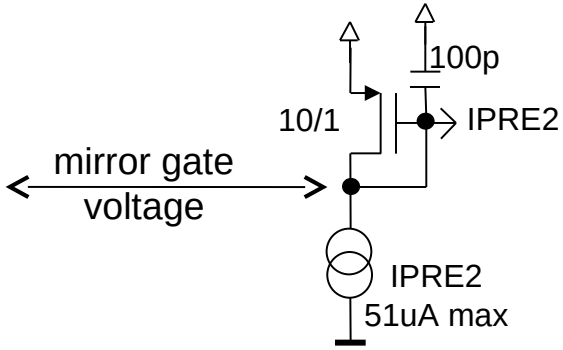
IPRE2 mirroring

current mirrors well if IPRE2
produced by ideal current source

current in mirror device ~ 1.33 x IPRE2
(ideally 1.40)







I/P device bias currents for simulation

normal strip length = 5 cm

Cstrip = 5 x (1.7 pF/cm) = 8.5 pF
add something for stray (e.g. tracking on hybrid)

Cin = 10 pF

input device current ~ 210 uA [+ 20 uA (IPRE2)]

=> IPRE1 = 35 uA

longer strip length = 8 cm

Cstrip = 13.6 pF
add something for stray

Cin = 15 pF

noise α C/$\sqrt{I_{DS}}$ ($g_m \alpha I_{DS}$)
so to get same noise for C x 1.5
then I_{DS} x $(1.5)^2$ = 2.25

input FET current ~ 2.25 x 210 = 540 uA [+ 20 uA (IPRE2)]

=> IPRE1 = 90 uA

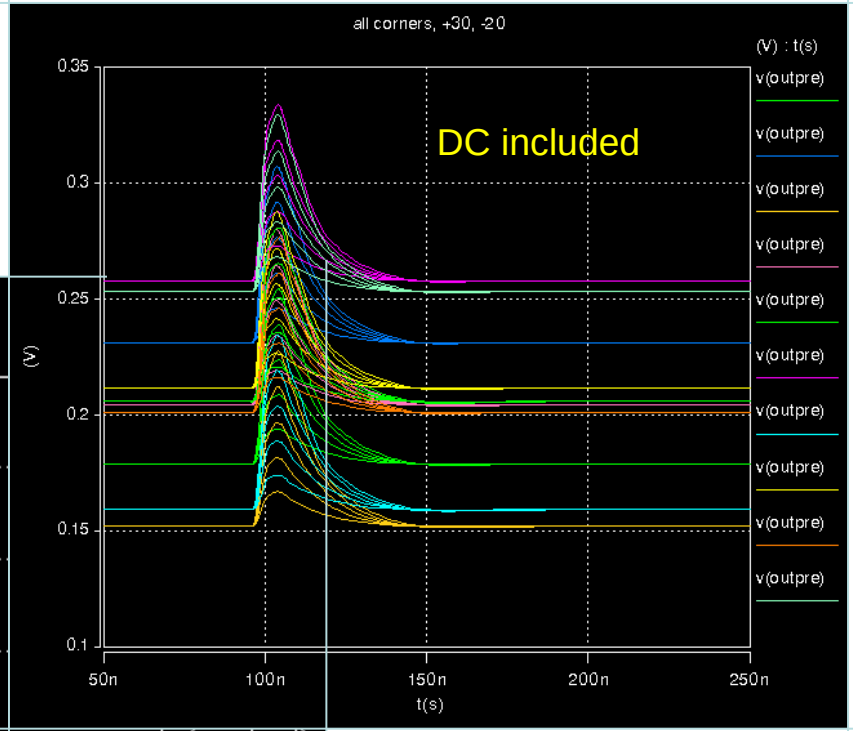
bare chip

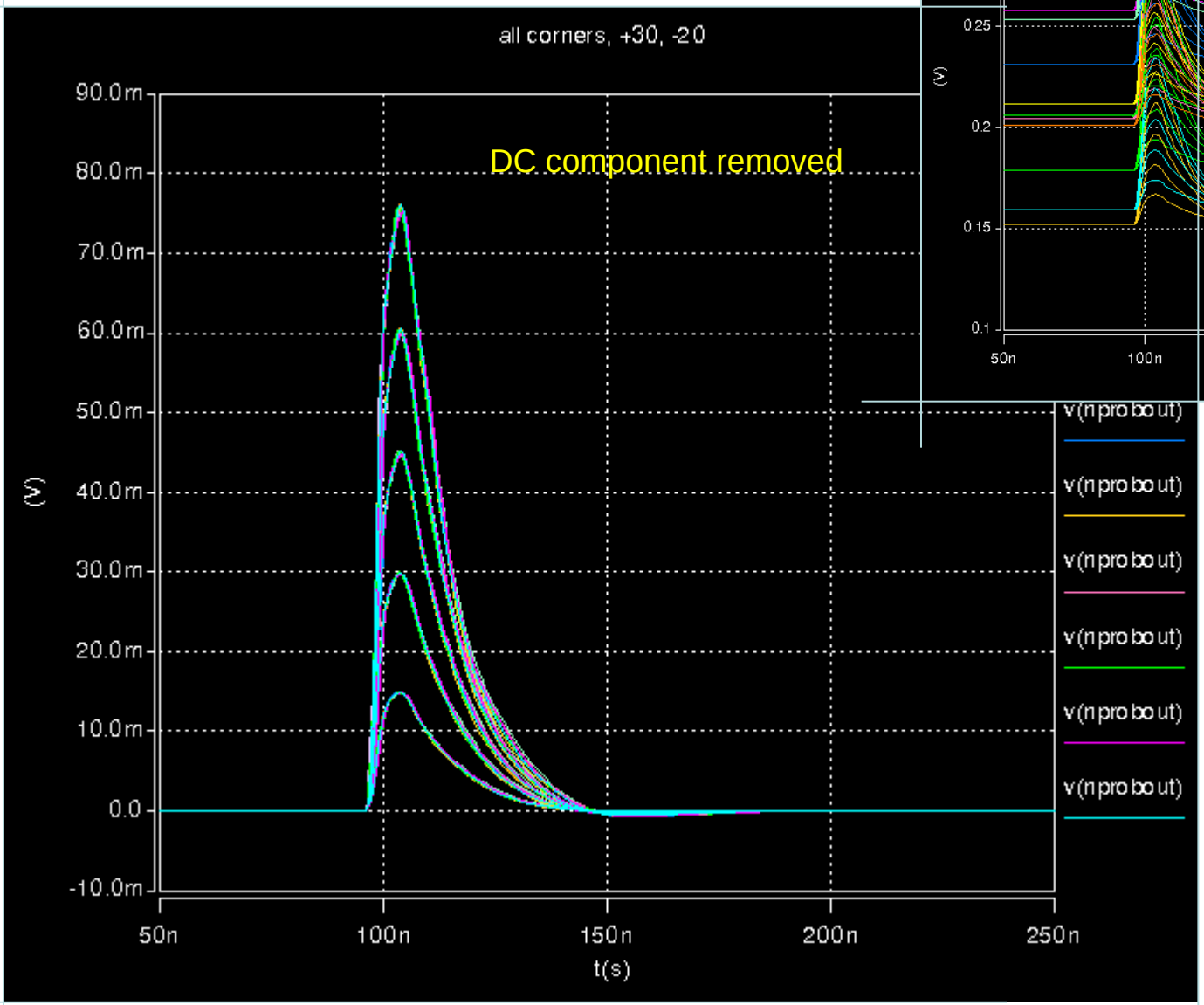
input FET current ~ 30 uA [+ 20 uA (IPRE2)]

=> IPRE1 = 5 uA

preamp O/P

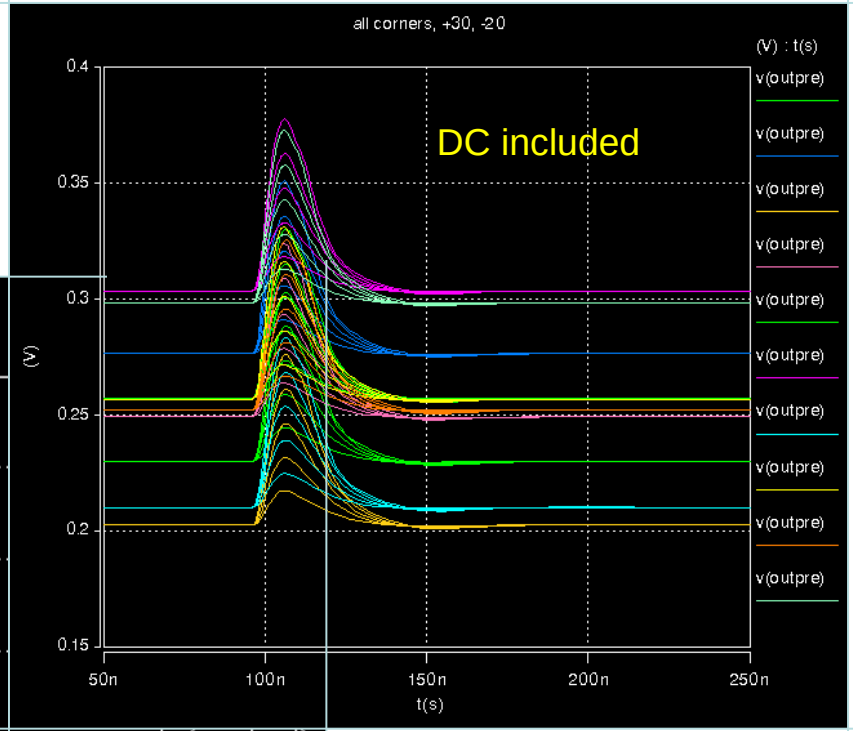
C = 0pF, IPRE1 = 5 uA
all corners, T=+30, -20
signal = (2.5 - 12.5) fC, 2.5 fC steps

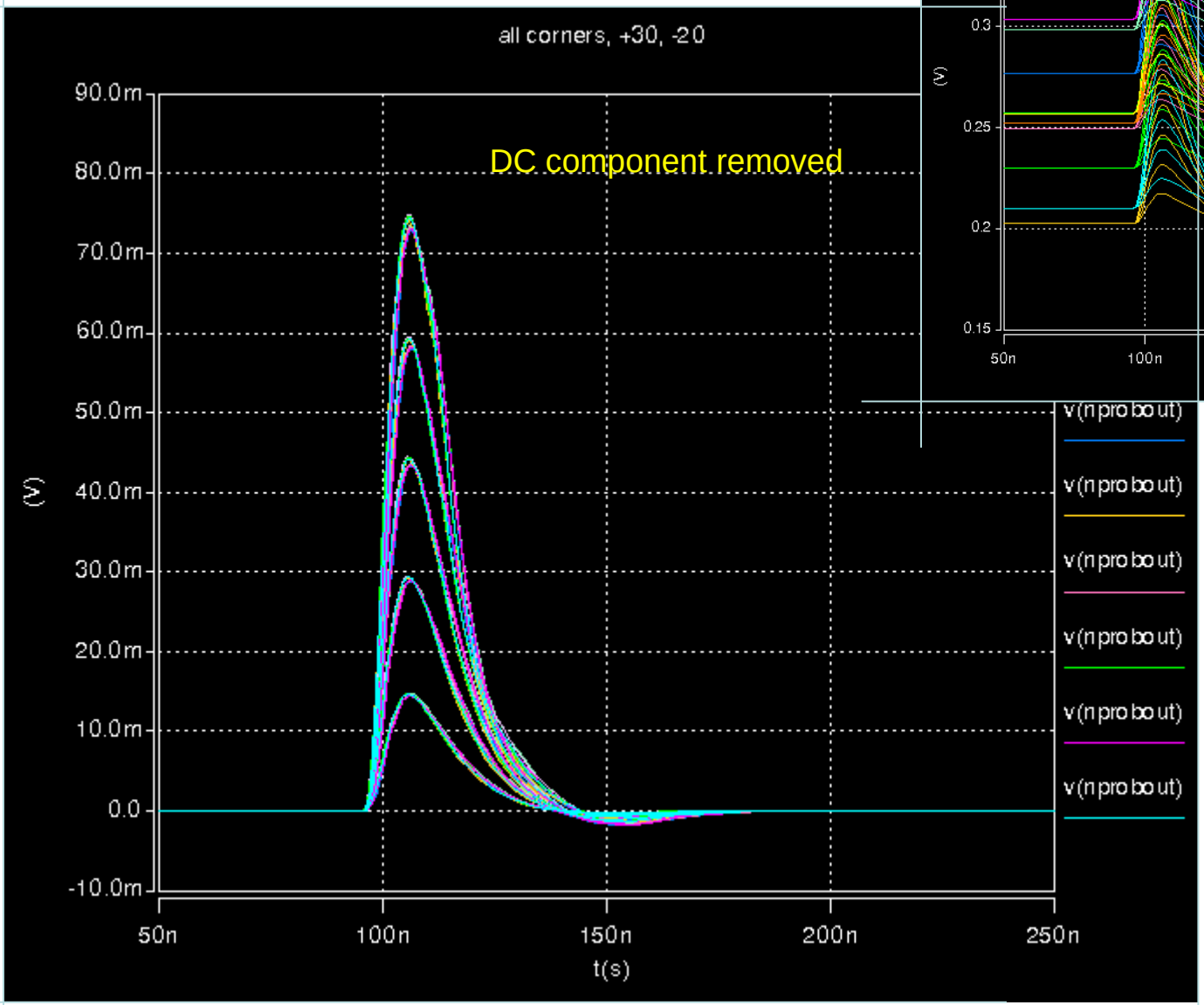




preamp O/P

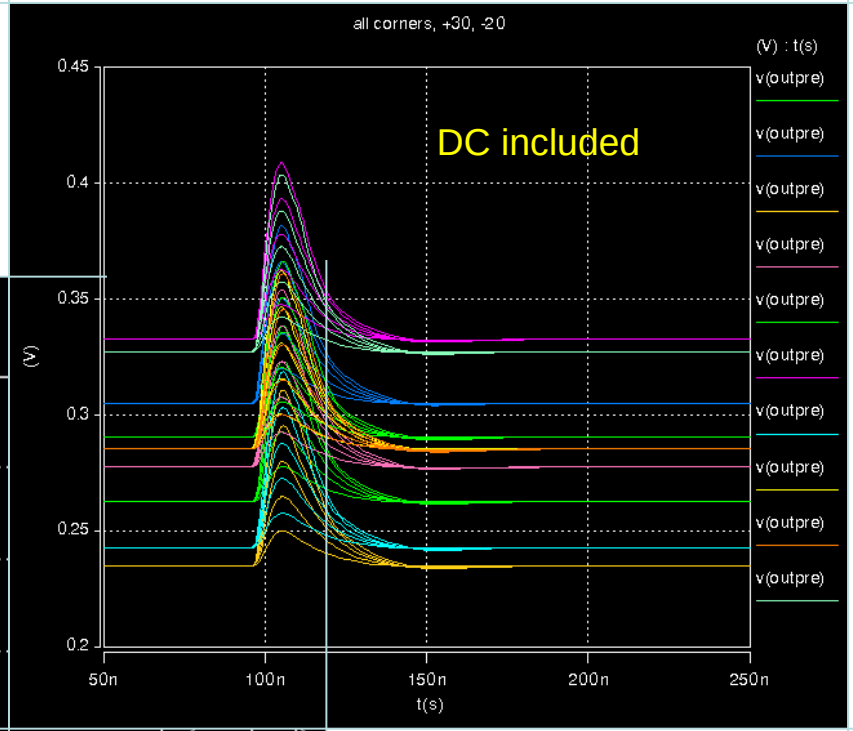
C = 10pF, IPRE1 = 35 uA
all corners, T=+30, -20
signal = (2.5 - 12.5) fC, 2.5 fC steps

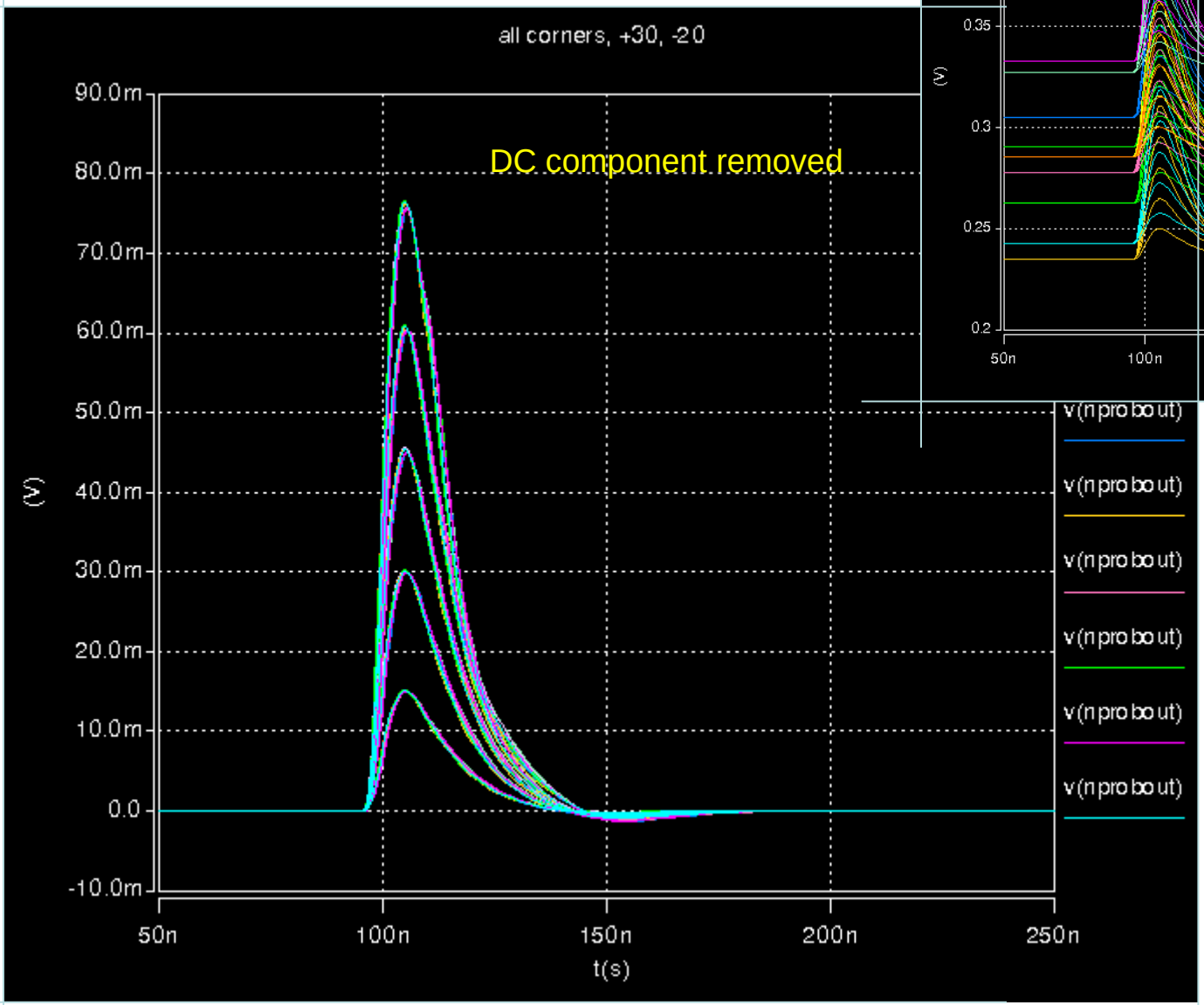




preamp O/P

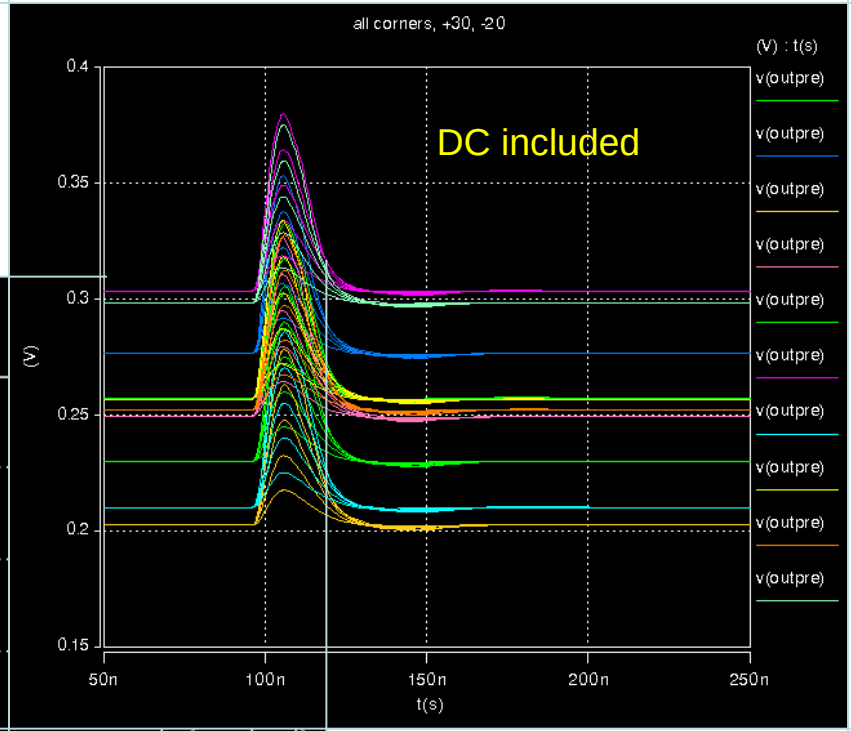
C = 15pF, IPRE1 = 90 uA
all corners, T=+30, -20
signal = (2.5 - 12.5) fC, 2.5 fC steps

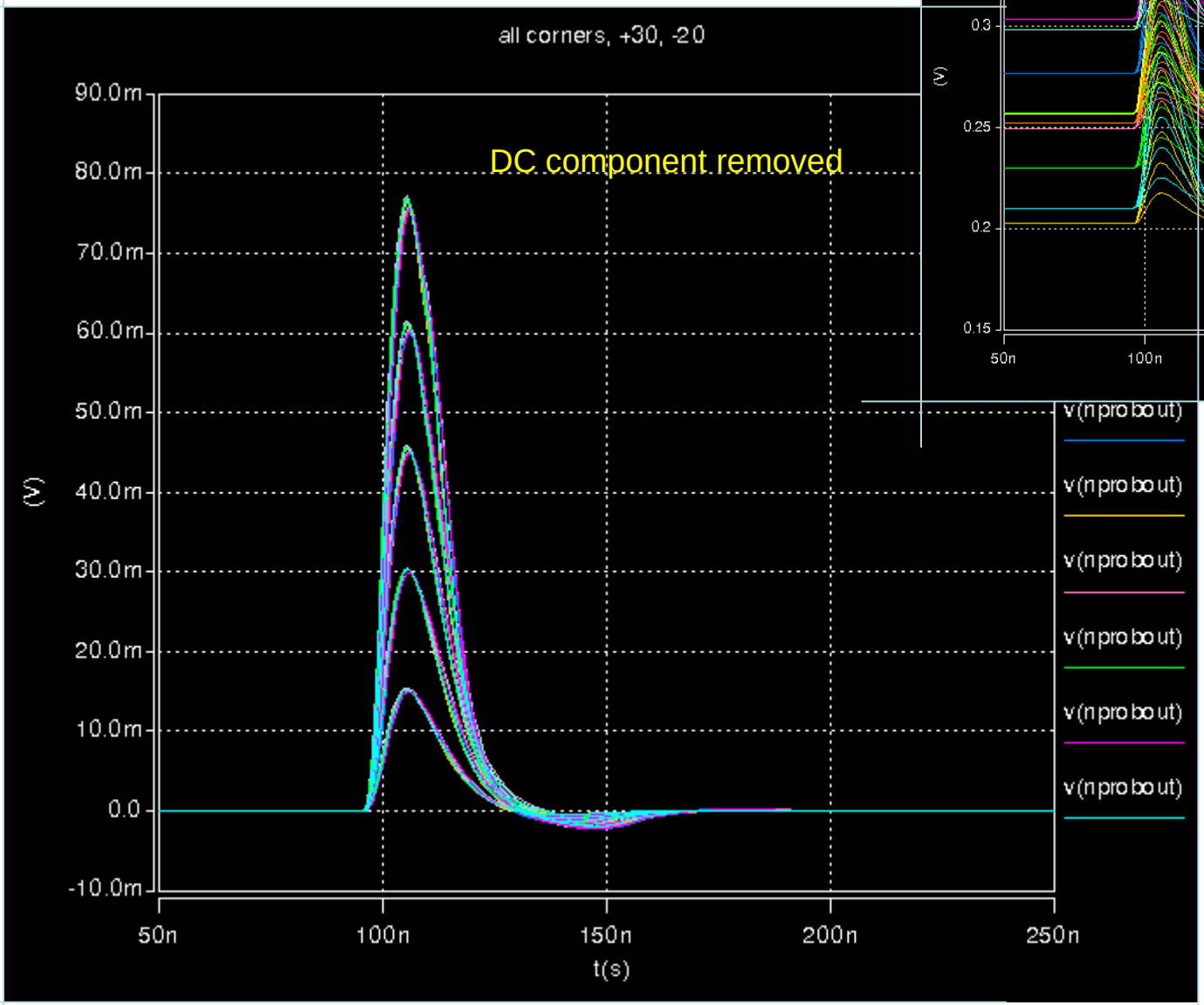




preamp O/P: min. feedback

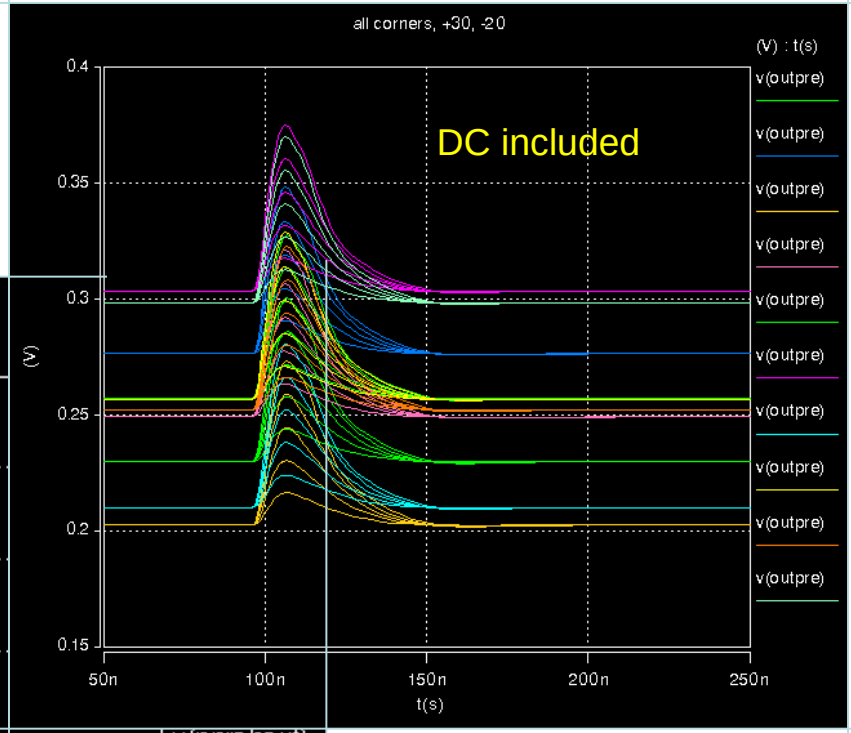
C = 10pF, IPRE1 = 35 uA, Rf=100k - 15% = 85k,
Cf = 100 fF - 10% = 90 fF
all corners, T=+30, -20
signal = (2.5 - 12.5) fC, 2.5 fC steps

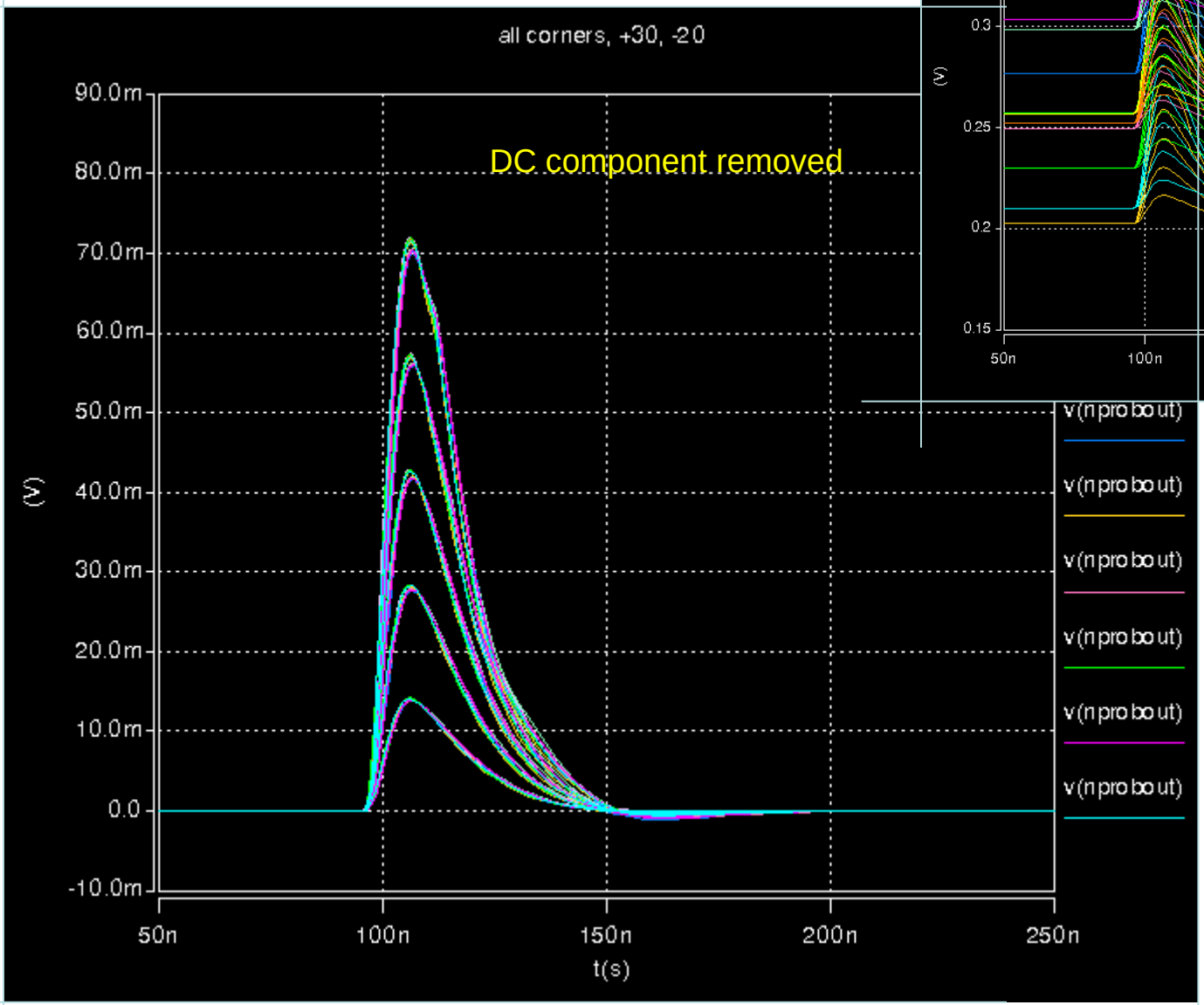




preamp O/P: max. feedback

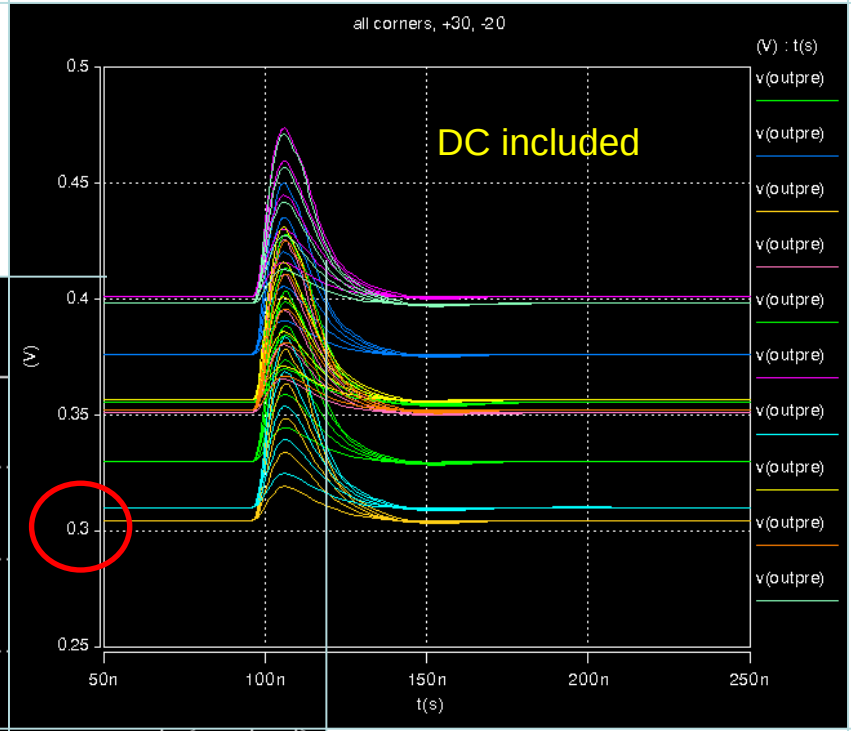
C = 10pF, IPRE1 = 35 uA, Rf=100k +15% = 115k,
Cf = 100 fF + 10% = 110 fF
all corners, T=+30, -20
signal = (2.5 - 12.5) fC, 2.5 fC steps

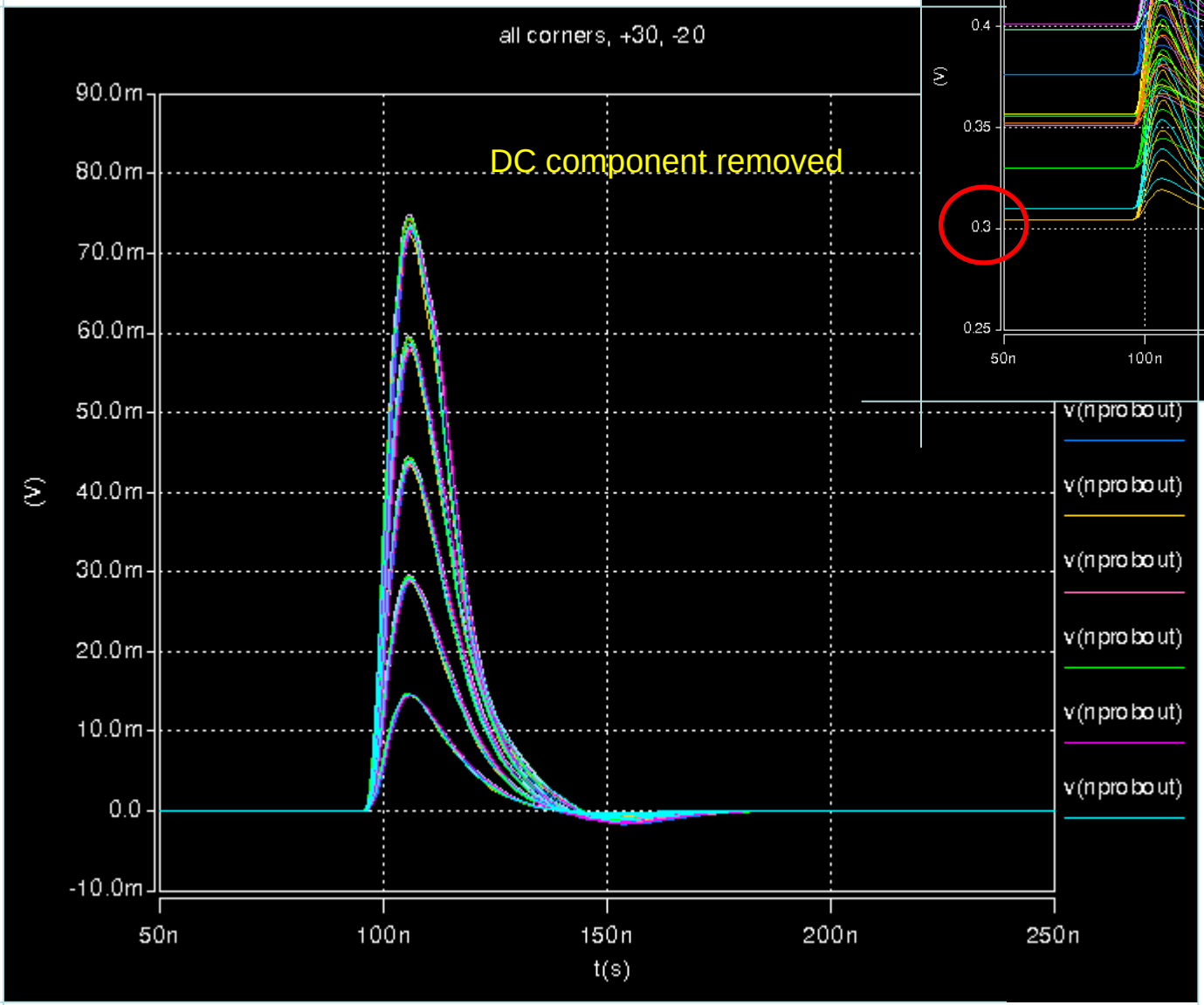




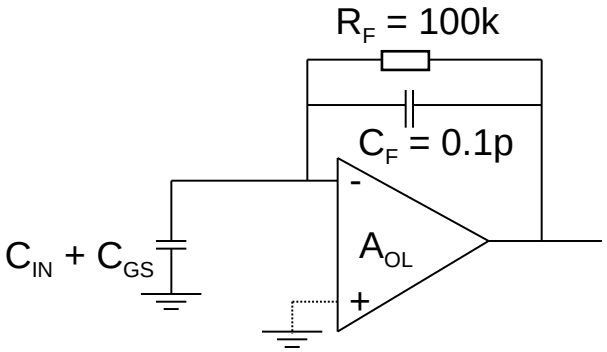
preamp O/P: Ileak=1uA

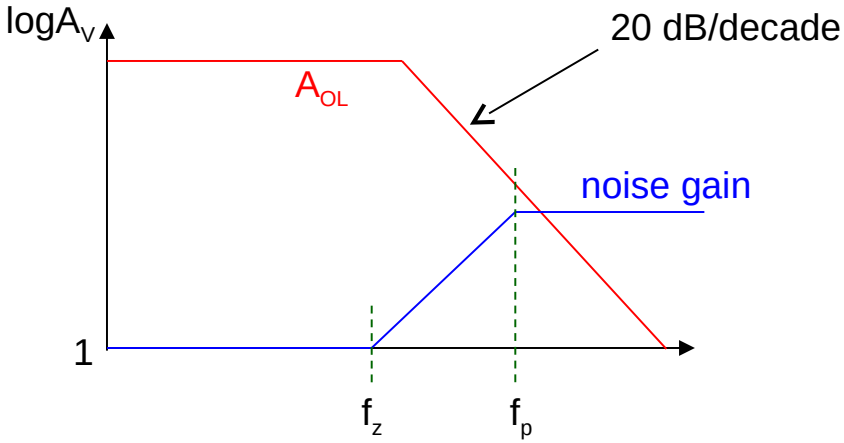
C = 10pF, IPRE1 = 35 uA, Rf = 100k, Cf = 100fF
all corners, T=+30, -20
signal = (2.5 - 12.5) fC, 2.5 fC steps





stability





$f_z = 1/(2\pi R_F(C_{IN}+C_{GS}+C_F))$

= **1.3 MHz** (**C_{IN}=0pF**, C_{GS}=1.1pf)

= **140 kHz** (**C_{IN}=10pF**)

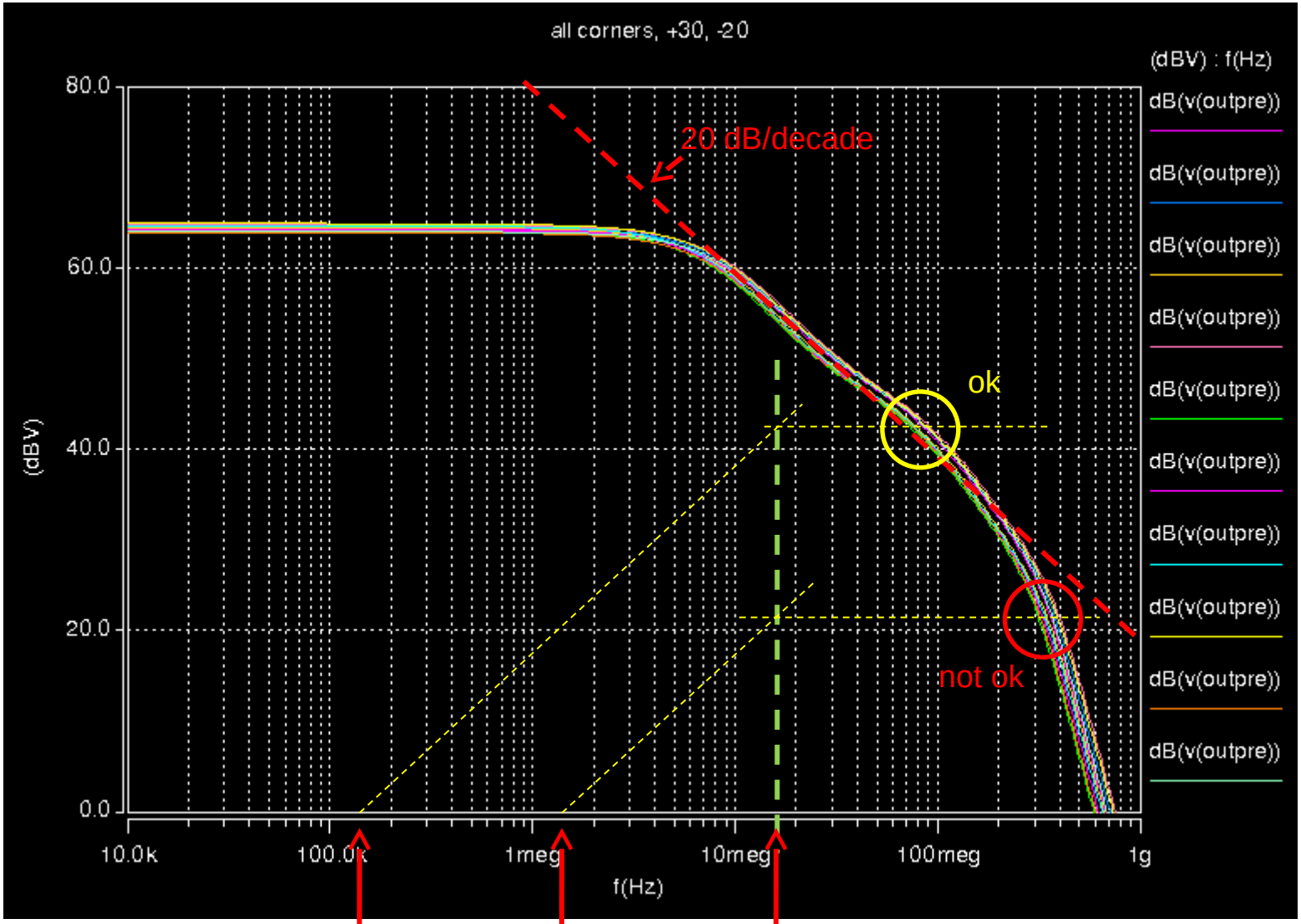
= **100 kHz** (**C_{IN}=15pF**)

$f_p = 1/(2\pi R_F C_F)$

= **16 MHz**

for stability need noise gain to intersect A_{OL} in 20 dB/decade region

preamp open loop: IPRE1 = 35uA



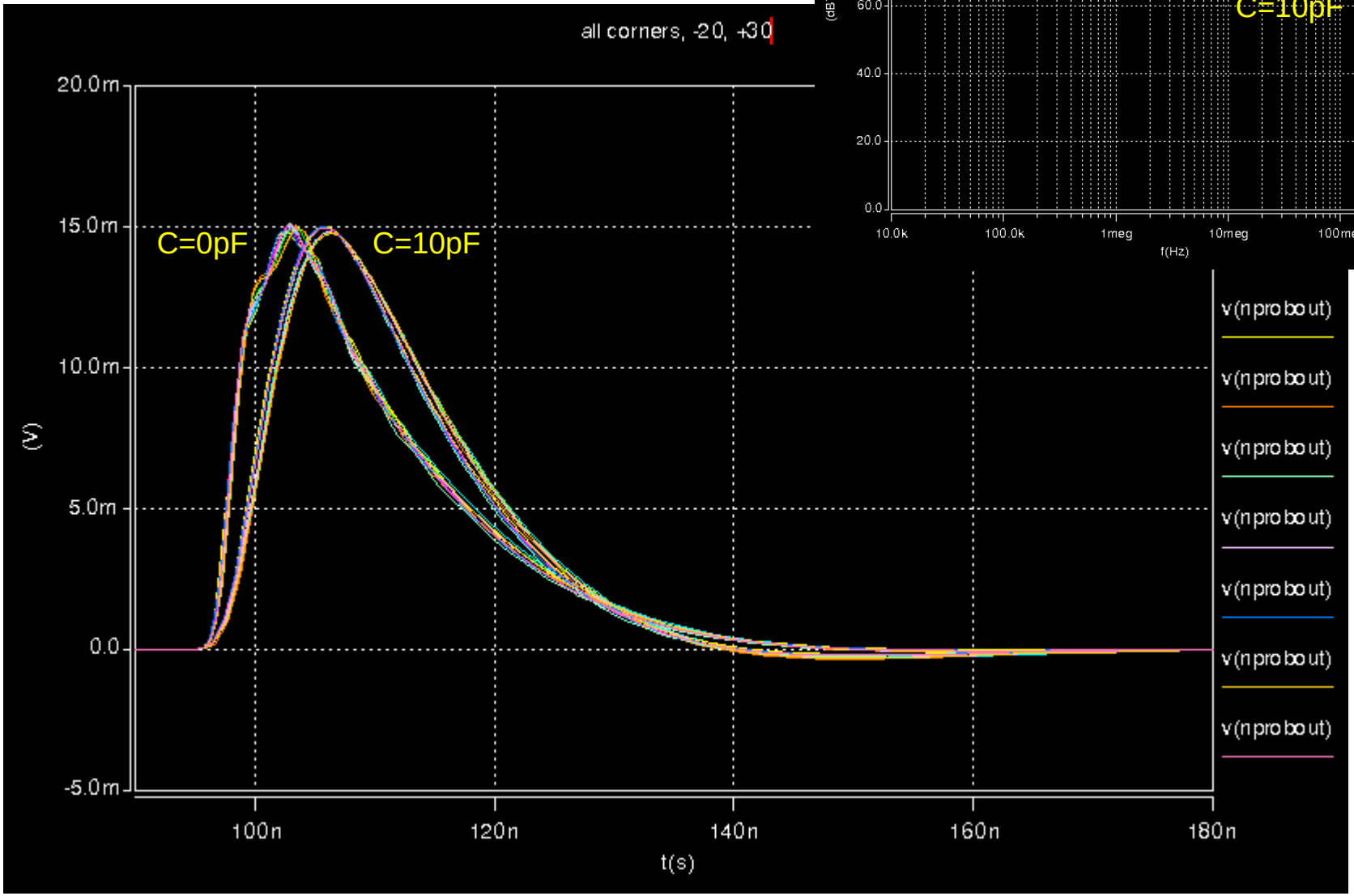
f_z = 140 kHz
C_{IN} = 10 pF

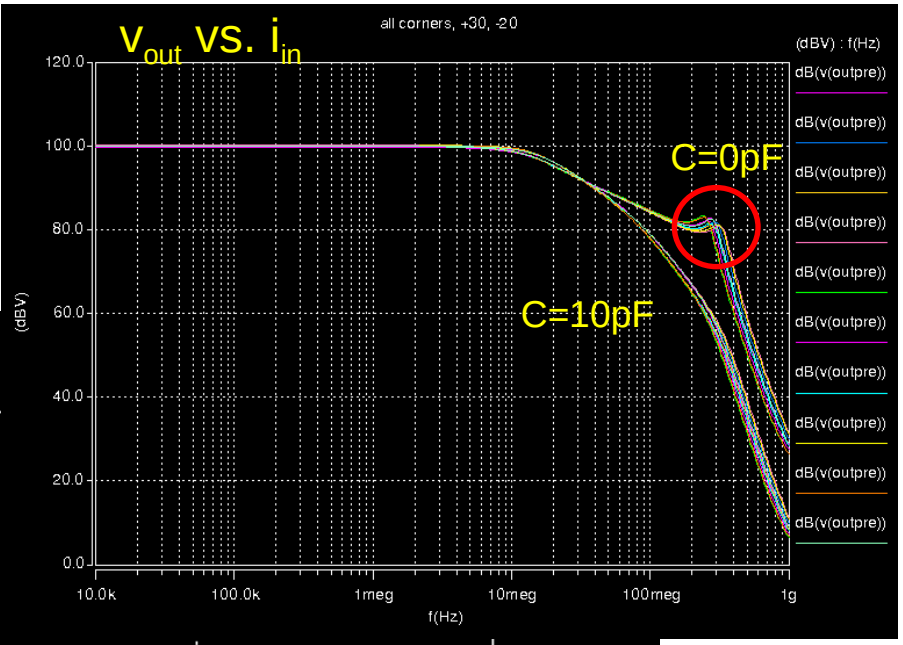
f_z = 1.3 MHz
C_{IN} = 0 pF

f_p = 16 MHz

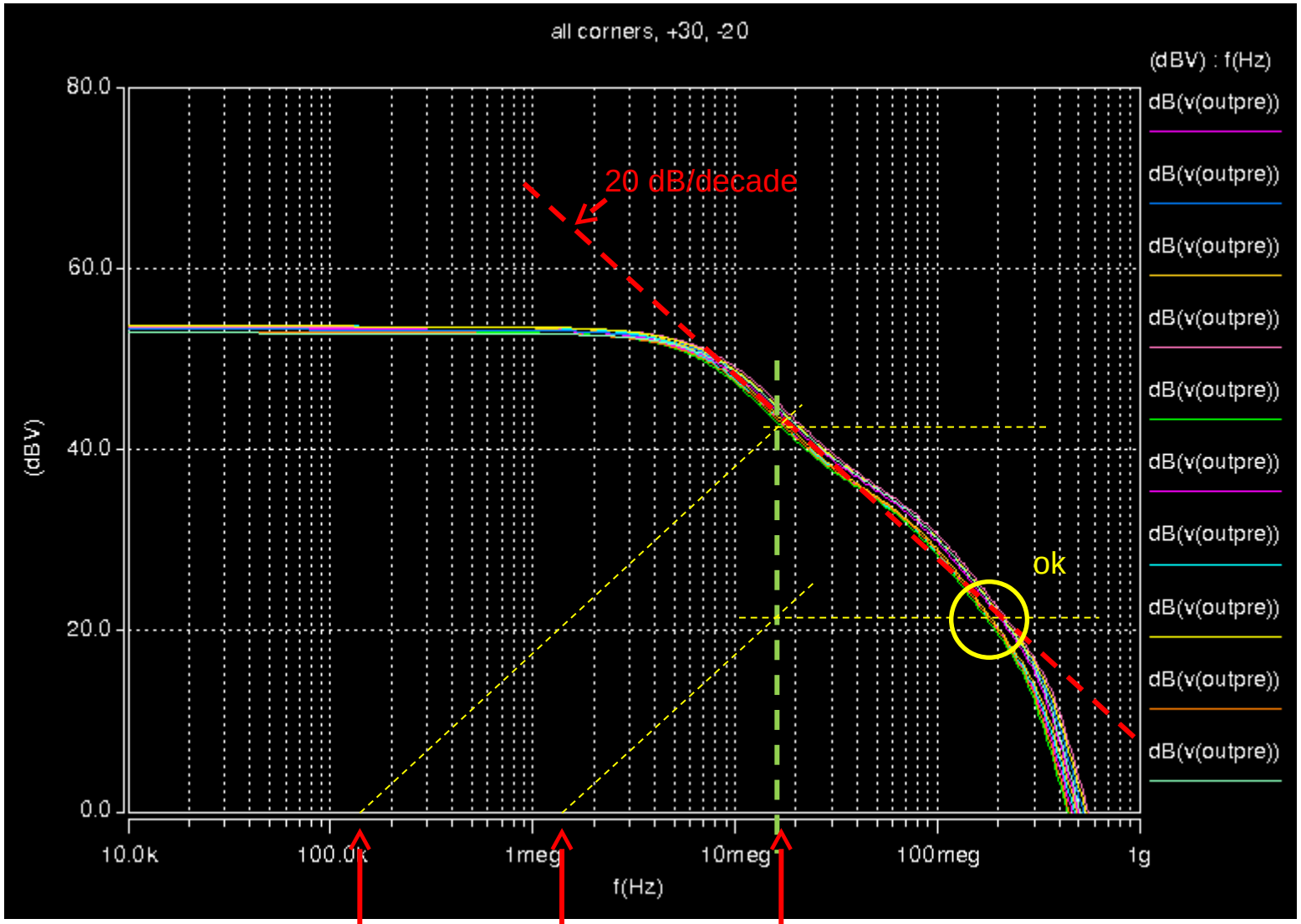
preamp O/P pulseshapes: IPRE1 = 35uA

gain peaking for C=0pF





preamp open loop: IPRE1 = 5uA

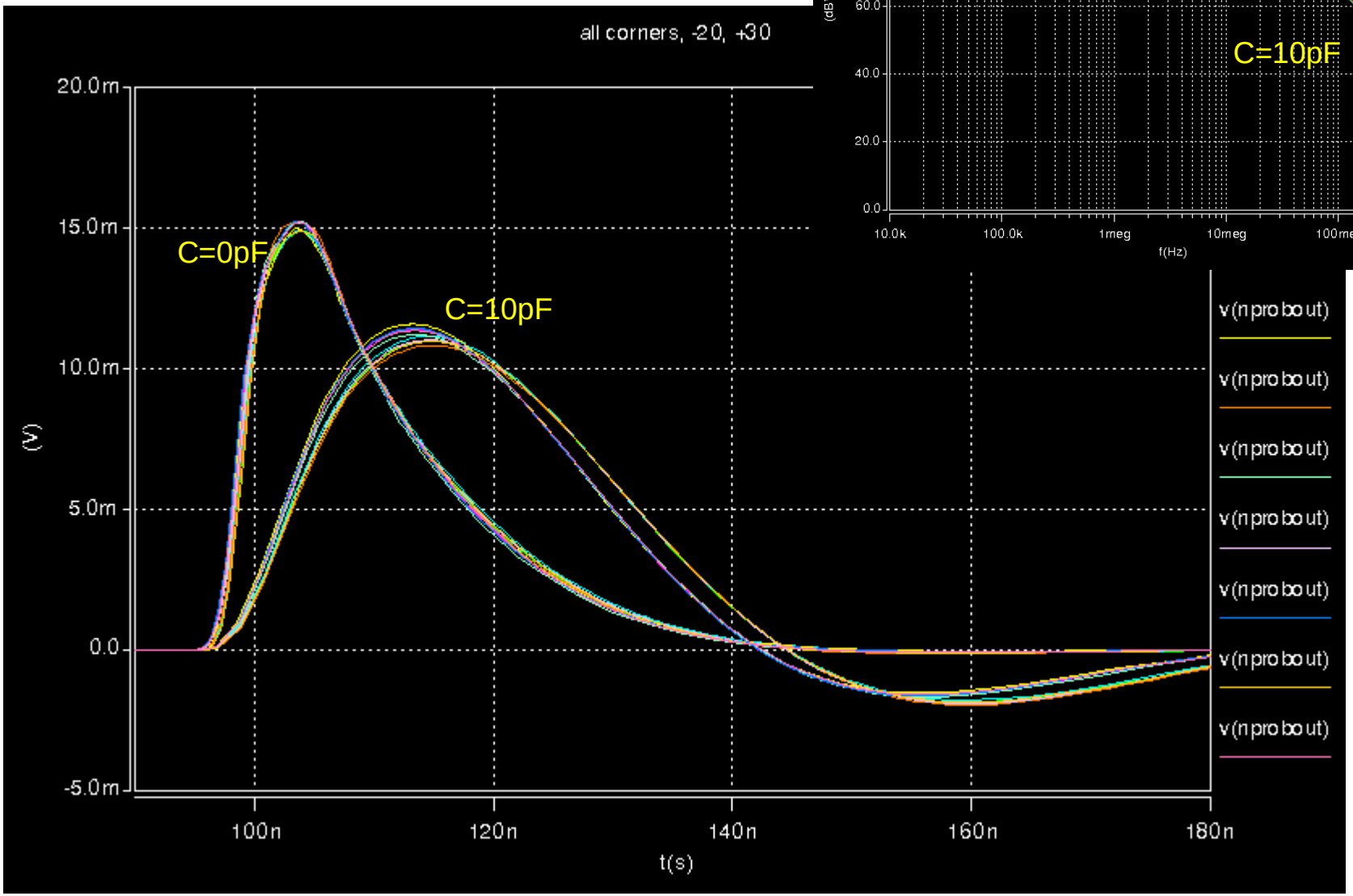


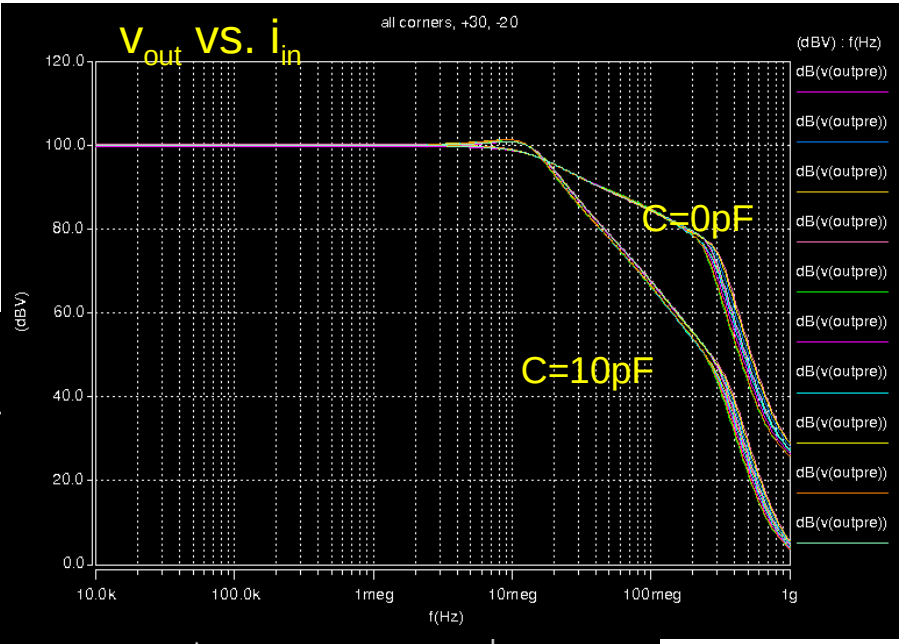
f_z = 140 kHz
C_{IN} = 10 pF

f_z = 1.3 MHz
C_{IN} = 0 pF

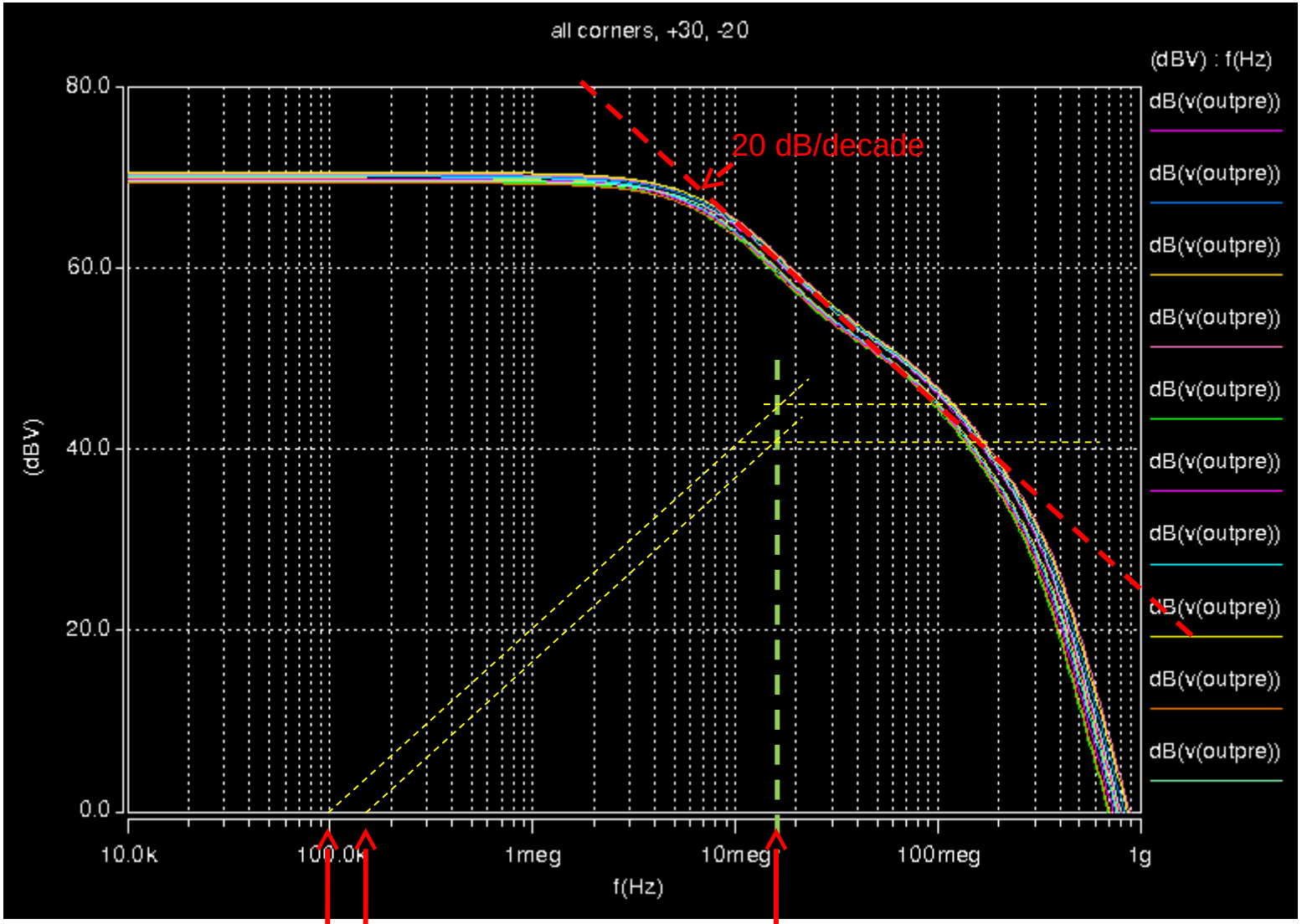
f_p = 16 MHz

preamp O/P pulseshapes: IPRE1 = 5uA





preamp open loop: IPRE1 = 90uA

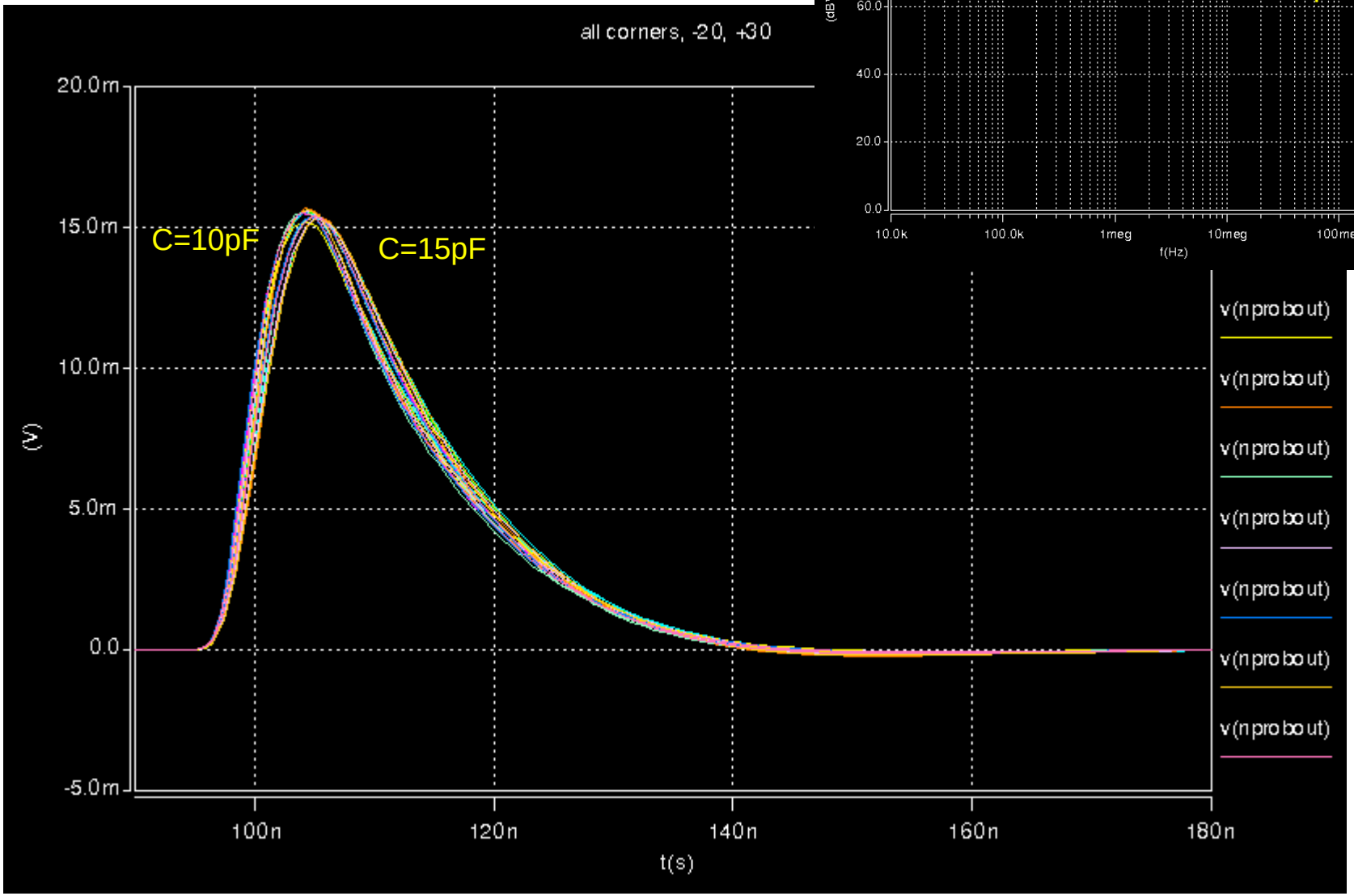


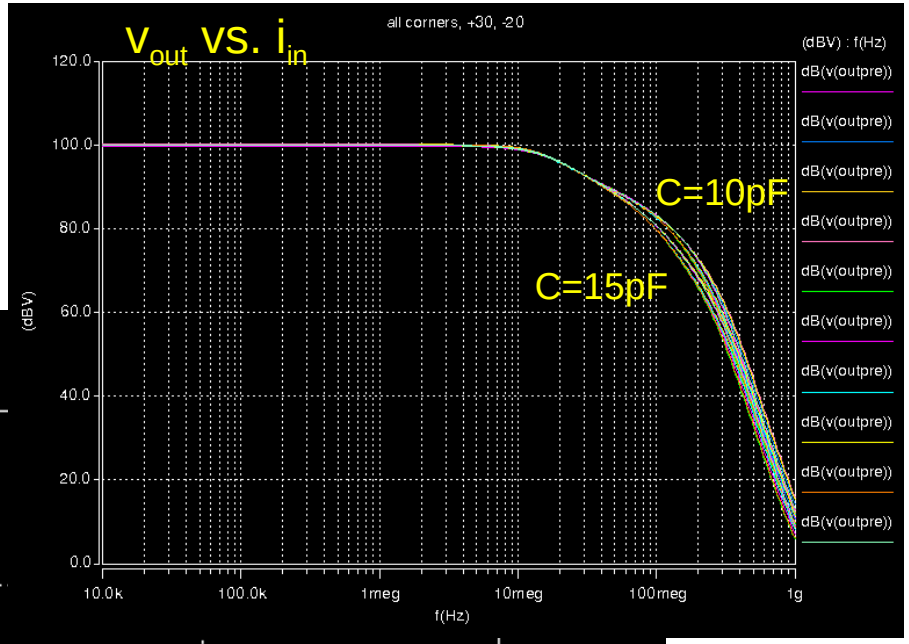
f_z = 100 kHz
C_{IN} = 15pF

f_z = 140 kHz
CIN = 10 pF

f_p = 16 MHz

preamp O/P pulseshapes: IPRE1 = 90uA





preamp conclusions

preamp design for n-in-p looks ok for:

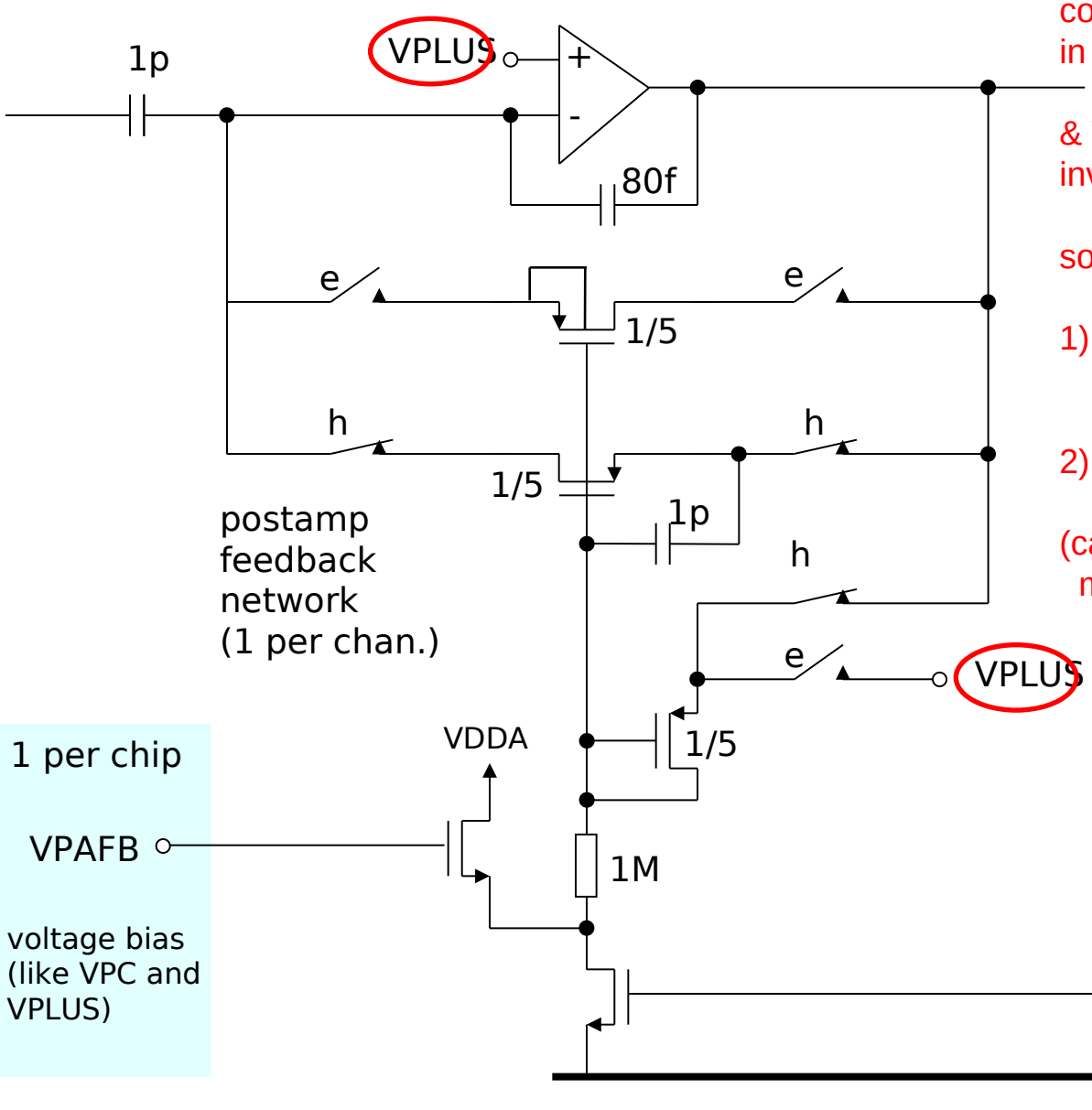
- leakage current: 0 & 1 μA
- temperature: -20 to +30
- feedback resistor and capacitor variation: +/- 15%, +/- 10%
- all process corners

stability looks ok

- may want to reduce IPRE1 for bare chip (i.e. probe testing)
- (but transient simulation doesn't show oscillation even if leave IPRE1 higher)

postamp

CBC2 postamp



evidence that disturbance on VPAFB (when many comparators fire) couples to VPLUS when postamp in electrons mode

& VPLUS also feeds opamp non-inverting input

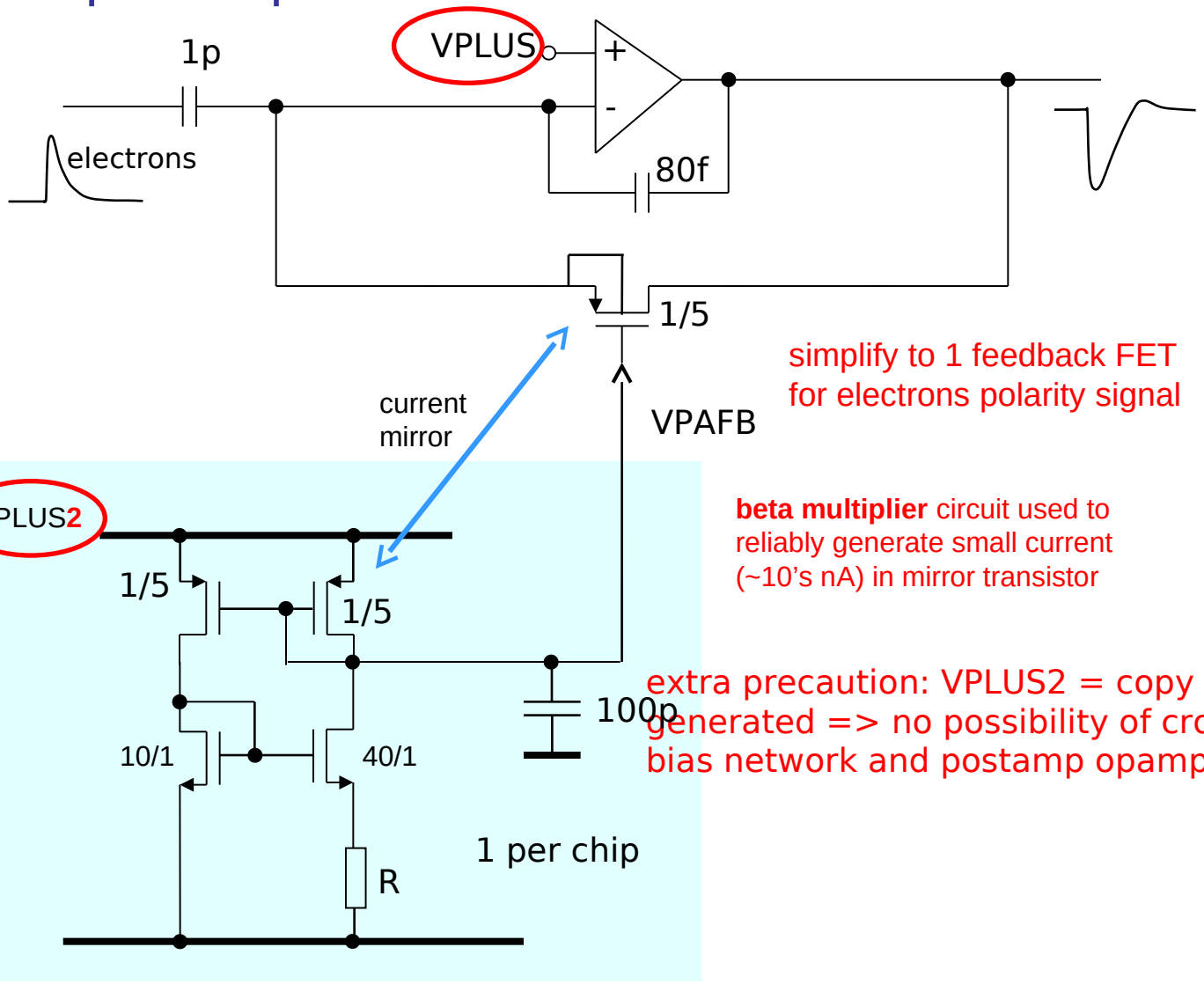
solution:

1) stop comparator causing disturbance in 1st place (see comparator section)

2) remove coupling path in postamp

(can also simplifiy since don't need holes mode any more)

CBC3 postamp



simplify to 1 feedback FET
for electrons polarity signal

beta multiplier circuit used to reliably generate small current (~10's nA) in mirror transistor

extra precaution: VPLUS2 = copy of VPLUS, independe
generated => no possibility of cross-coupling between
bias network and postamp opamp +ve input

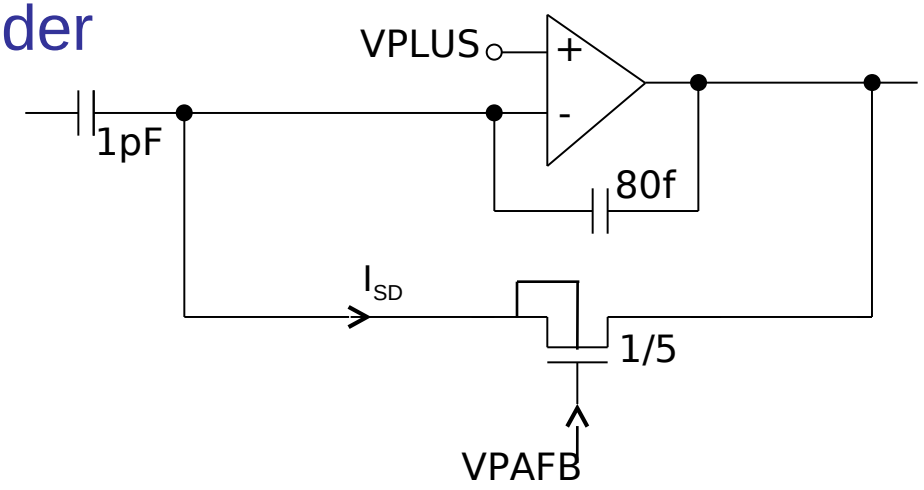
feedback characteristics reminder

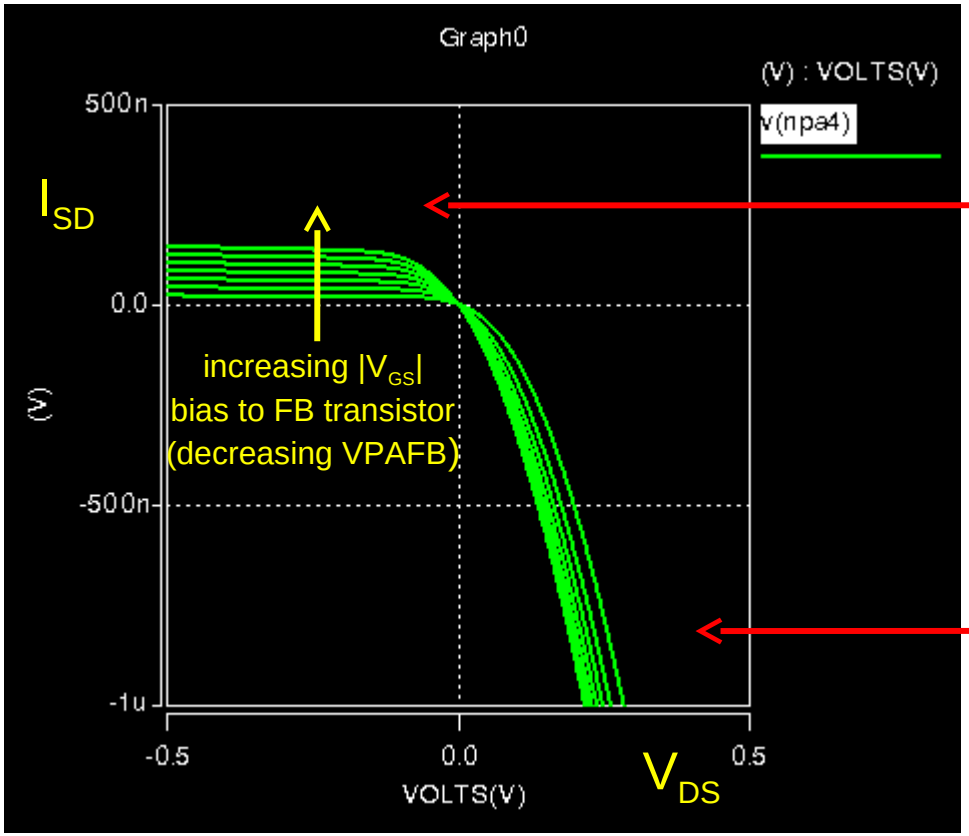
positive going overshoot
(low resistance quadrant)

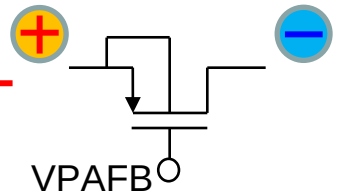
VPLUS

electrons mode signal

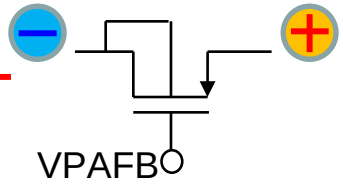
negative going signal
(high resistance quadrant)







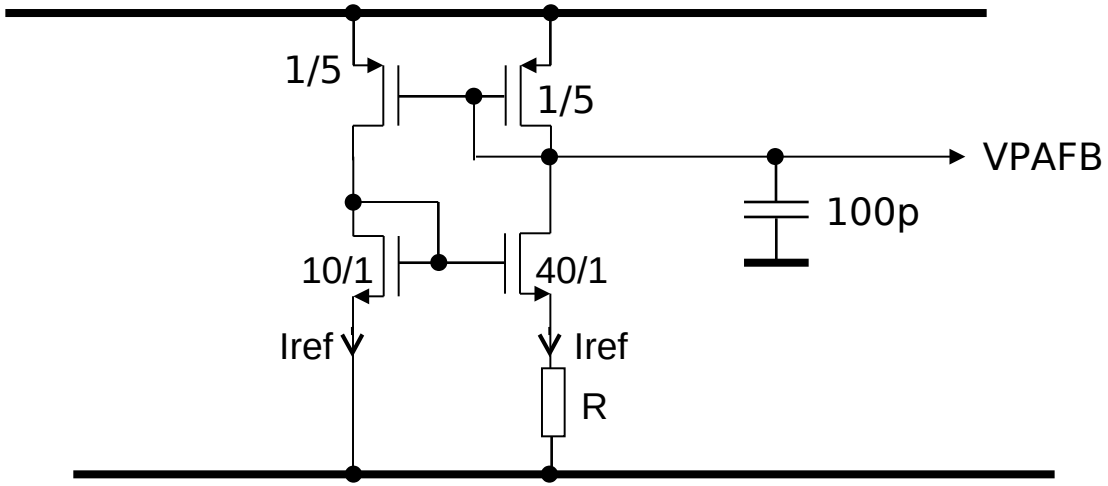
-ve going signal region
source at input side of postamp
V_{GS} ~ constant
only V_{DS} varies



+ve going overshoot region
source swaps to output side
V_{GS} increases as postamp output overshoot increases

beta multiplier “explained”

$\beta = \mu C_{OX}(W/L)$ [proportional to W]



upper mirror forces same current (Iref) to flow in both lower transistors

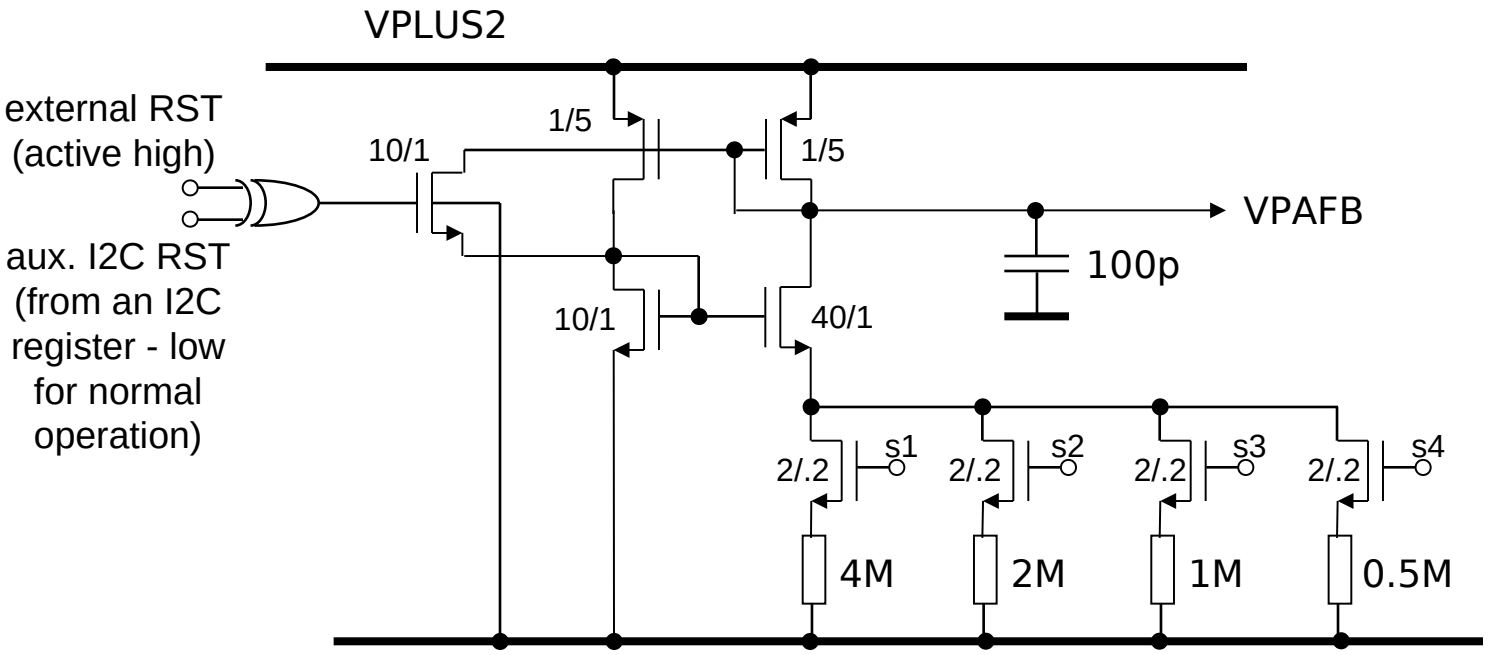
ok if V_{GS}(left) > V_{GS}(right), which can be achieved by making right NMOS wider than left by multiplier factor K (40/10)

in weak inversion $I_{ref} = \frac{nU_T \ln K}{R}$ ($U_T = kT/q$)

=> R ~ 5M for Iref = 10nA (n ~ 1.4, K=4, U_T ~ 25 mV)

see *CMOS Circuit Design, Layout and Simulation (3rd ed.) R. Jacob Baker*, chapter 20 (particularly page 635 for weak inversion design)

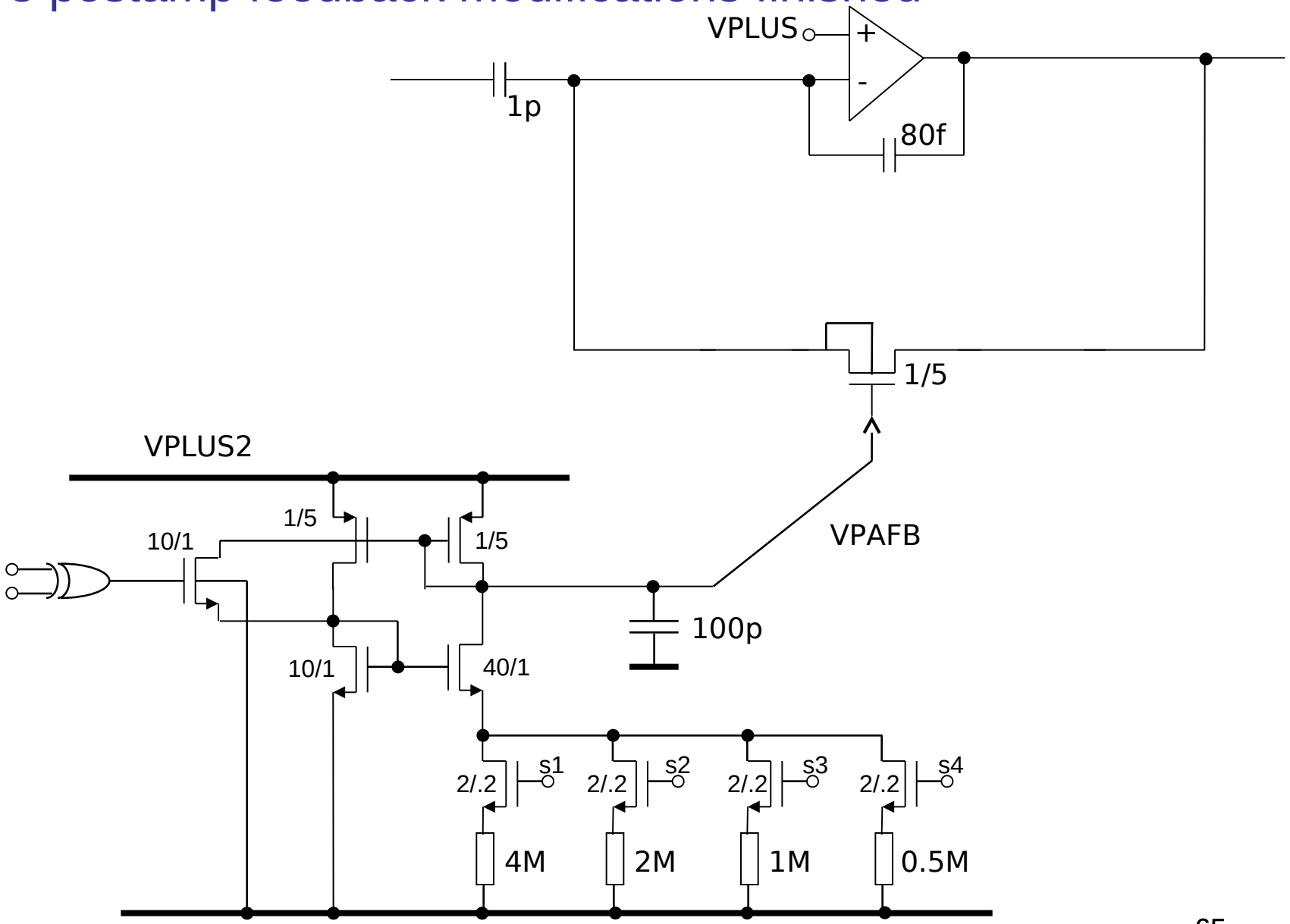
beta multiplier plus start-up and adjustable R



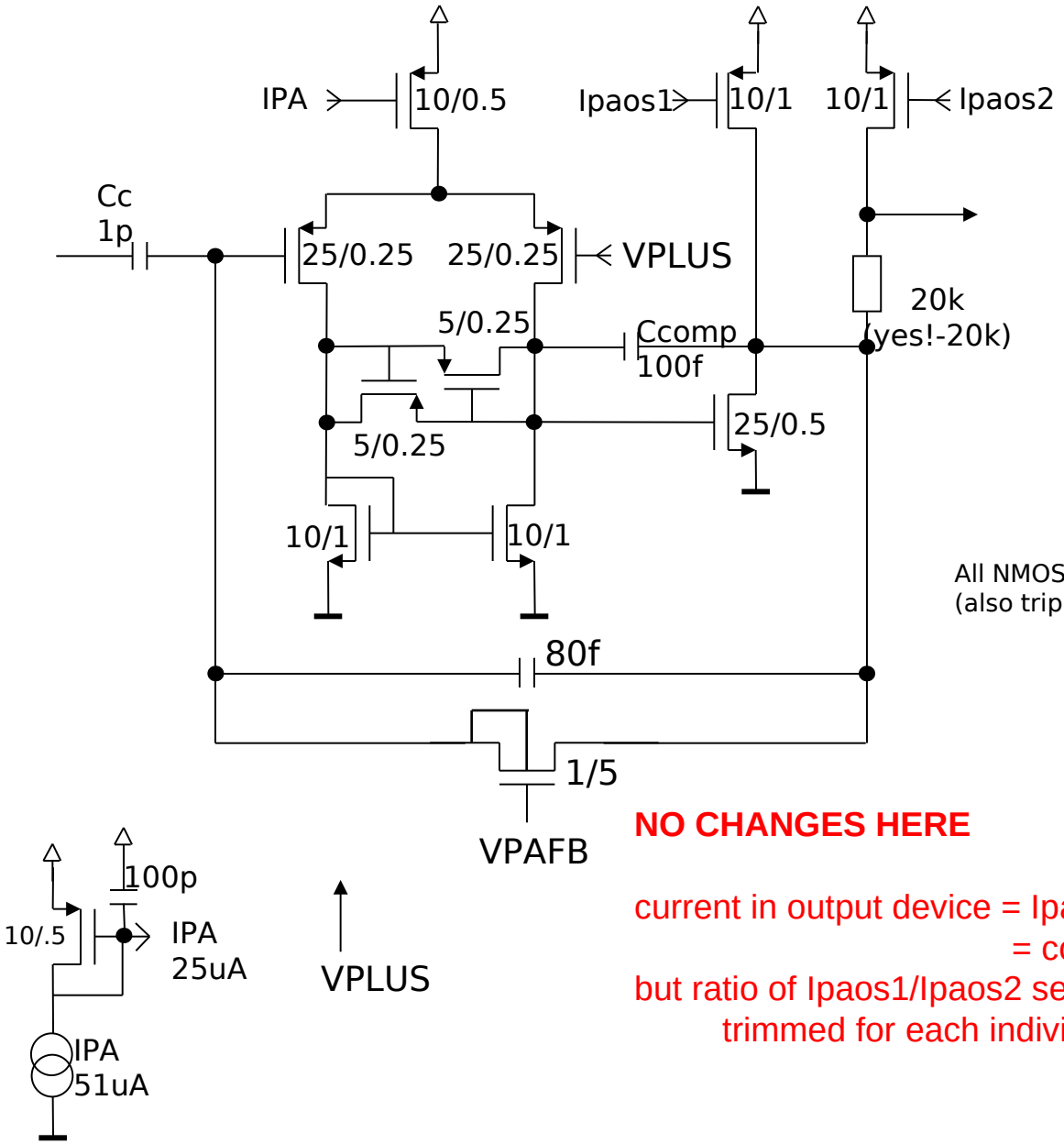
all NMOS enclosed (leakage currents would mess things up)

exclusive OR of RST (startup) lines ensures we can't have a disaster (i.e. get polarity wrong and get stuck in permanent reset!!)

CBC3 postamp feedback modifications finished



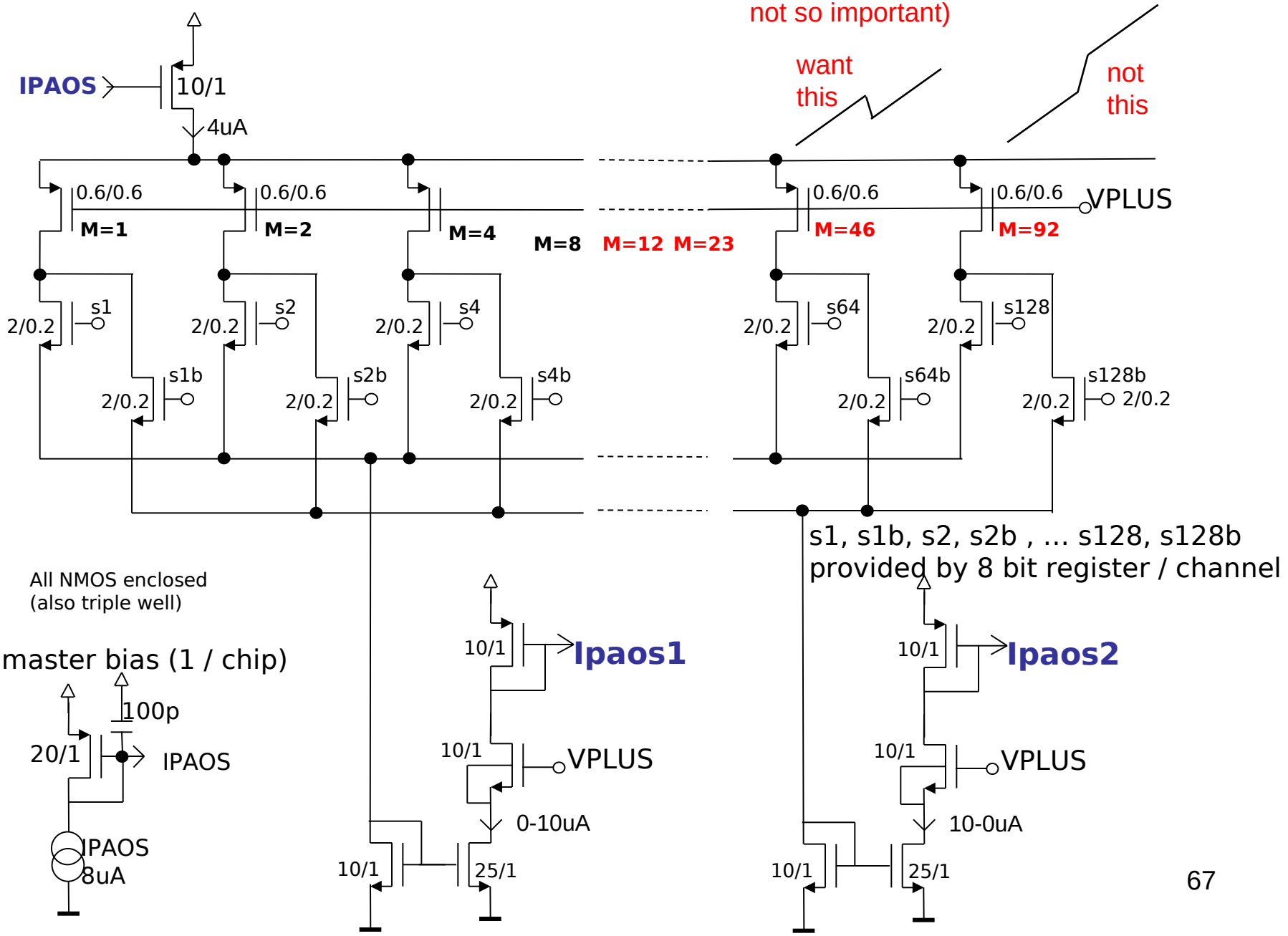
CBC3 postamp opamp



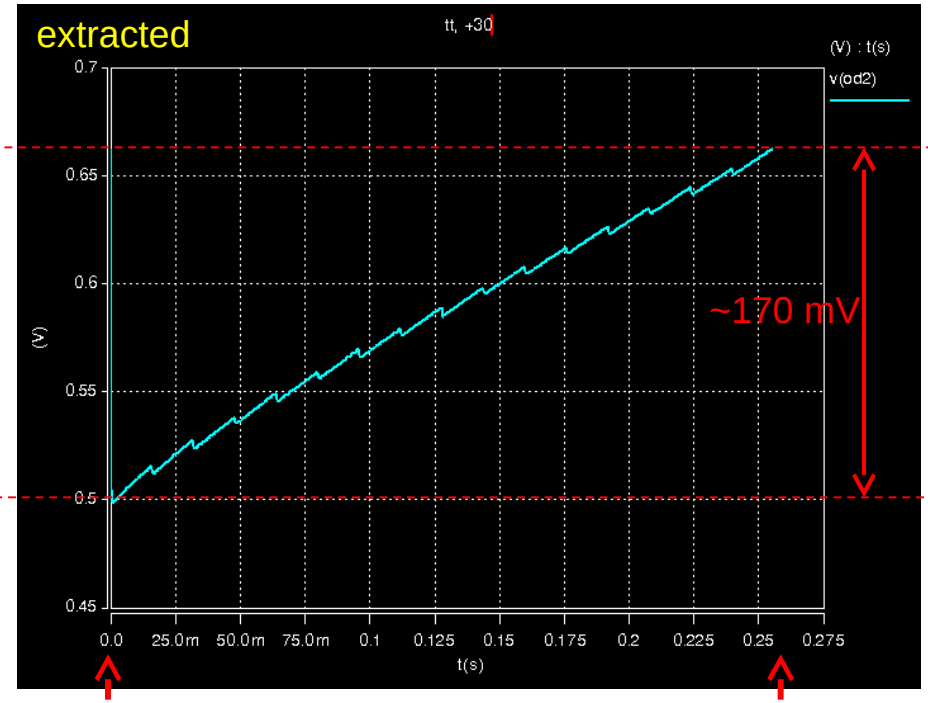
NO CHANGES HERE

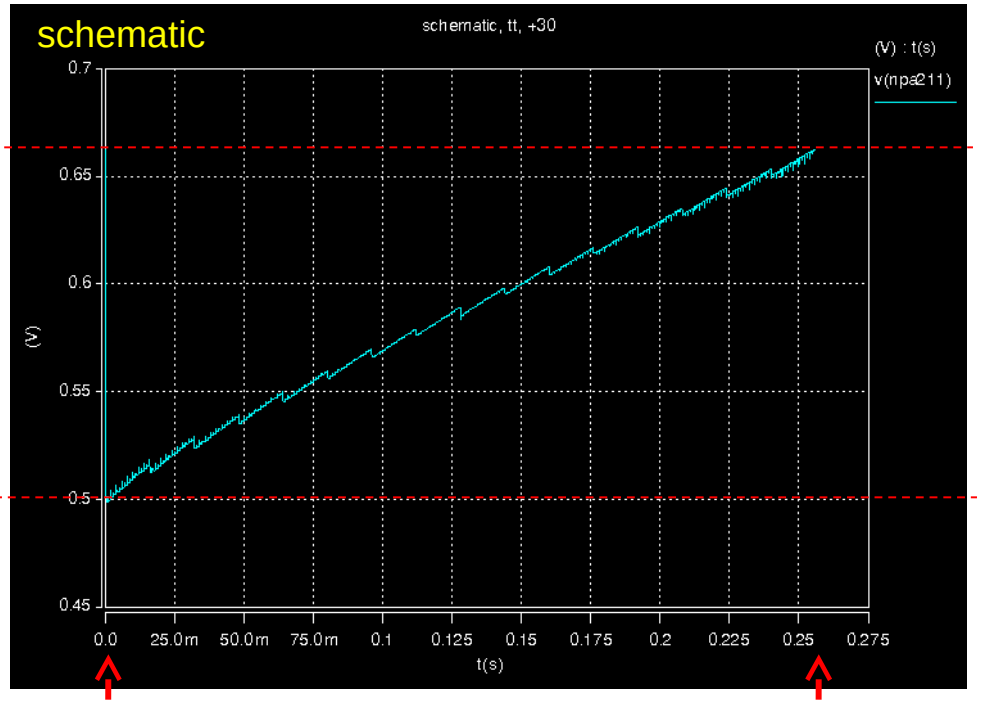
current in output device = Ipaos1 + Ipaos2
= constant
but ratio of Ipaos1/Ipaos2 sets DC level shift at output
trimmed for each individual channel

CBC3 offset trim method



offset trim: extracted vs. schematic





no current in level shift resistor

max. current in level shift resistor

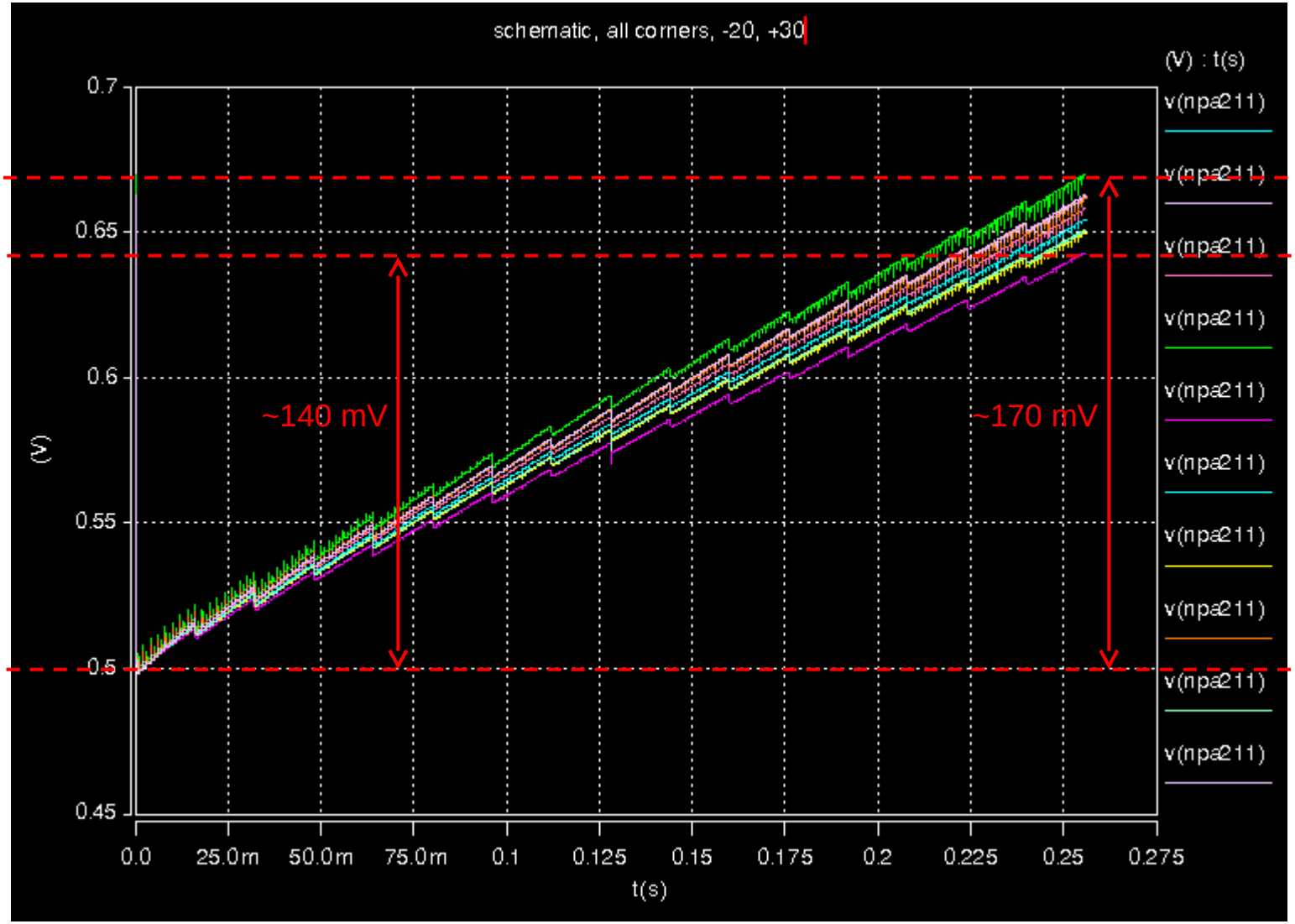
no current in level shift resistor

max. current in level shift resistor

IPAOS = 6 uA

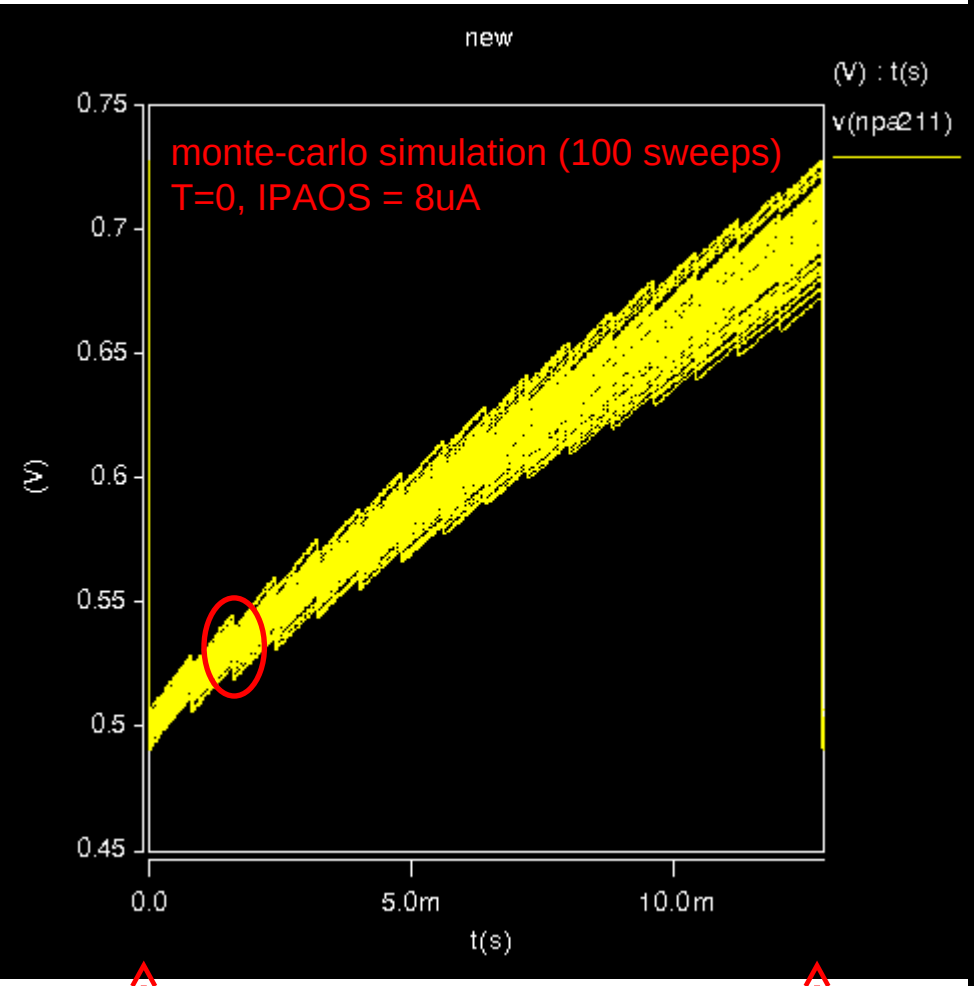
no difference in range covered (schematic vs. extracted)
=> can rely on schematic sims
(extracted takes long time)

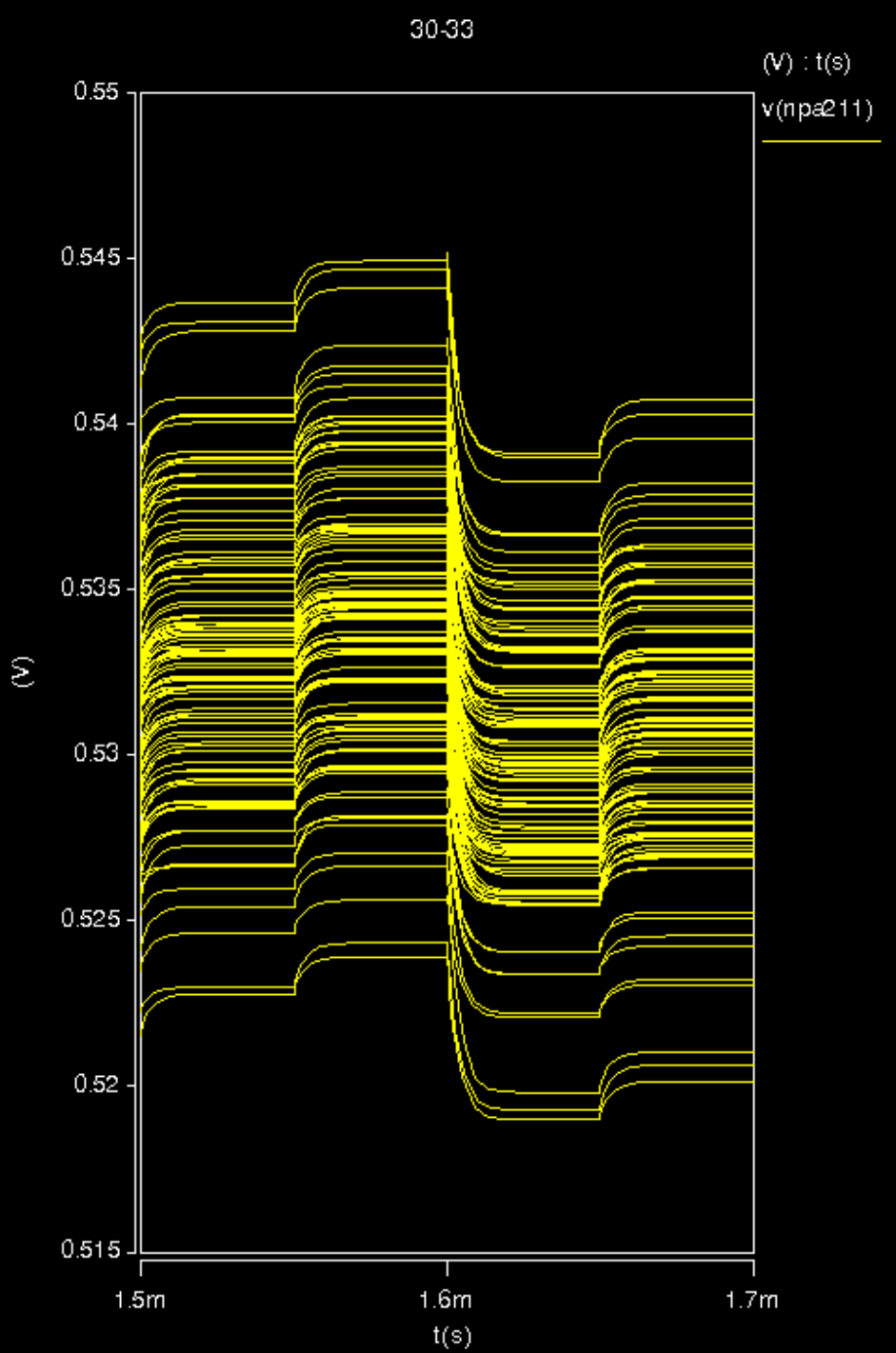
offset trim: schematic, all corners, +30, -20



non-monotonicity but overlap

schematic simulation



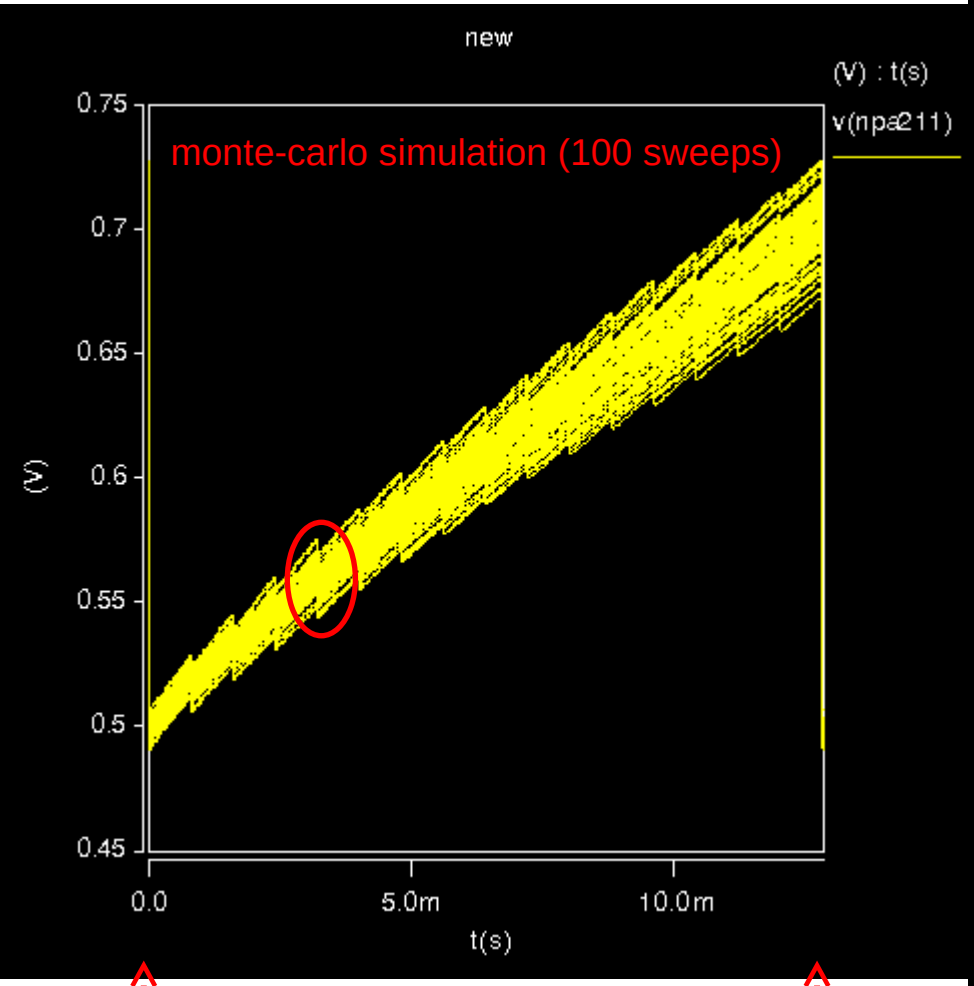


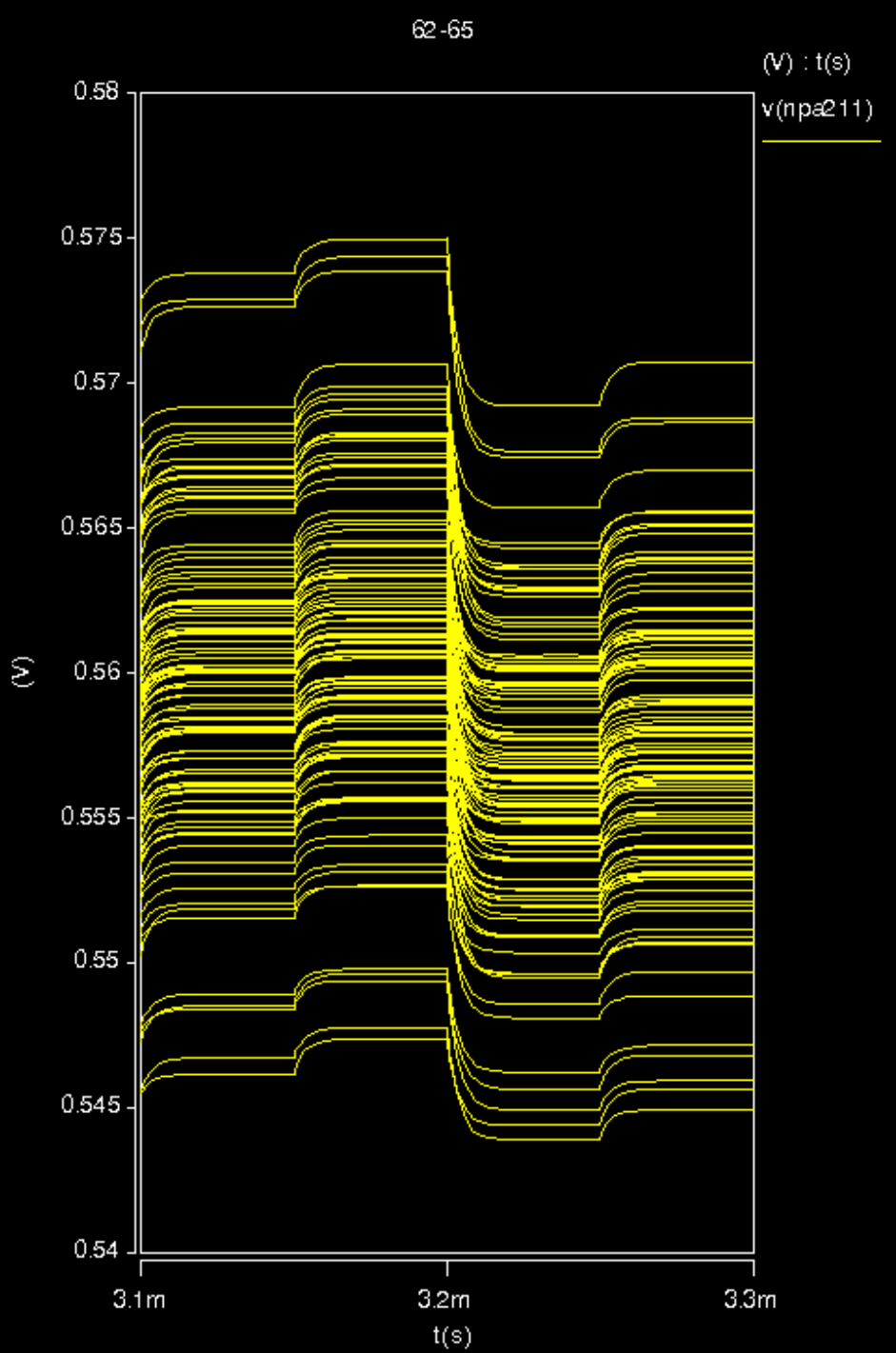
no current in level shift resistor

maximum current in level shift resistor

non-monotonicity but overlap

schematic simulation



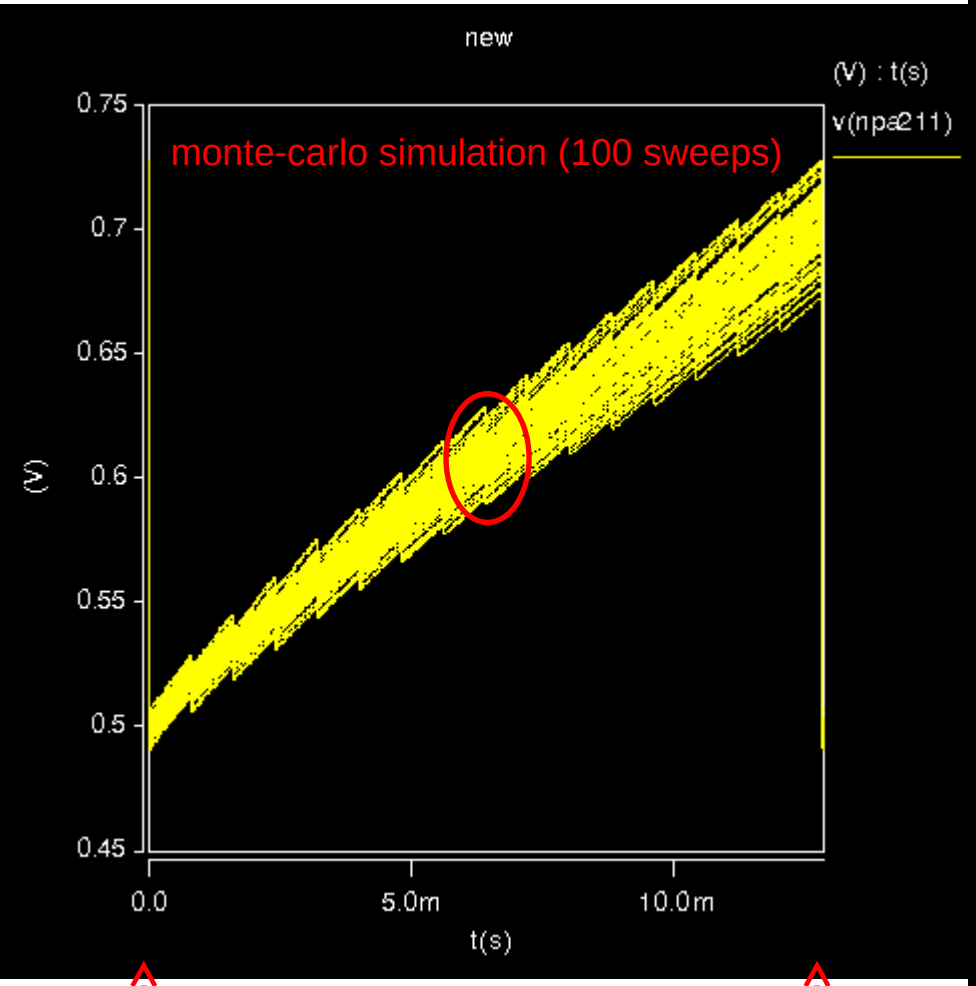


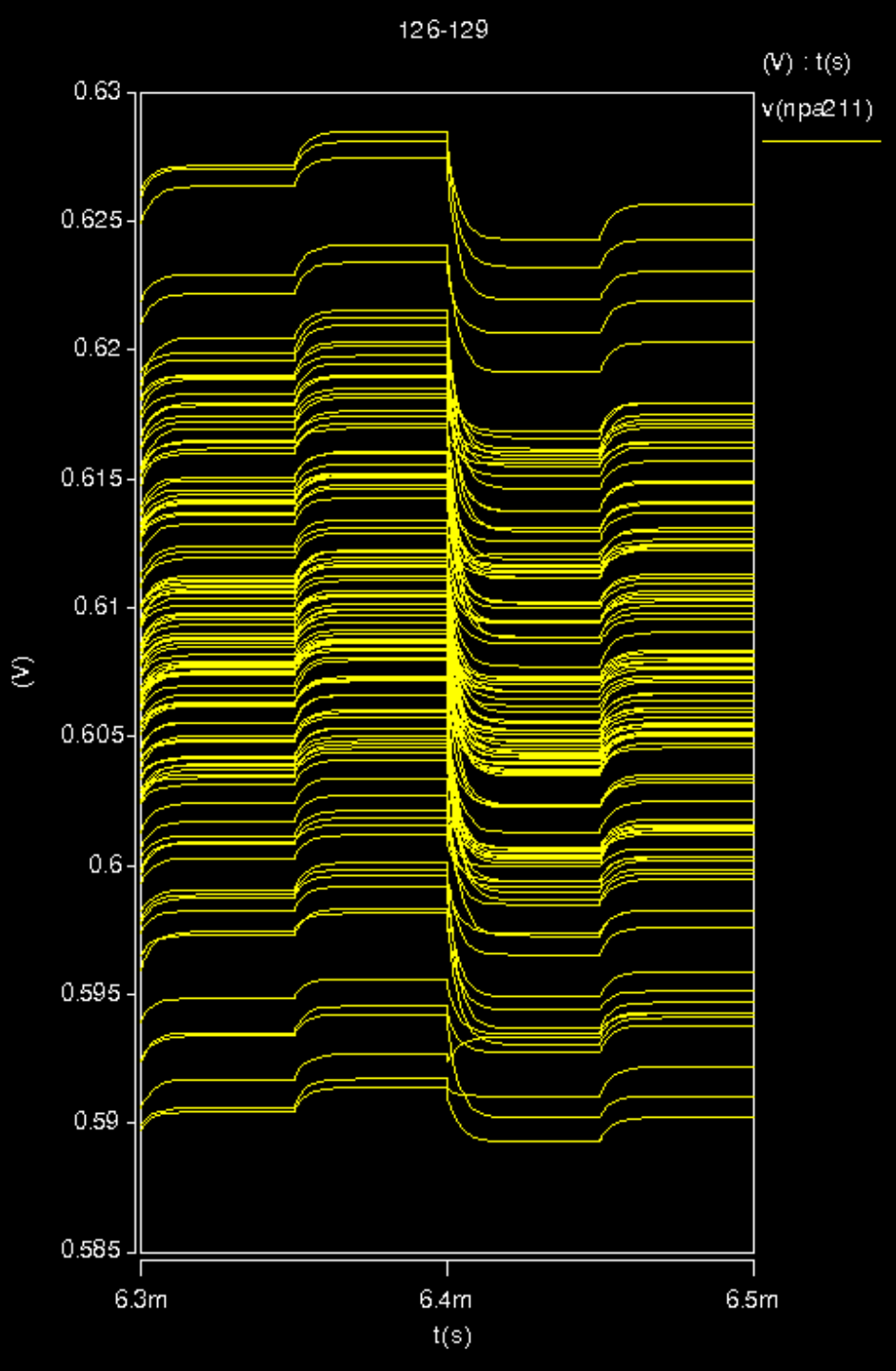
no current in
level shift resistor

maximum current in
level shift resistor

non-monotonicity but overlap

schematic simulation



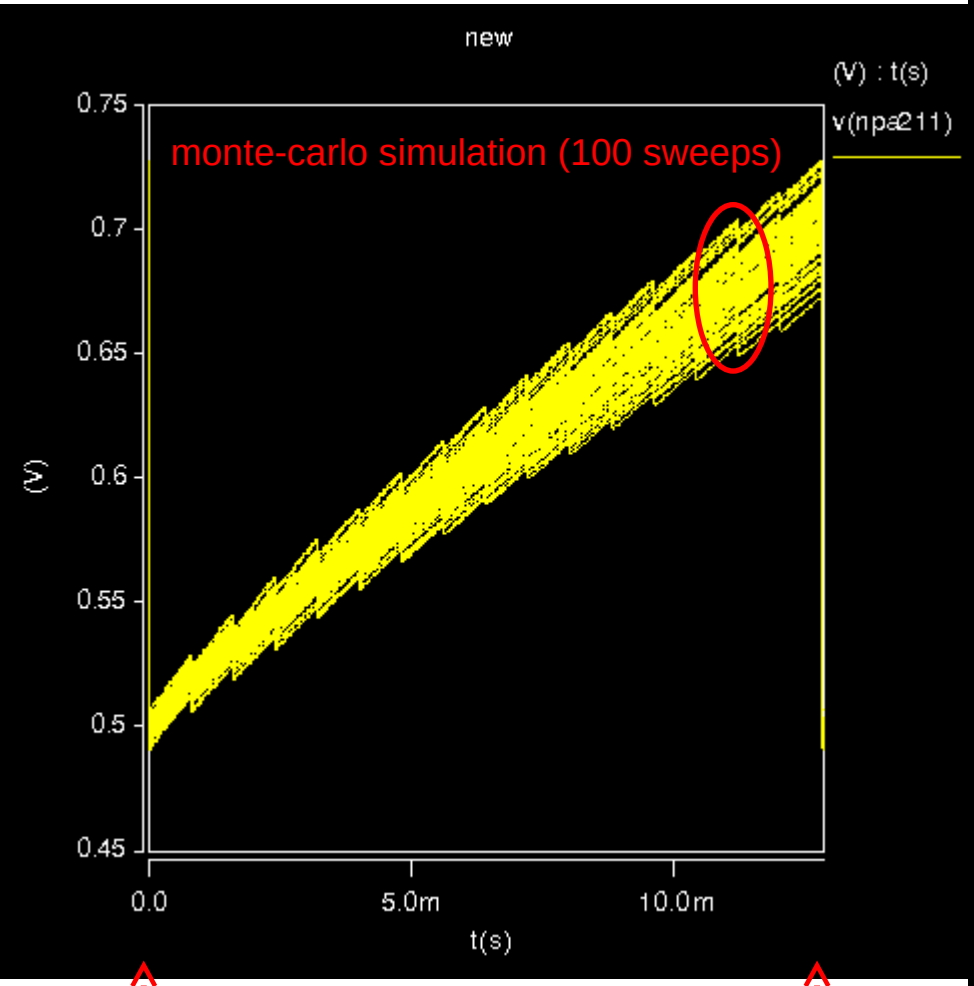


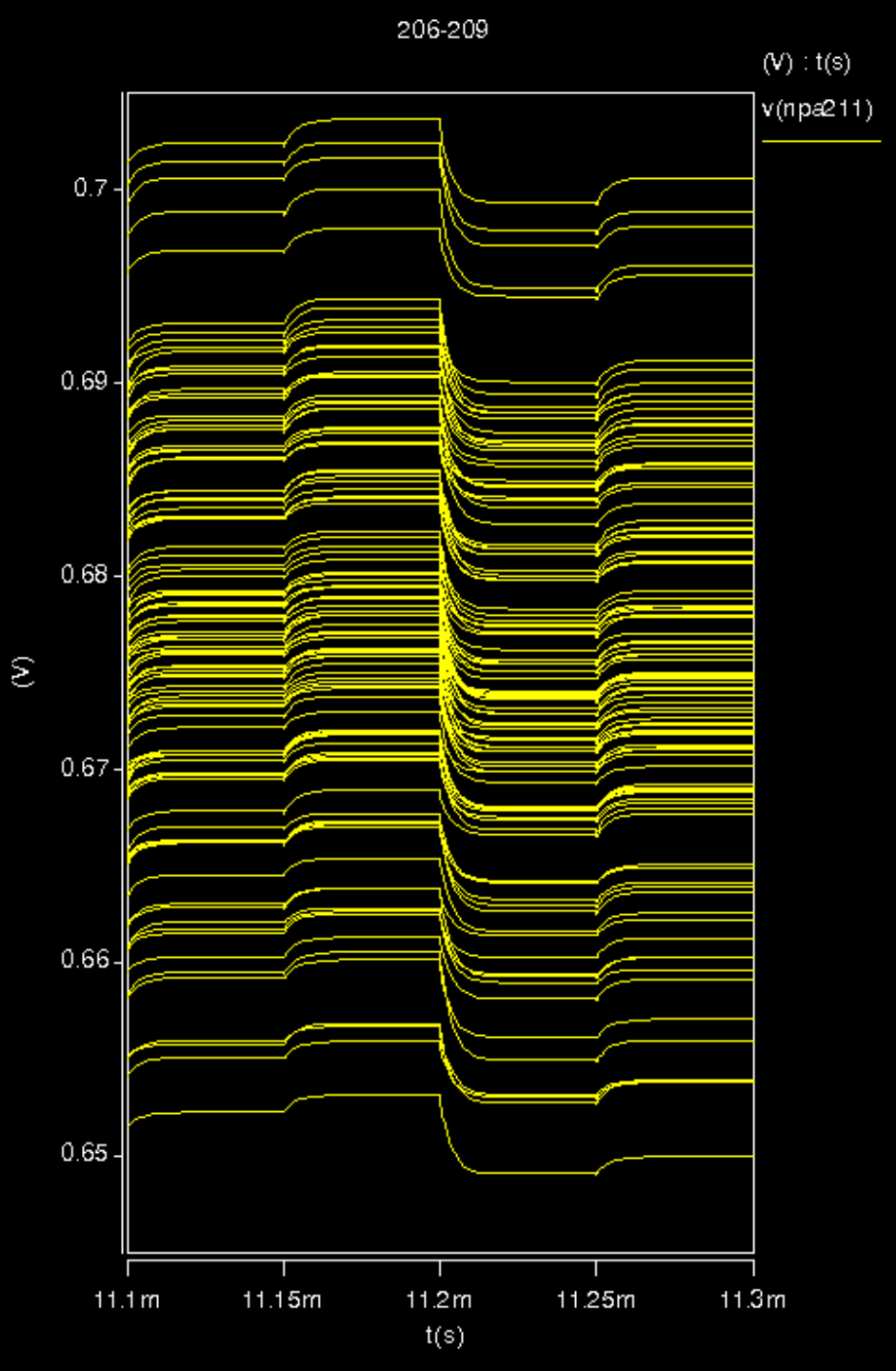
no current in
level shift resistor

maximum current in
level shift resistor

non-monotonicity but overlap

schematic simulation





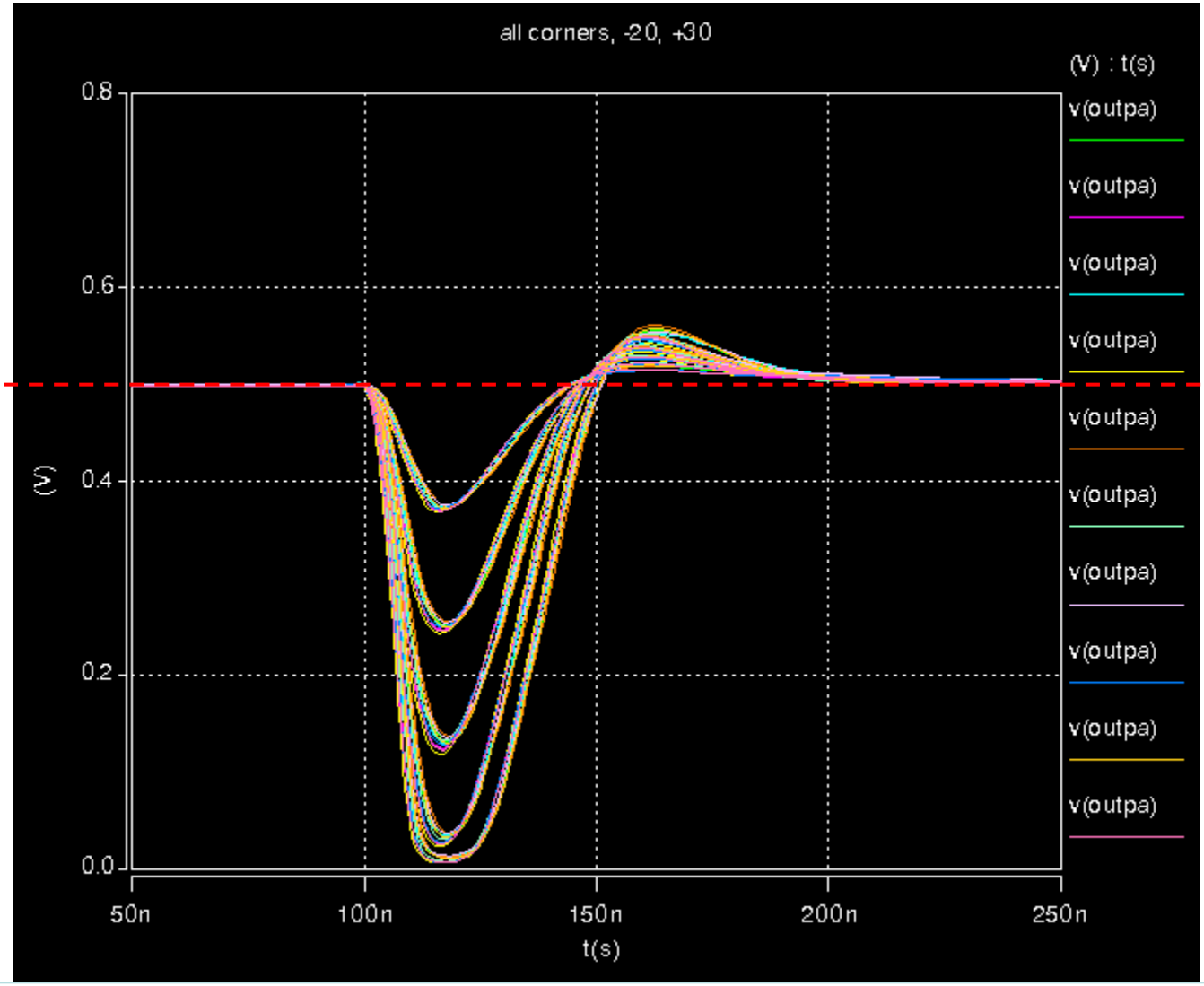
no current in
level shift resistor

maximum current in
level shift resistor

output offset adjust range (including signal)

nominal bias values

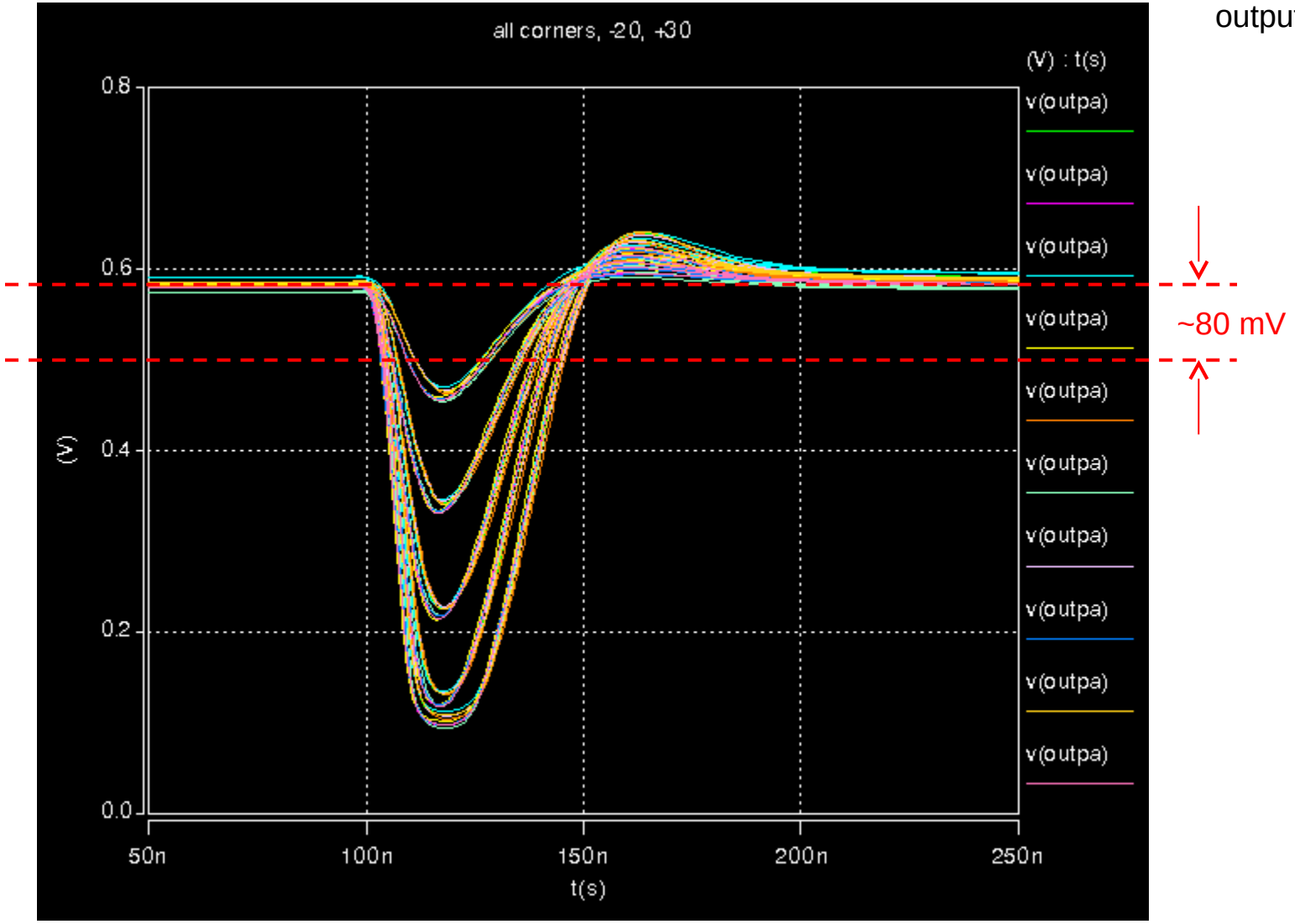
output offset = 0



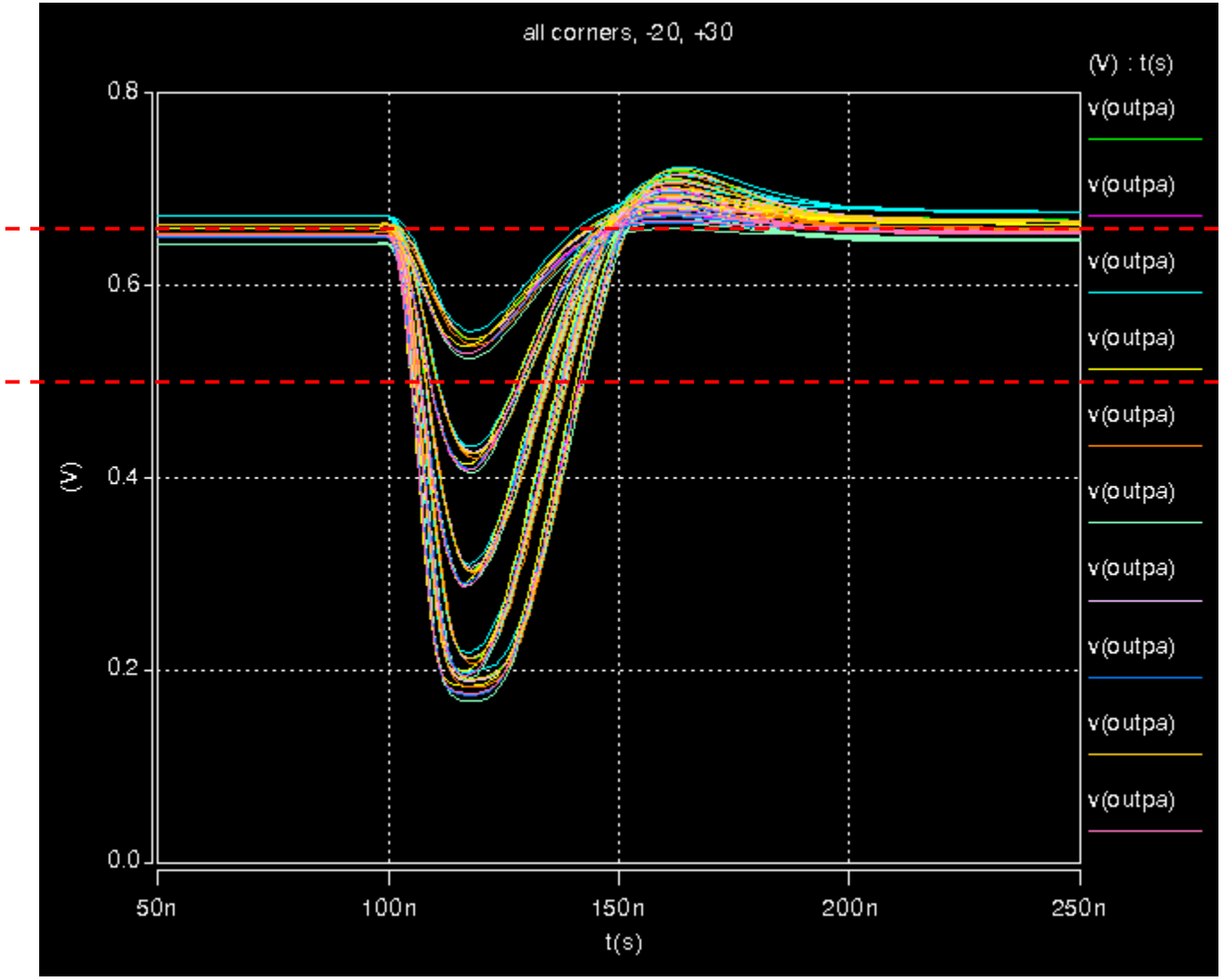
output offset adjust range (including signal)

nominal bias values

output offset = 128



output offset adjust range (including signal)



nominal bias values

output offset = 255

~160 mV

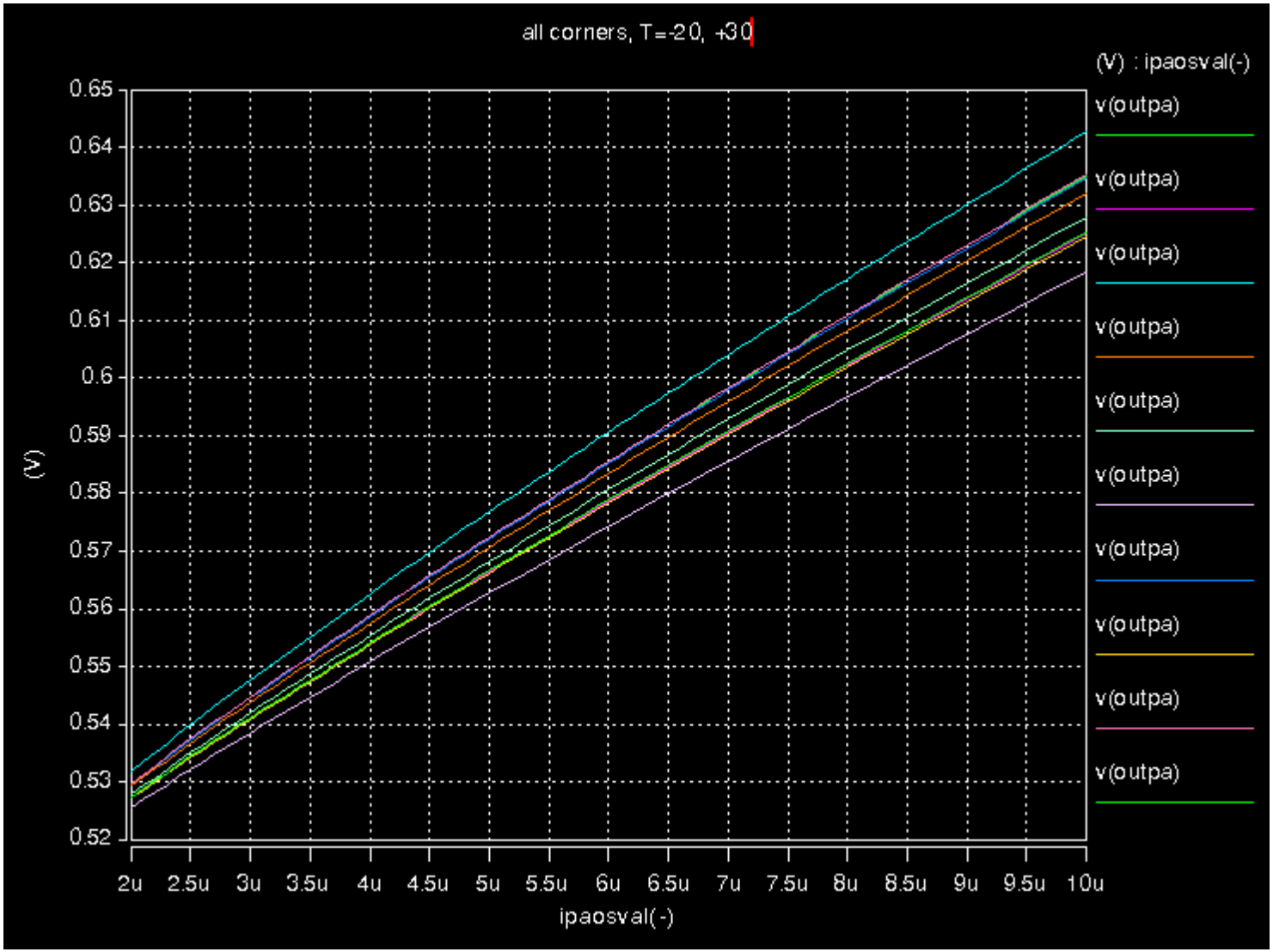
~ 0.6 mV res'n

conclusions

all working fine

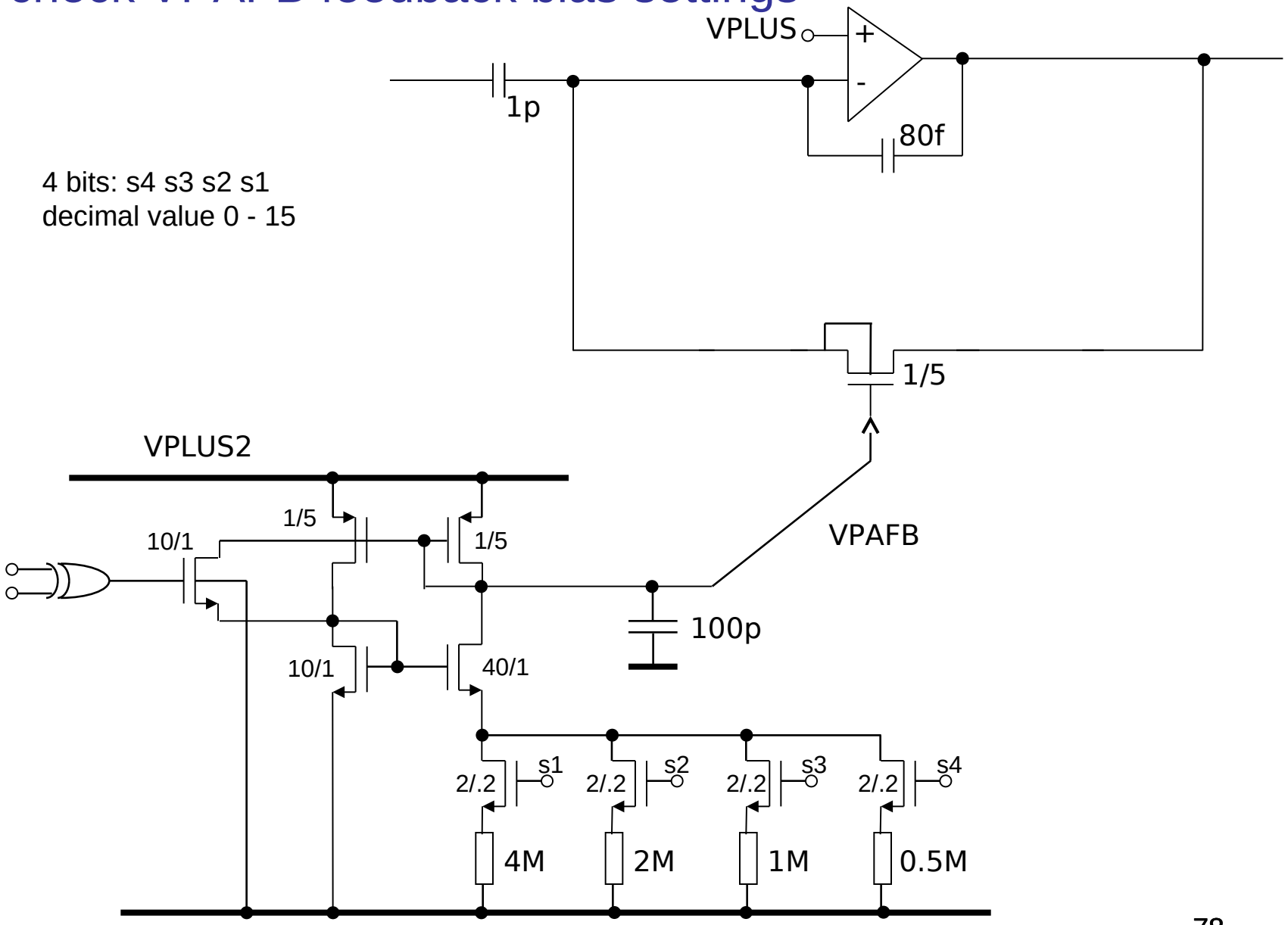
adjustment range ok
for IPAOS = 6uA

output offset vs. IPAOS

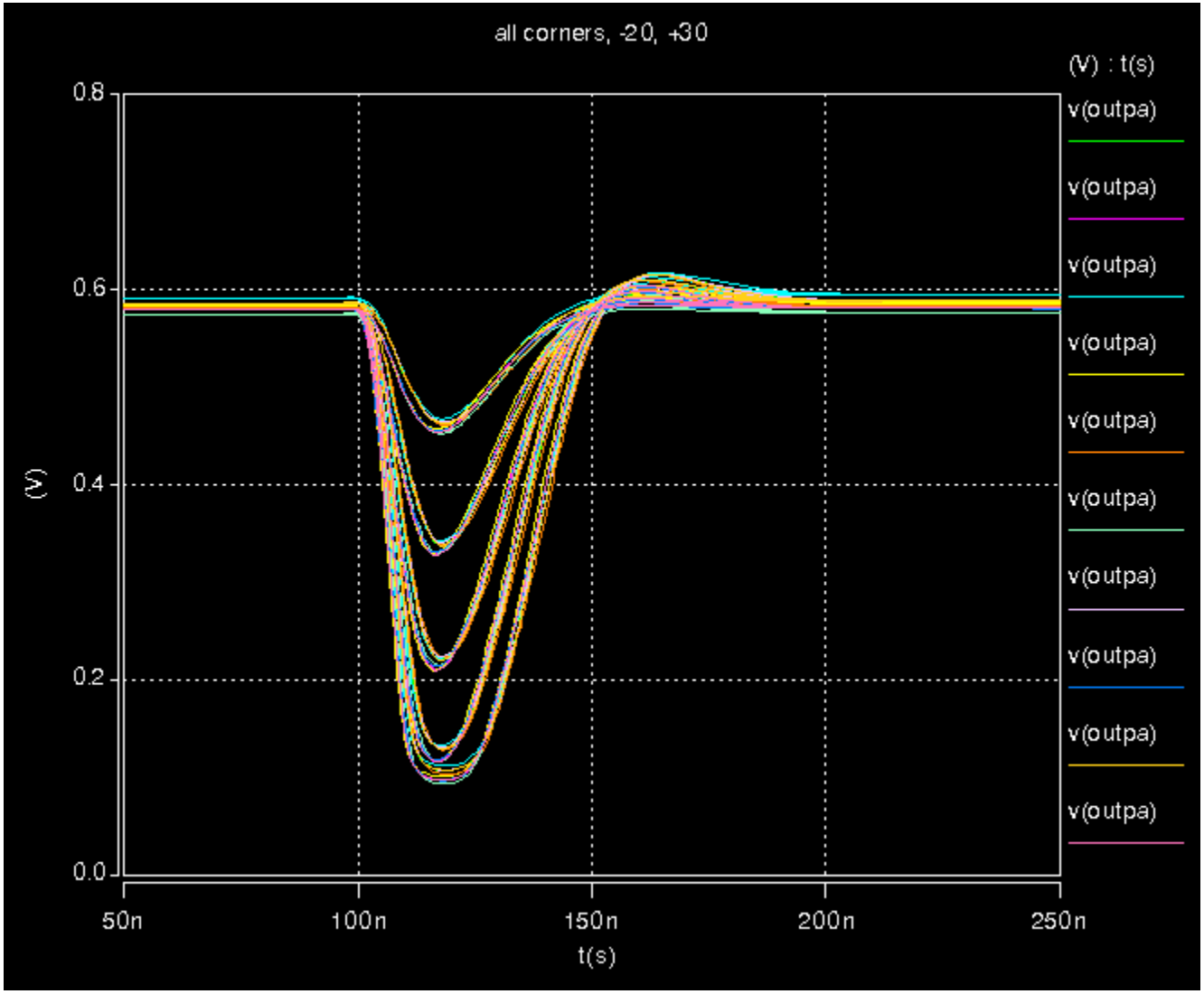


offset value programmed to 128
the stability of the pedestals should depend on how IPAOS varies with temperature

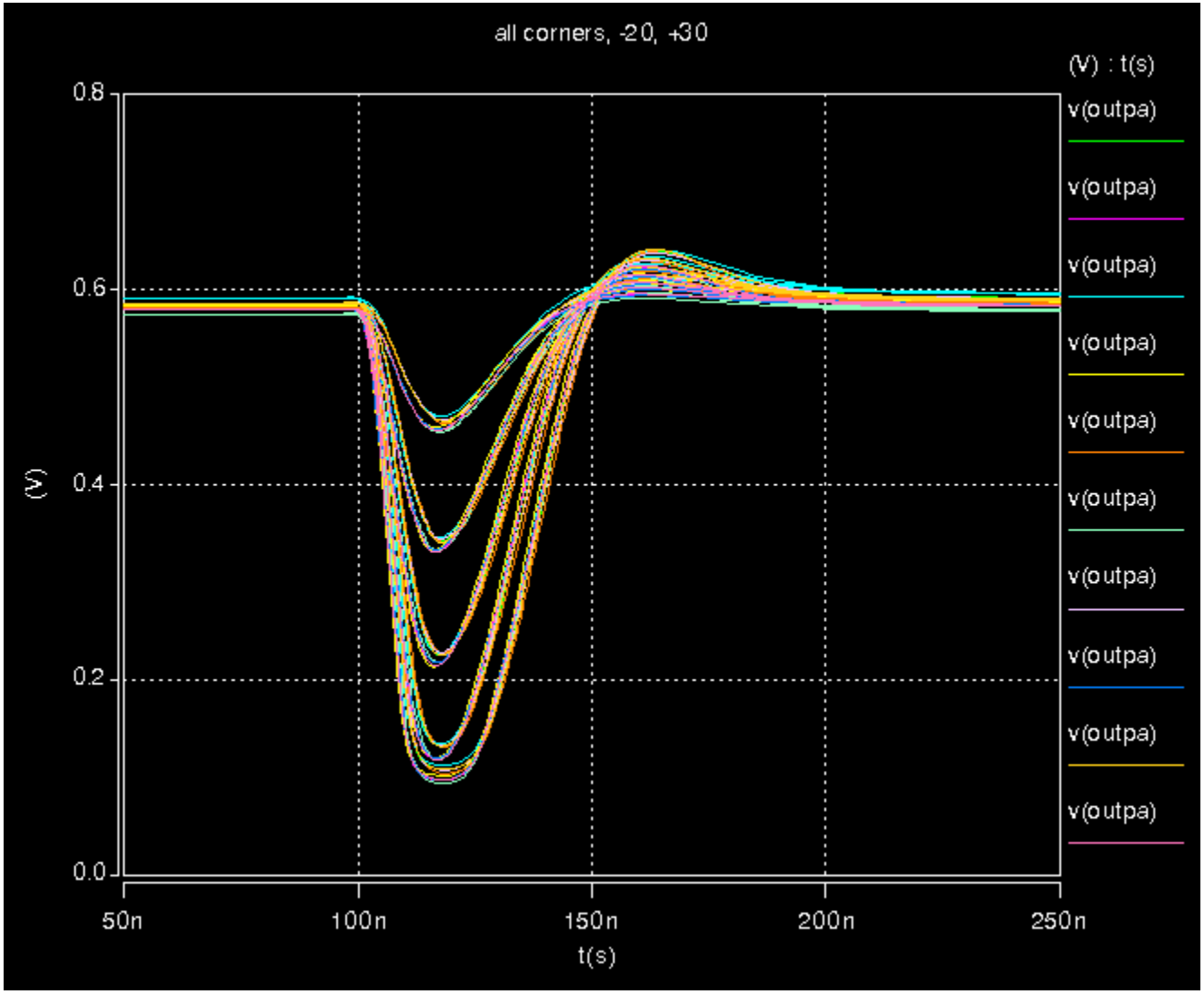
now check VPAFB feedback bias settings



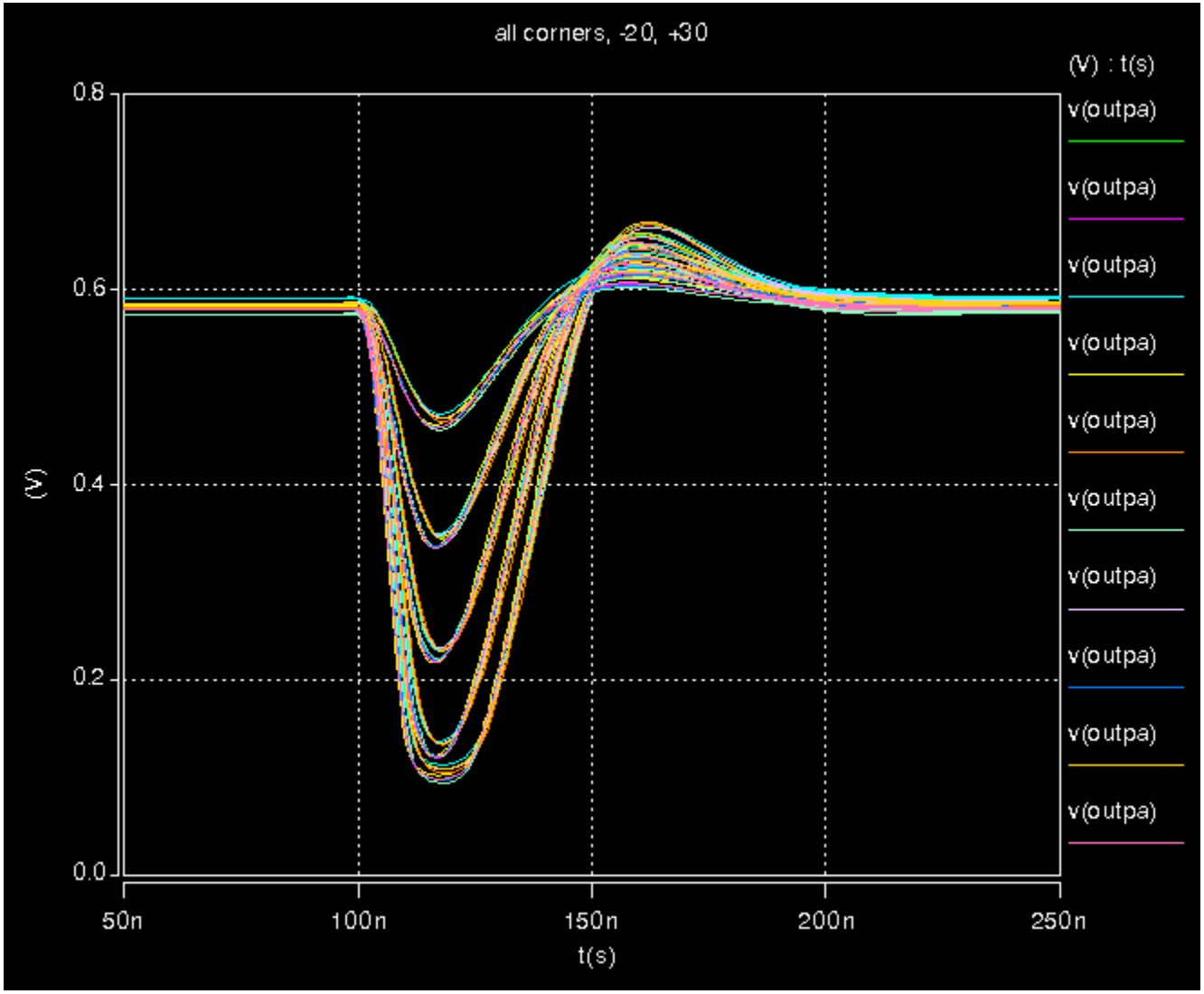
pulse shape vs. VPAFB: VPAFB = 1



pulse shape vs. VPAFB: VPAFB = 7



pulse shape vs. VPAFB: VPAFB = 15

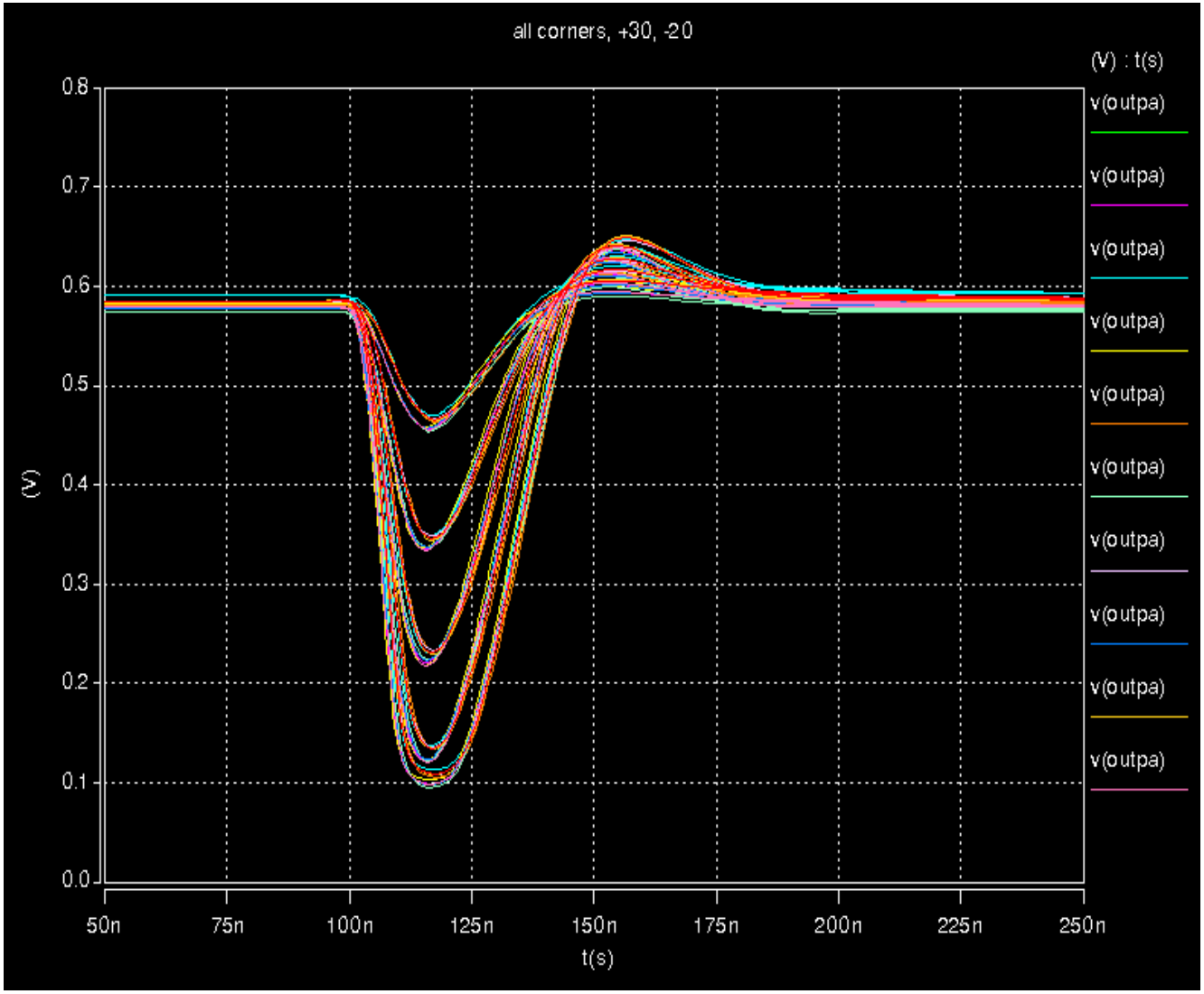


conclusions

some control over pulse duration

trade-off with overshoot

other factors affecting pulse shape: preamp feedback

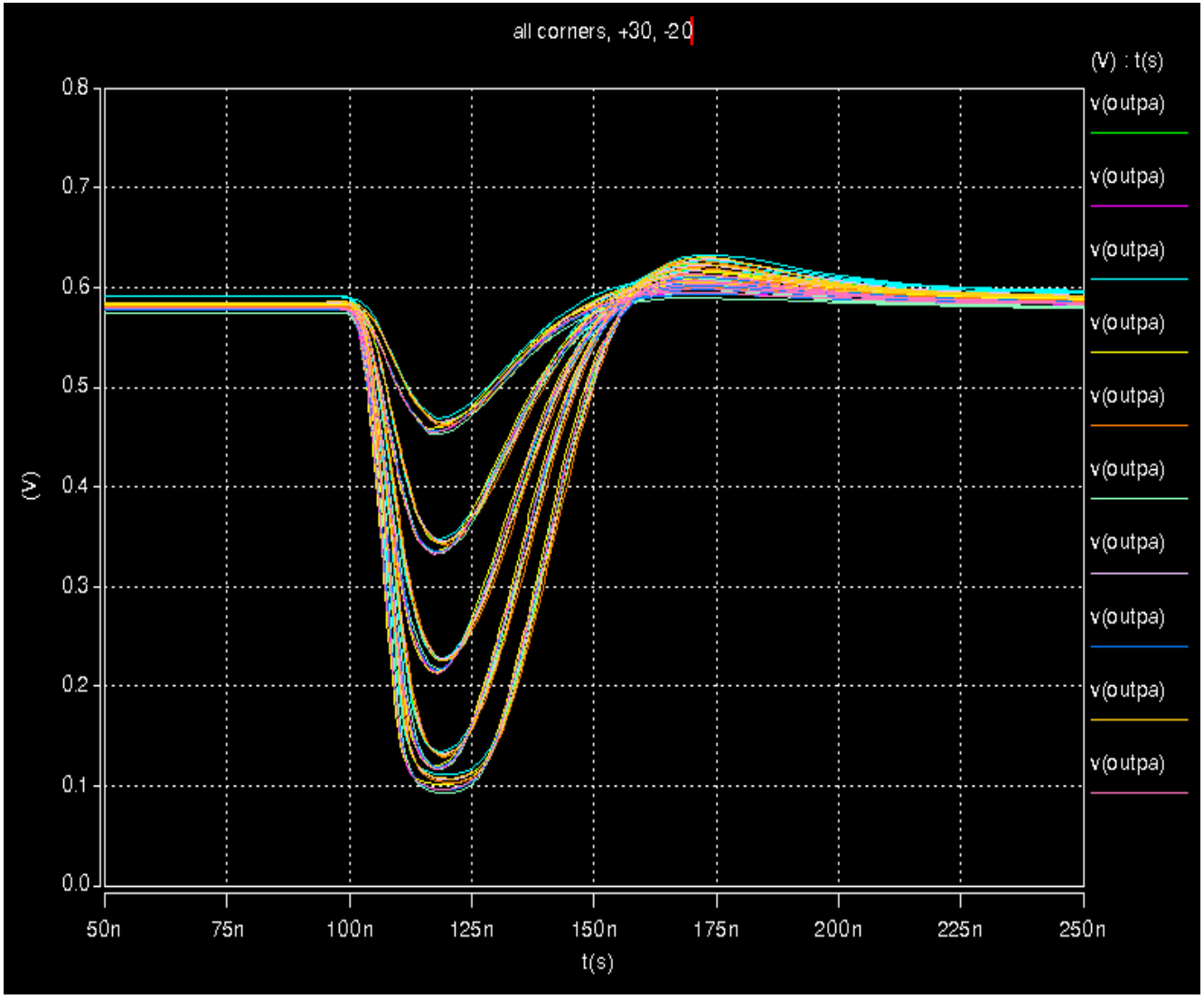


nominal bias settings

Rpf-15%, Cpf-10%

no significant loss of amplitude

other factors affecting pulse shape: preamp feedback

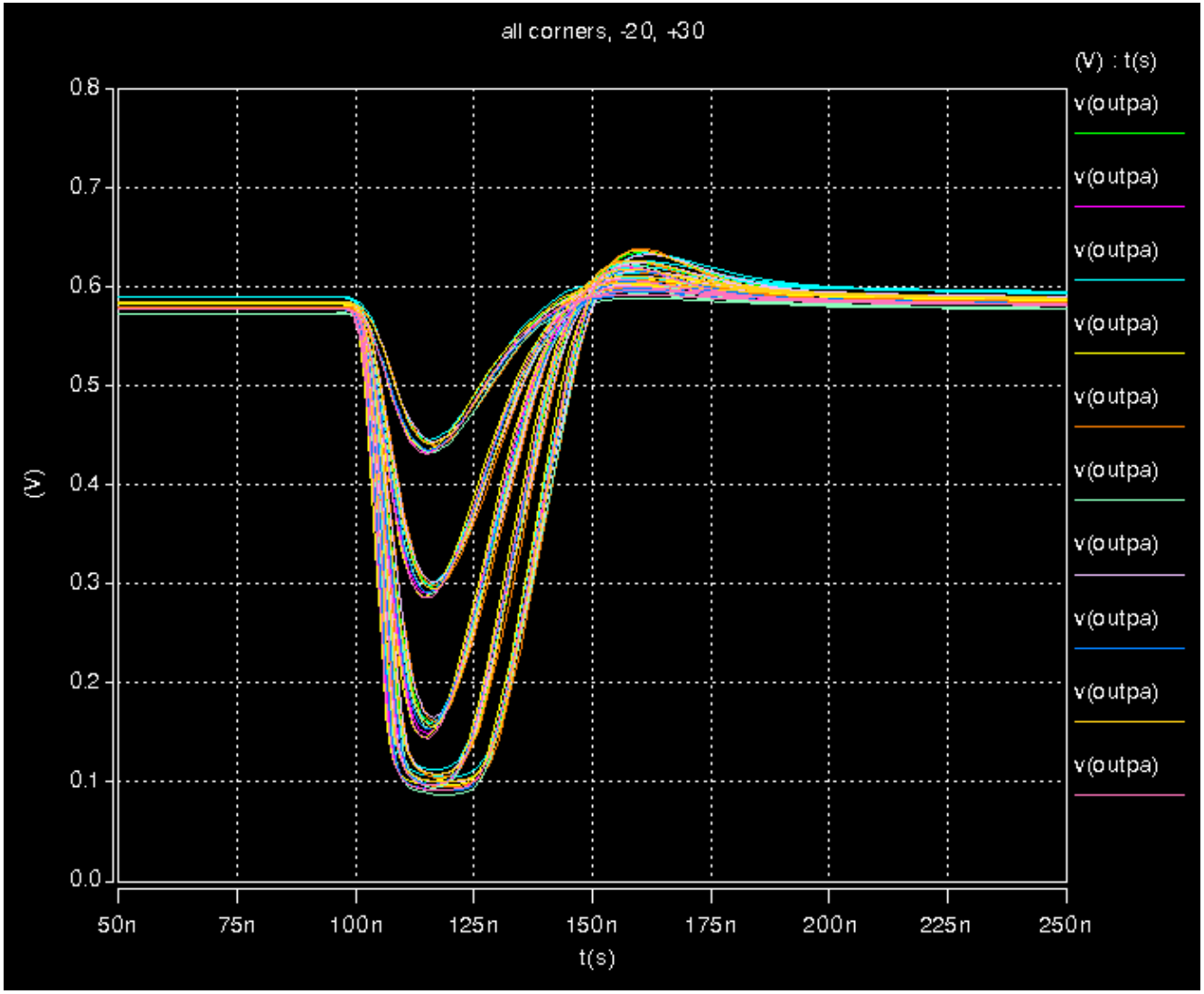


nominal bias settings

Rpf+15%, Cpf+10%

larger signal size pulse durations exceed 50 nsec, but not by much

other factors affecting pulse shape: postamp bias current IPA



nominal bias settings

Rpf+15%, Cpf+10%

IPA -> 40 uA

some reduction in pulse width achievable

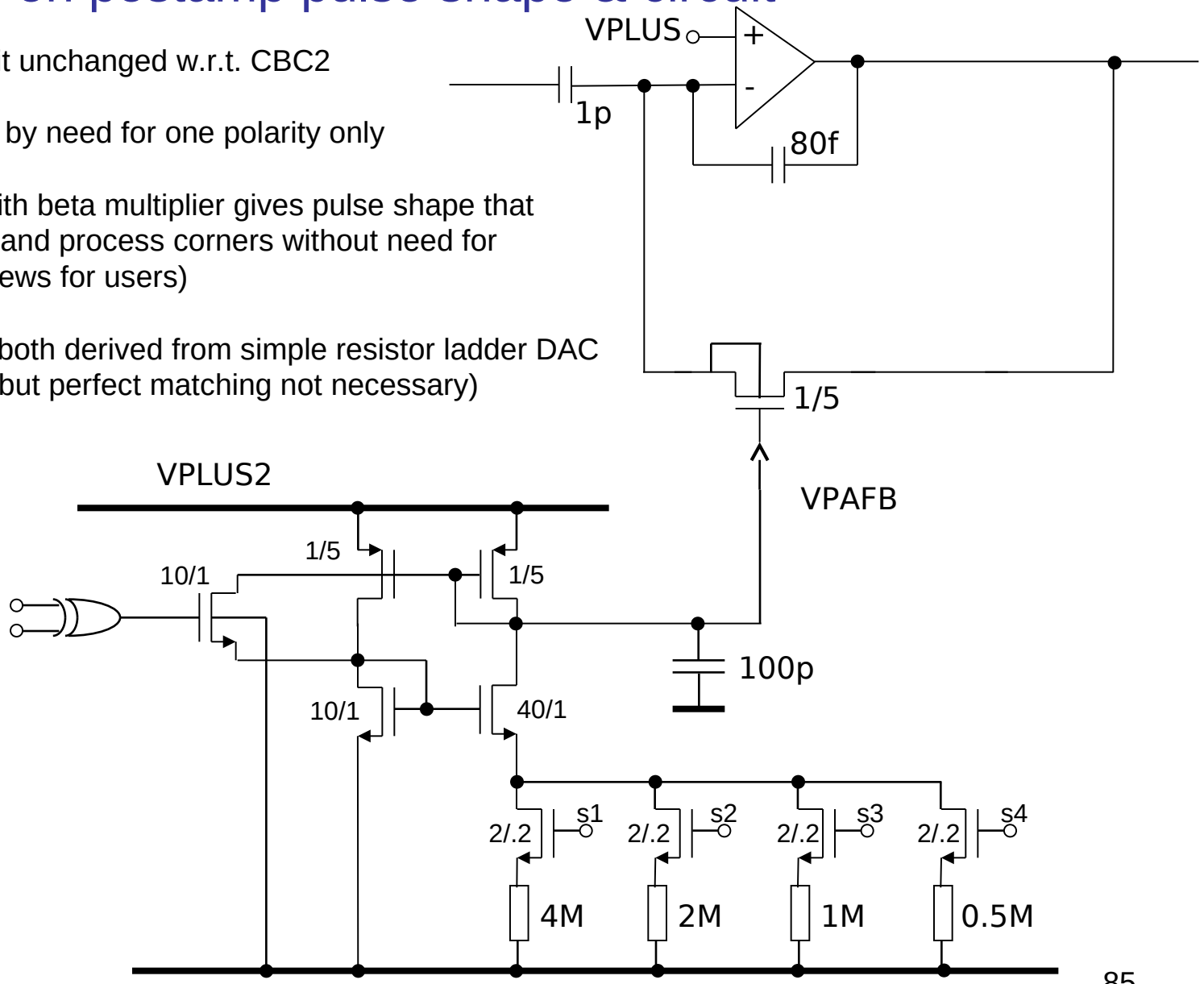
conclusions on postamp pulse shape & circuit

postamp core circuit unchanged w.r.t. CBC2

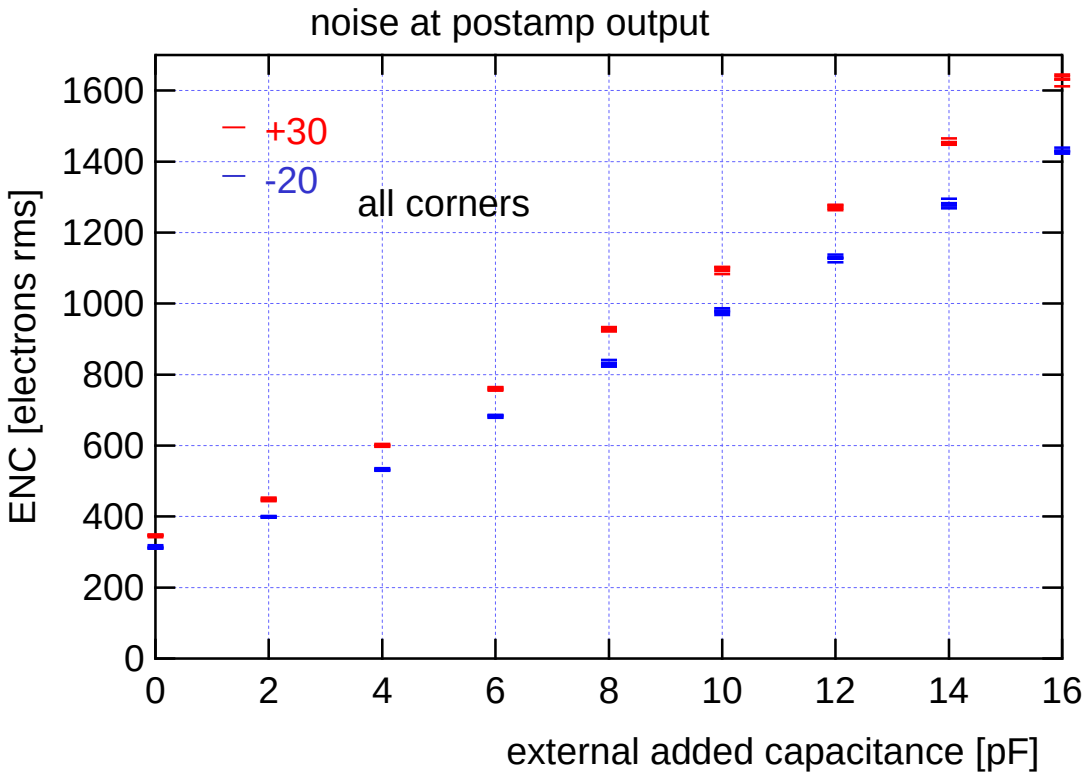
feedback simplified by need for one polarity only

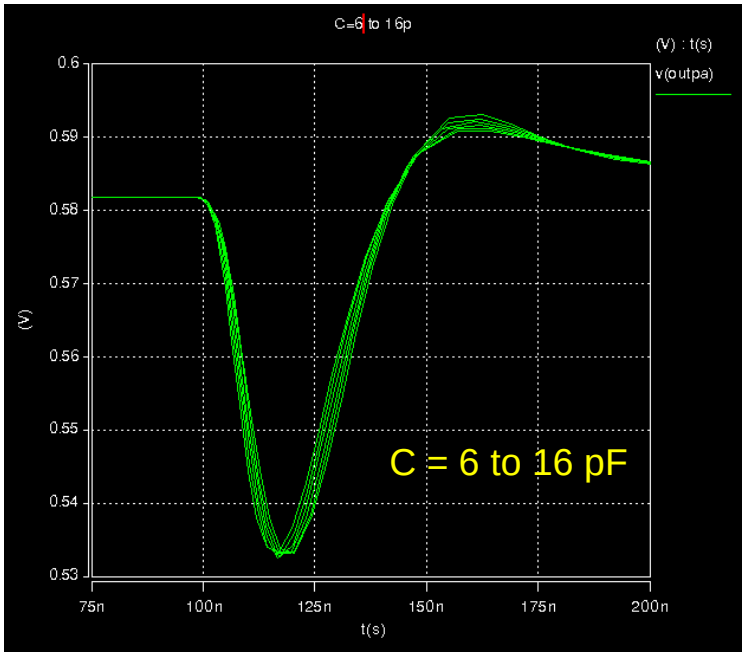
feedback biasing with beta multiplier gives pulse shape that tracks temperature and process corners without need for adjustment (good news for users)

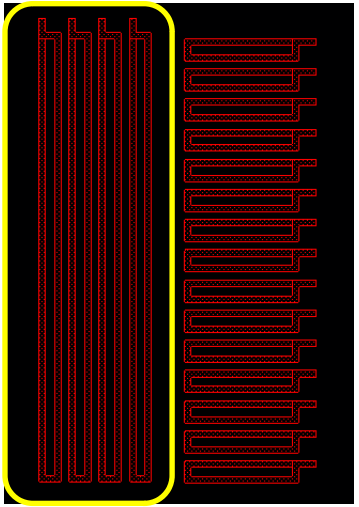
VPLUS = VPLUS2 both derived from simple resistor ladder DAC (should match well but perfect matching not necessary)



moving on to noise







above for nominal bias conditions (~230 uA in input transistor)

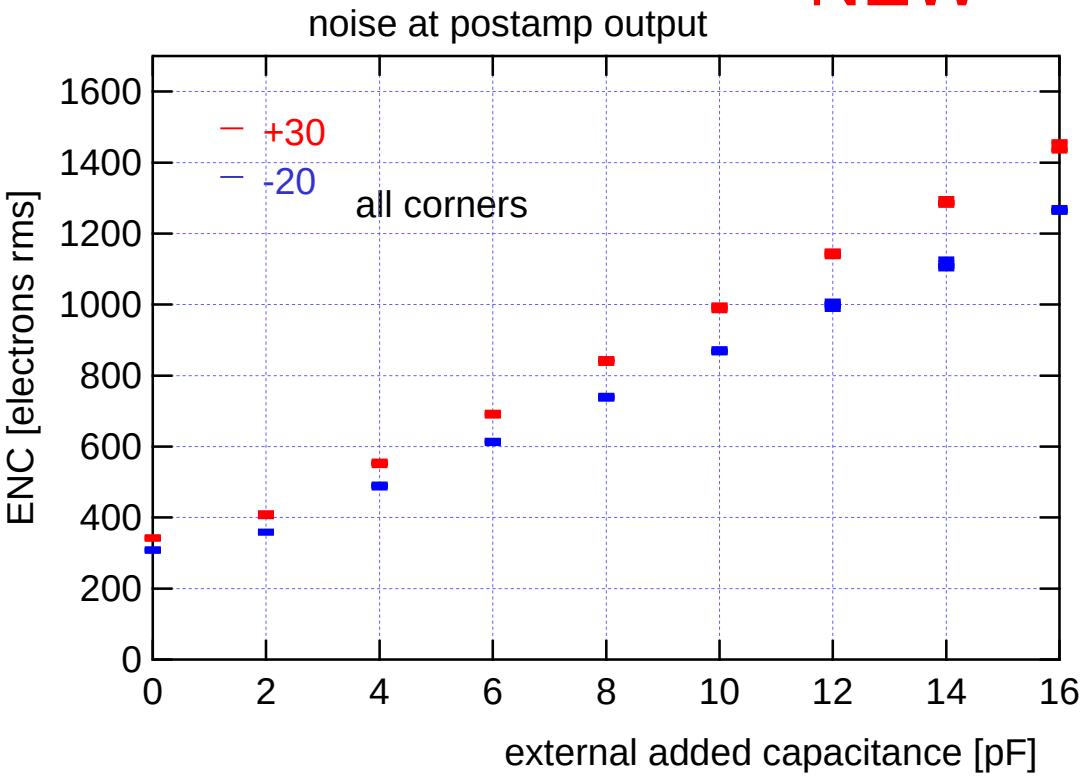
1000e ~achievable for external cap. up to ~10 pF at preamp input

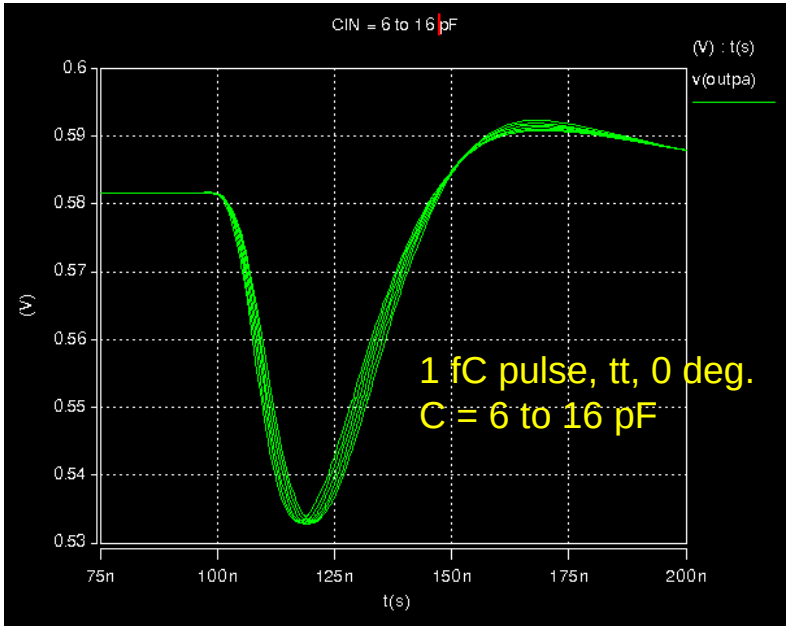
no strong dependence on process corners, can rely on tt sims

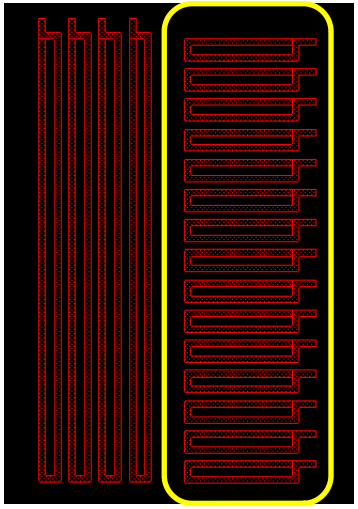
pulse shape varies not much over quite large input capacitance range

moving on to noise

NEW







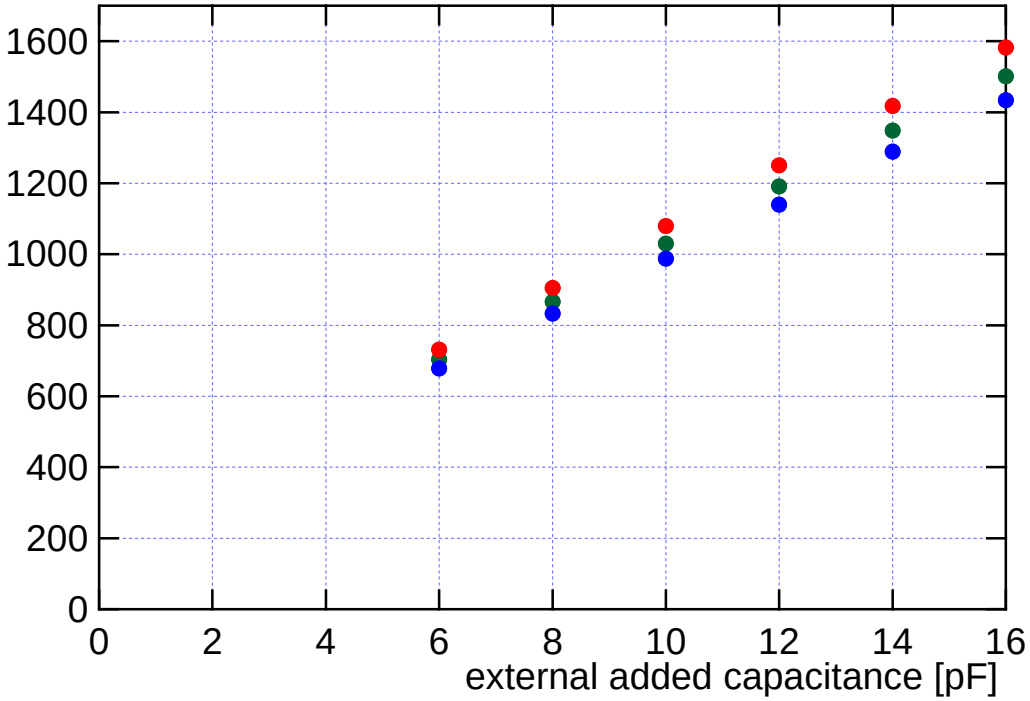
above for nominal bias conditions (~230 uA in input transistor)

1000e ~achievable for external cap. up to ~10 pF at preamp input

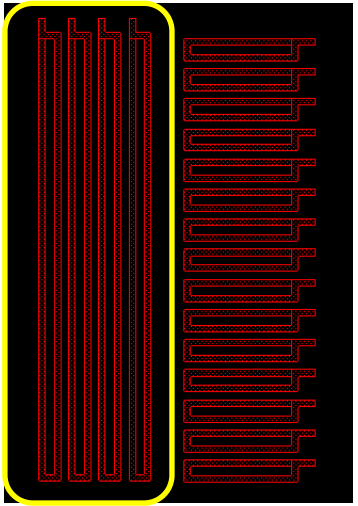
no strong dependence on process corners, can rely on tt sims

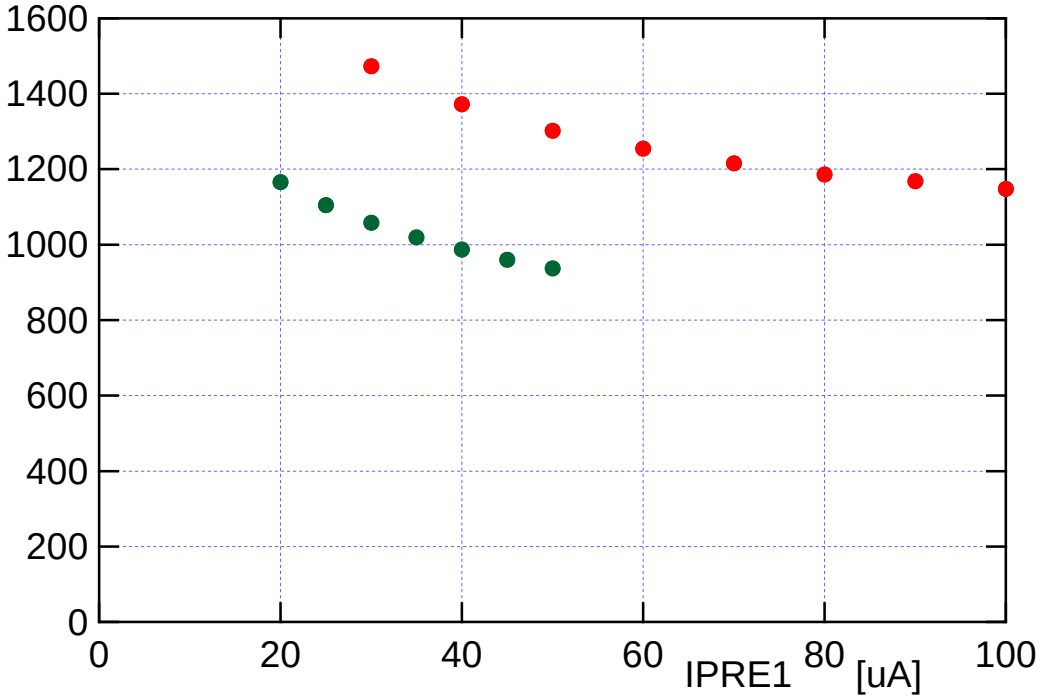
pulse shape/height varies not much over quite large input capacitance range

more noise sims

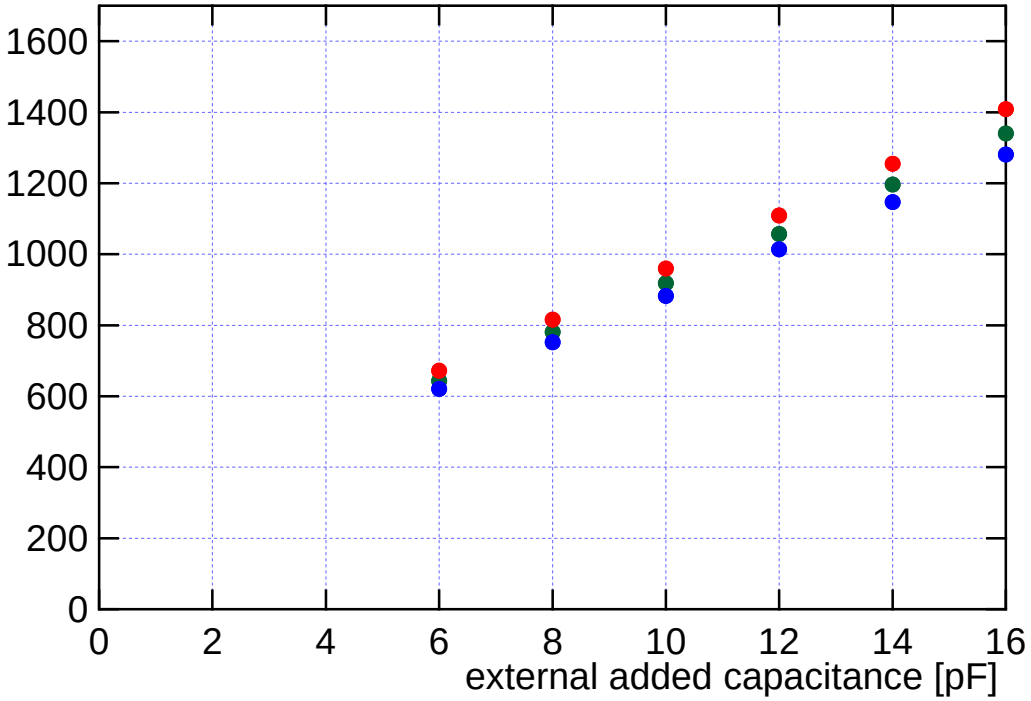


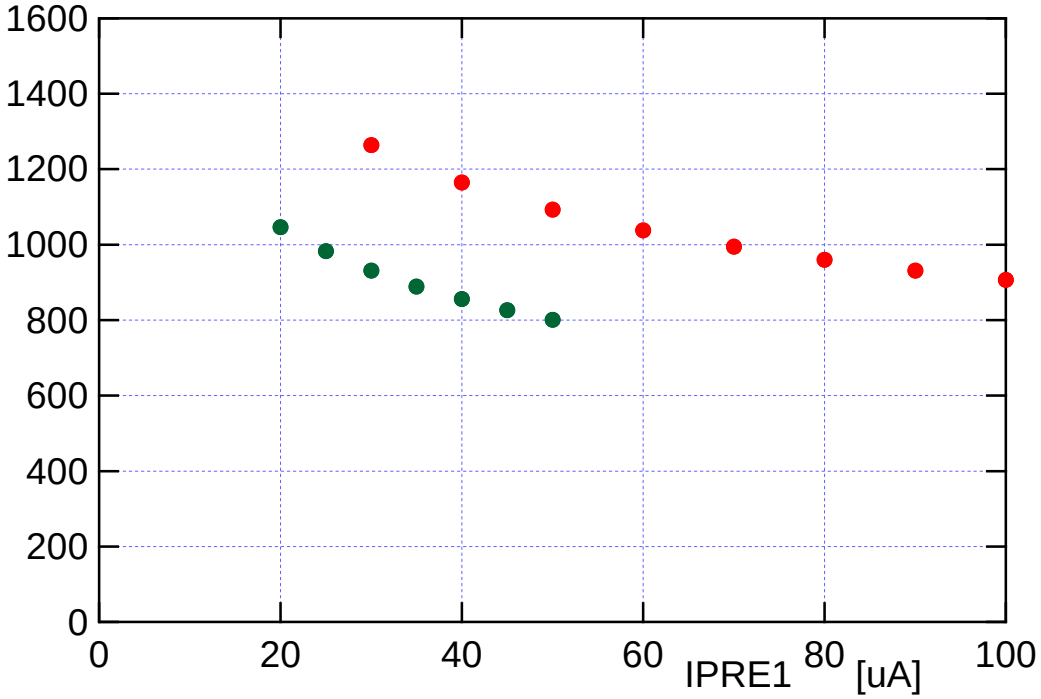
tt, T=0, IPRE1=35uA
Rpf =100k, Cpf = 100fF
Rpf -15%, Cpf-10%
Rpf +15%, Cpf+10%





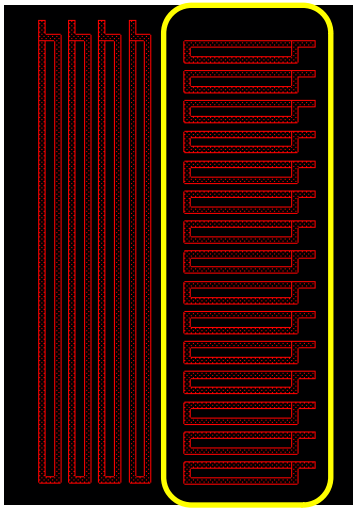
tt, T=0,
external C = 10 pF
external C = 15 pF





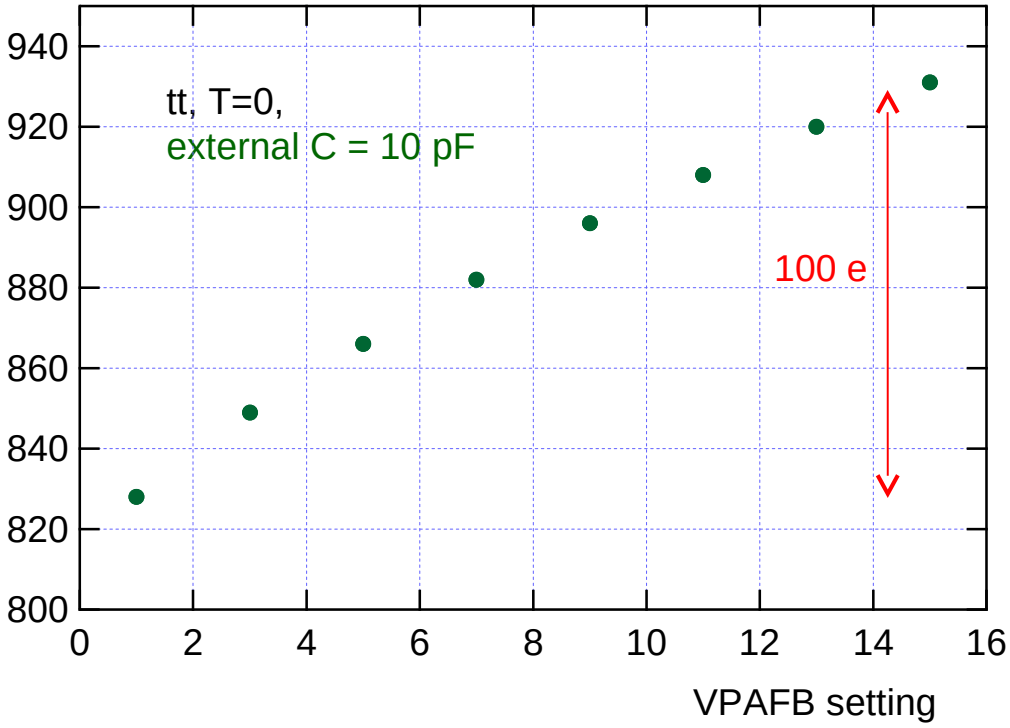
NEW more noise sims

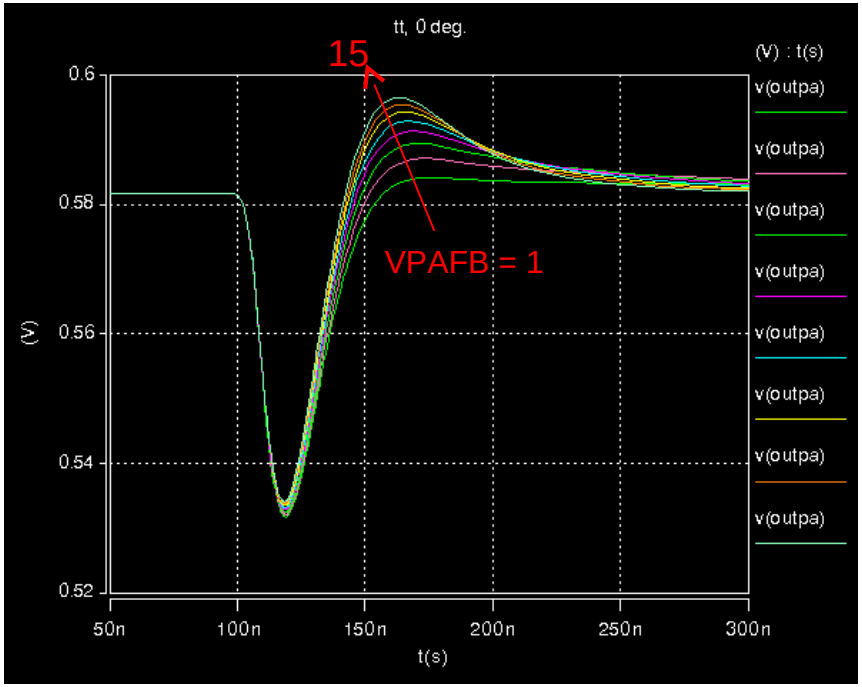
tt, T=0, IPRE1=35uA
Rpf =100k, Cpf = 100fF
Rpf -15%, Cpf-10%
Rpf +15%, Cpf+10%

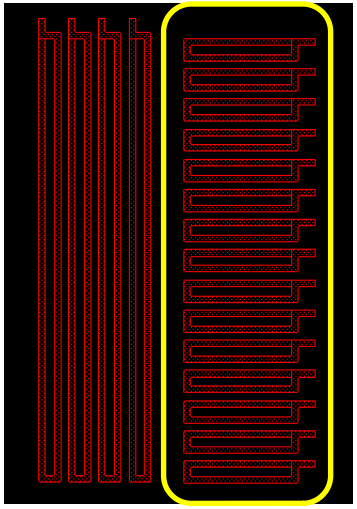


tt, T=0,
external C = 10 pF
external C = 15 pF

more noise sims

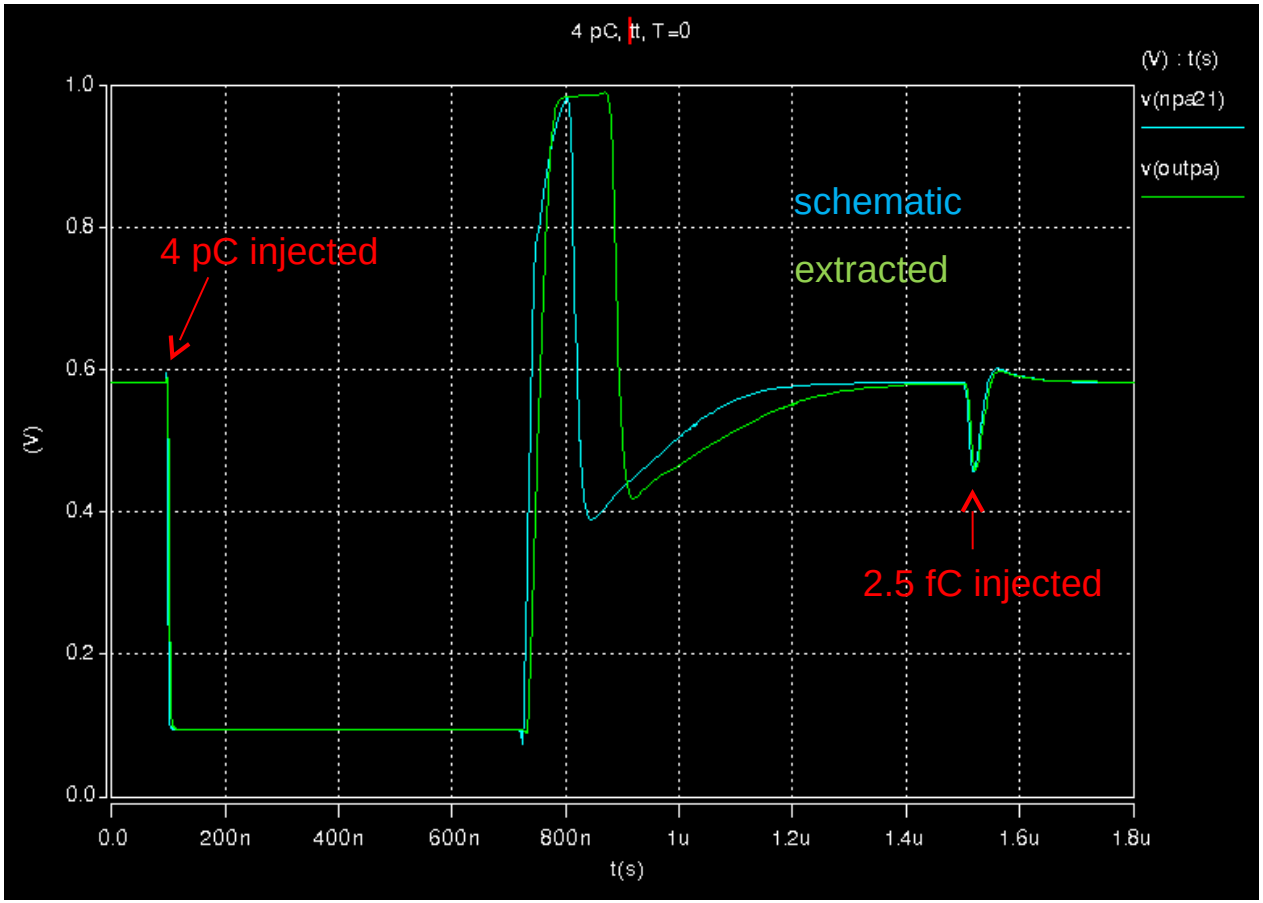






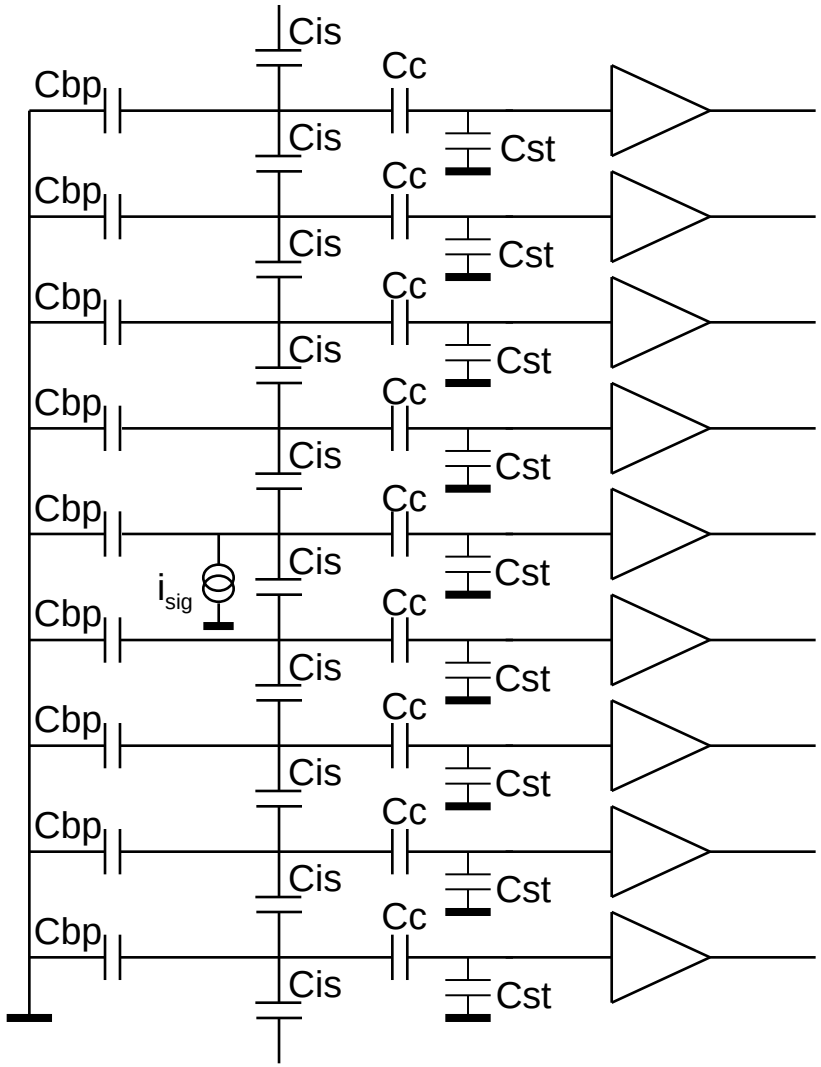
hips

postamp output



single channel response to 4 pC
some differences in response between schematic and extracted
overall recovery time similar

hips - multichannel



using extracted preamp&postamp

21 channels simulated (centre + 10 either side)

(previously simulated more but for schematic only)

Cbp = 4p, Cis = 2.5p, Cc = 150p, Cst = 1p
(Ctot = ~10pF)

signal channel

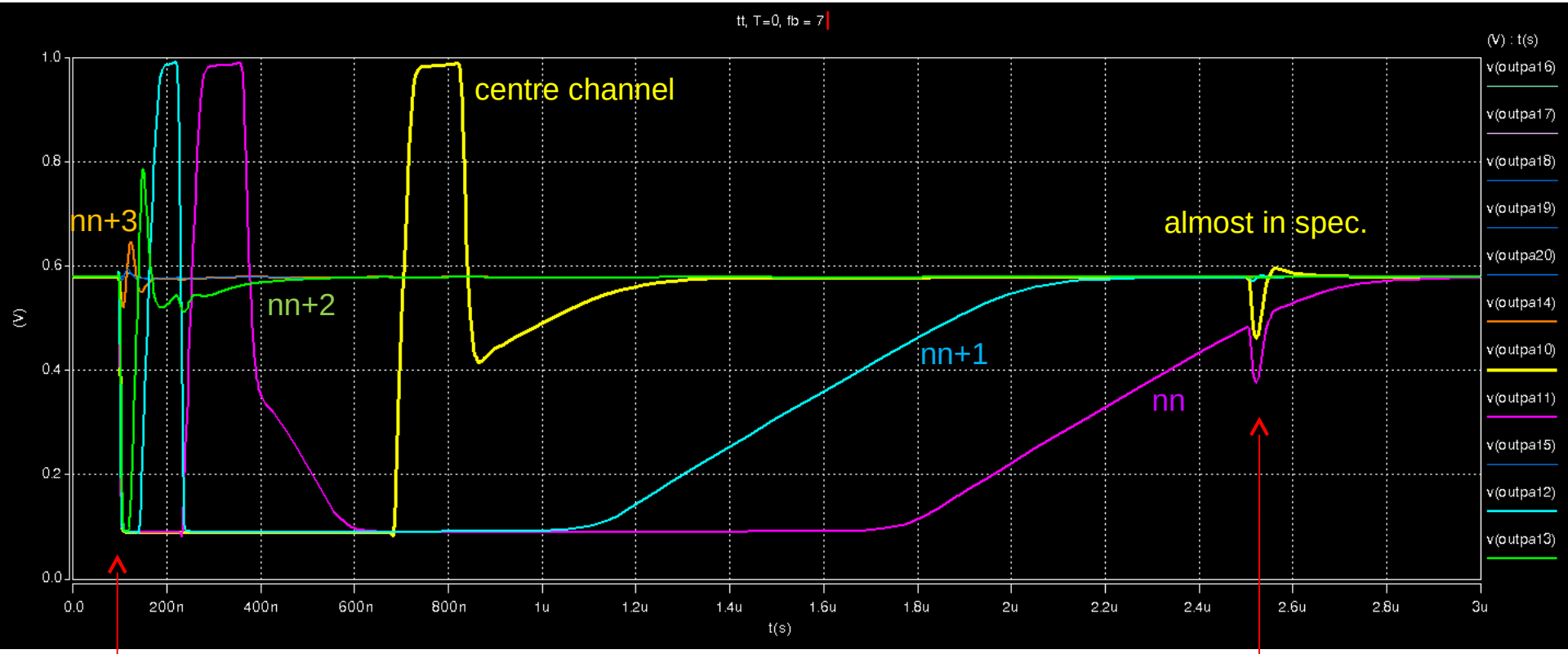
nn

nn + 1

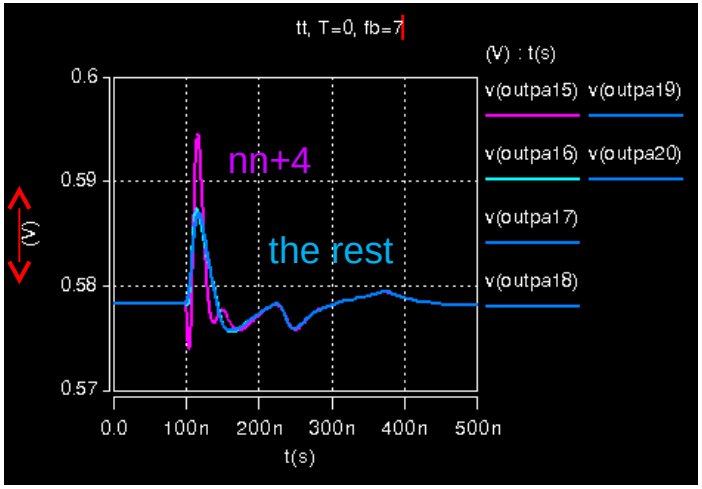
nn + 2

etc..

hips - multichannel - VPAFB bias 7 (0-15)



4 pC injected on centre channel

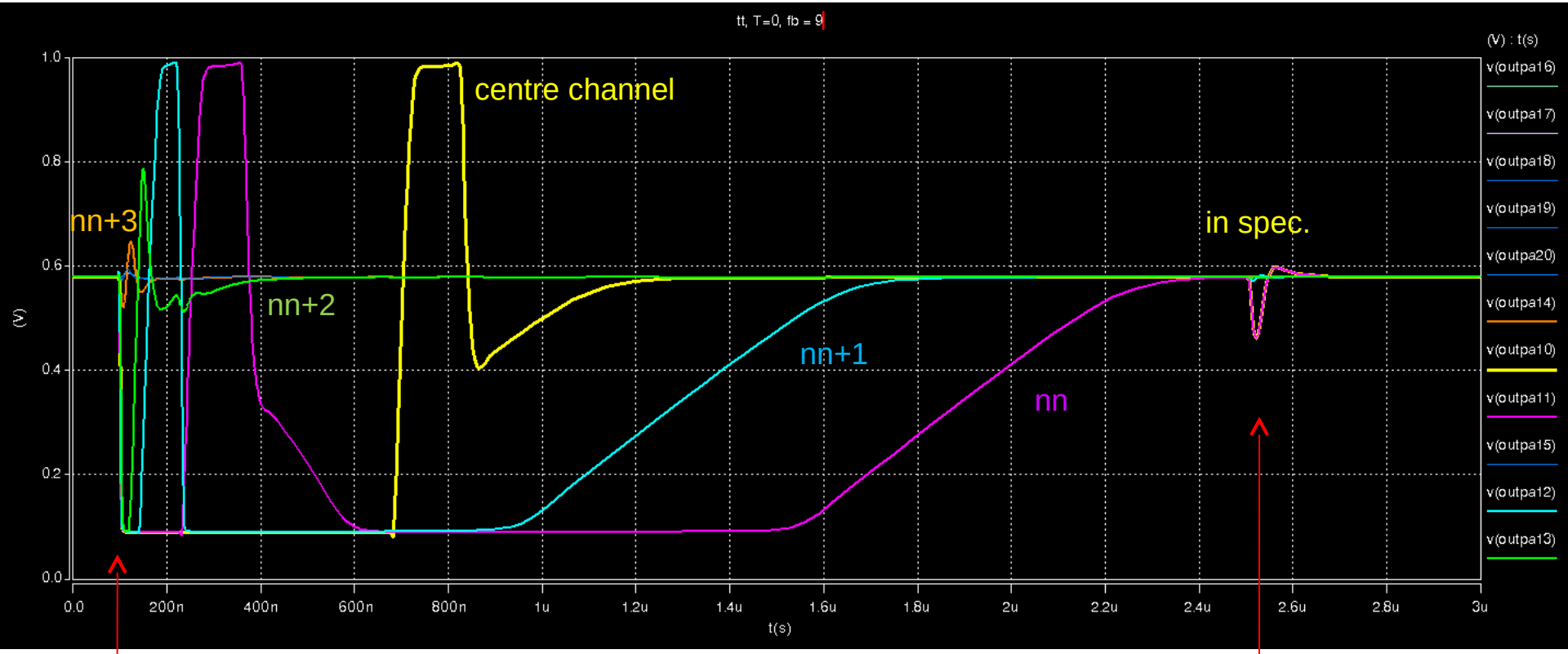


10 mV
= ~0.2 fC

2.5 fC injected on centre channel & nearest neighbour

tt sim, T = 0
(Not much dependence on process. Baseline recovery slightly faster at higher T)

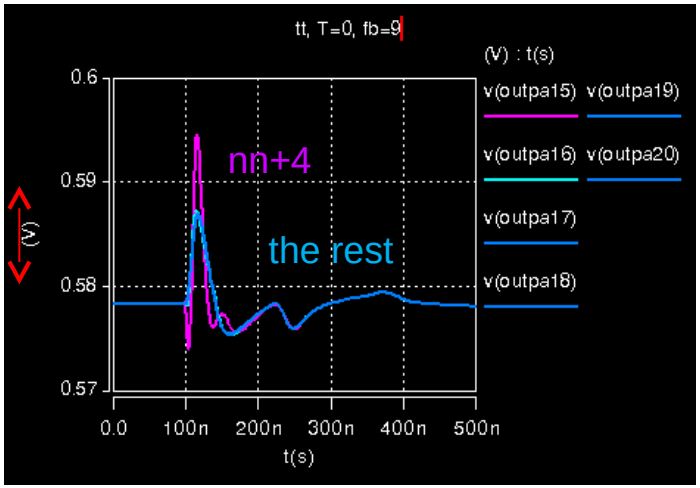
hips - multichannel - VPAFB bias **9** (0-15)



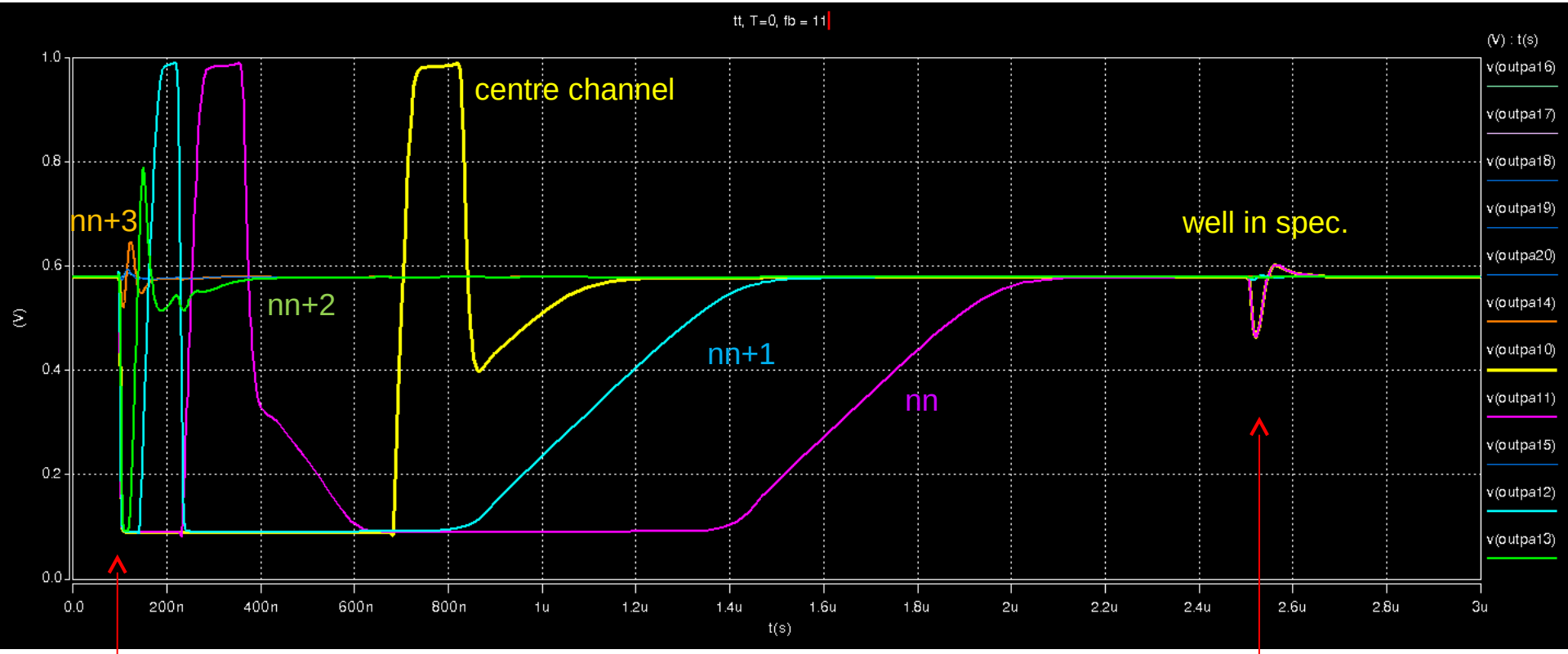
4 pC injected on centre channel

2.5 fC injected on centre channel & nearest neighbour

10 mV
= ~0.2 fC



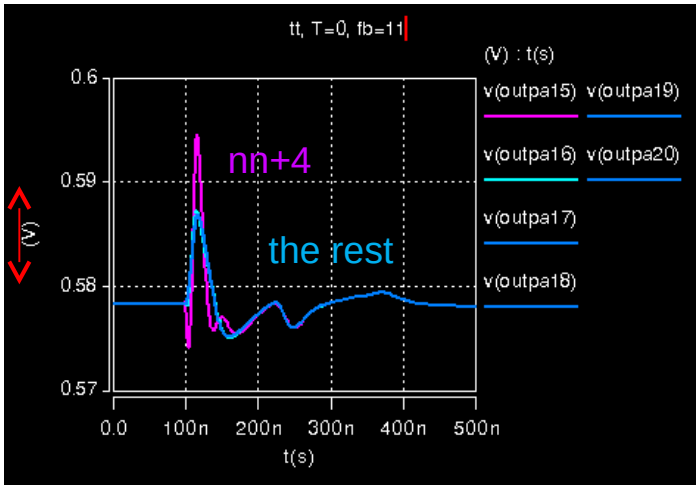
hips - multichannel - VPAFB bias **11** (0-15)



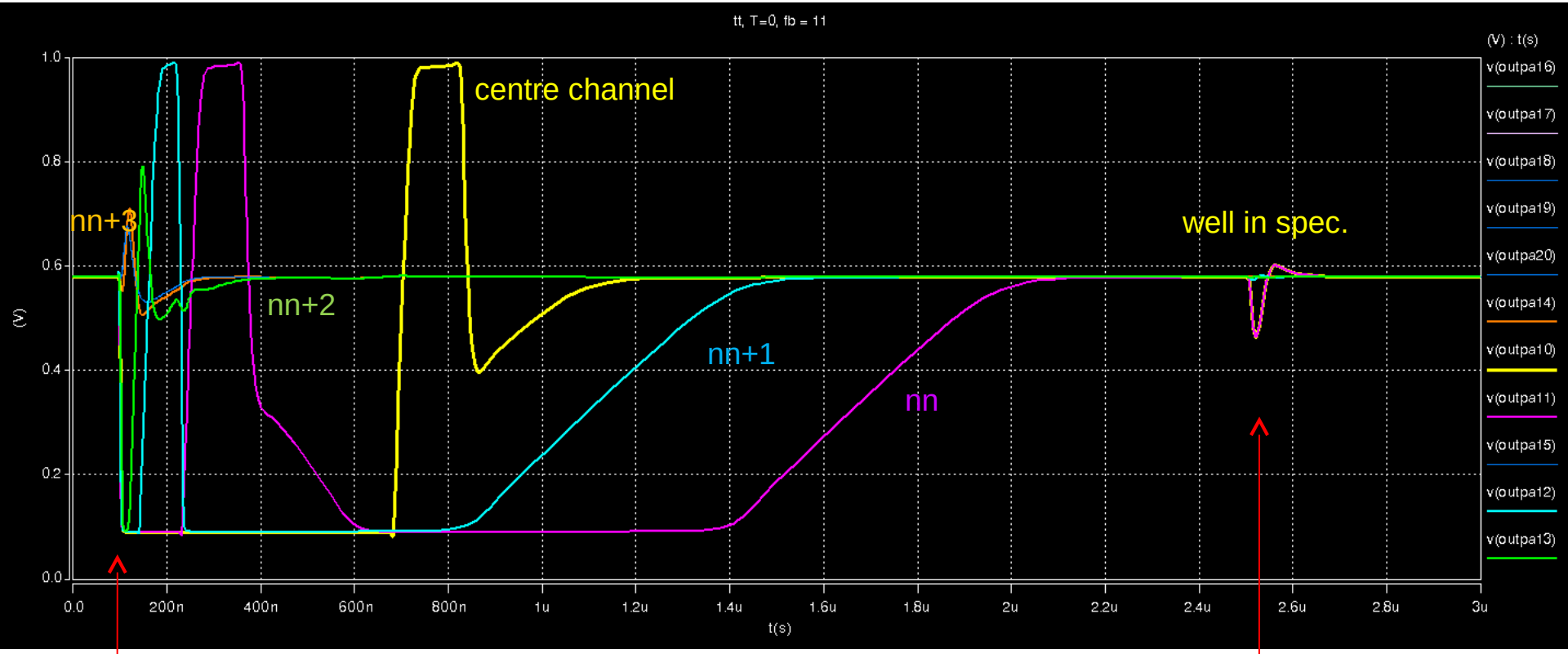
4 pC injected on centre channel

2.5 fC injected on centre channel & nearest neighbour

10 mV
= ~0.2 fC



hips - multichannel - effect of removing IPRE1 decoupling

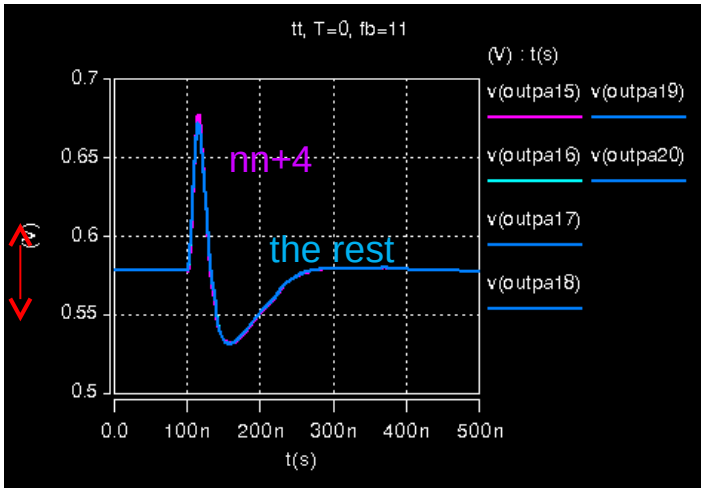


4 pC injected on centre channel

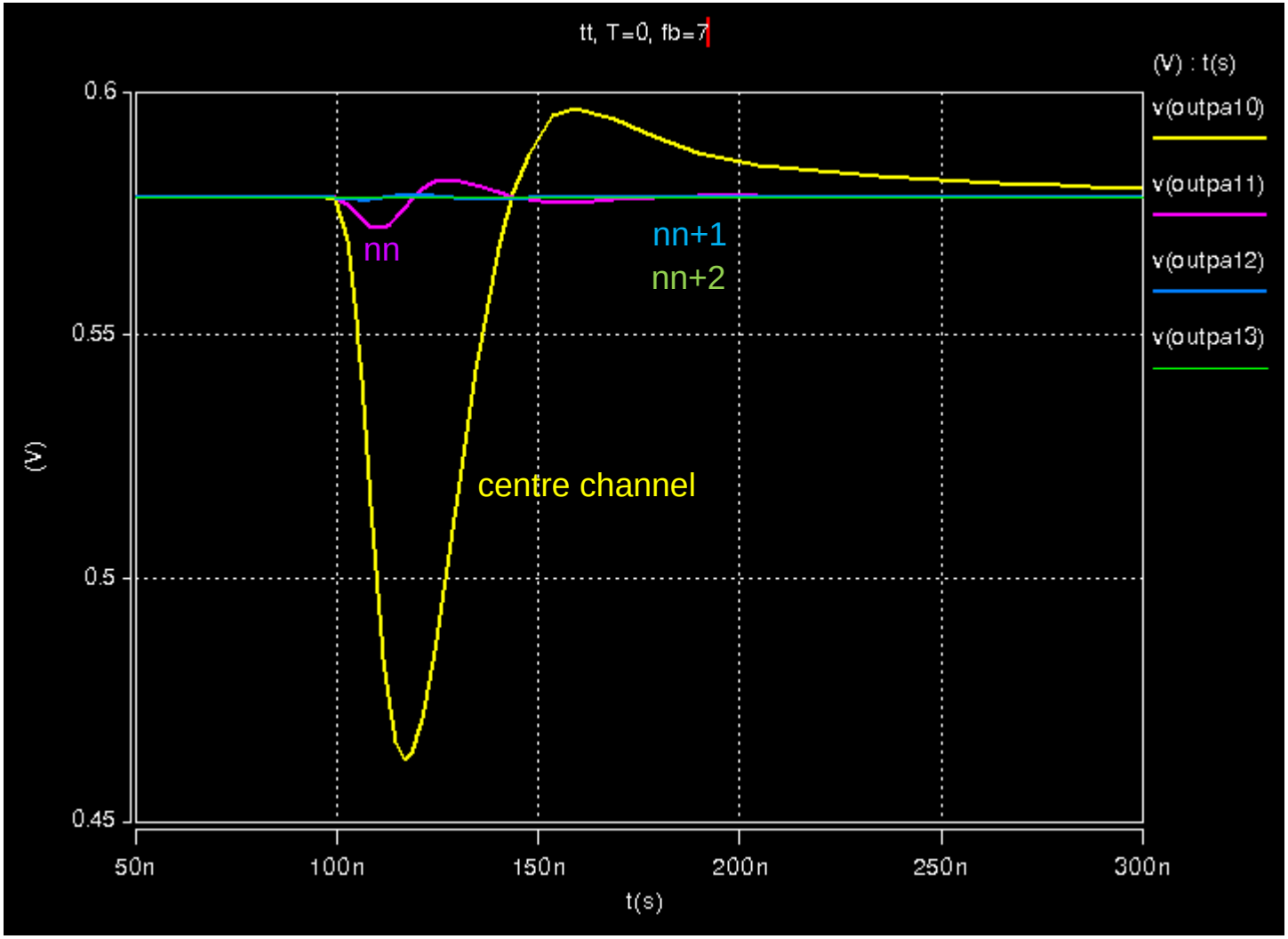
2.5 fC injected on centre channel & nearest neighbour

effect of removing decoupling on IPRE1 bias node

50 mV = ~1 fC



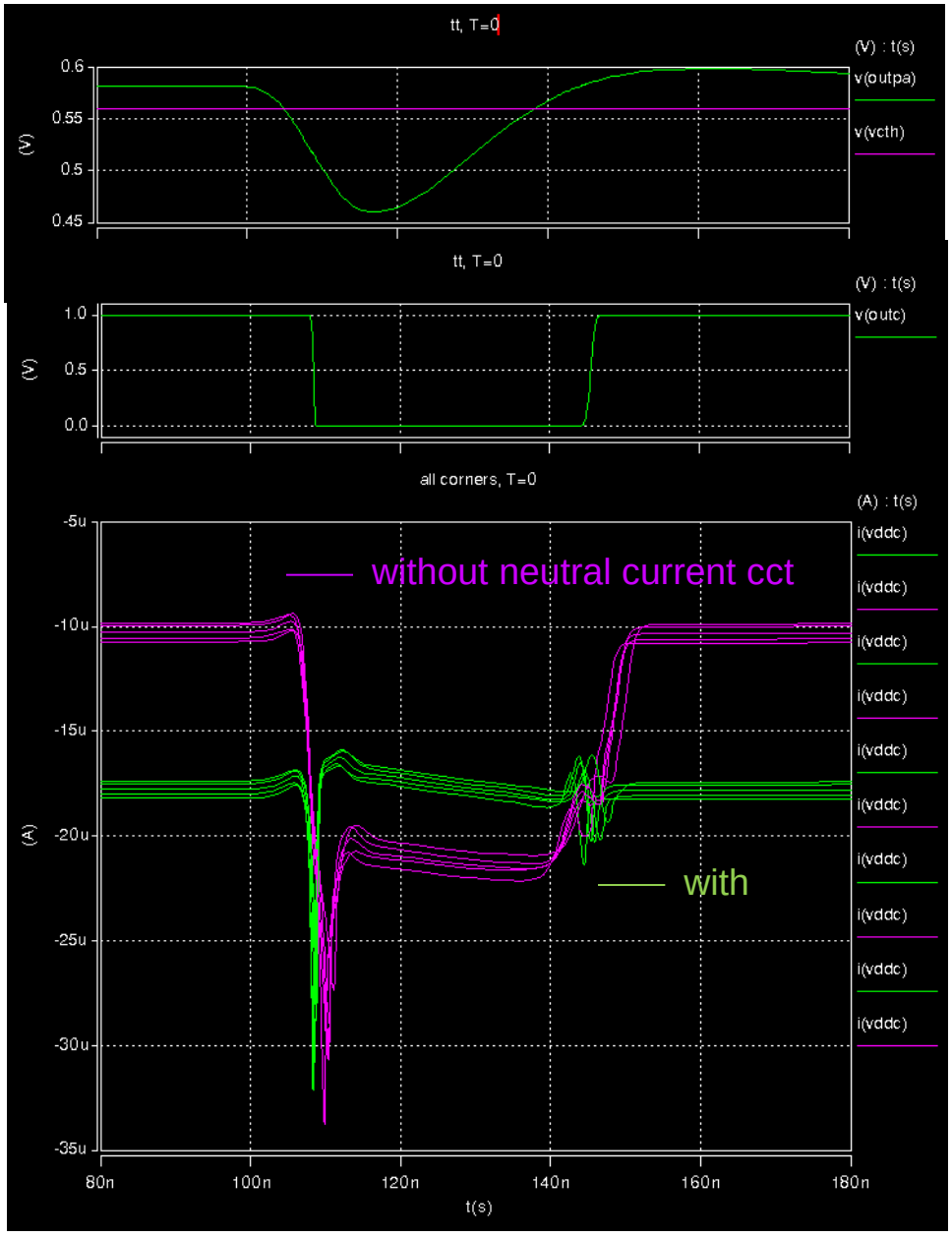
multichannel crosstalk



~5% crosstalk to nearest neighbour

comparator

current neutral circuit



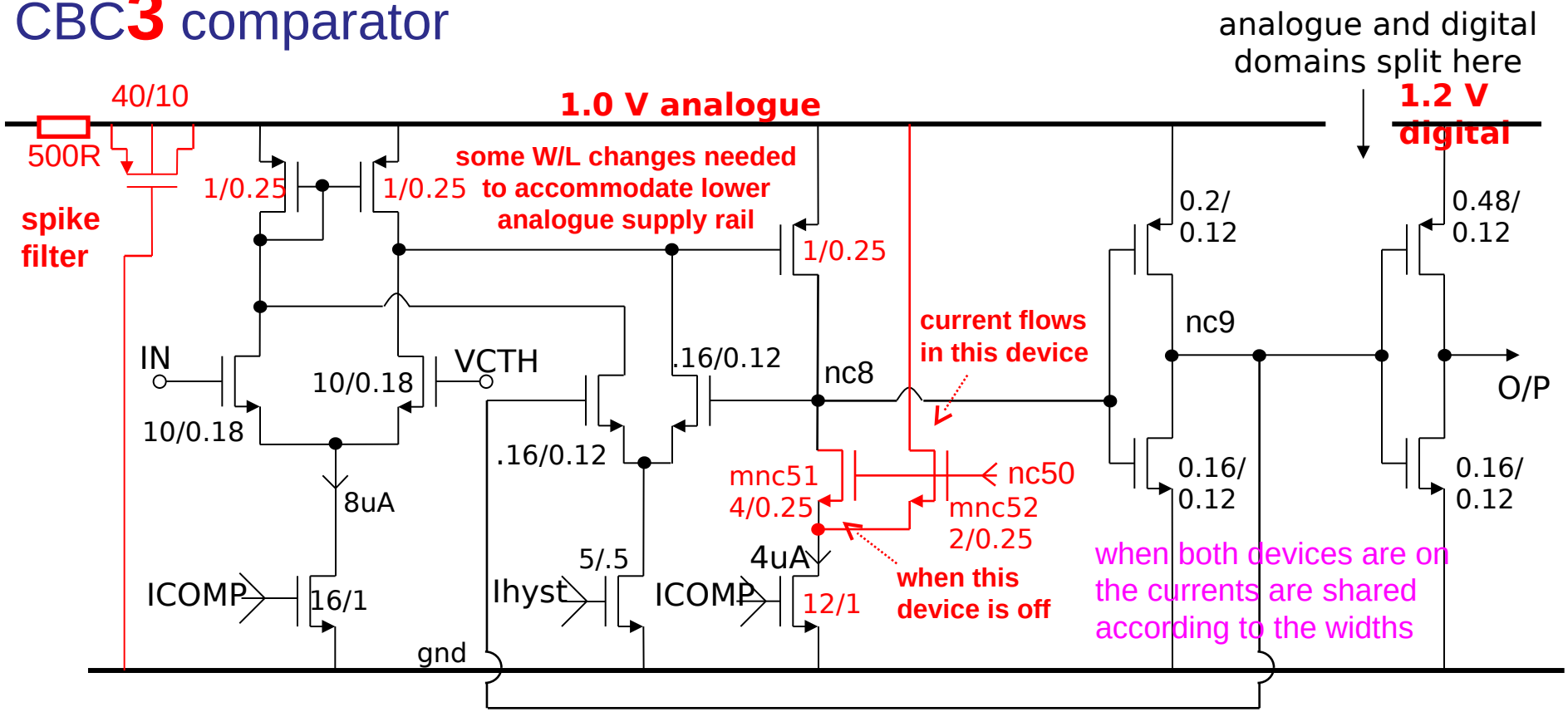
← postamp output & threshold

← comparator output

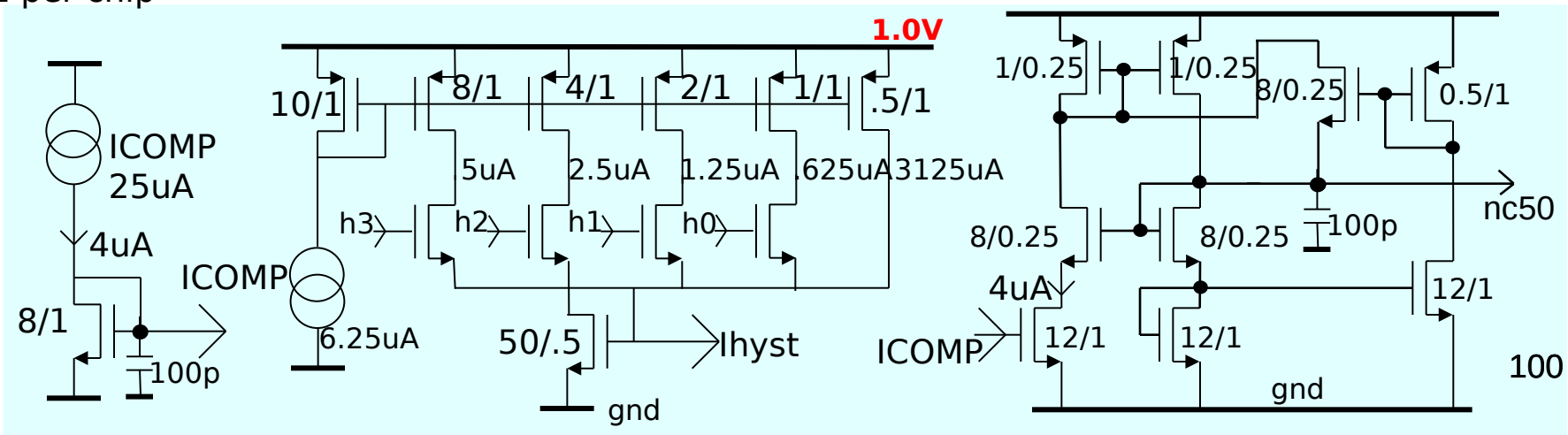
← current drawn by extracted comp. cct.
ICOMP = 5 uA
all corners, T=0
RC filter removed

some sharp spikes

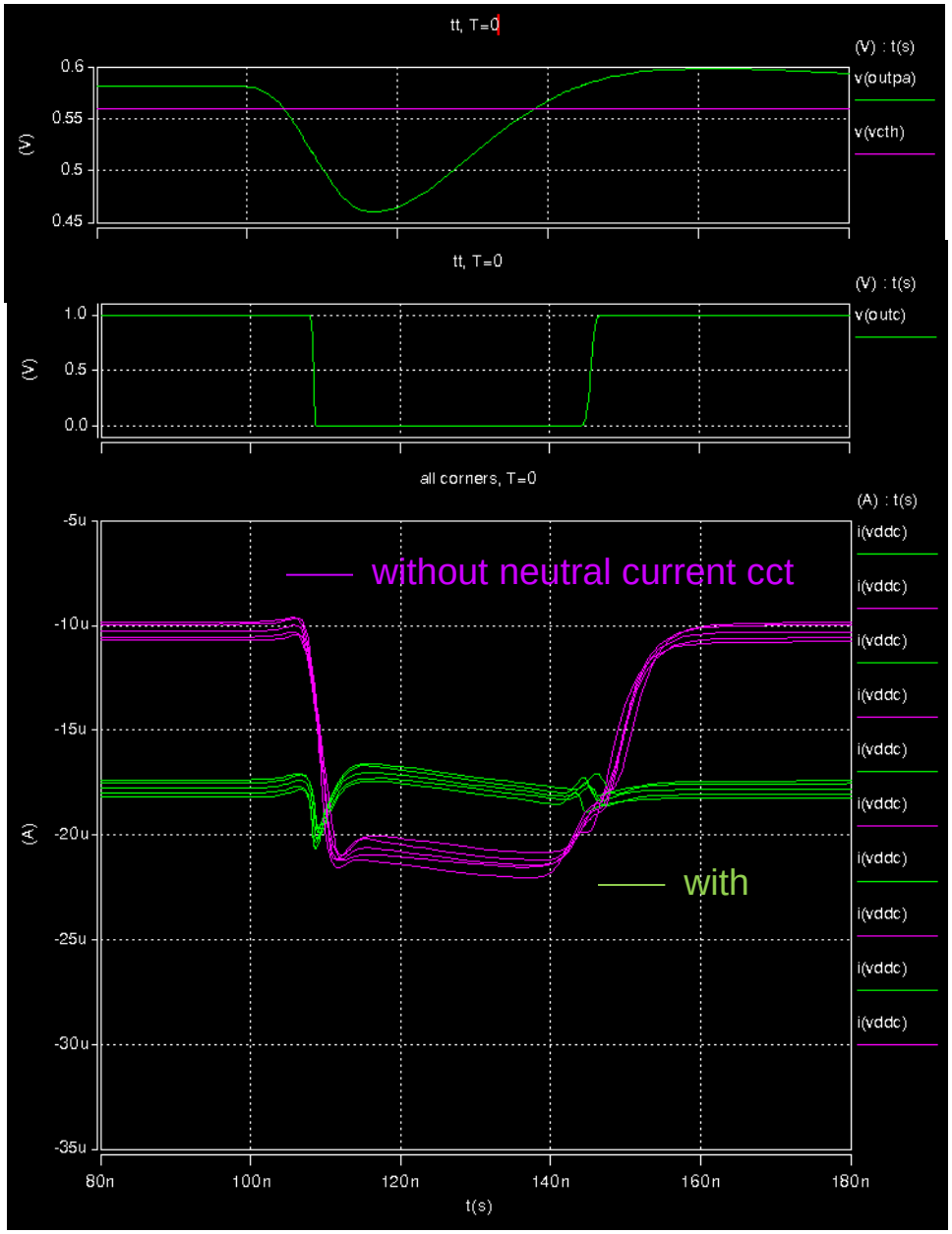
CBC3 comparator



1 per chip



current neutral circuit



← postamp output & threshold

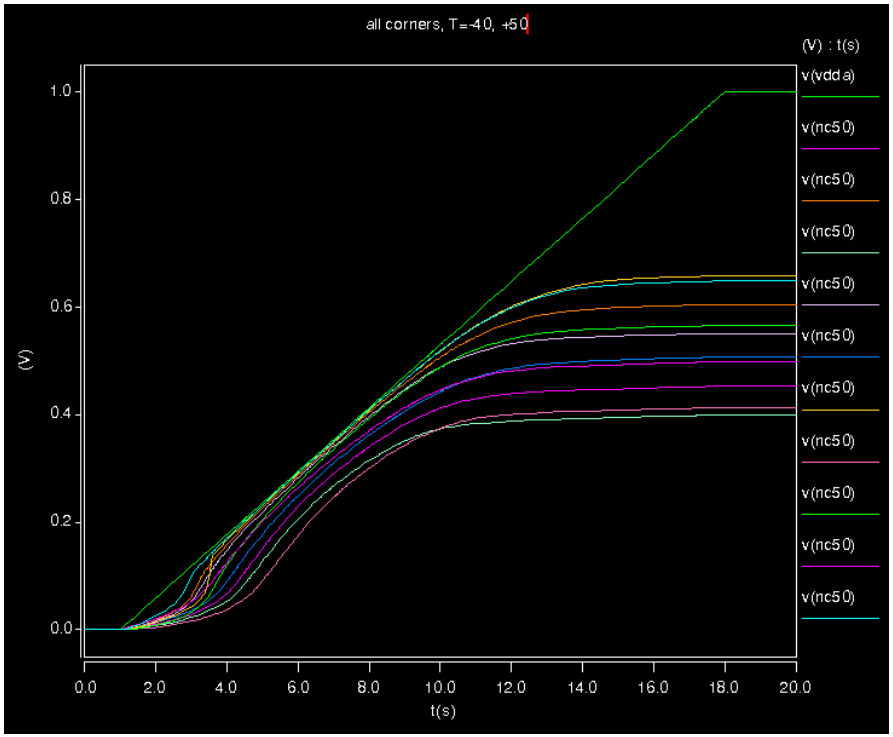
← comparator output

← current drawn by extracted comp. cct.
ICOMP = 5 uA
all corners, T=0
RC filter replaced

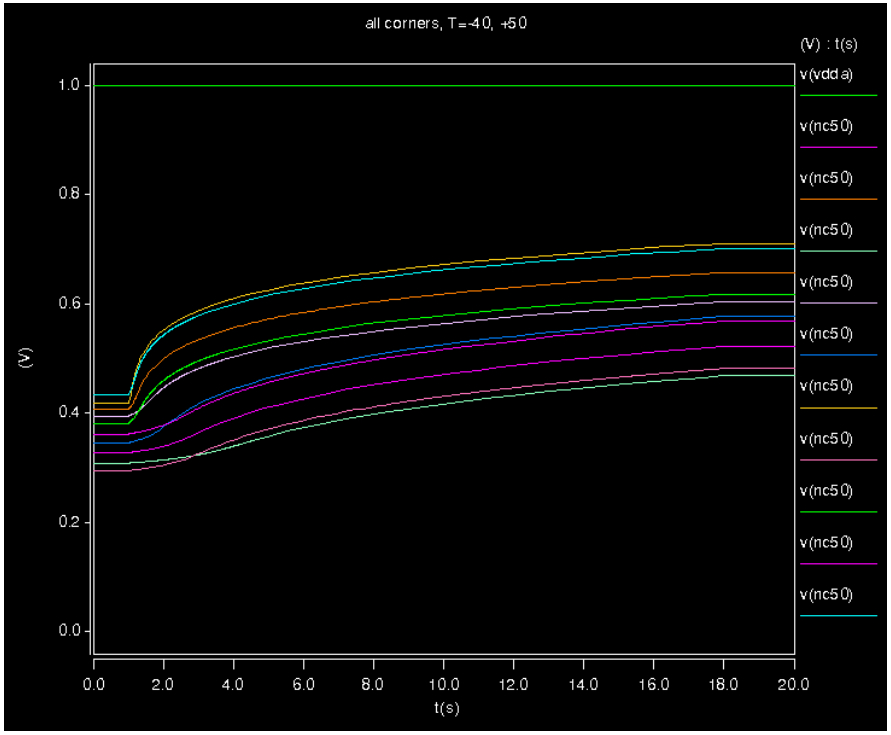
spikes substantially attenuated

nc50 startup

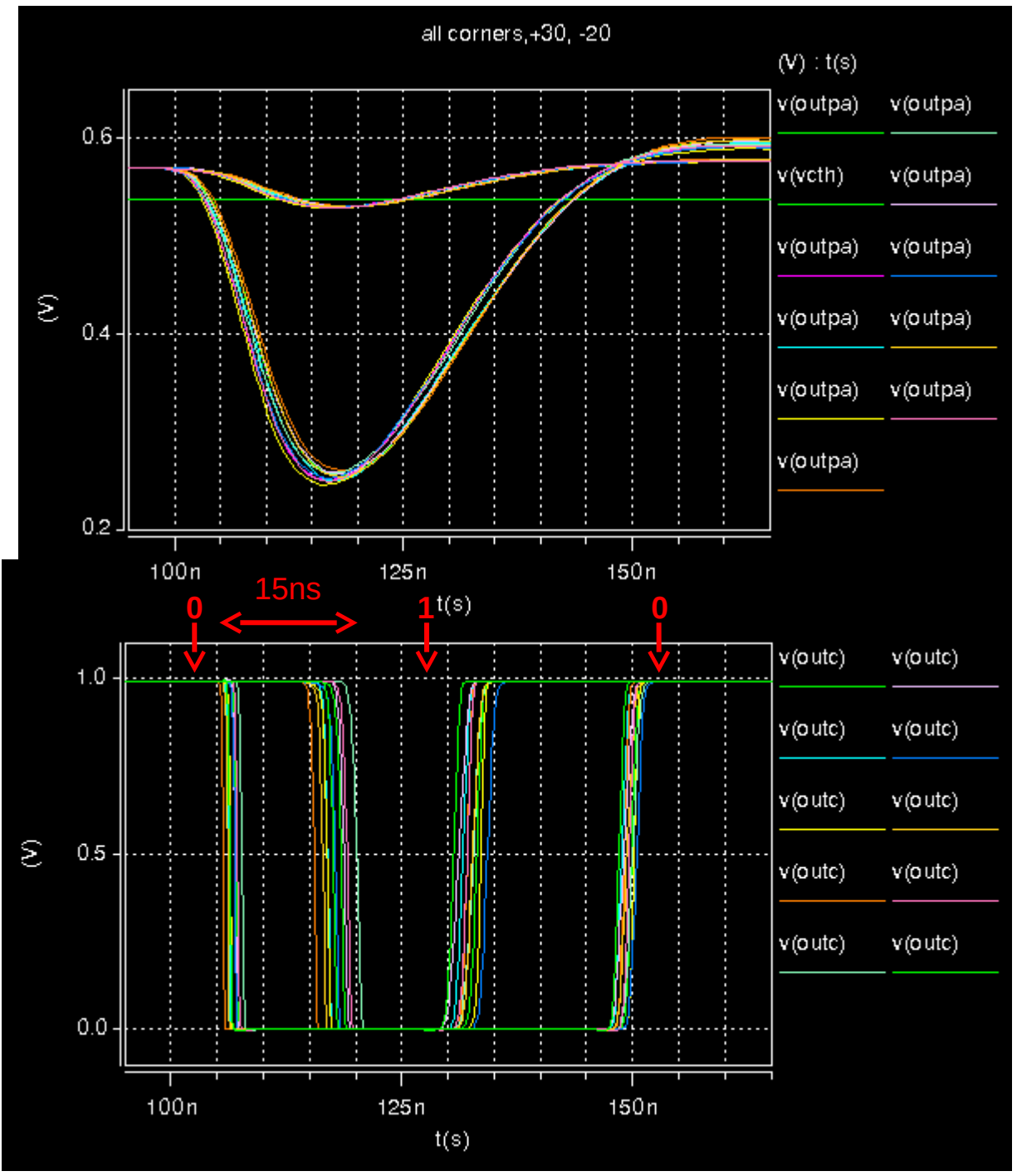
VDDA ramps to 1V in ~ 20secs
all corners, extracted circuit
ICOMP = 5u
+50, -40



VDDA = 1V
all corners, extracted circuit
ICOMP ramps to 12uA in ~ 20secs
+50, -40

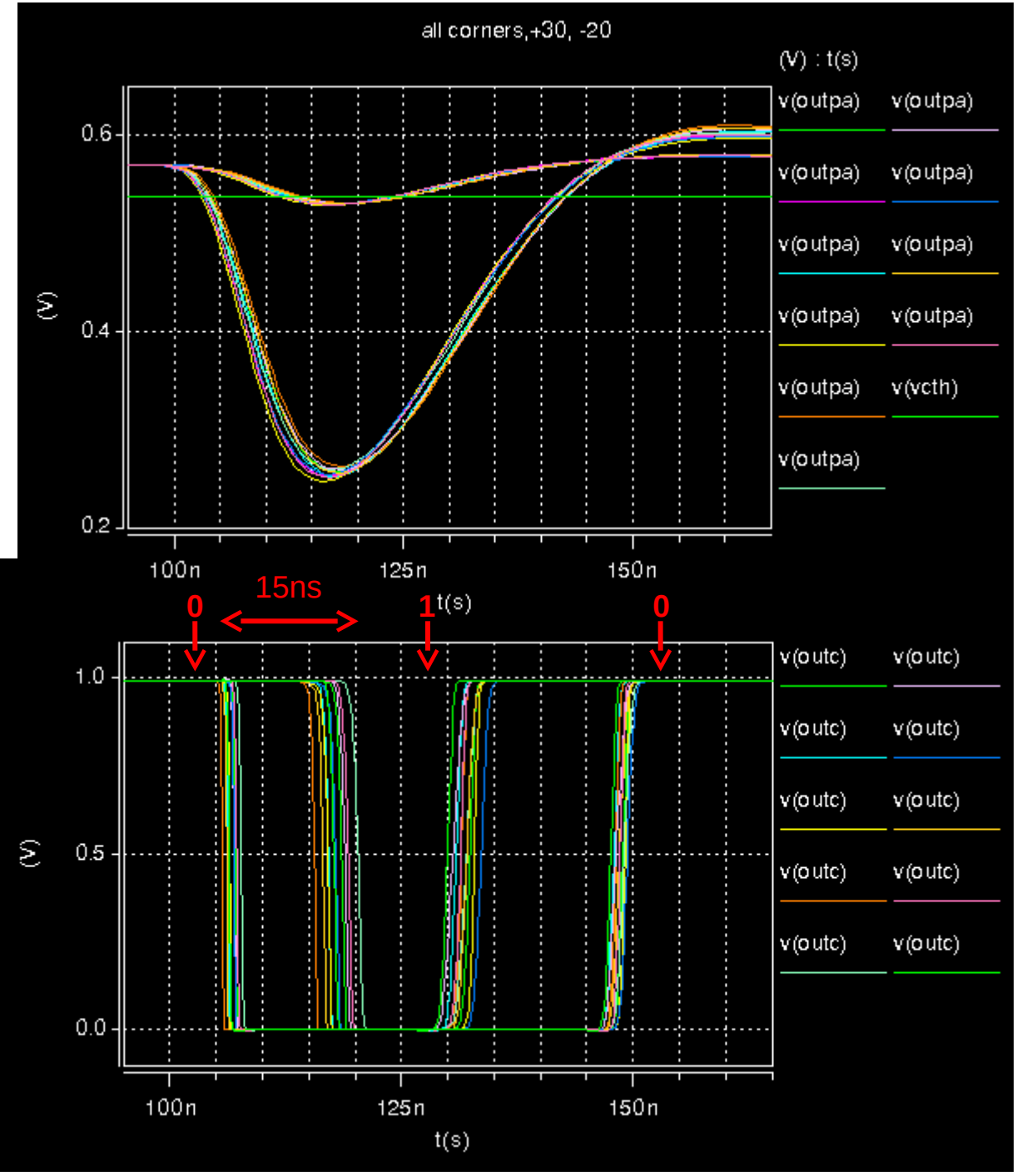


timewalk



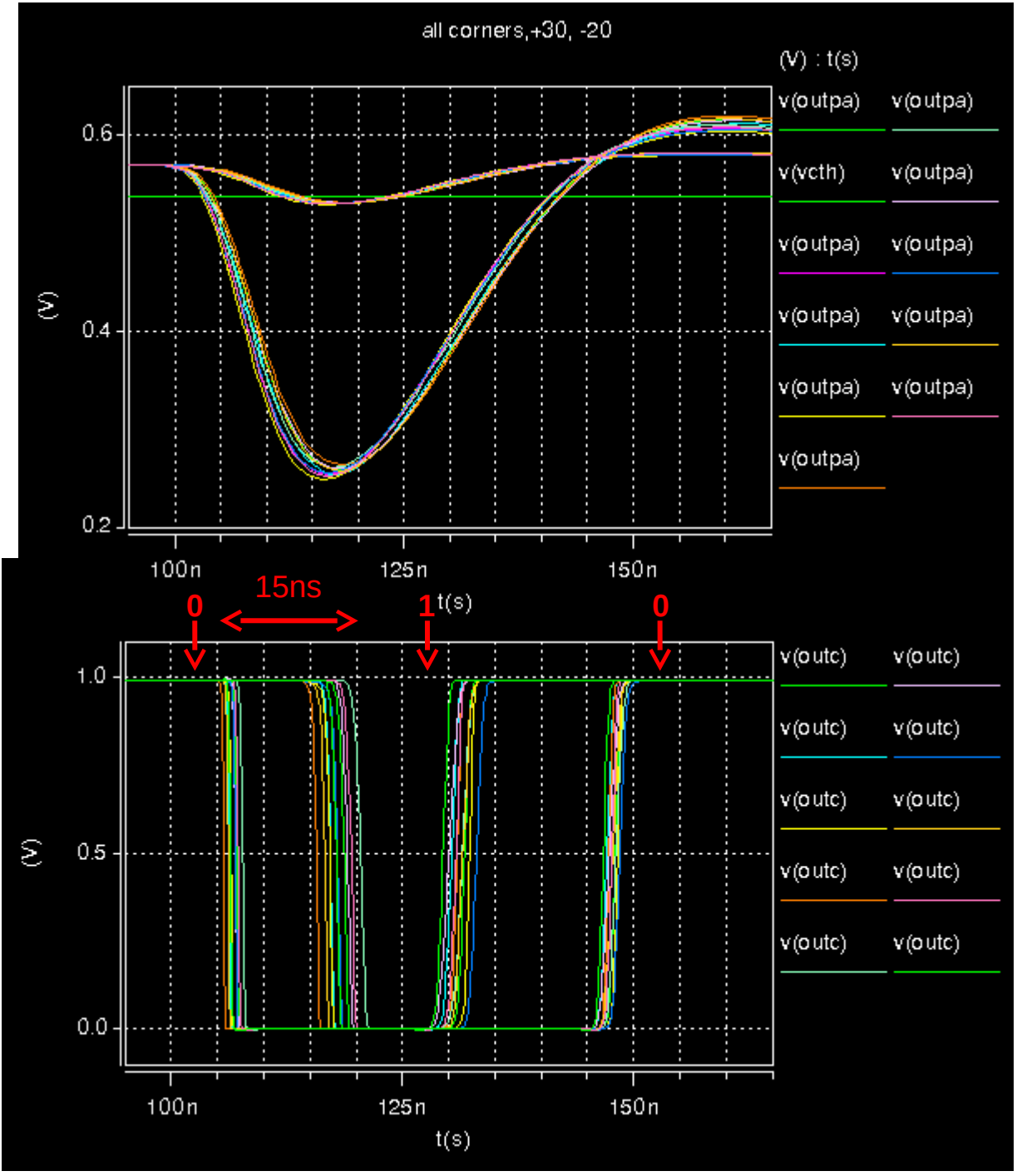
VPAFB = 7
thresh = .67 fC
sig=0.83 fC & 6.7 fC
hyst = 0 (minimum)

timewalk



VPAFB = 11
thresh = .67 fC
sig=0.83 fC & 6.7 fC
hyst = 0

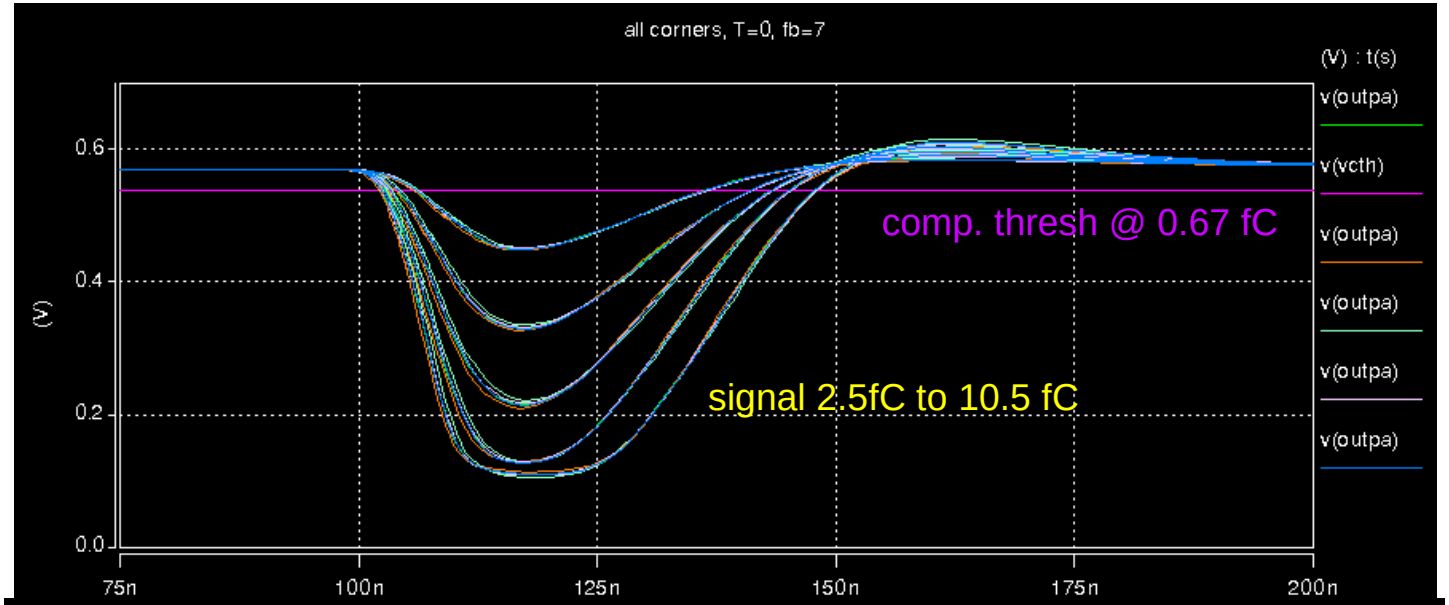
timewalk

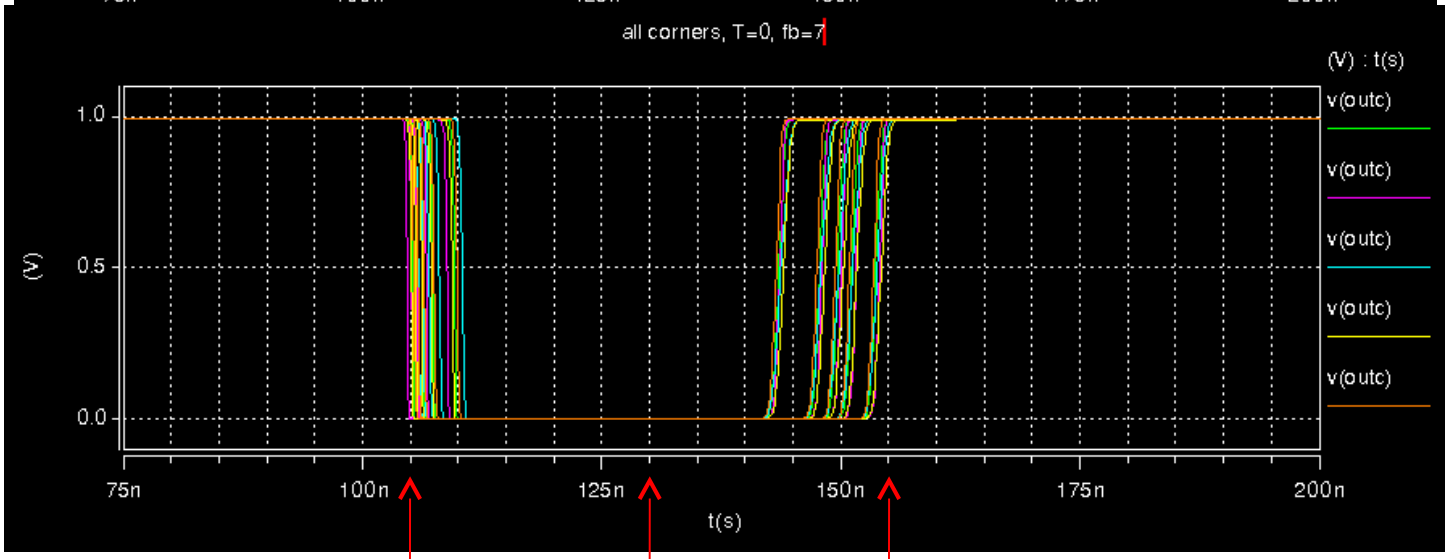


VPAFB = 15
thresh = .67 fC
sig=0.83 fC & 6.7 fC
hyst = 0

timewalk within spec.

comp. response: T=0, VPAFB = 7, nom params, all corners



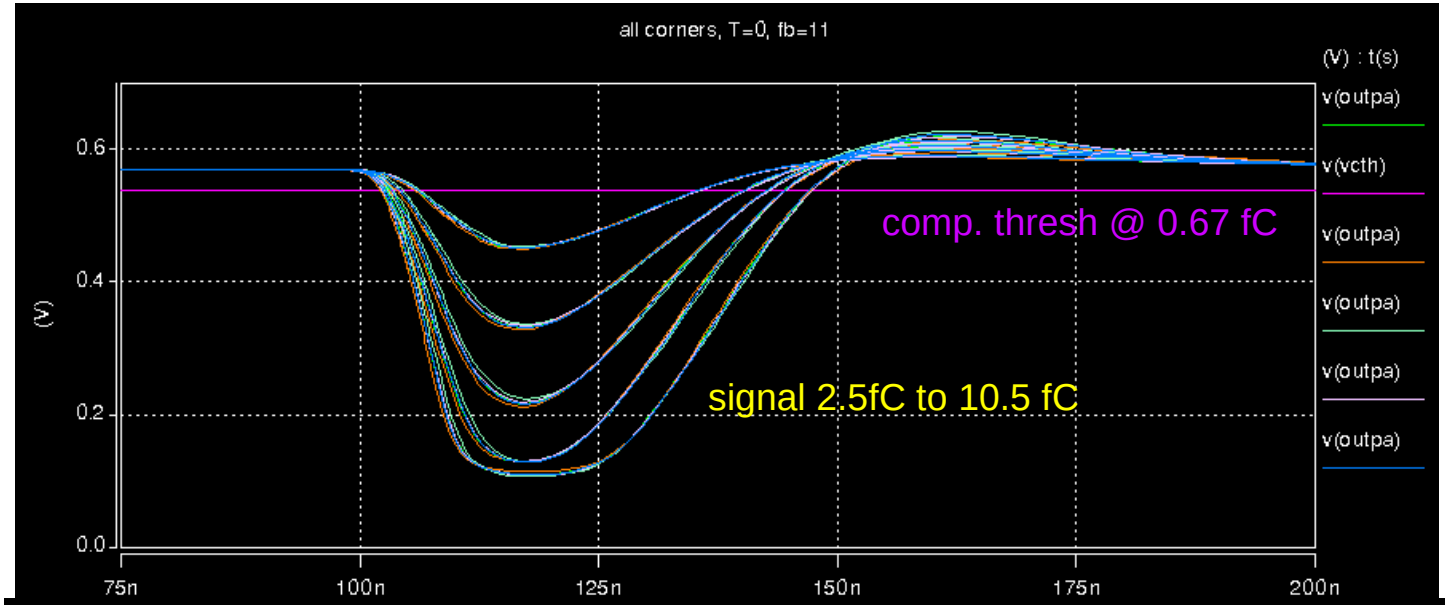


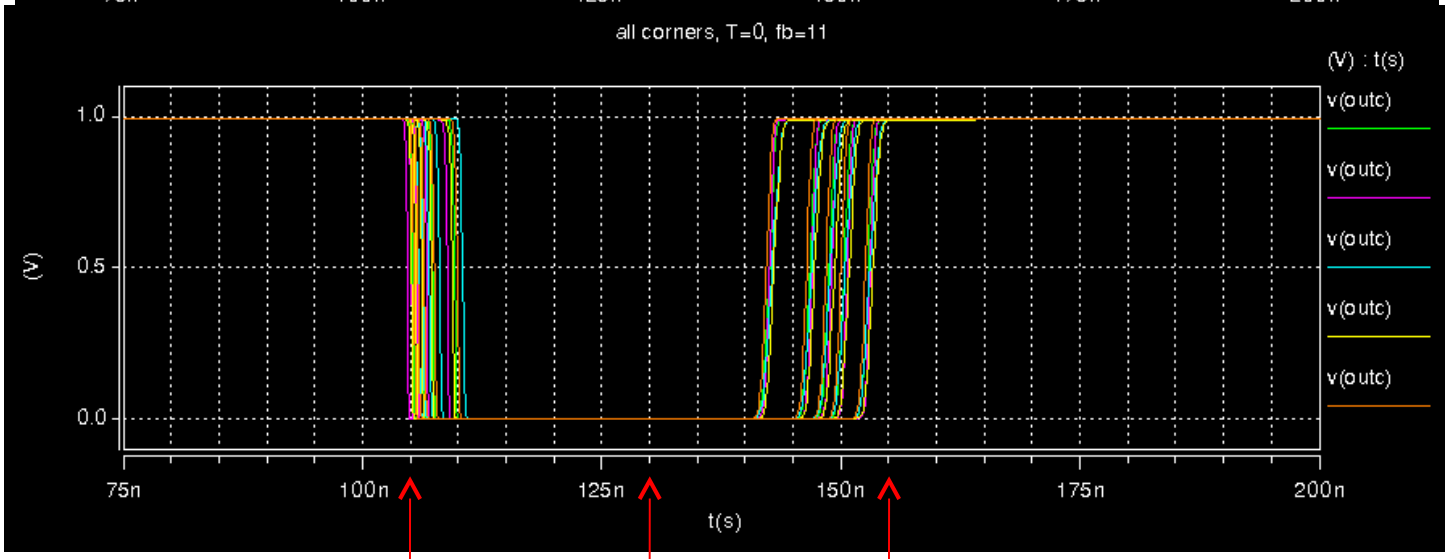
25 nsec sampling points

signals in range 1-4 mips can be constrained to 1 BX

5 mip signals may stray into neighbouring BX

comp. response: T=0, VPAFB = 11, nom params, all corners

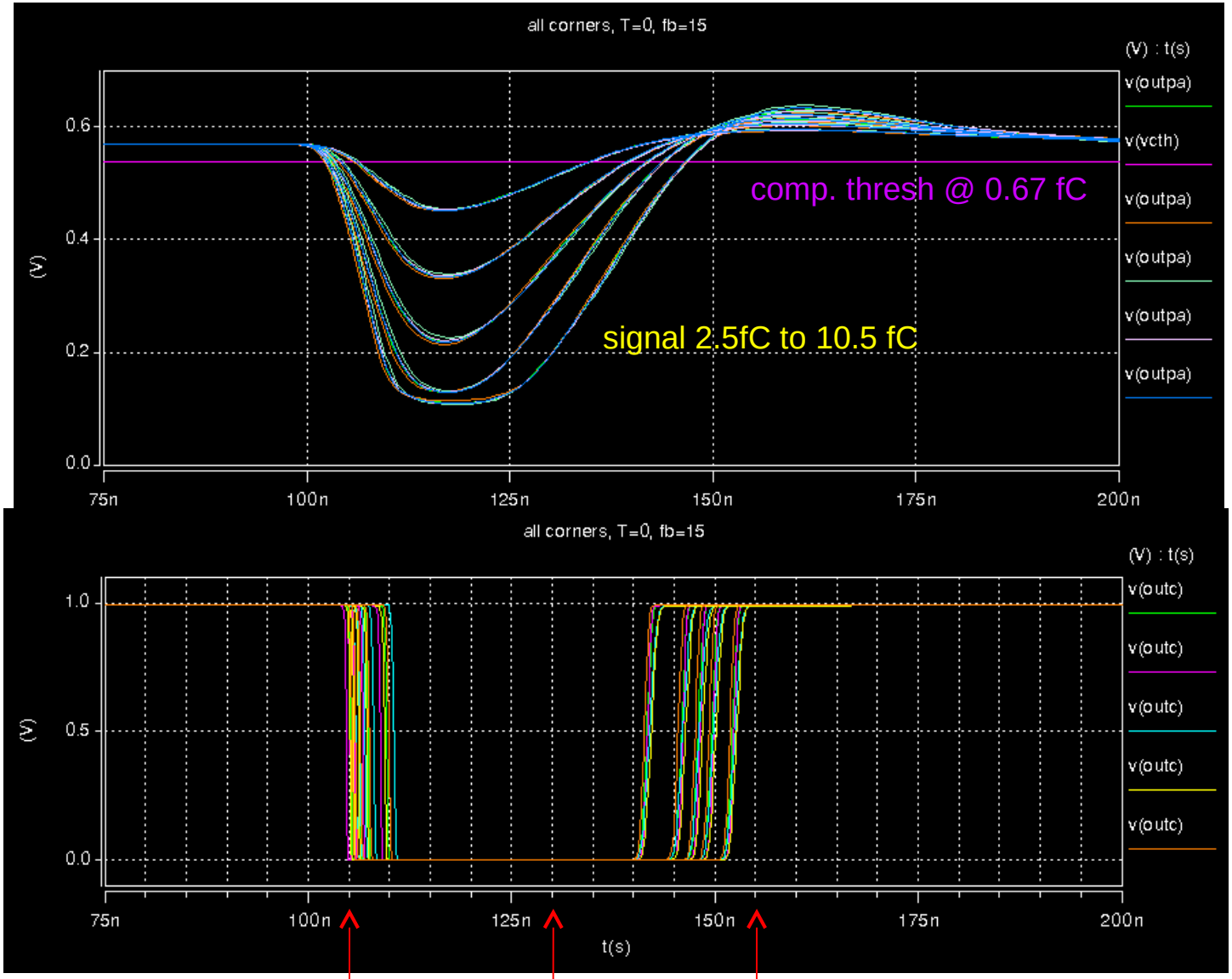




25 nsec sampling points

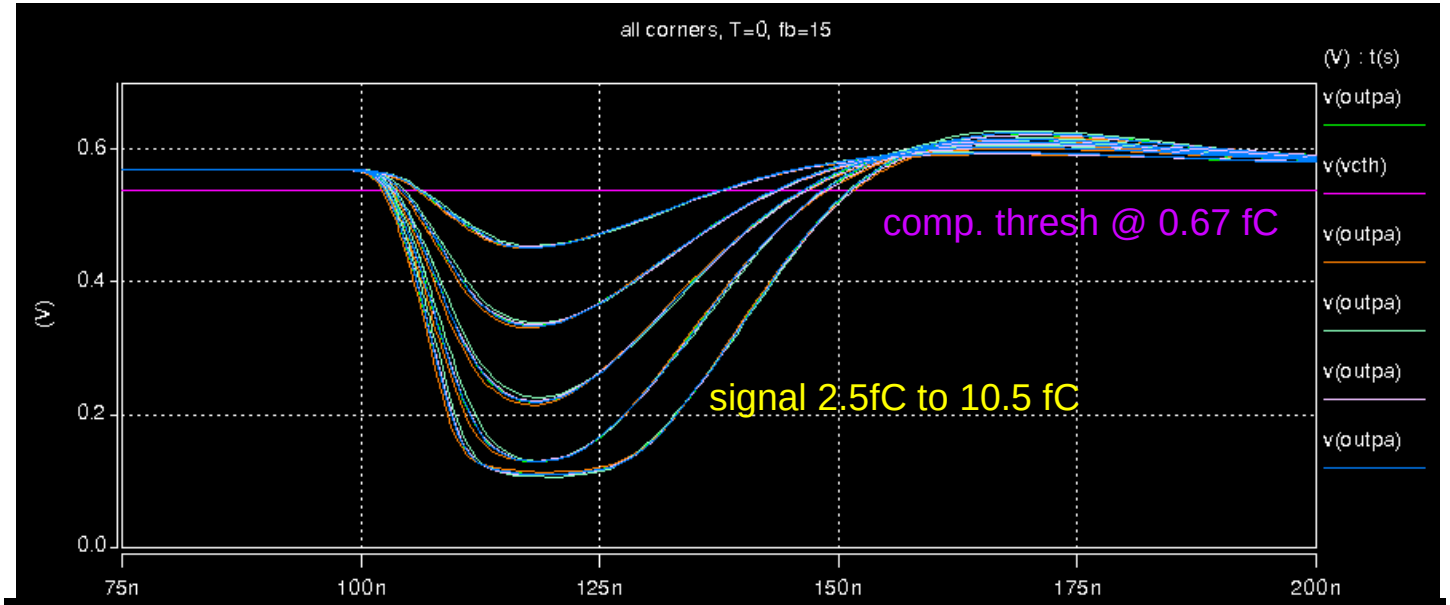
signals in range 1-5 mips can be constrained to 1 BX

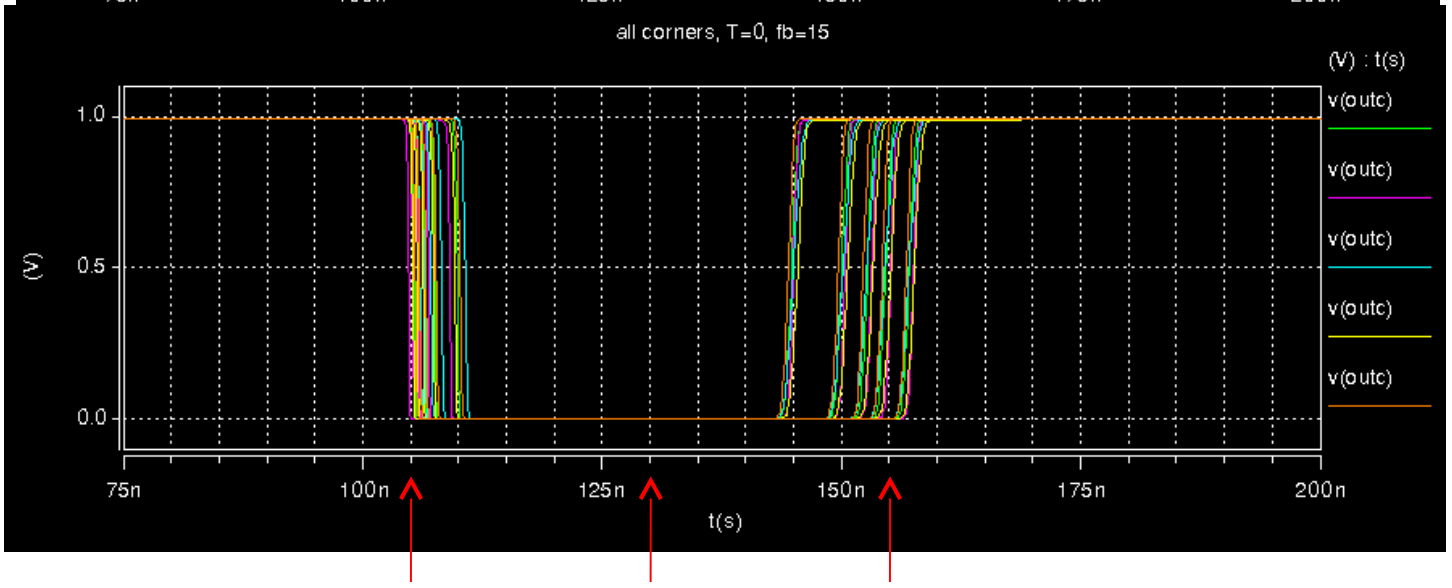
comp. response: T=0, VPAFB = 15, nom params, all corners



signals in range 1-5 mips can be constrained to 1 BX

comp. response: T=0, VPAFB = 15, nom params, all corners





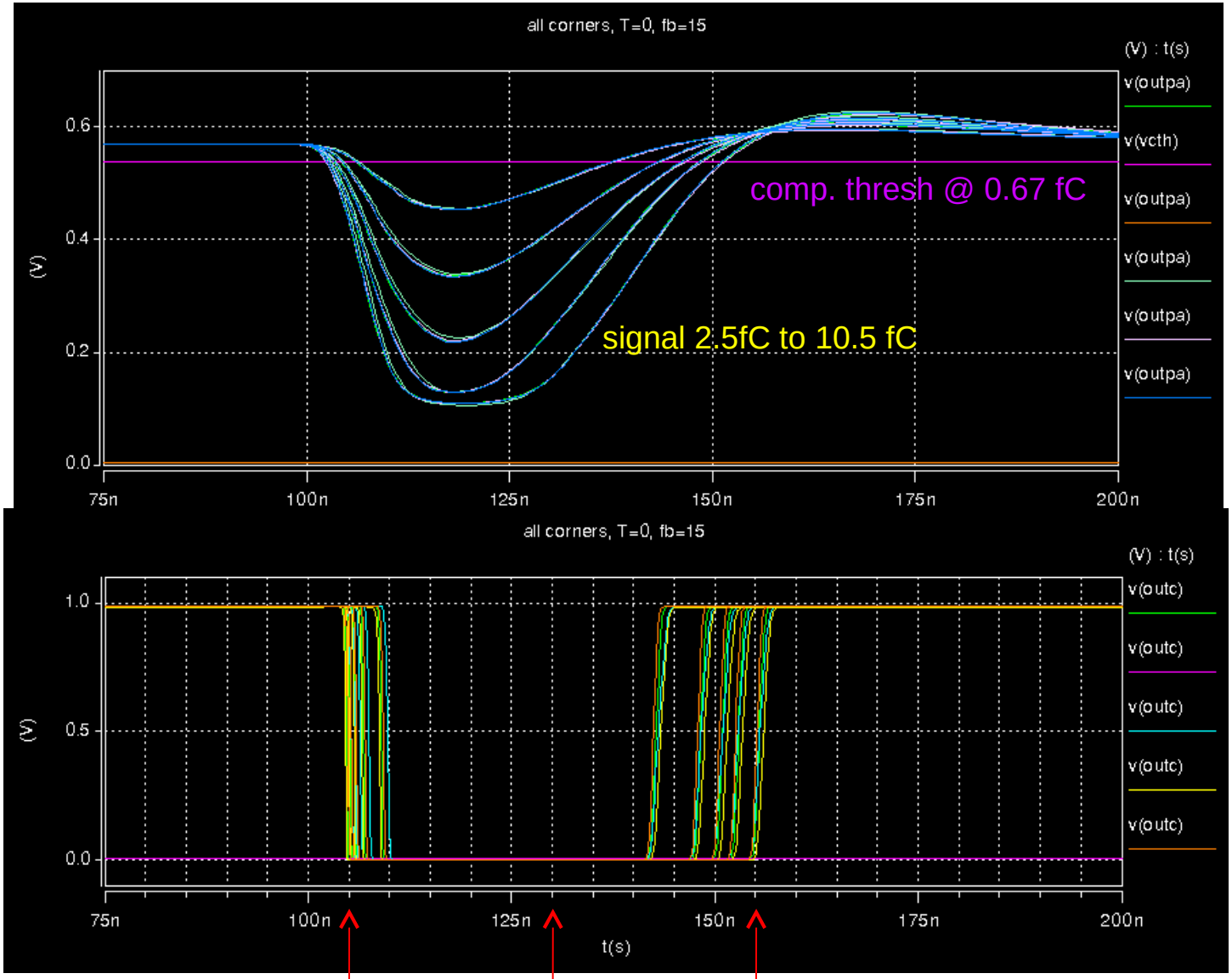
Rpf+15%
Cpf+10%

signals in range 1-3 mips can be constrained to 1 BX

4, 5 mip signals will stray into neighbouring BX

25 nsec sampling points

comp. response: T=0, VPAFB = 15, nom params, all corners



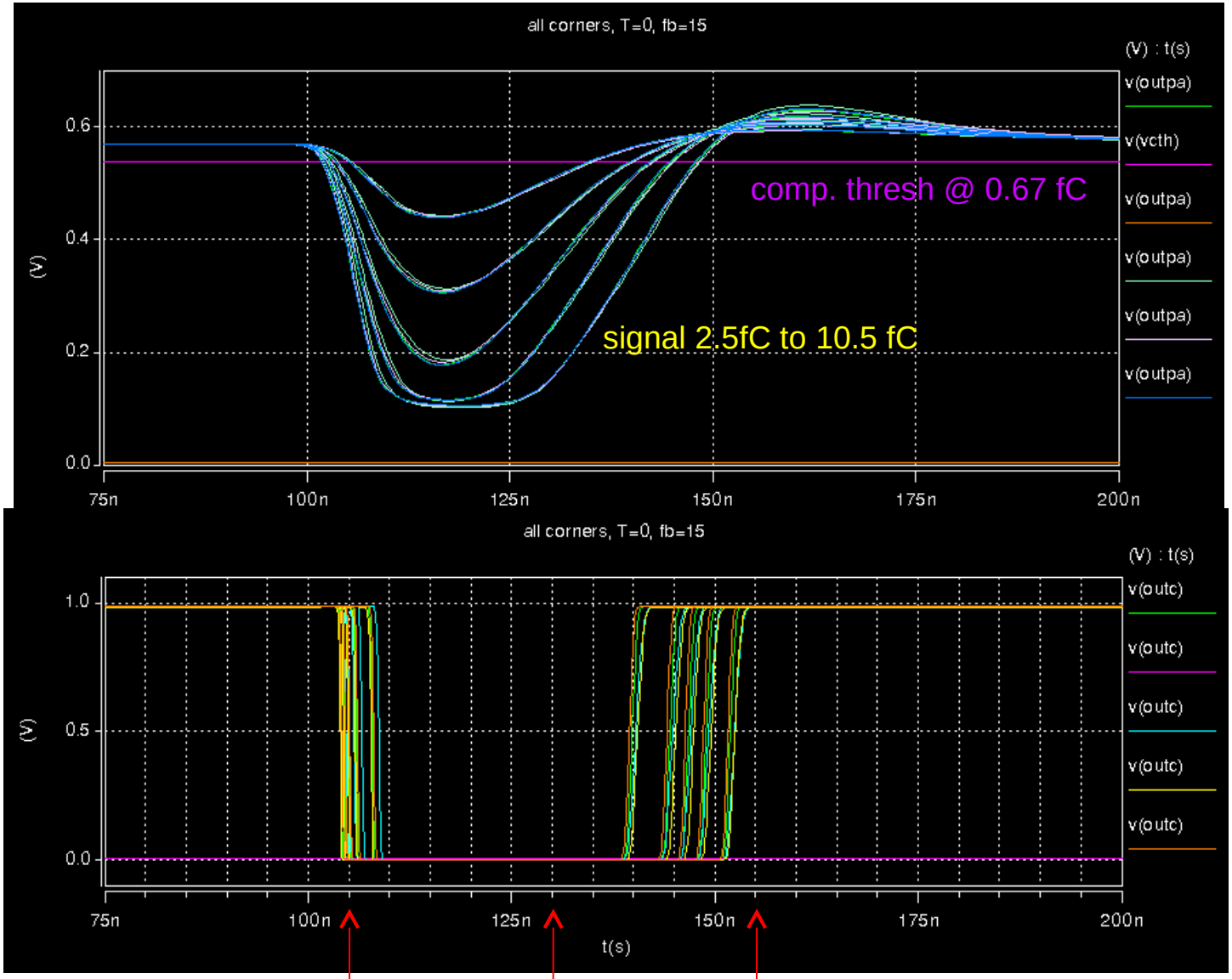
Rpf+15%
Cpf+10%

Icomp 5 -> 8 uA

signals in range 1-4 mips can be constrained to 1 BX

5 mip signals will stray into neighbouring BX

comp. response: T=0, VPAFB = 15, nom params, all corners



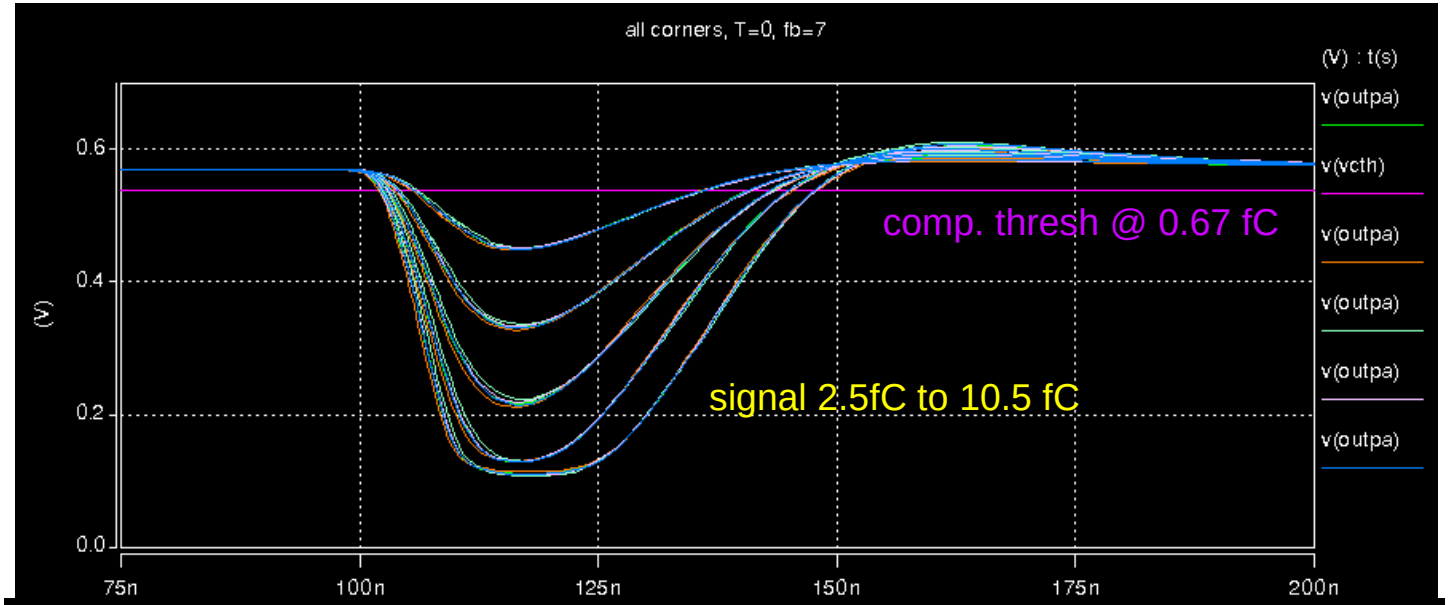
Rpf+15%
Cpf+10%

Icomp: 5 -> 8 uA

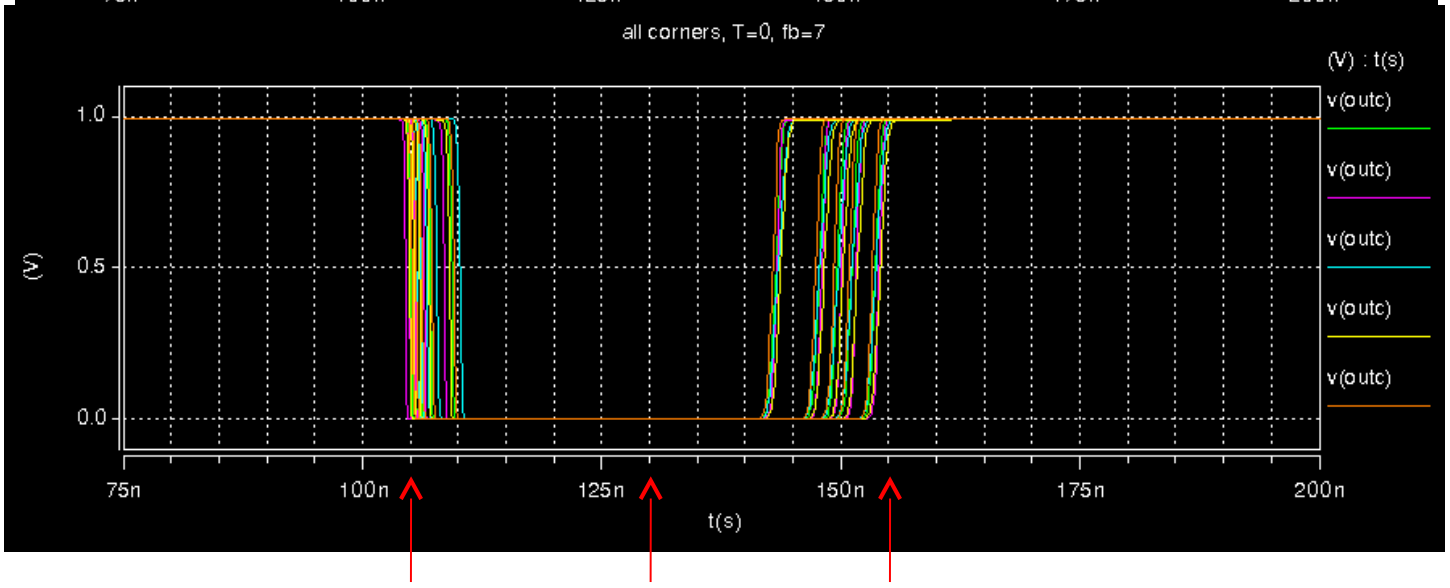
IPA: 20 -> 30 uA

signals in range 1-5 mips can be constrained to 1 BX

comp. response: T=0, VPAFB = 7, nom params, all corners



C=16p
IPRE1 = 80uA



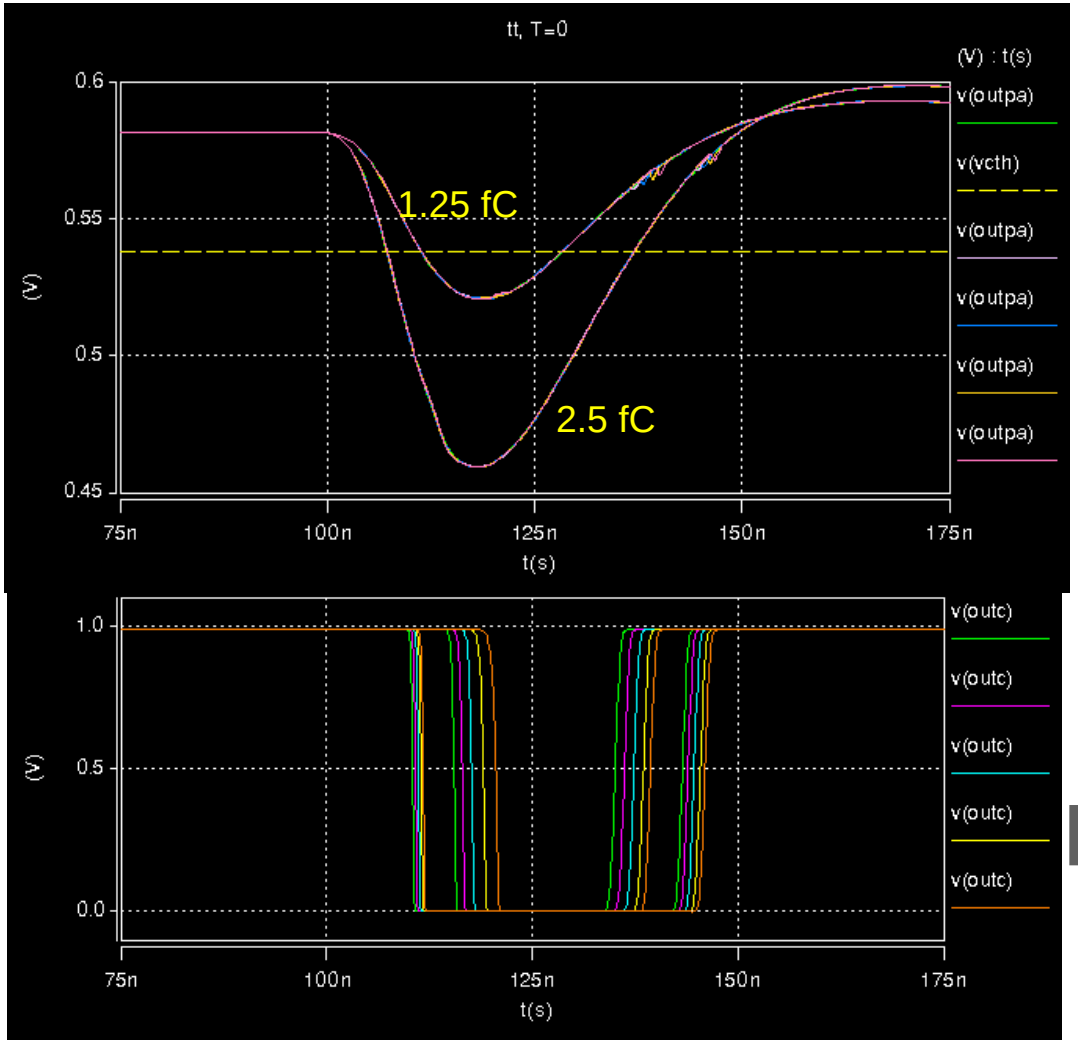
signals in range
1-~5 mips can be
constrained to 1 BX

25 nsec sampling points

hysteresis

have always used CBC on minimum hysteresis setting

but check it's working



hyst value

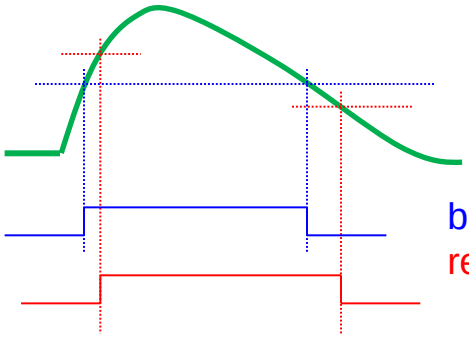
0

4

8

12

15



blue = no hysteresis

red = with hysteresis

conclusions on comparator

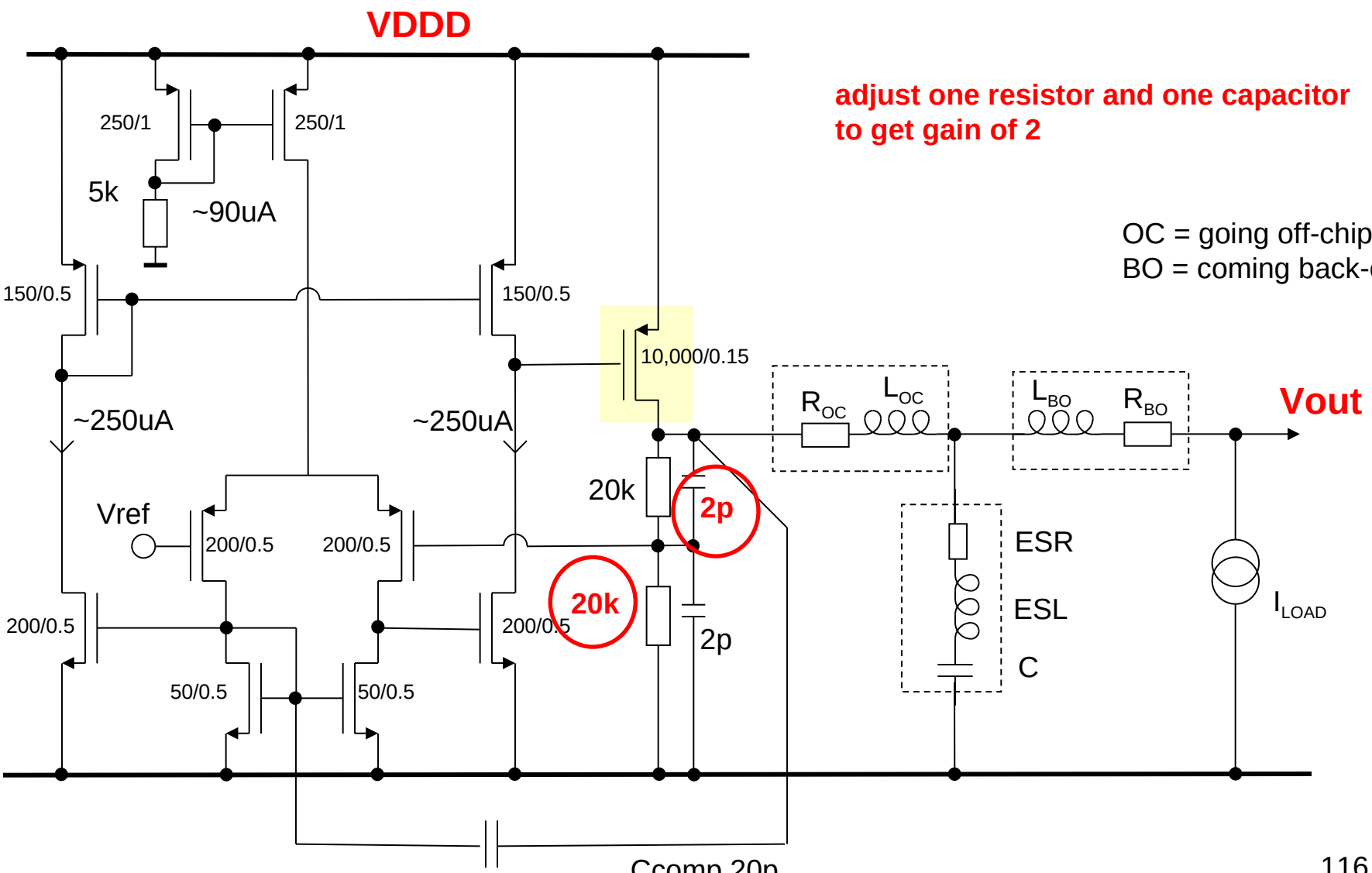
fast enough

- timewalk within spec.
- signal can be constrained to single bunch crossing in most cases
- adjustment available, if necessary

LDO

CBC3 LDO

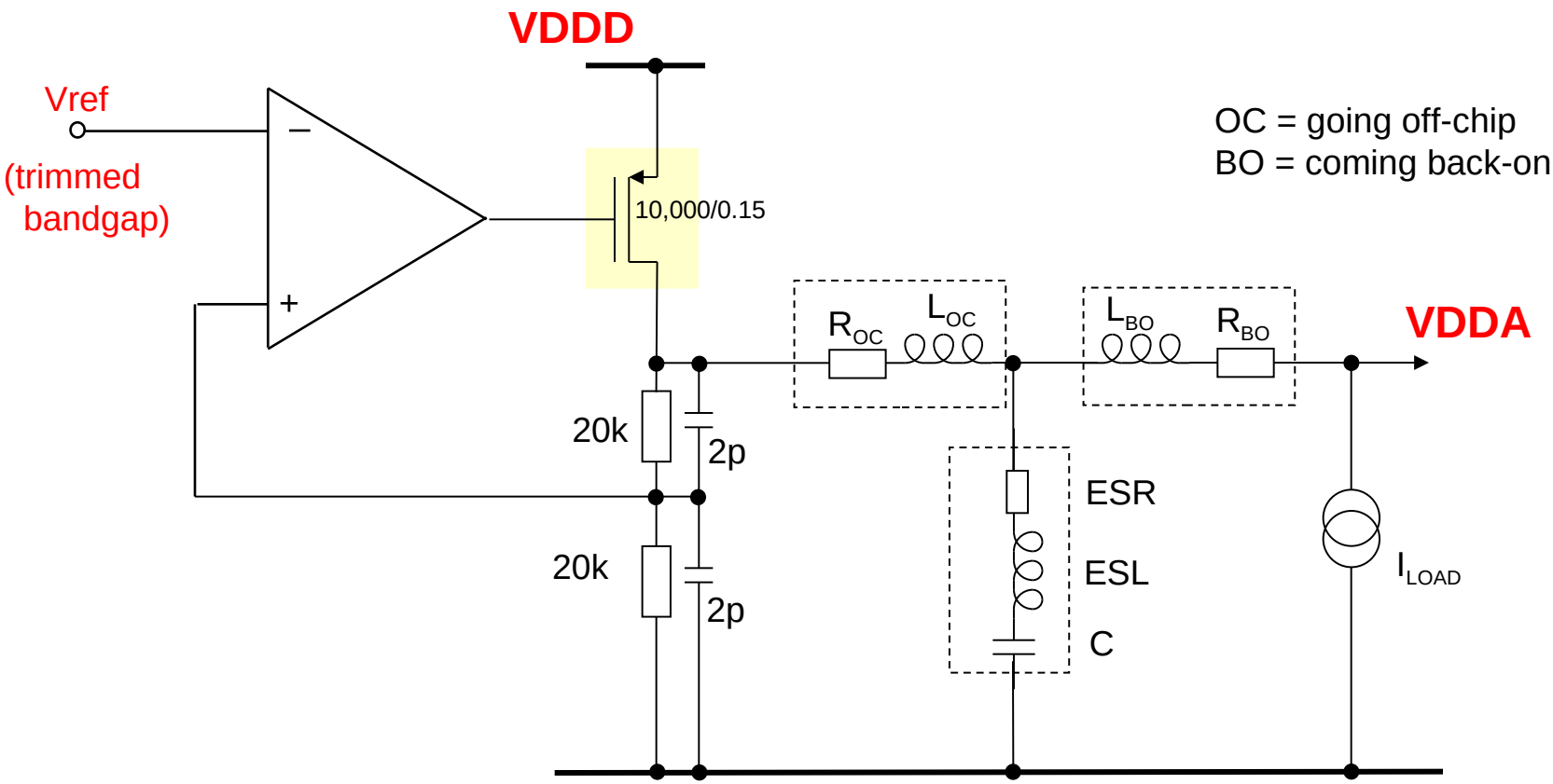
draws ~1200 μA from Vin (bias resistor -> 5k)



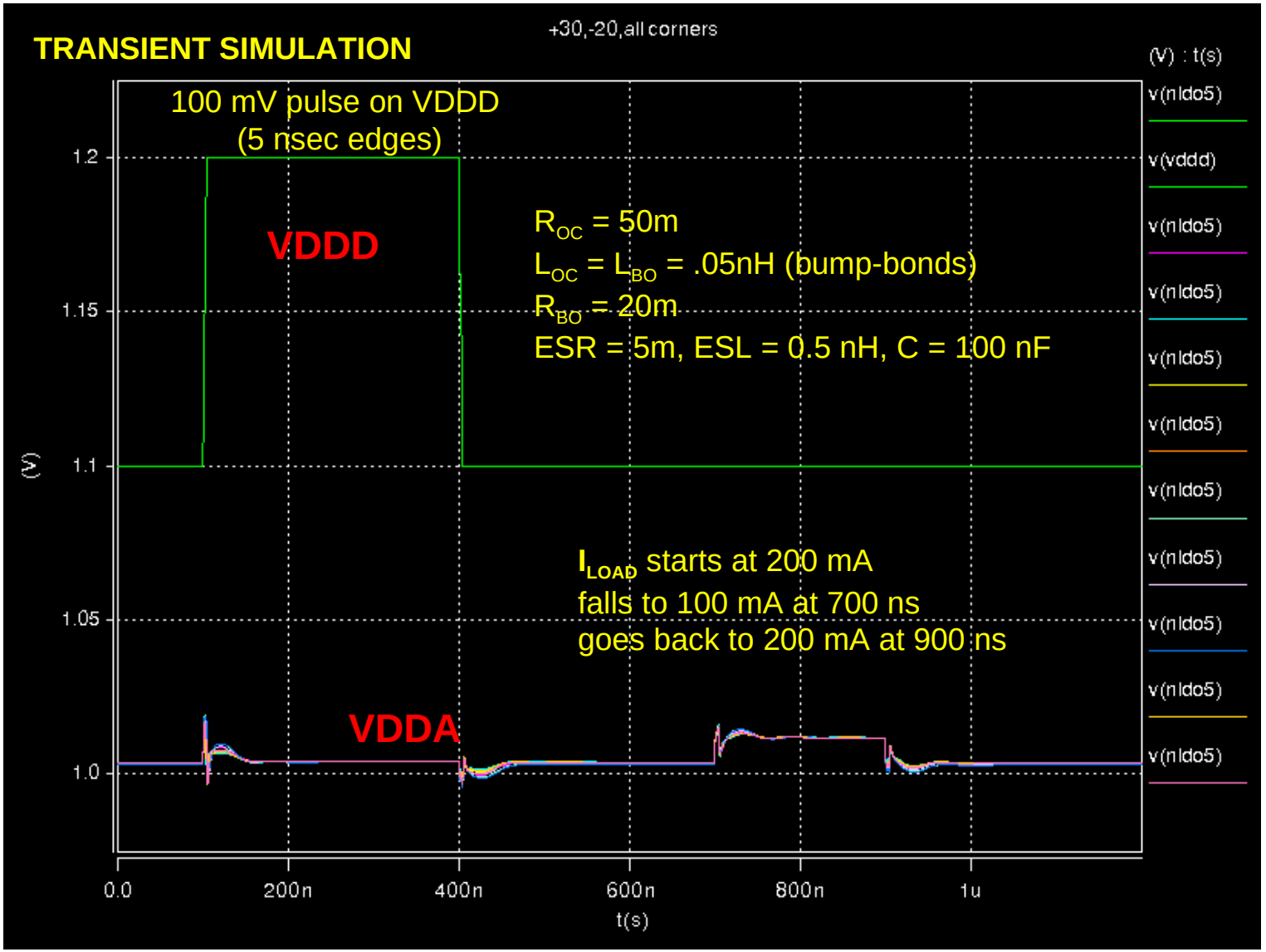
adjust one resistor and one capacitor to get gain of 2

OC = going off-chip
BO = coming back-on

CBC3 LDO (simplified)



simulation approach



better capacitor models

found some commercial models for external capacitor

can now get up to 4.7 uF in 0402 package

(0.22 uF used on CBC2 hybrids)

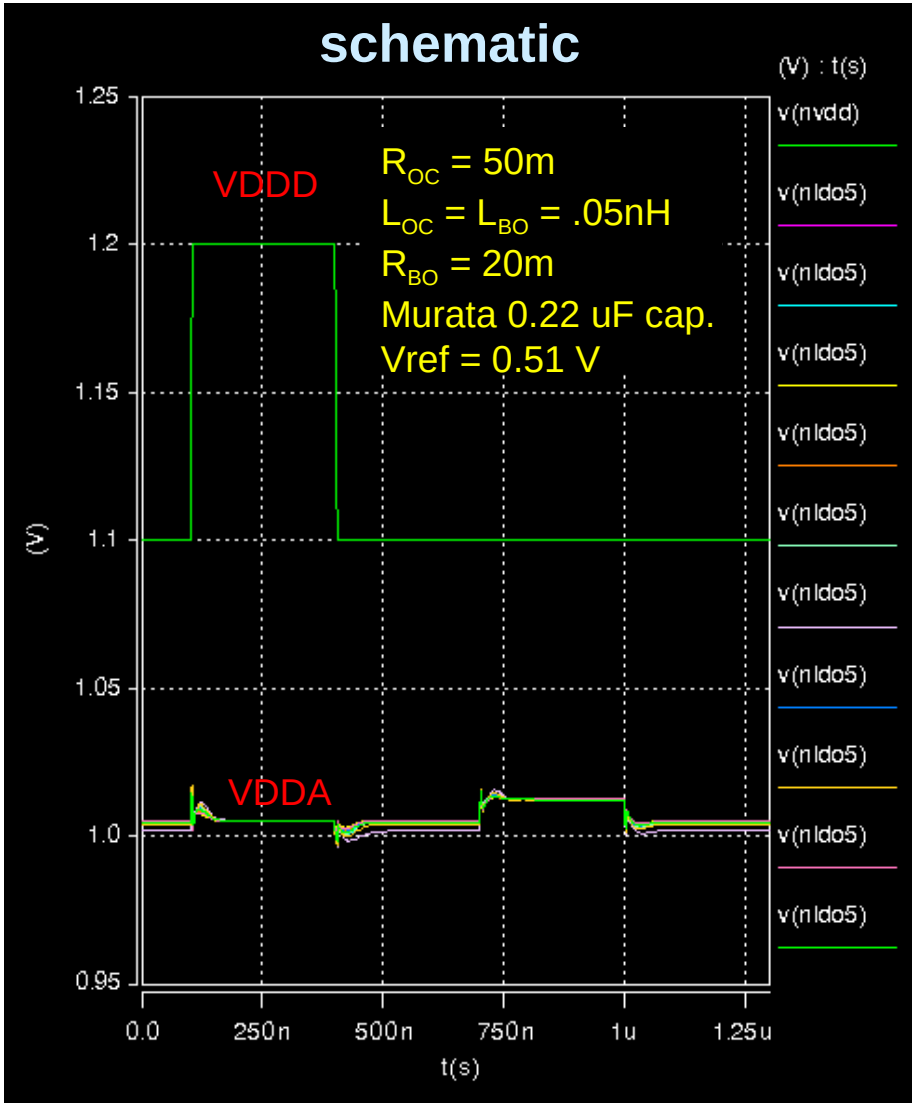
have tried 0.22, 0.33, 0.47, 0.68 and 1 uF models from Murata

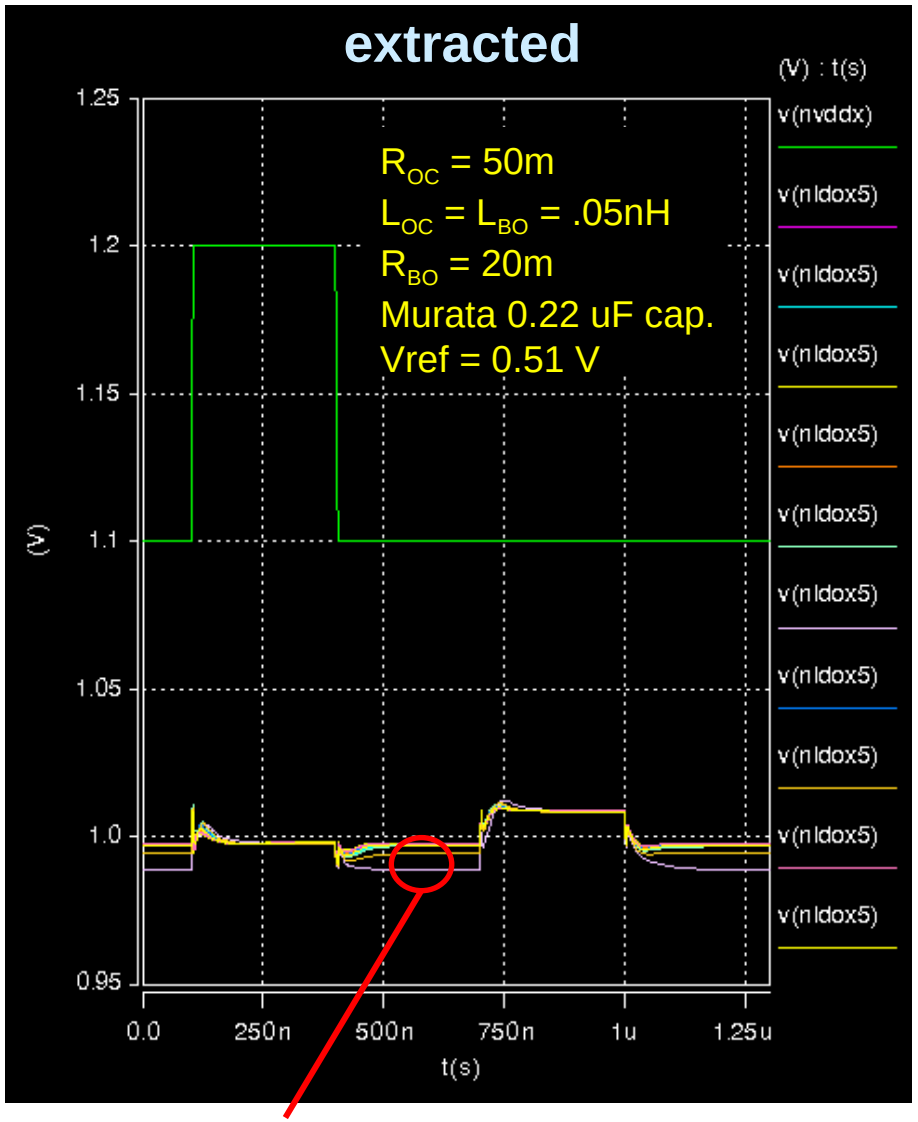
no issues with higher values

- will only show results for 0.22 uF model here ⟶

```
*---------------------------------------------------------------------
* SPICE Model generated by Murata Manufacturing Co., Ltd.
* Copyright(C) Murata Manufacturing Co., Ltd.
* Description :1005/X5R/0.22uF/25V
* Murata P/N :GRM155R61E224KE01
* Property : C = 0.22[uF]
*---------------------------------------------------------------------
* Applicable Conditions:
*   Frequency Range = 100000Hz-6000000000Hz
*   Temperature = 25 degC
*   DC Bias Voltage = 0V
*   Small Signal Operation
*---------------------------------------------------------------------
.SUBCKT cu22 port1 port2
C1 port1 11 1.37e-7
L2 11 12 1.44e-10
R3 12 13 1.65e-2
C4 13 14 1.10e-6
R4 13 14 2.80
C5 14 15 3.01e-6
R5 14 15 8.31e-2
C6 15 16 2.16e-6
R6 15 16 2.22e-2
L7 16 17 2.55e-11
R7 16 17 2.19e-1
L8 17 18 1.34e-10
R8 17 18 6.69e-2
C9 18 19 1.58e-6
L9 18 19 7.07e-12
R9 18 19 6.37e-3
C10 19 20 5.41e-7
L10 19 20 1.11e-11
R10 19 20 1.09e-2
C11 20 port2 2.55e-12
L11 20 port2 8.73e-11
R11 20 port2 19.5
R100 port1 11 2.27e+8
.ENDS cu22
```

schematic vs extracted: +40, -40, all corners

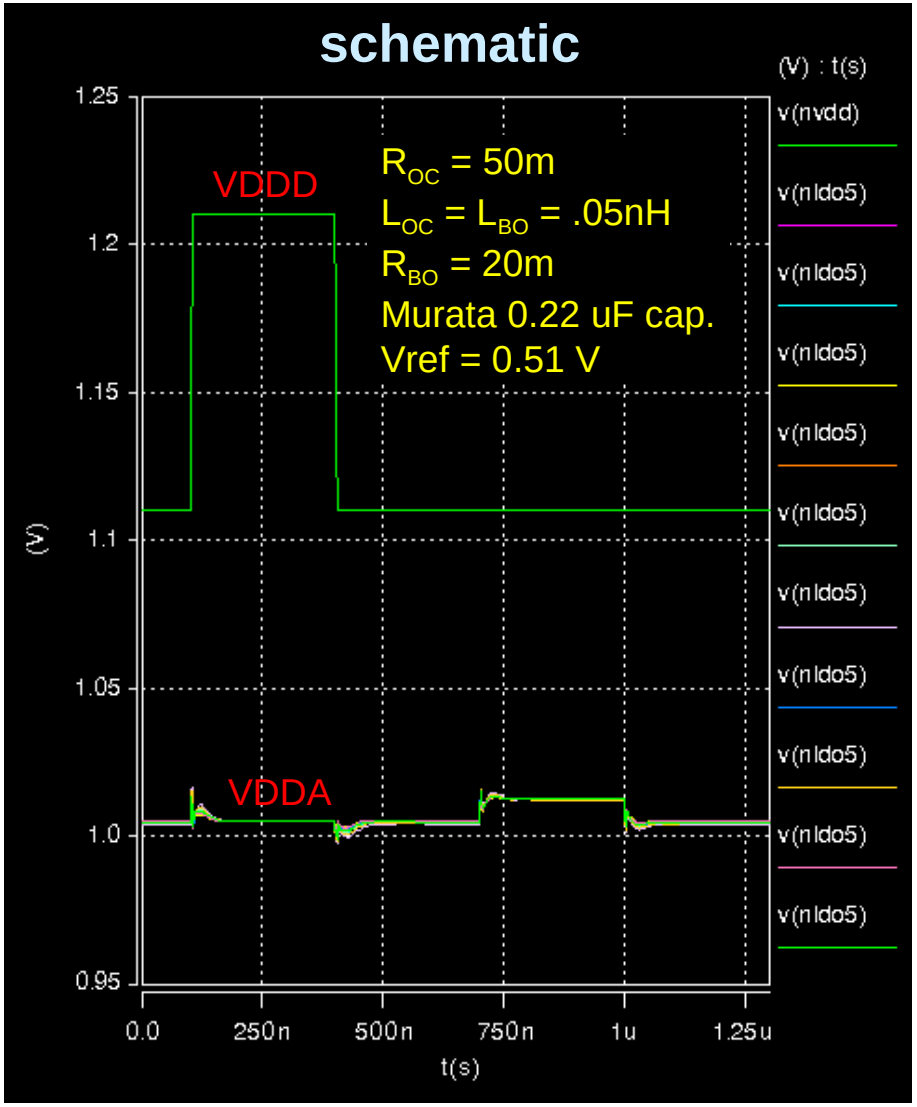


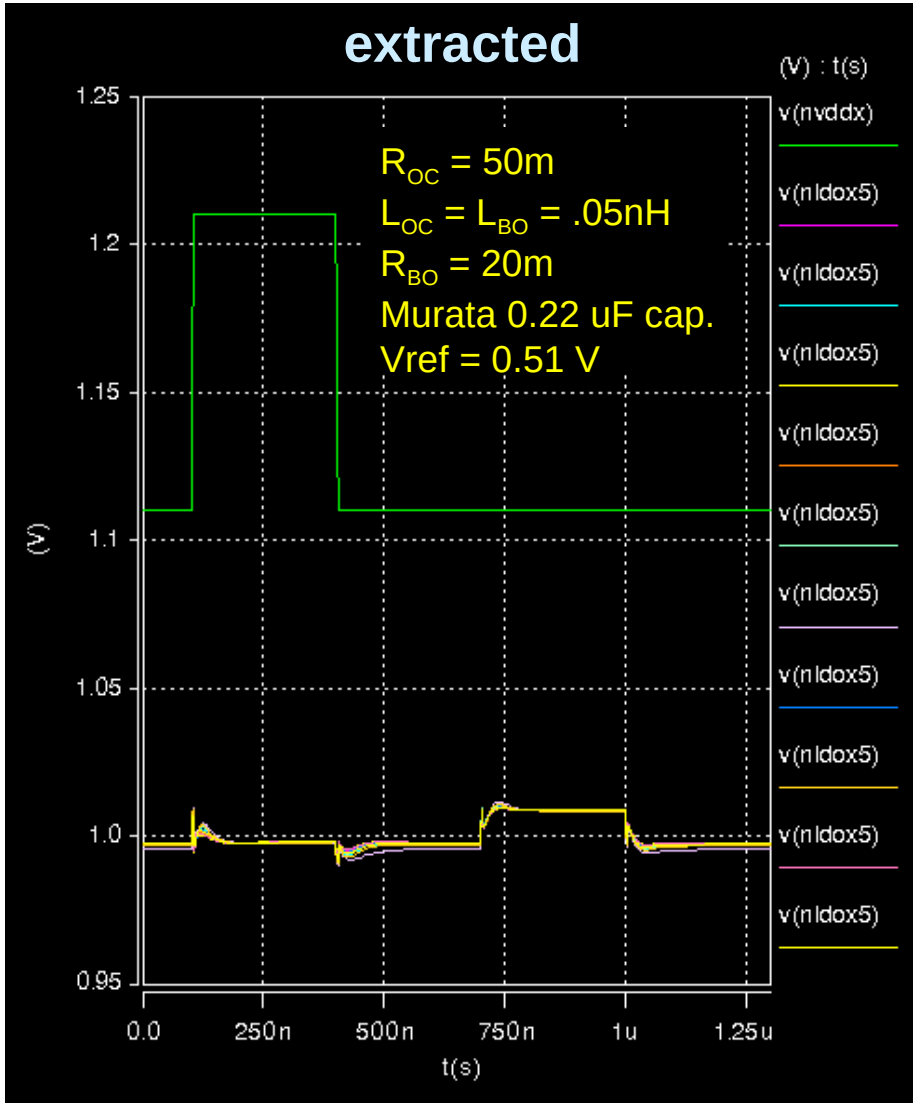


extracted circuit: output voltage a bit lower
struggling at higher load current for slow P corners

slow P corners
(cold and hot)

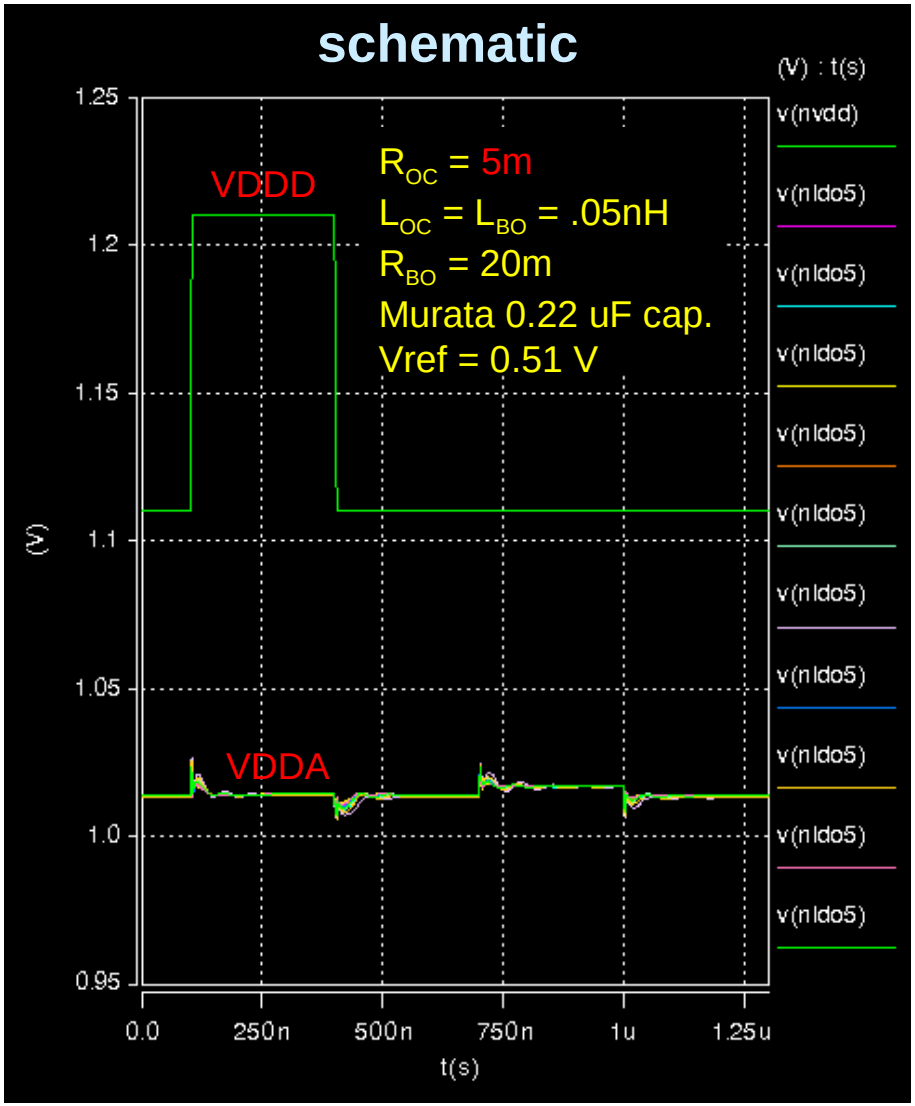
schematic vs extracted: +40, -40, all corners

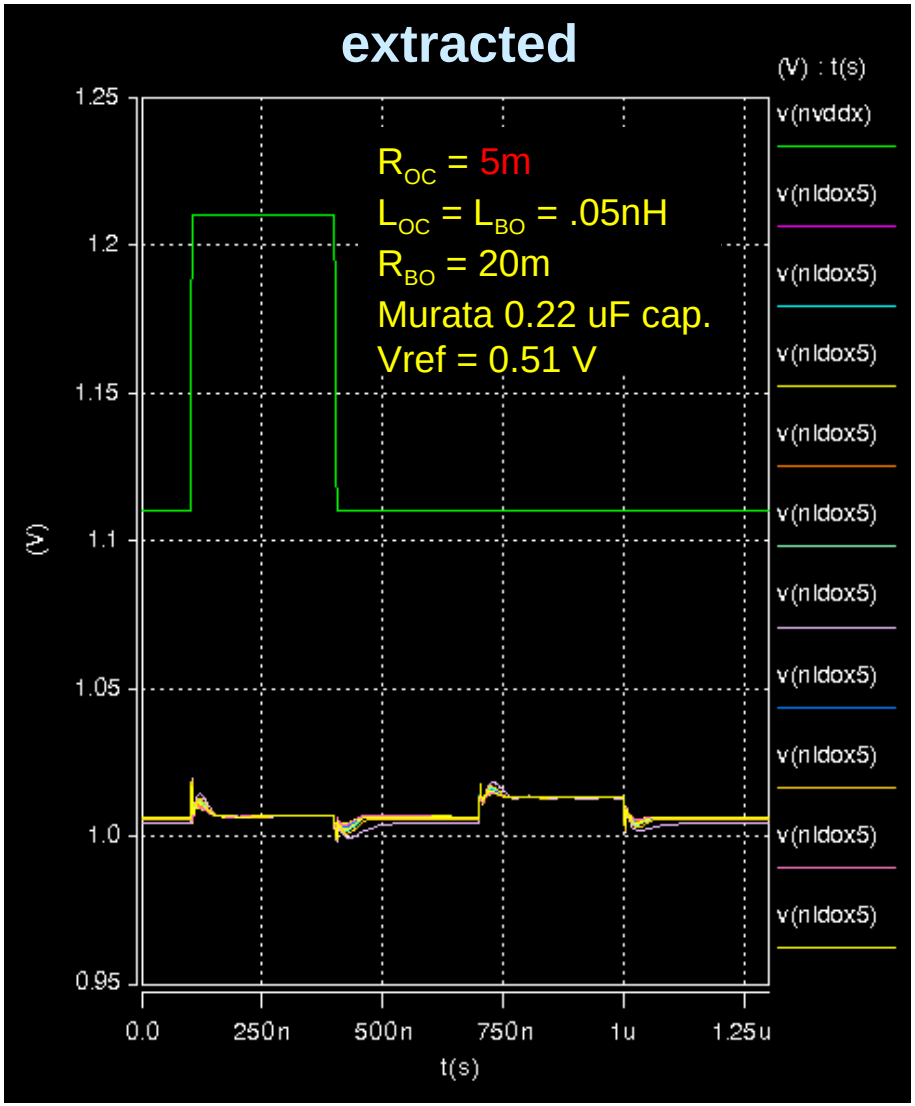




increasing VDDD by 10 mV helps

schematic vs extracted: +40, -40, all corners





increasing VDDD by 10 mV and R_{OC} = 5m still seems ok for extracted circuit

startup check

simulation shows all corners, +/- 40 deg

between .2 and 1.2 secs

VDDD ramps up to 1.11 V
Vref ramps up to 0.51 V

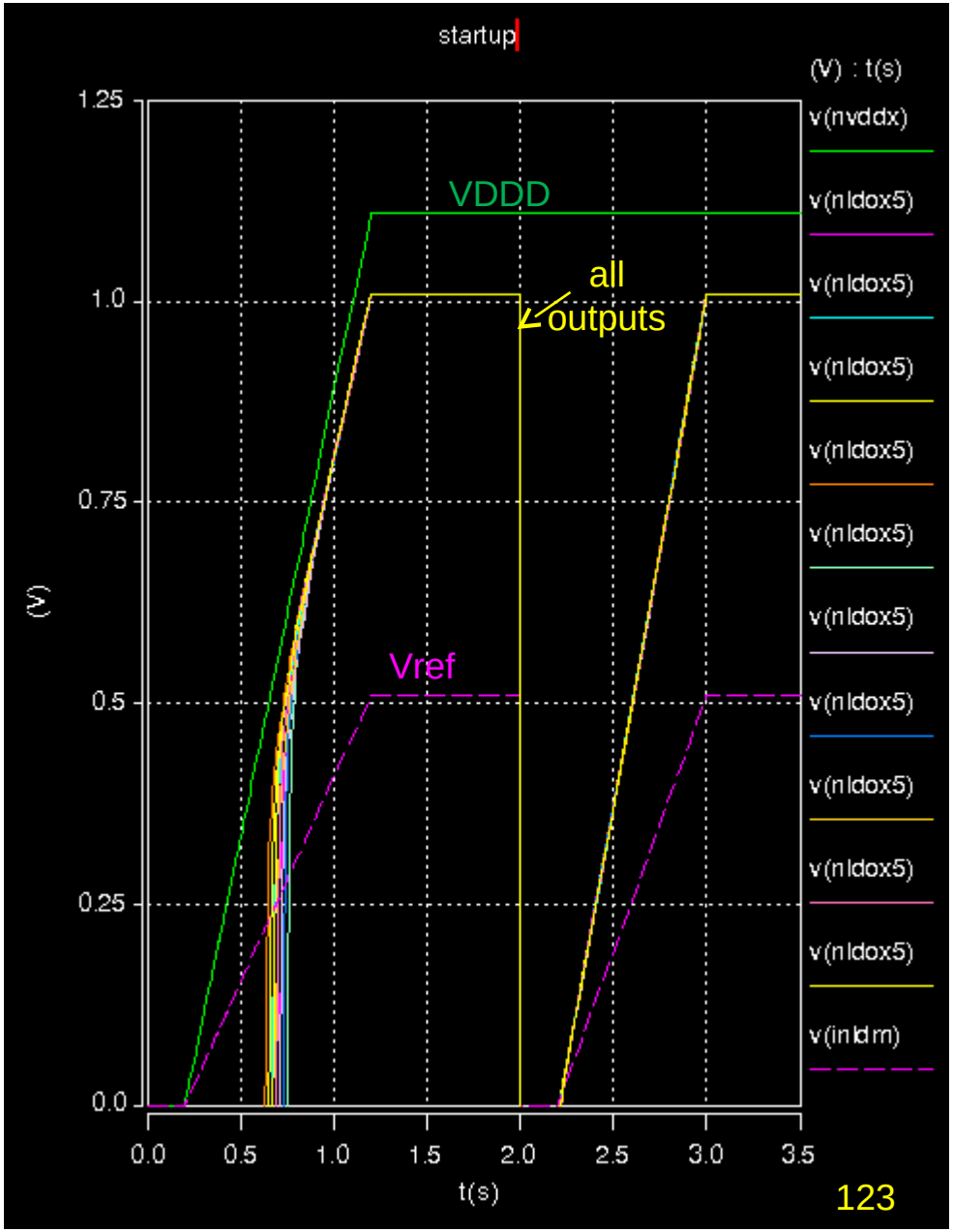
at 2 secs

Vref goes to zero

between 2.2 and 3 secs

Vref ramps back up to 0.51 V

no startup issues (no reason to expect)

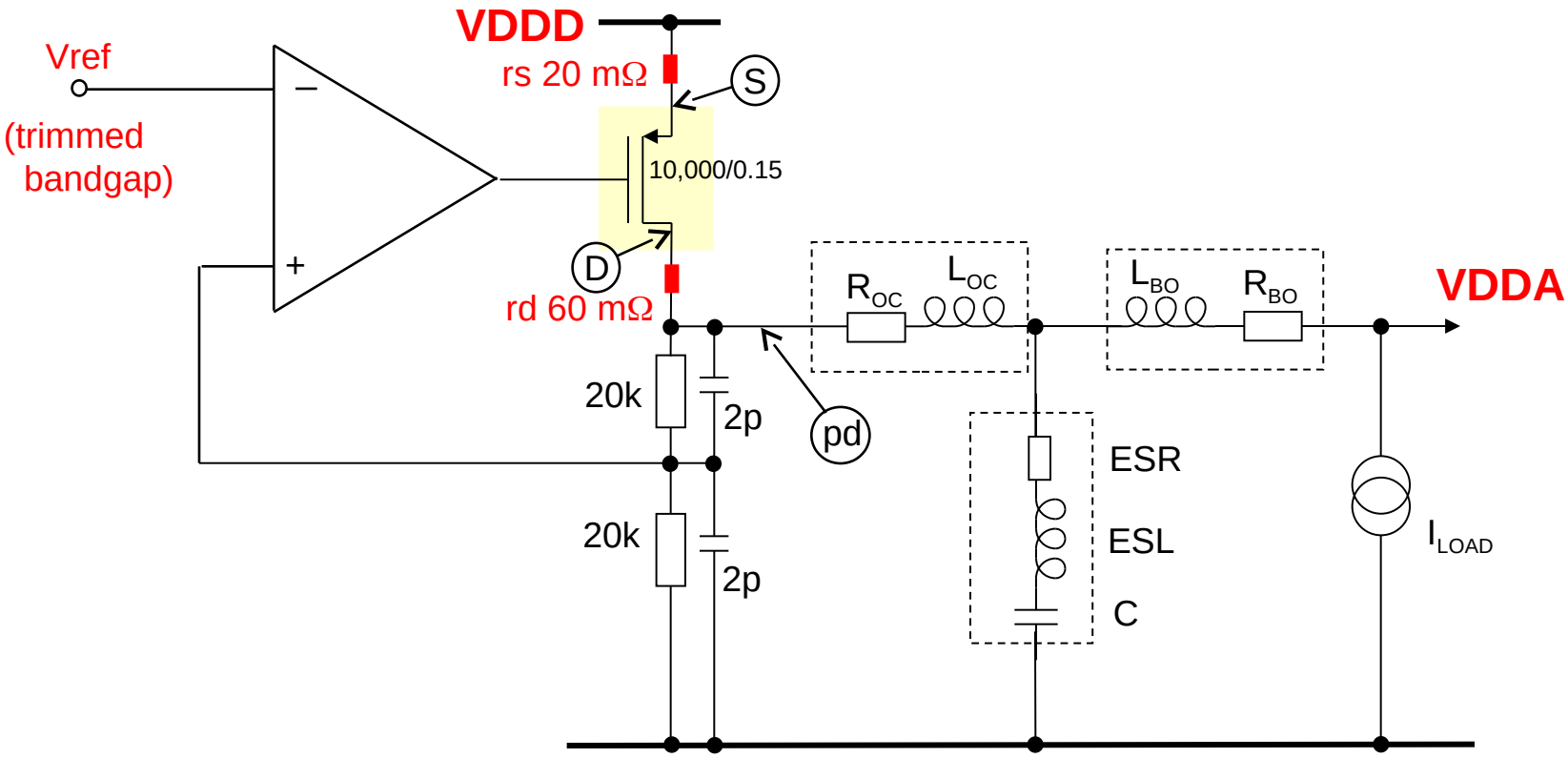


LDO conclusions

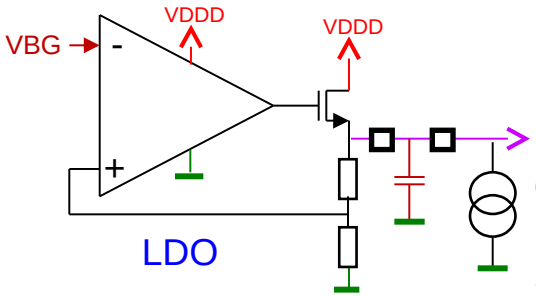
at nominal ~100 mA VDDD down to ~1.1 V can be tolerated

at 200 mA VDDD down to 1.11 V is ~ok
(no harm in reducing R_{OC})

most likely VDDD spec for DC-DC converter on module will be 1.25 +/- 0.05
(requirement for MPA asic)

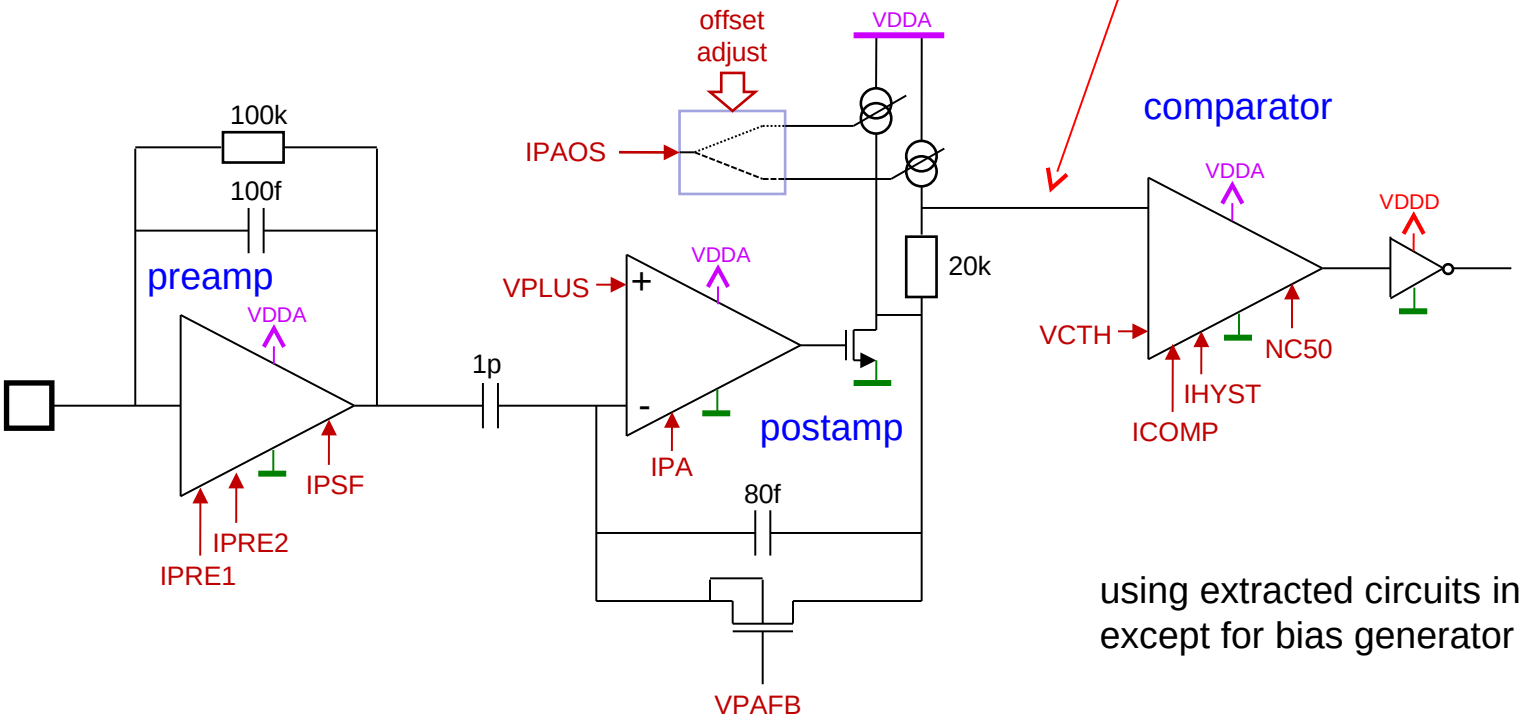


power supply rejection

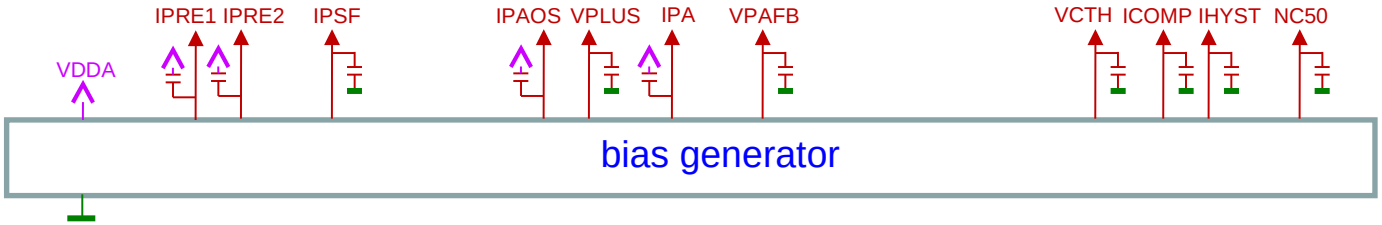


extra 75 mA DC
load to represent
253 channels

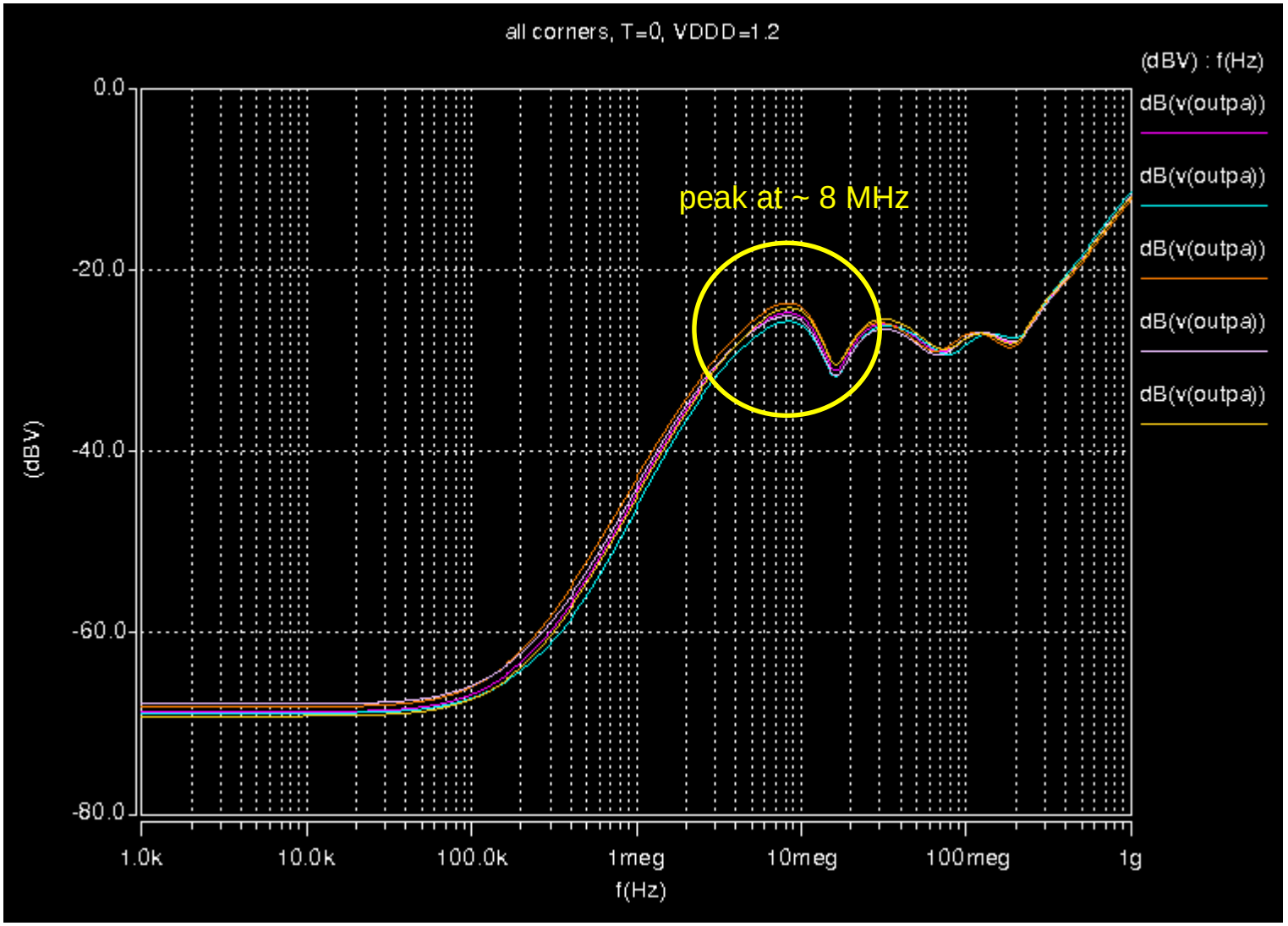
impose a signal on VDDD
look at the result at the postamp output



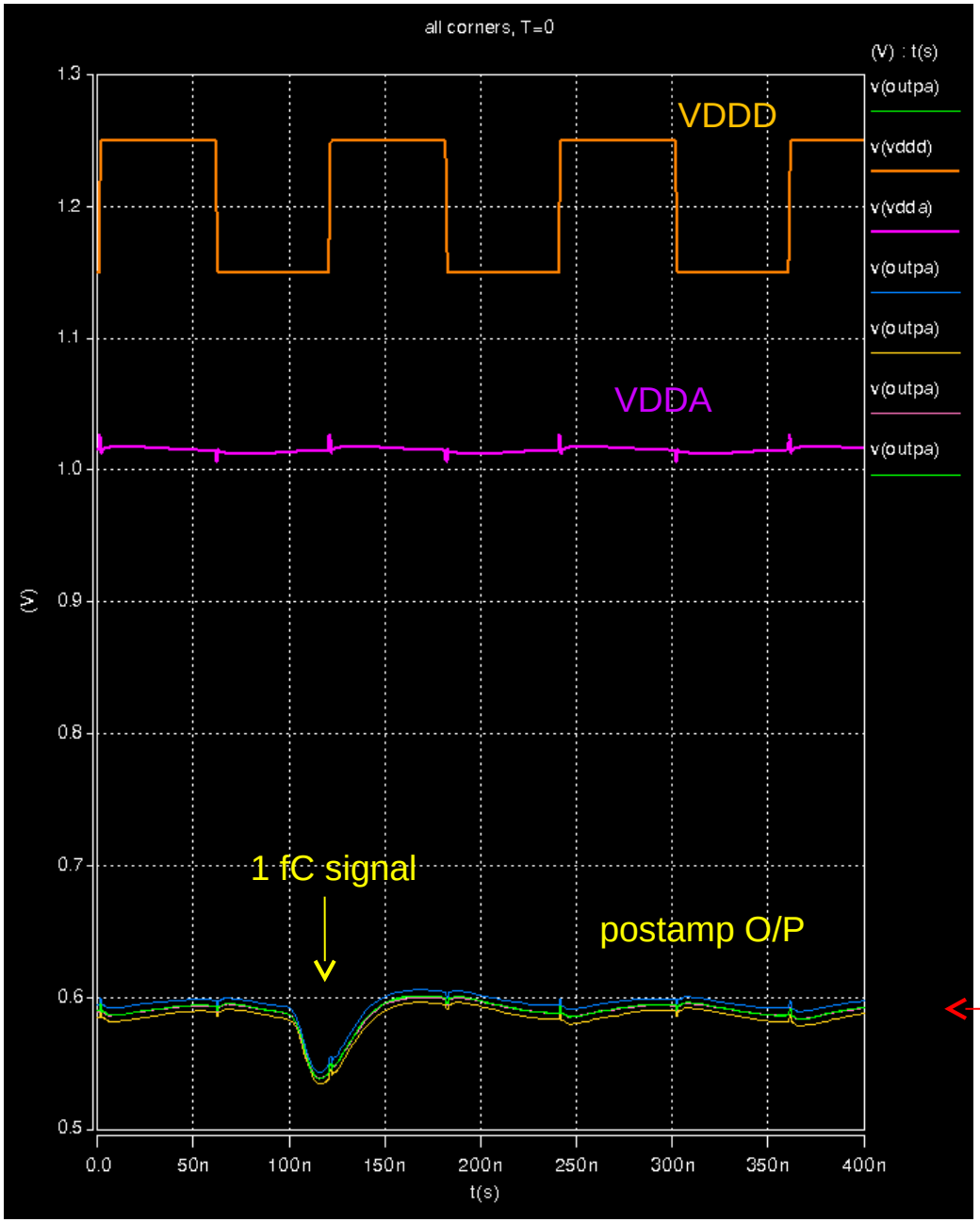
using extracted circuits in all cases
except for bias generator



power supply rejection



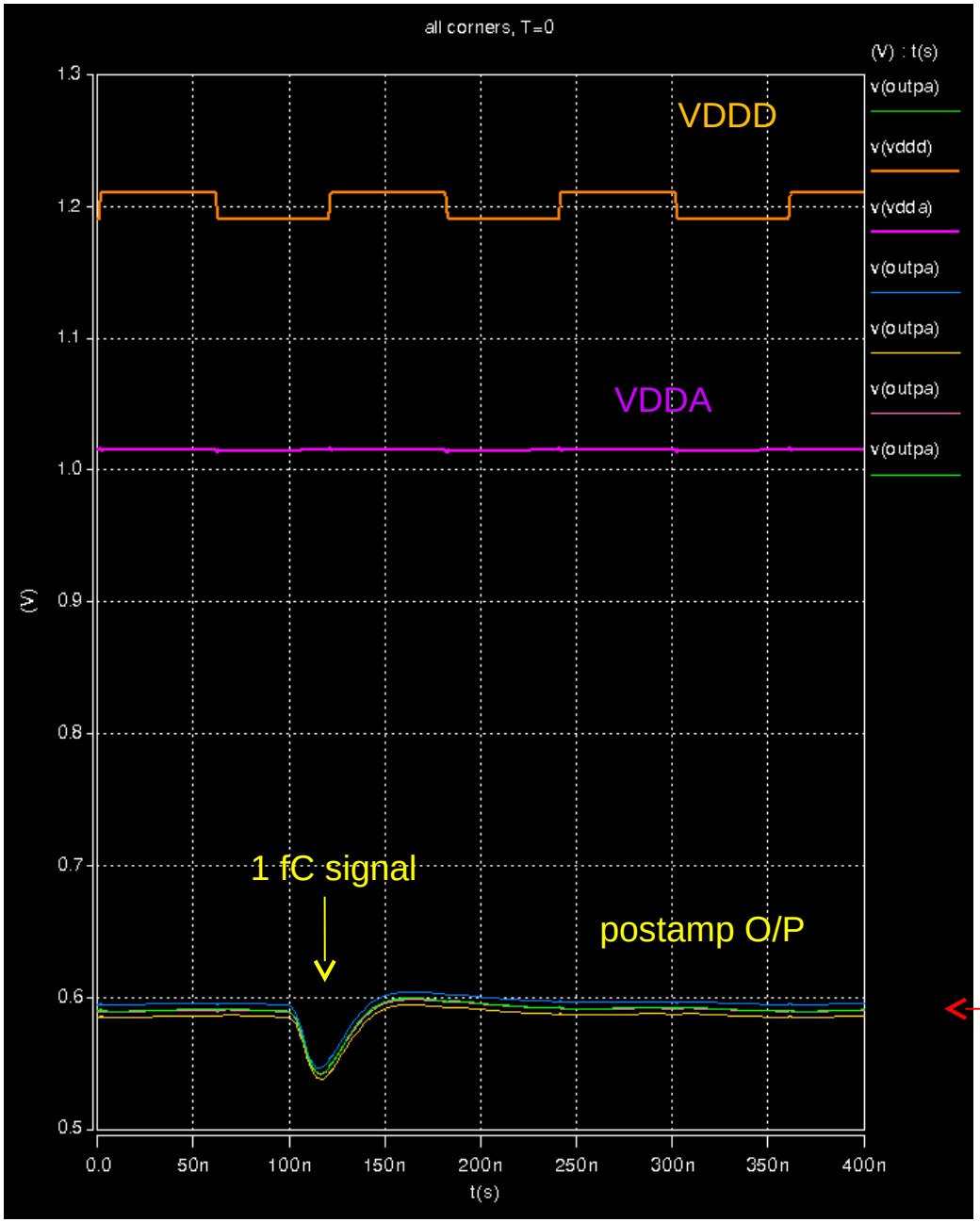
power supply rejection



VDDD = 8 MHz square wave, 100 mV pk-pk centred on 1.2 V - unrealistic

interference visible here would add to intrinsic noise but probably not dominate

power supply rejection

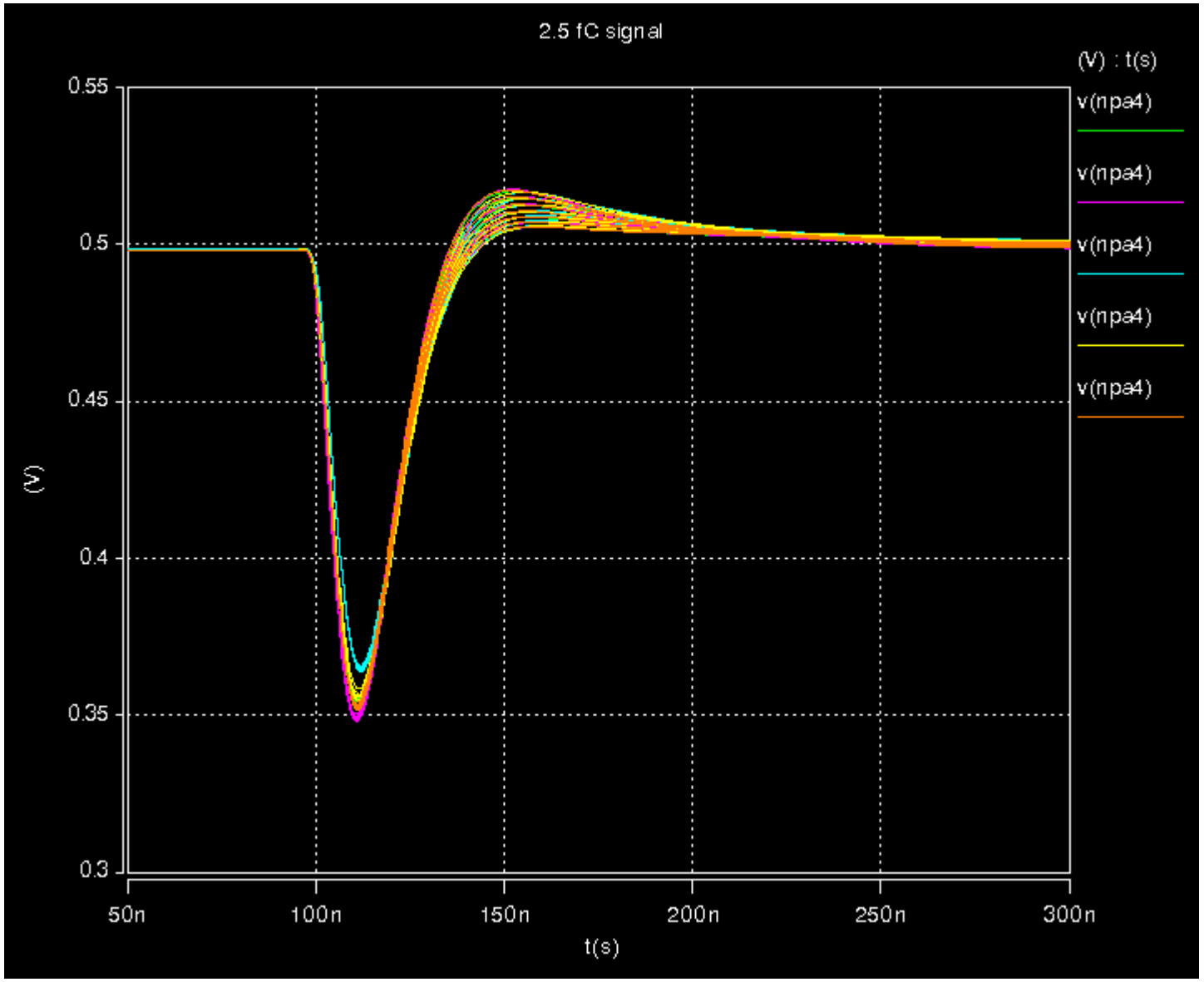


VDDD = 8 MHz square wave, 20 mV pk-pk centred on 1.2 V - probably still unrealistic

interference barely visible here but in reality would be lost in intrinsic noise

OTHER SIMULATIONS

effect of VPLUS/VPLUS2 mismatch - 1 mip signal



VPLUS: 0.5 V
VPLUS2: 0.47 to 0.53, 10mV steps

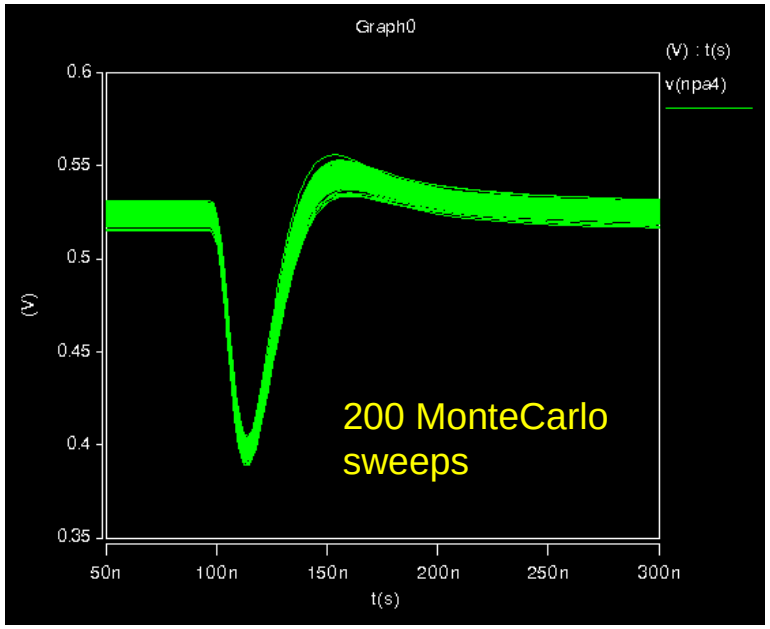
2.5 fC signal

T=0

all corners

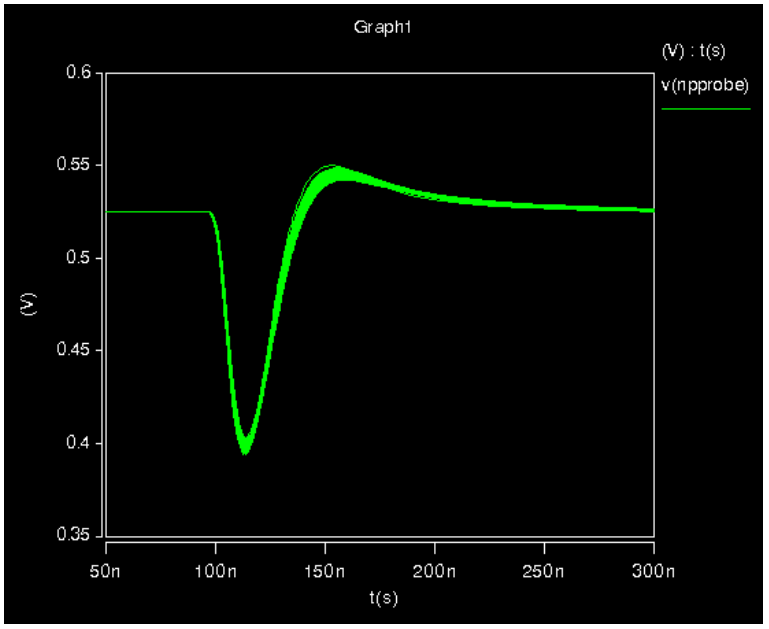
VPAFB: 0100

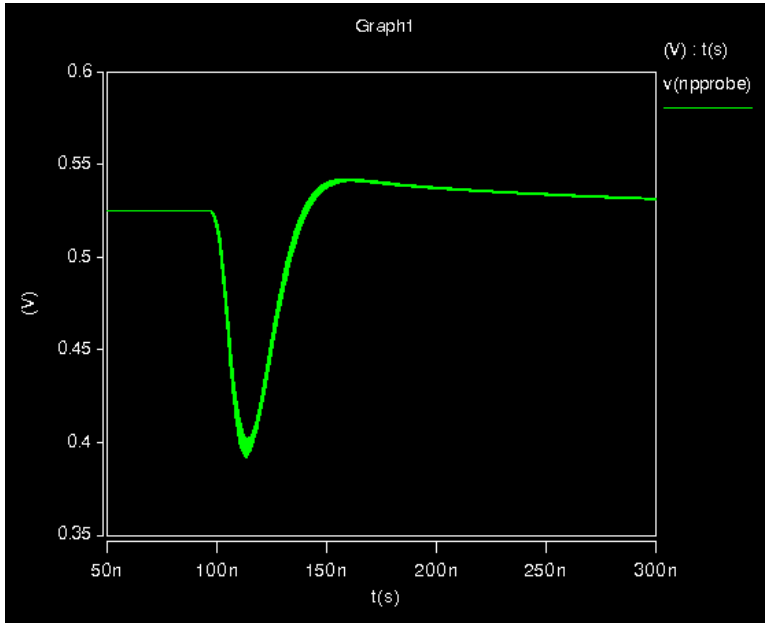
postamp feedback bias mismatch



remove DC

shape variation becomes visible





run same simulation but replace feedback FET with a fixed resistor

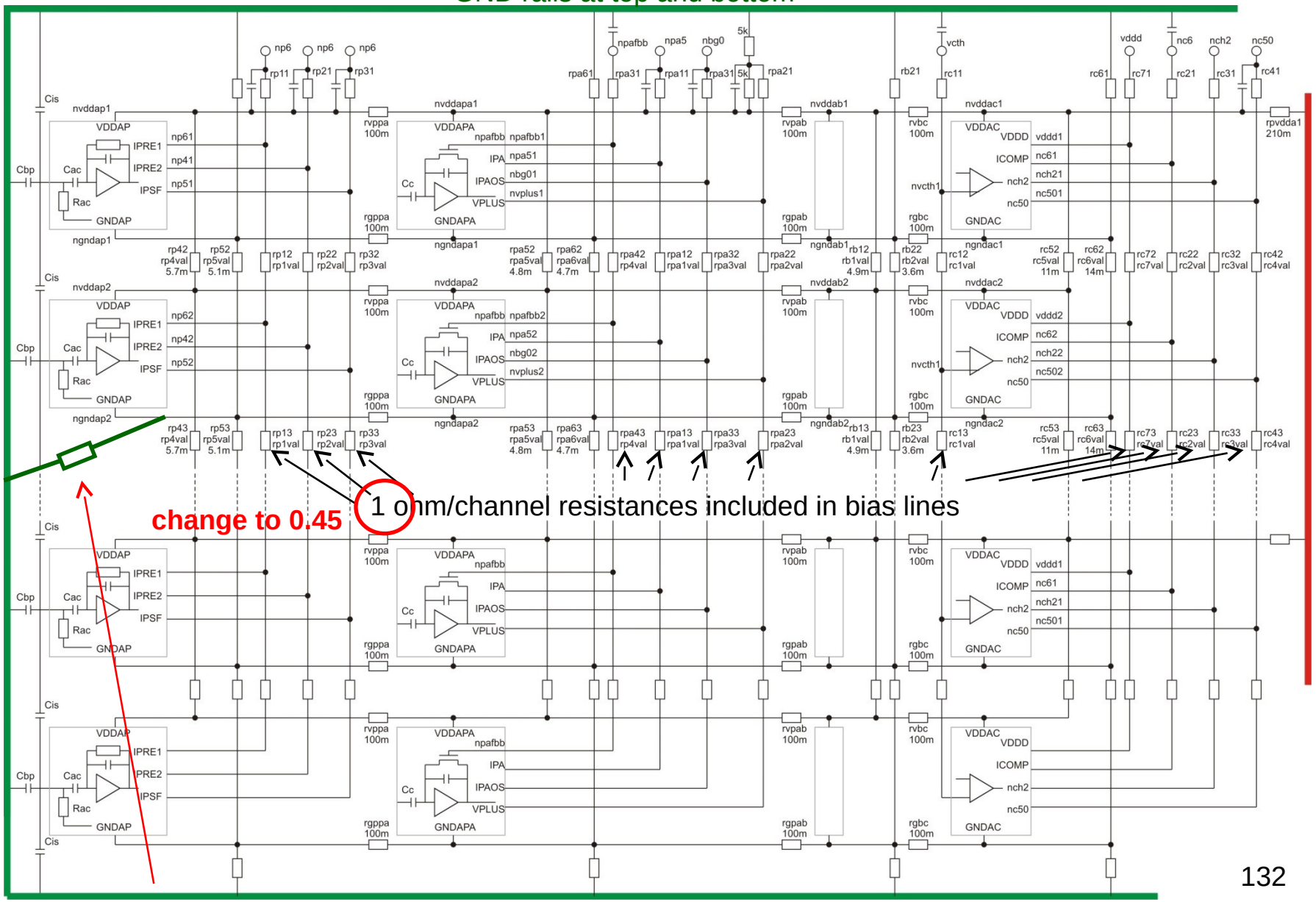
shape variation becomes minimal

conclusion: mismatch effects present but effect is small

multi-channel simulations - effect of power and bias resistance

VDDA: every 5th channel

GND rails at top and bottom



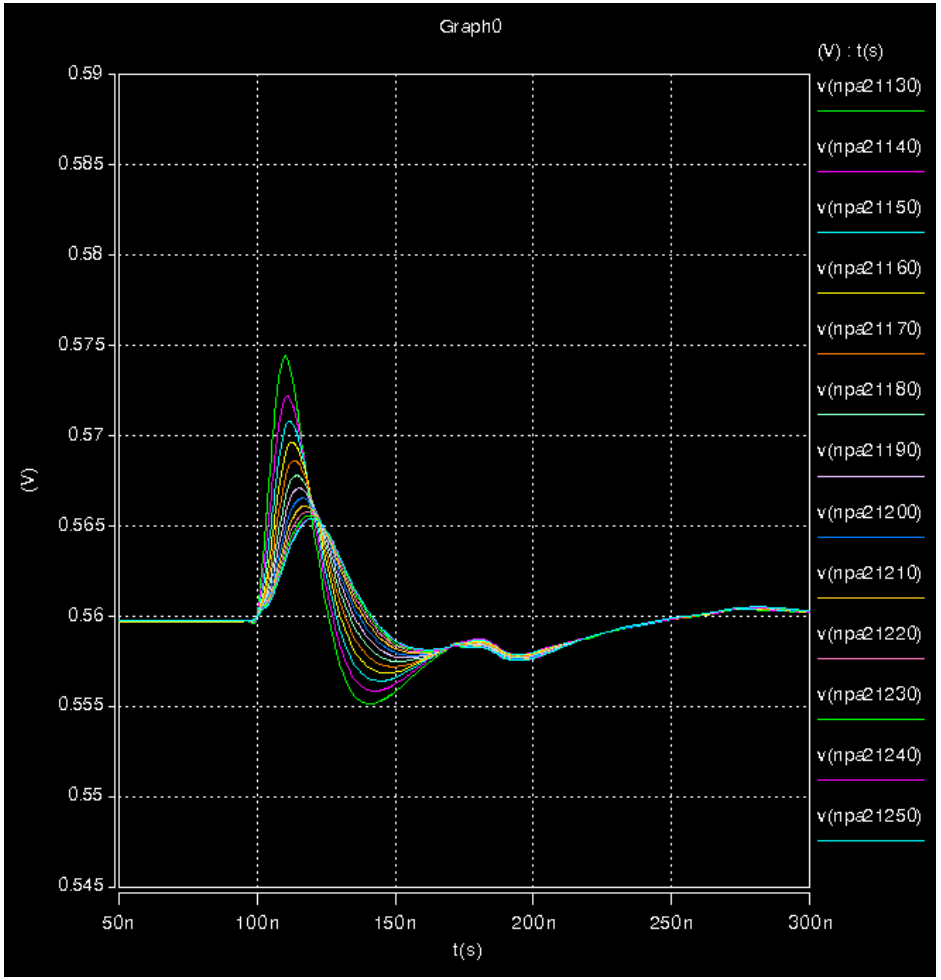
also provide extra ground connections at front edge

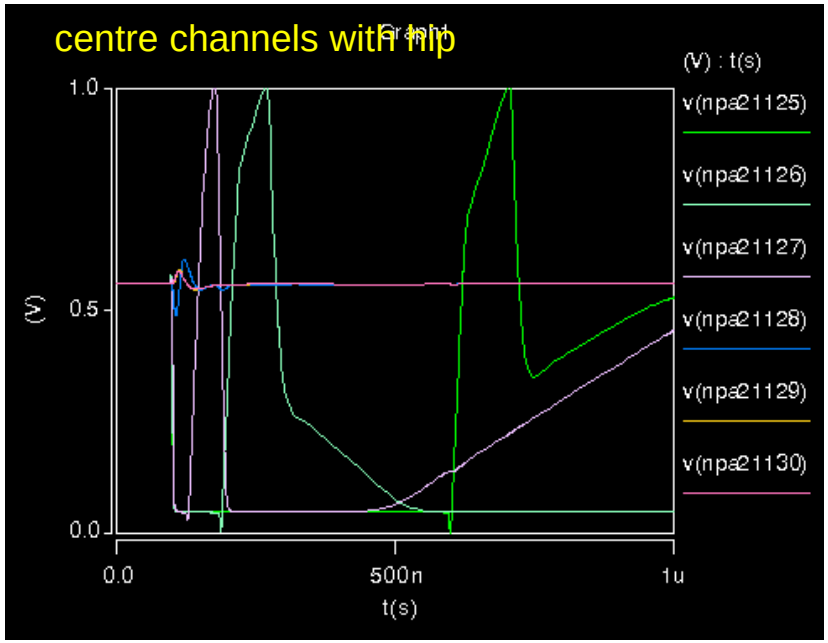
simulation conditions

250 channels
power supply and ground resistances as per Lawrence's information
bias line resistances - 1 ohm -> 0.45 ohms between channels
adding extra ground connections at preamp edge every 10th channel
tt case, 0 deg.

hip signal crosstalk

0.45 ohm, extra grounds (0.21 ohms)

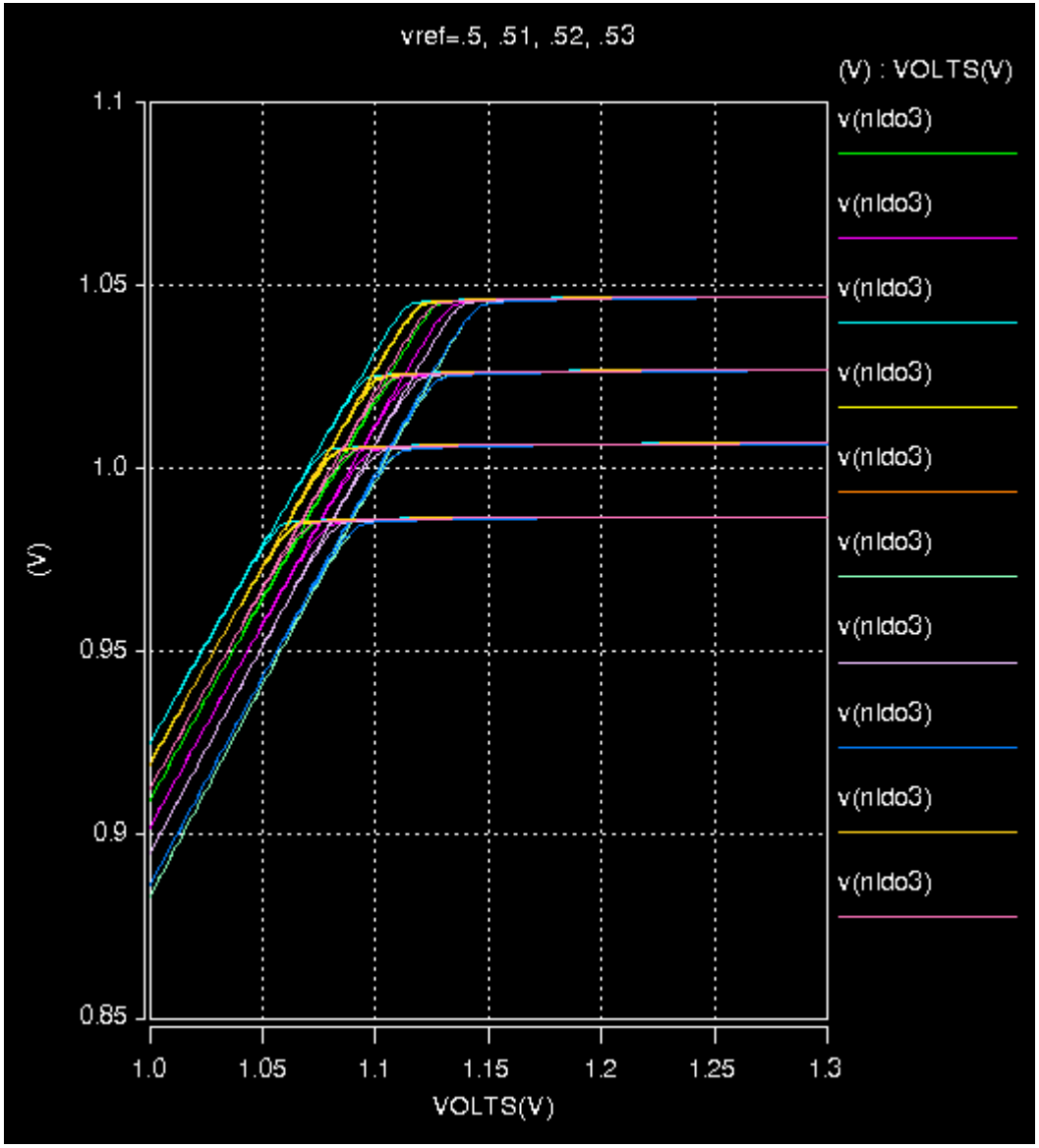




4pC hip signal on channel 125
postamp output shows < 5mV disturbance
(in signal direction) for other channels

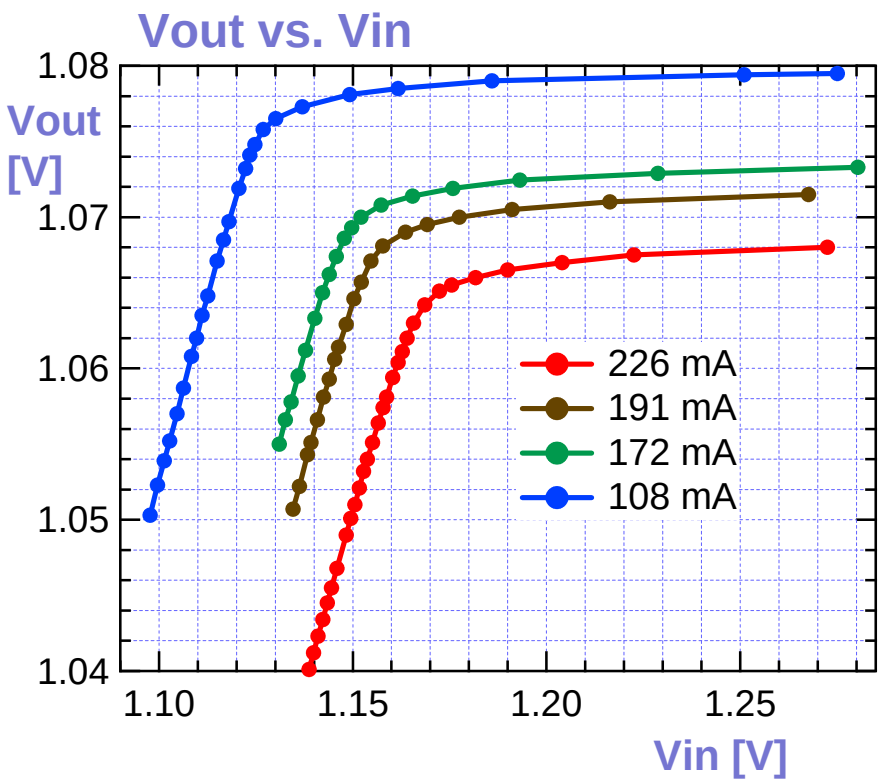
spare

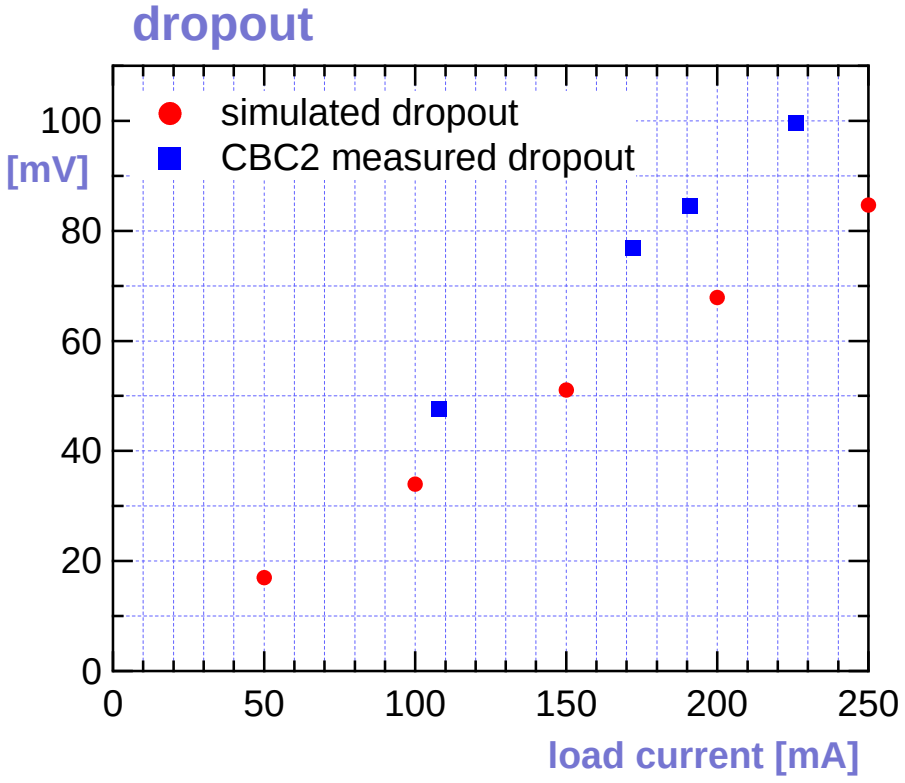
dropout check



vout vs vin for vref = .5 to .53
iload = 250 mA
T= +30, -20
all process corners

CBC2 LDO measurements





analogue current consumption
- ~ 300uA / chan. for 5 cm strips
- => ~80 mA / chip
- => ~40 mV dropout => plenty of headroom

analogue current consumption
- ~ 700uA / chan. for **8** cm strips
- => ~180 mA / chip
- => ~80 mV dropout => just enough headroom

=> no need to change core LDO design (only feedback resistor tweaks)

NMOS noise

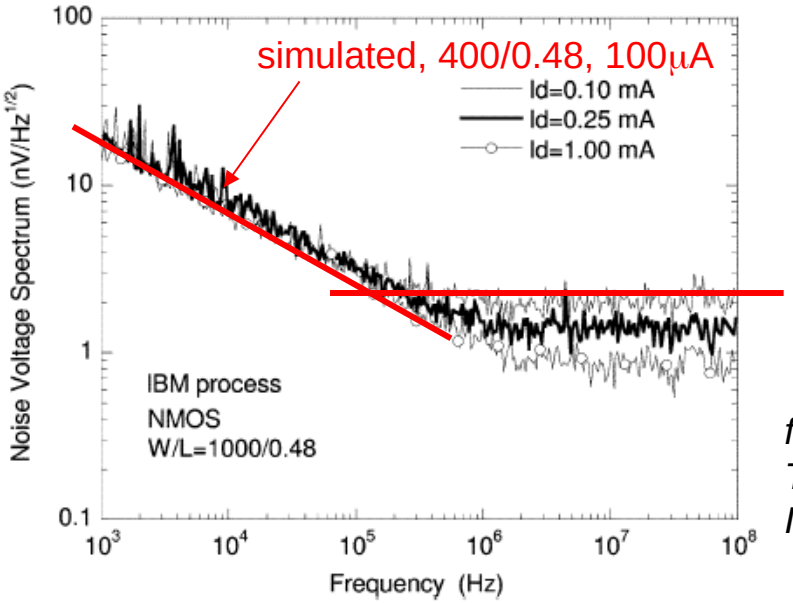
Ok if don't choose minimum device length

doesn't give much advantage in thermal region

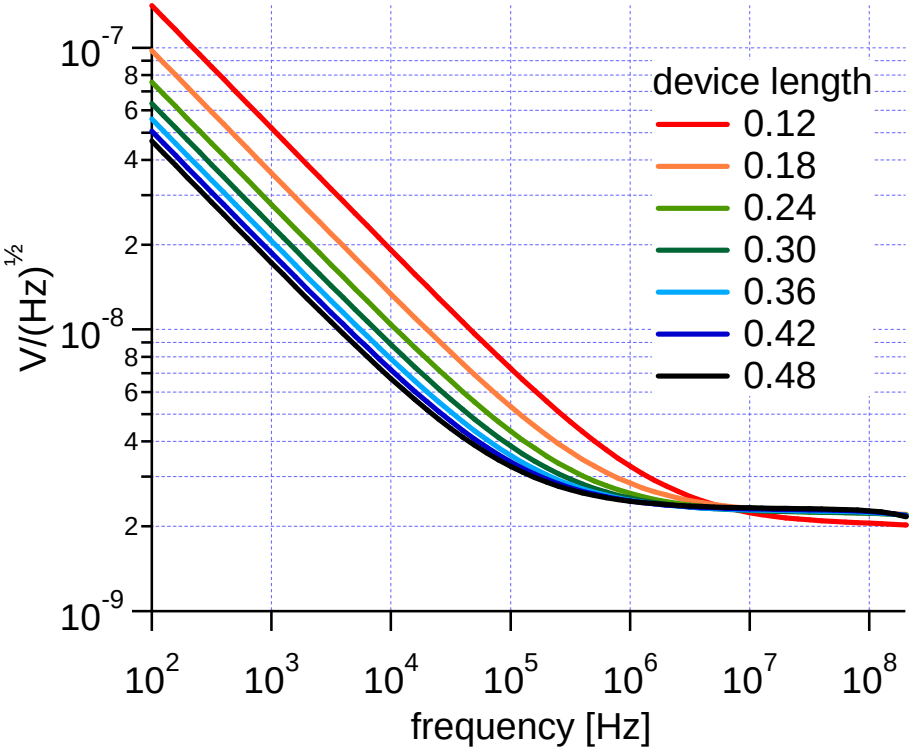
keep well clear of 1/f corner

0.36 seems about right

do we trust simulated noise?



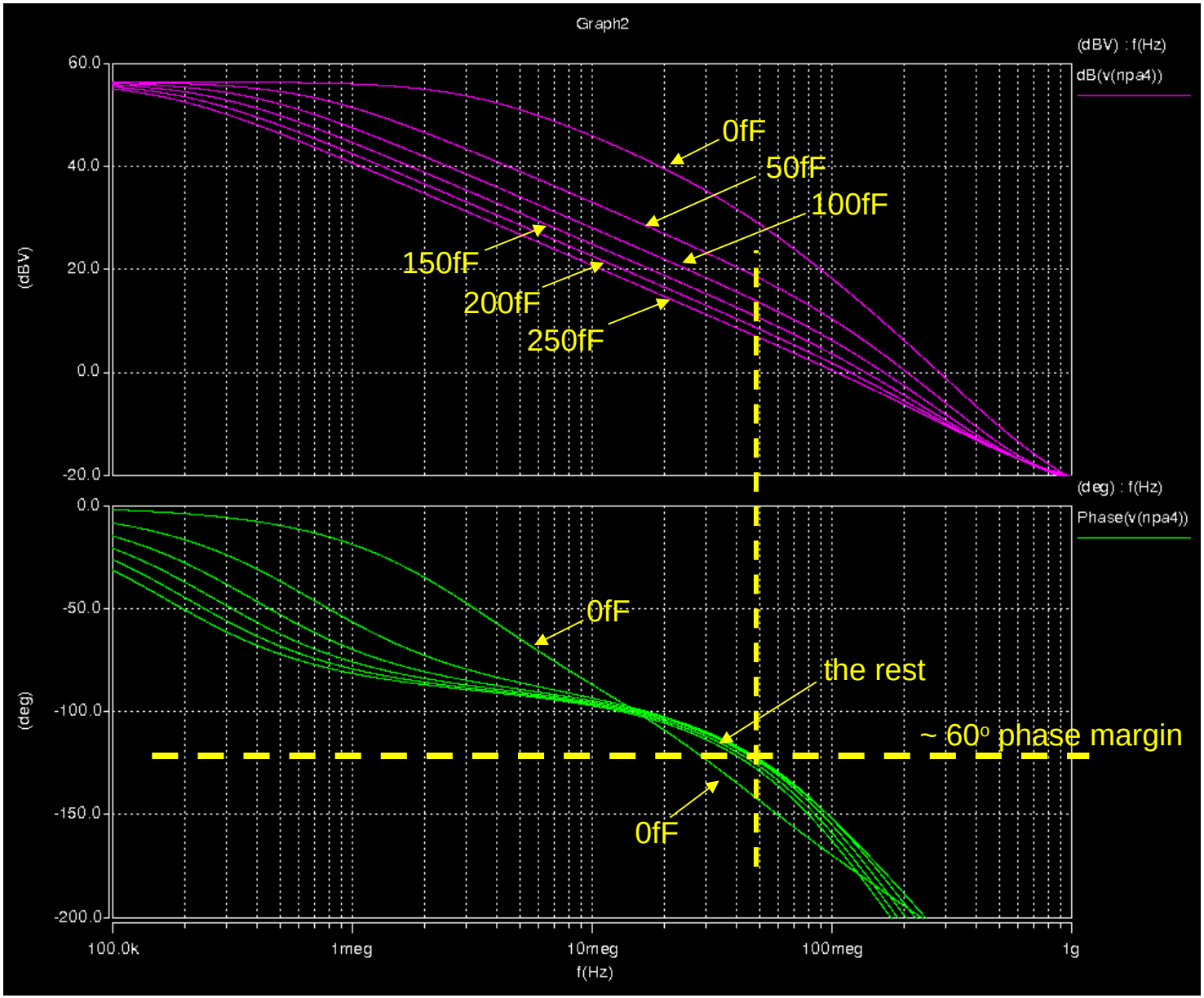
simulated device noise for I_{DS} = 100 μA, W=400 μm



from Manghisoni et al, Noise performance of 0.13μm Technologies for detector front-end applications IEEE Trans.Nucl.Sci. Vol.53, no.4,Aug.2006 (2456-2462)

Fig. 11. Noise voltage spectra of an NMOS with $W/L = 1000/0.48$ at different values of the drain current I_D ($V_{DS} = 0.6$ V). The samples belong to the IBM 0.13 μm process.

postamp compensation



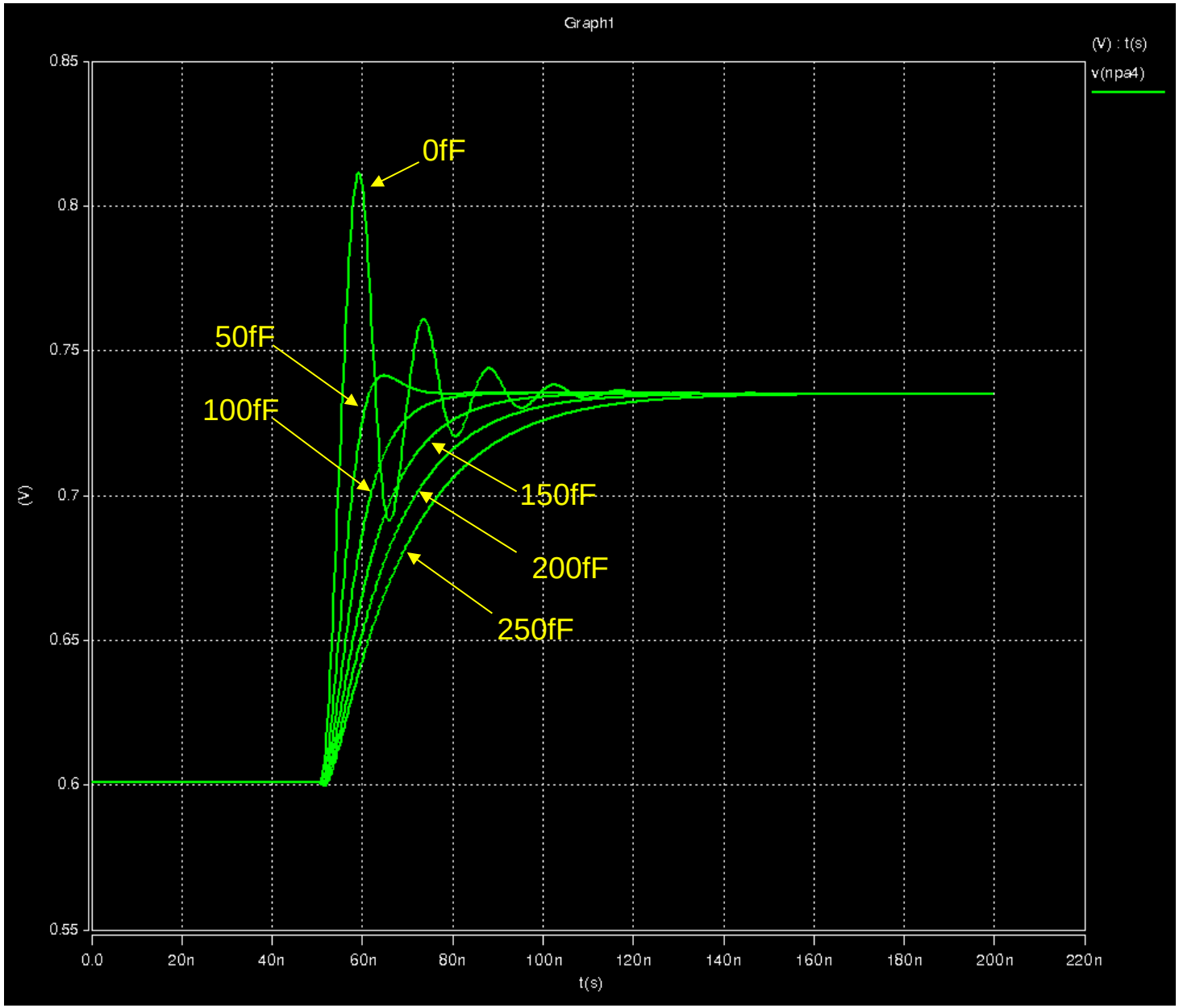
OL gain and phase vs. Ccomp

want gain of ~12 from postamp so need > 60° phase margin at ~ 20 dB for stability

plots show stable for gain > 20 dB with Ccomp > 50fF

choose Ccomp = 100 fF for greater margin

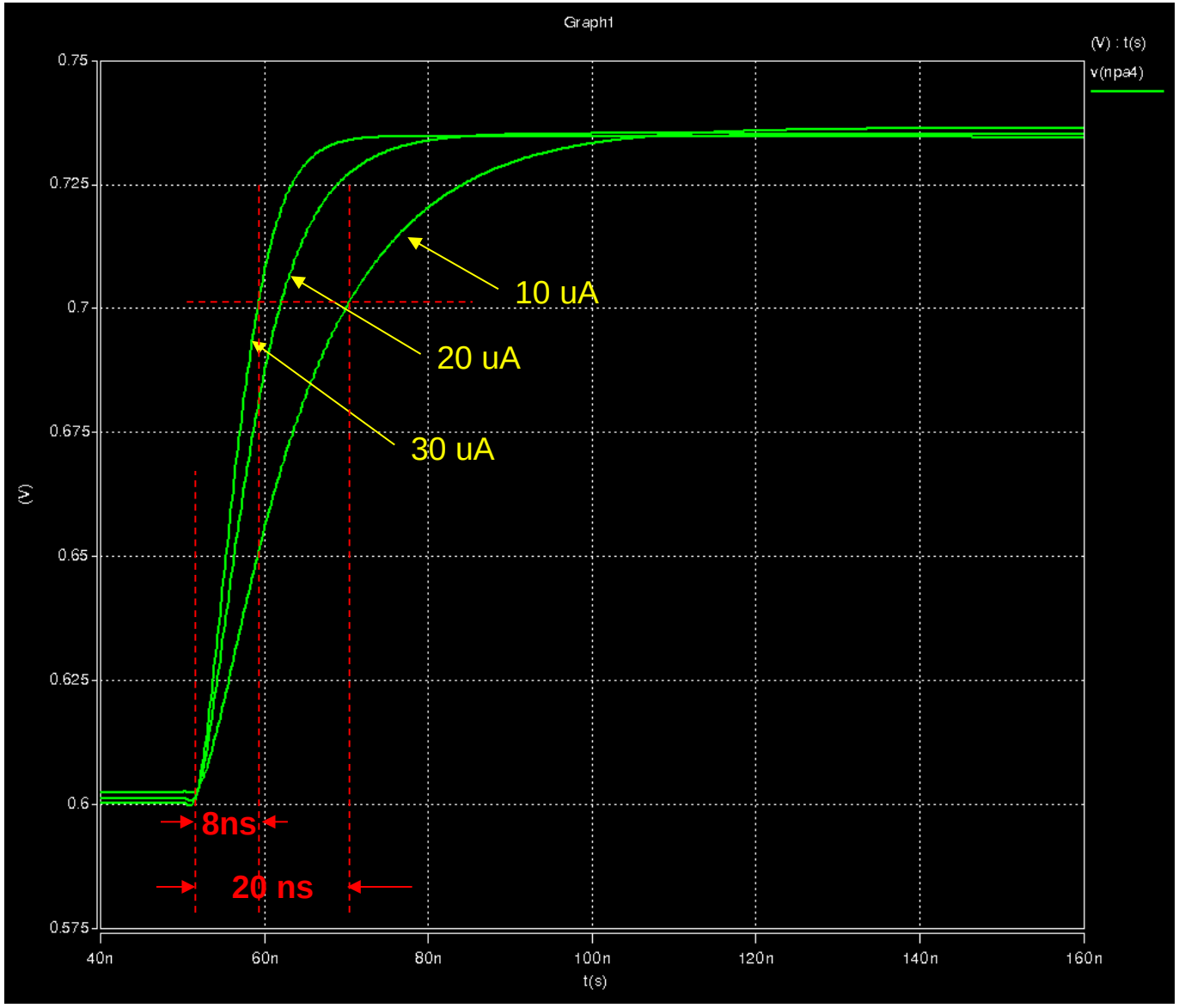
postamp compensation



transient closed loop (G = 12.5) step response vs. Ccomp shows expected behaviour

well-behaved for Ccomp = 100fF

postamp tuning



can use diff. pair tail current to tune frequency response

10 - 30 uA gives rise time constant 8 – 20 us