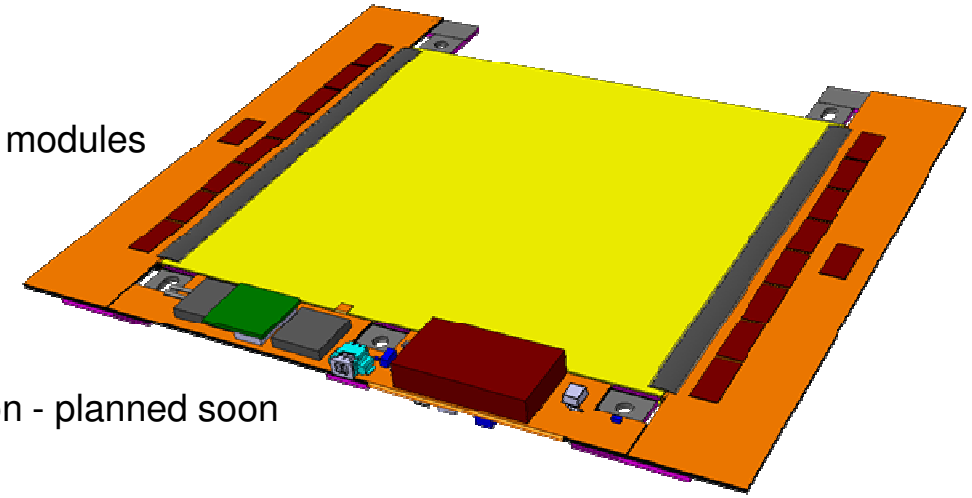
CBC3 status

Tracker Upgrade Week, 10th March, 2017

Mark Raymond, Imperial College
Mark Prydderch, Michelle Key-Charriere, Lawrence Jones, Stephen Bell, RAL

introduction



CBC3 is the final prototype front end chip for the 2S modules

submitted for manufacture July 2016
shared run with GBT-SCA asic

6 wafers received in October: wirebond finish
further processing required for bump deposition - planned soon

one wafer immediately sent for dicing
chips in hand since November

today will summarize

first results from single chips wire-bonded to carrier

wafer probe test preparations

for more detailed information, see:

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2016/CBC3_first_results_Dec_2016.pdf

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2017/CBC3_status_Feb_2017.pdf

CBC2 -> CBC3

- externally very similar (CBC3 has 1 extra column of pads)
  but many internal & interface differences

- front end optimisation
  shorter pulse shape, bug fixes, improved comparator threshold res'n, ...

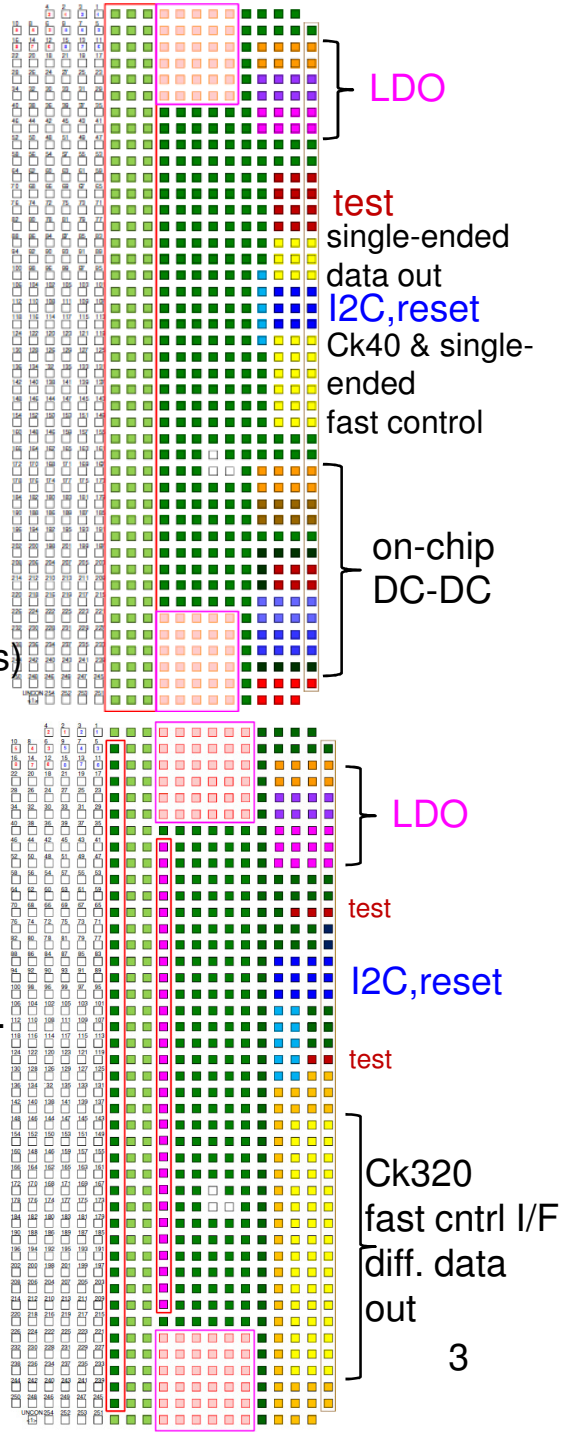
- stub logic
  cluster width rejection for clusters > 4 strips
  2 & 4 strip clusters used to give ½ strip resolution
  stub addresses + bend info produced, up to 3 stubs / BX
  ½ strip resolution for programmable window width (up to +/- 7 strips)
  ½ strip res'n for programmable window offset (4 groups, up to +/- 3 strips)

- longer pipeline: up to 12.8 usec

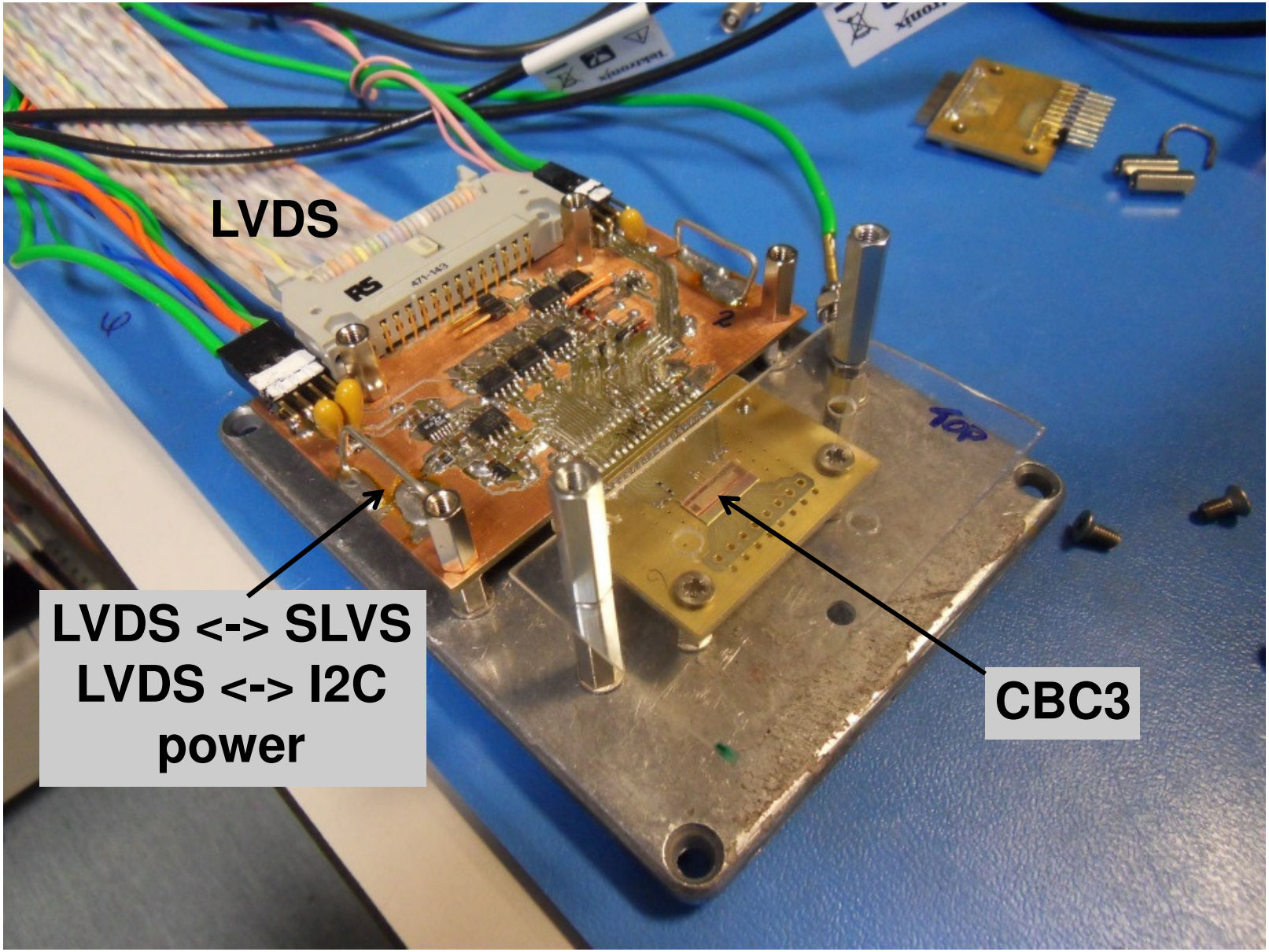
- up to 1 MHz L1 trigger rate capable

- fast differential interfaces
  6 x 320 Mbps stub data and L1 triggered readout
  320 MHz clock & fast control interface for trigger, sync reset, test pulse,..

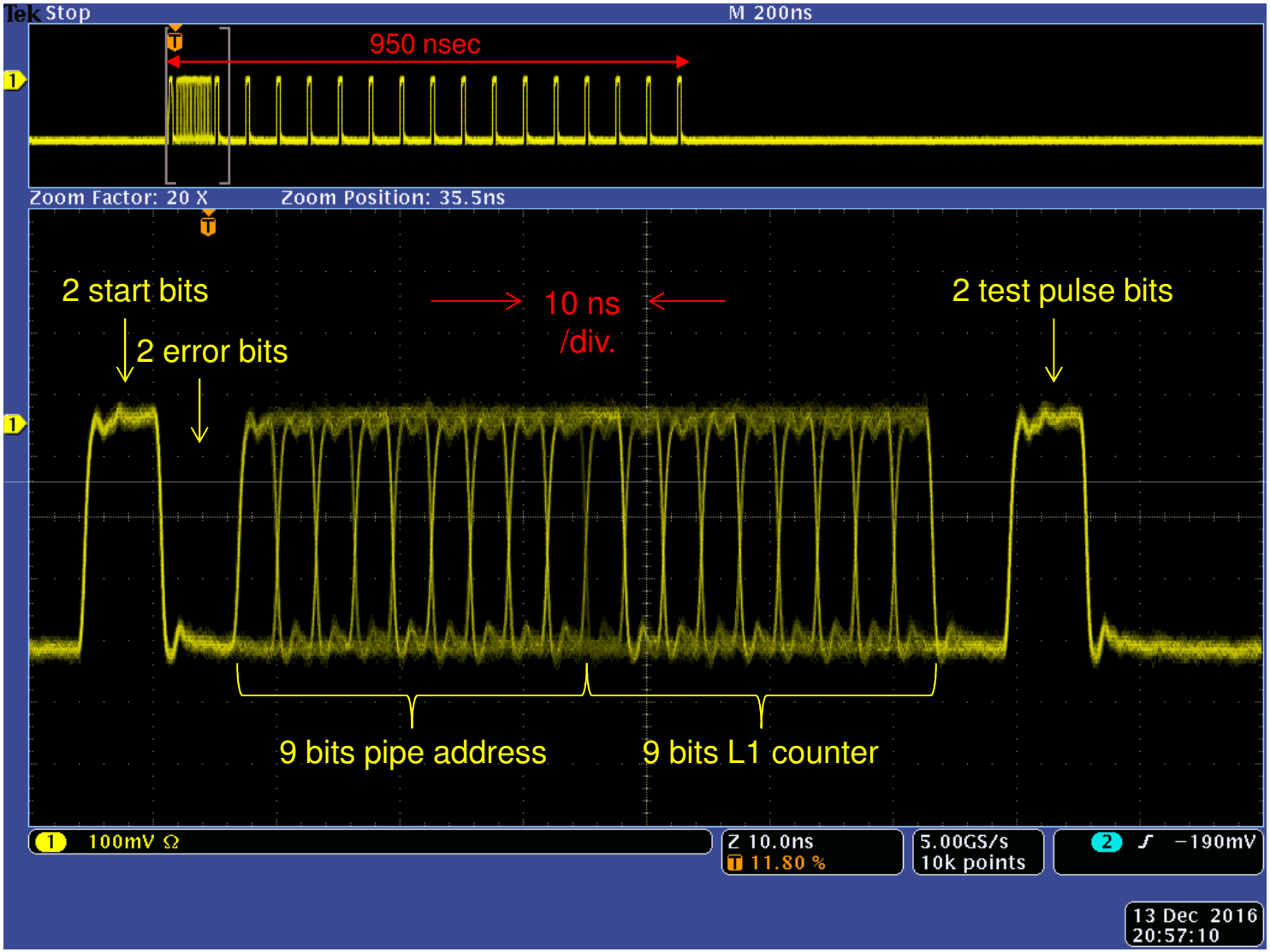
- system issues addressed
  synchronization, data formats, powering, ...



single chip test setup



scope picture of L1 triggered data

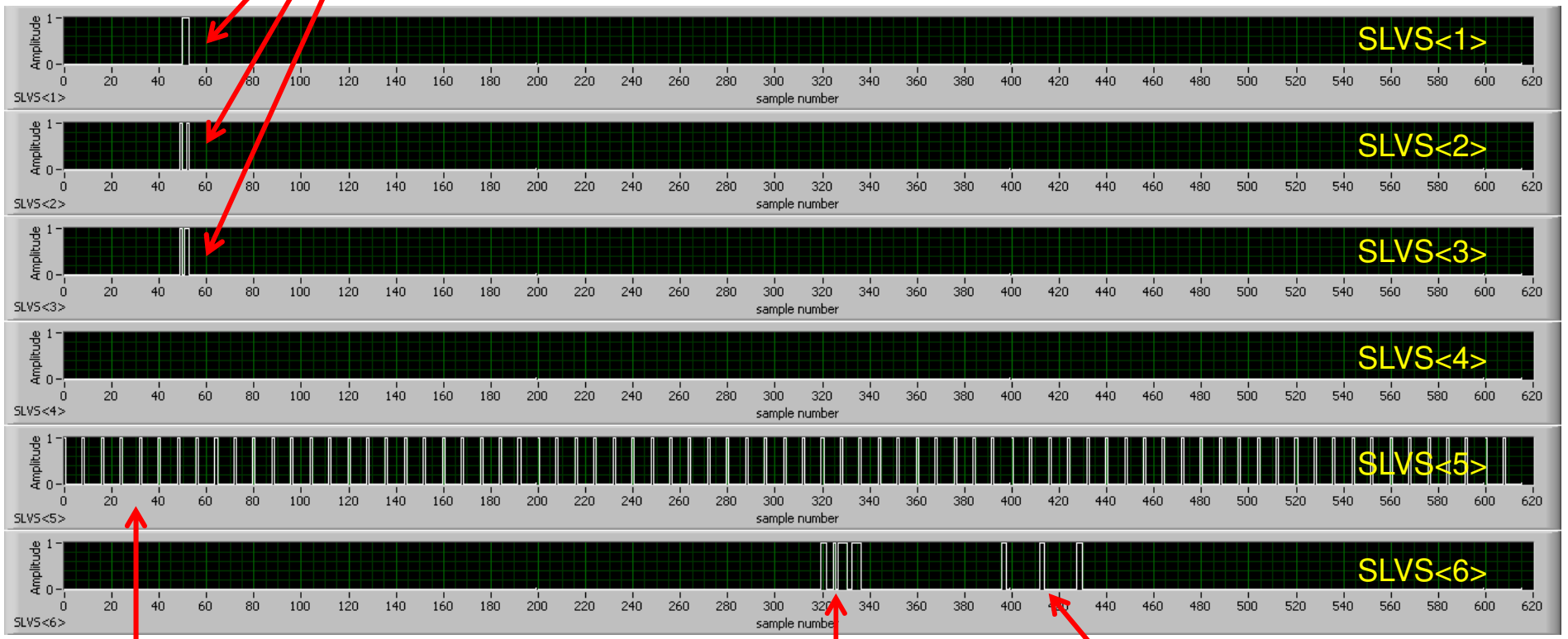


differential probe close to chip output, scope on persistence

DAQ picture of stub and triggered data

example here shows activity on 6 x 320Mbps output lines for 3 stubs generated using on-chip test pulse

SLVS<1>, <2> & <3> shows stub address data

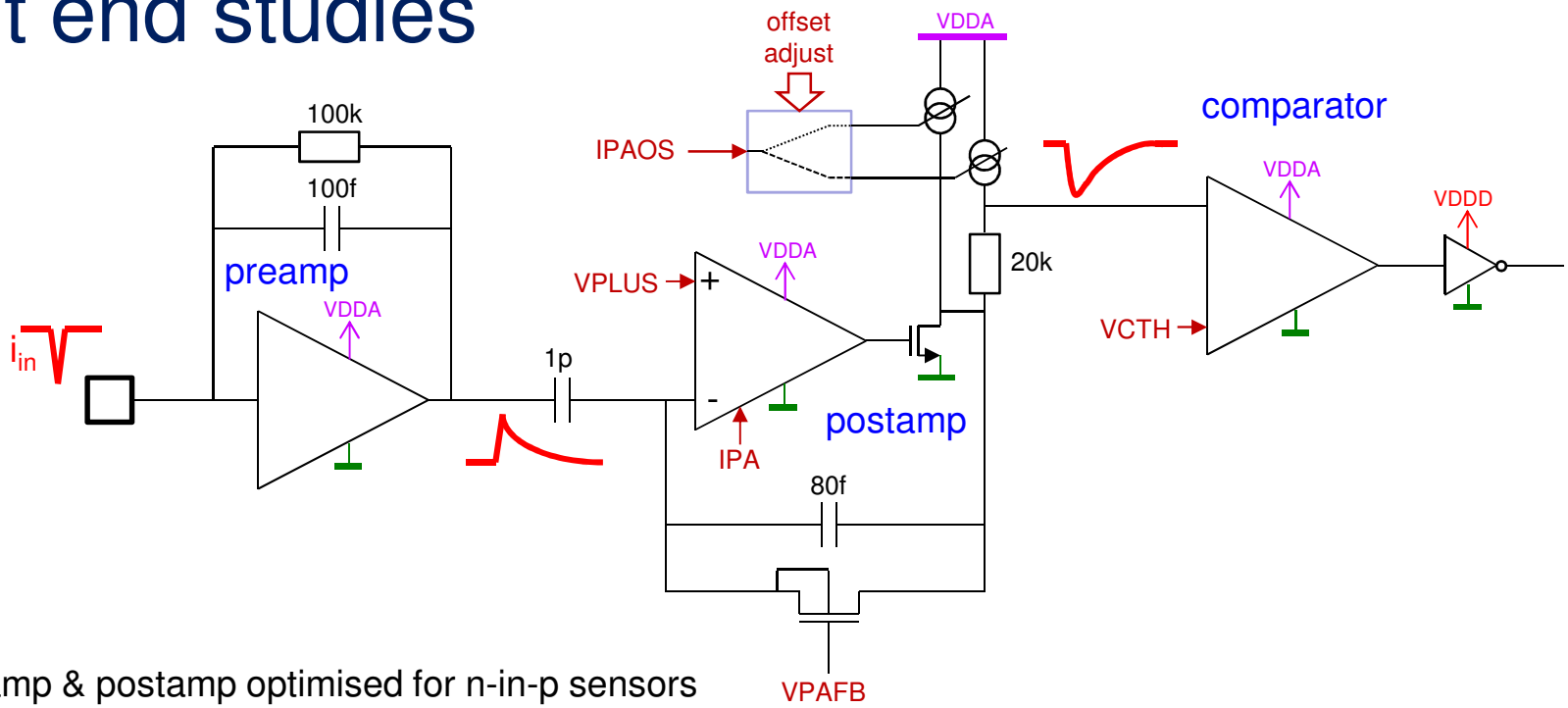


SLVS<5> shows sync pulse every 25 nsec

SLVS<6> shows digital header followed by 3 pairs of hits

note: no bend information, because test pulse fires channels directly above each other (seed channel and channel in centre of window => bend = 0)

front end studies



preamp & postamp optimised for n-in-p sensors
polarity switch options removed

provision to run more current in input device
(CBC2 at the limit for 5 cm strips)

faster shaping (return to baseline within 50 nsec)

global comparator threshold VCTH modified
for improved linearity and 10-bit resolution

global comparator threshold VCTH

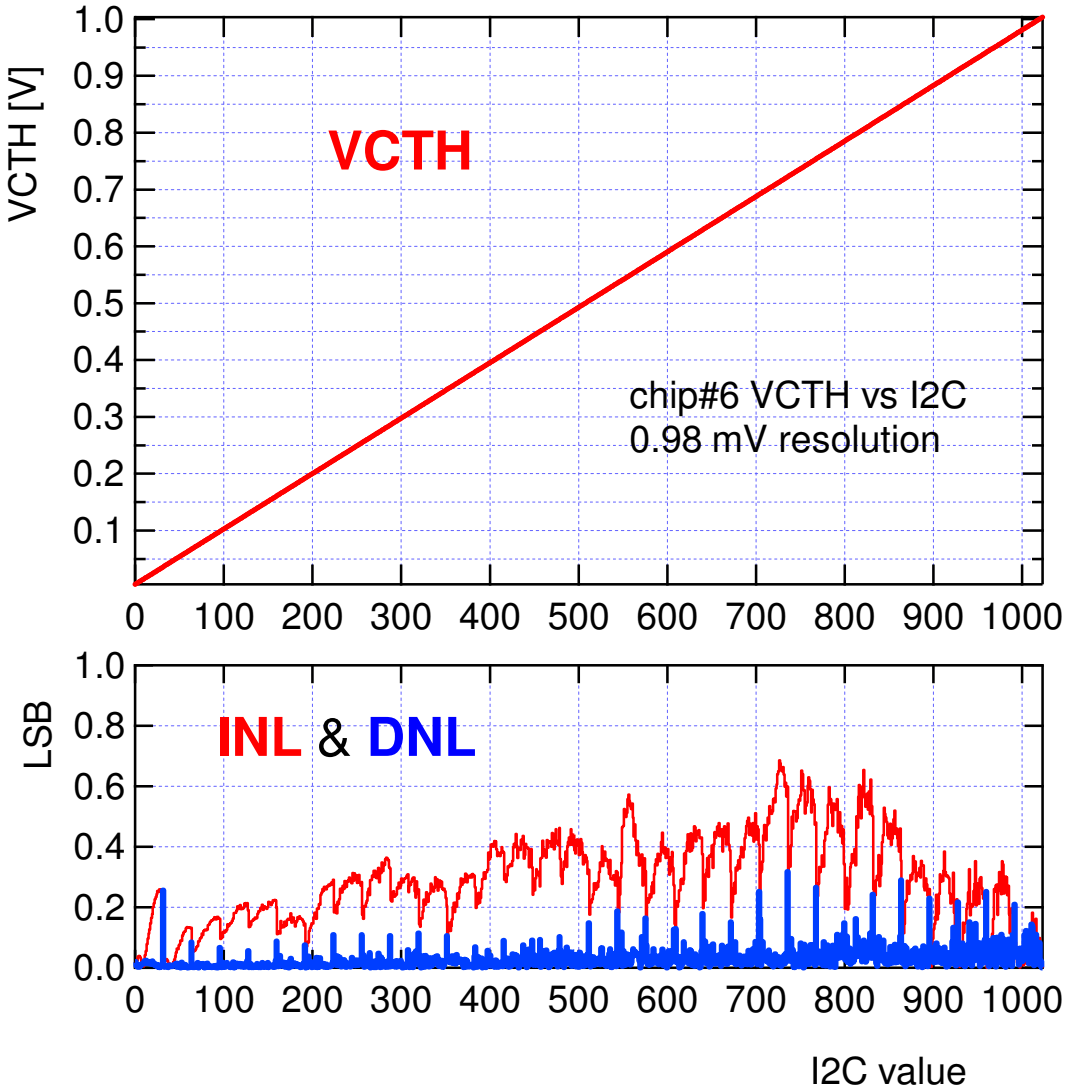
most of chip characterization studies involve sweeping VCTH (s-curves)

CBC2 VCTH not v. linear and not monotonic

for CBC3 VCTH now generated by 10-bit resistor ladder DAC

~ 1 mV resolution (~ 150 electrons)

non-linearity << 1 LSB



$$INL = \left| \left(\frac{V_{meas} - V_{zero}}{V_{LSB\text{-}IDEAL}} \right) - I2C_{value} \right|$$

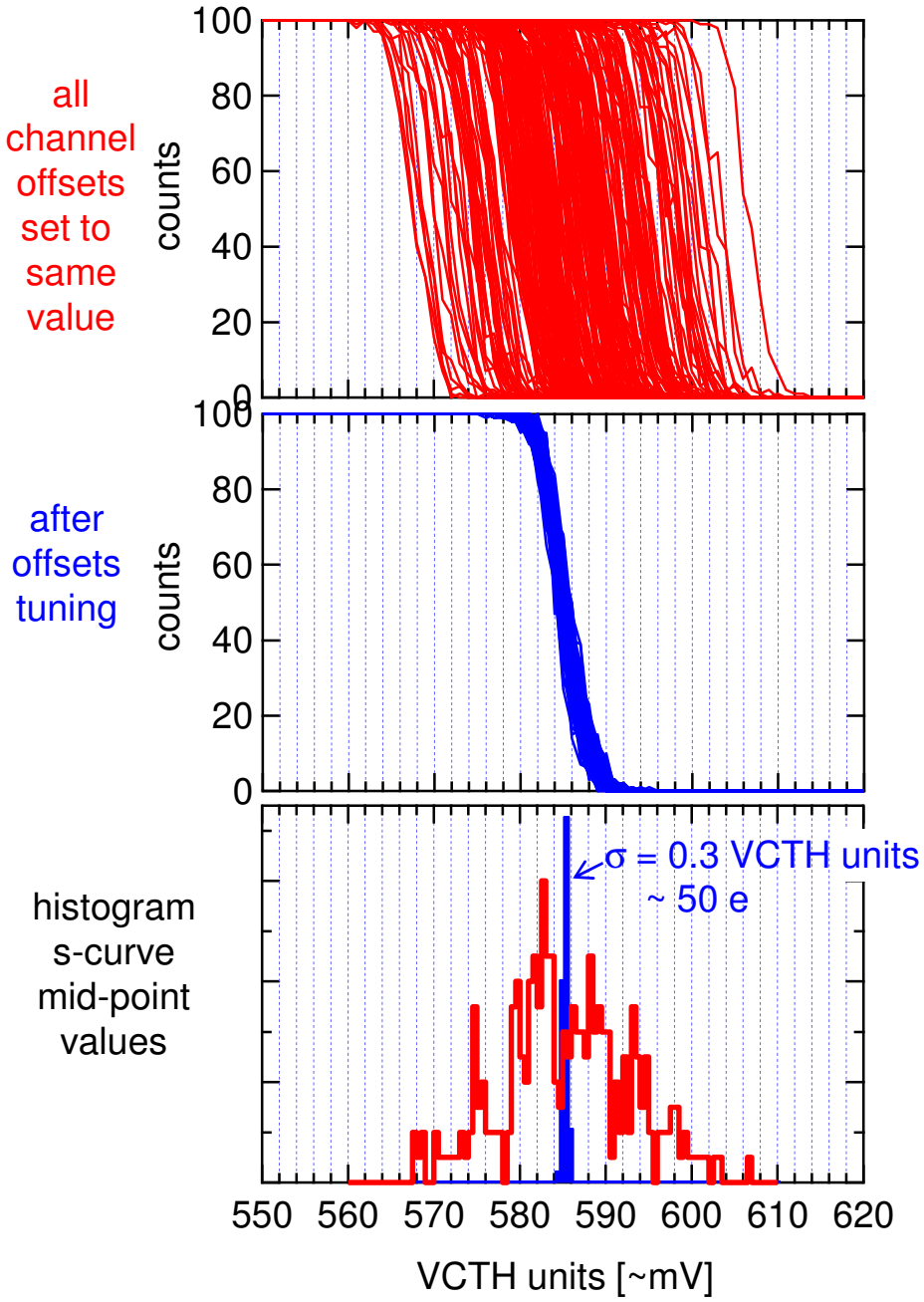
$$DNL = \left| \left(\frac{V_{m+1} - V_{m}}{V_{LSB\text{-}IDEAL}} \right) - 1 \right|$$

scurves and channel offsets tuning

s-curves useful for setup and performance studies

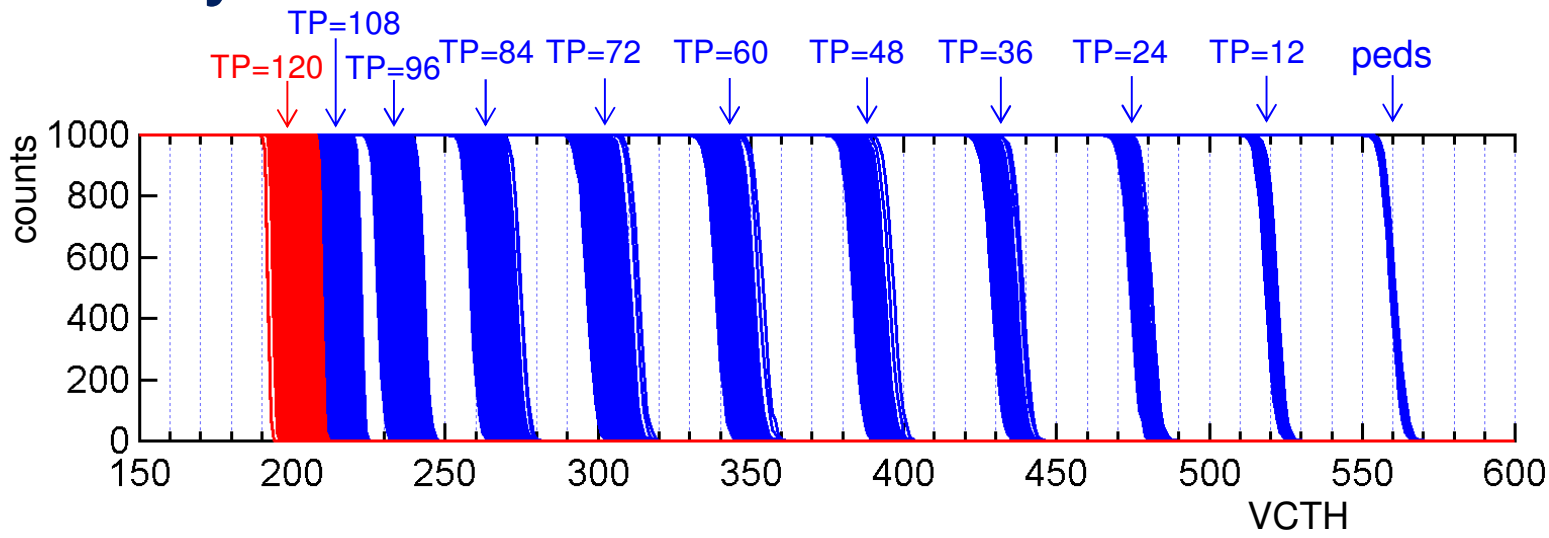
=> helps to have monotonic, linear and higher resolution DAC for VCTH

after tuning, channel offsets distribution has σ of ~50 electrons



gain & linearity

s-curves for different test pulse amplitides

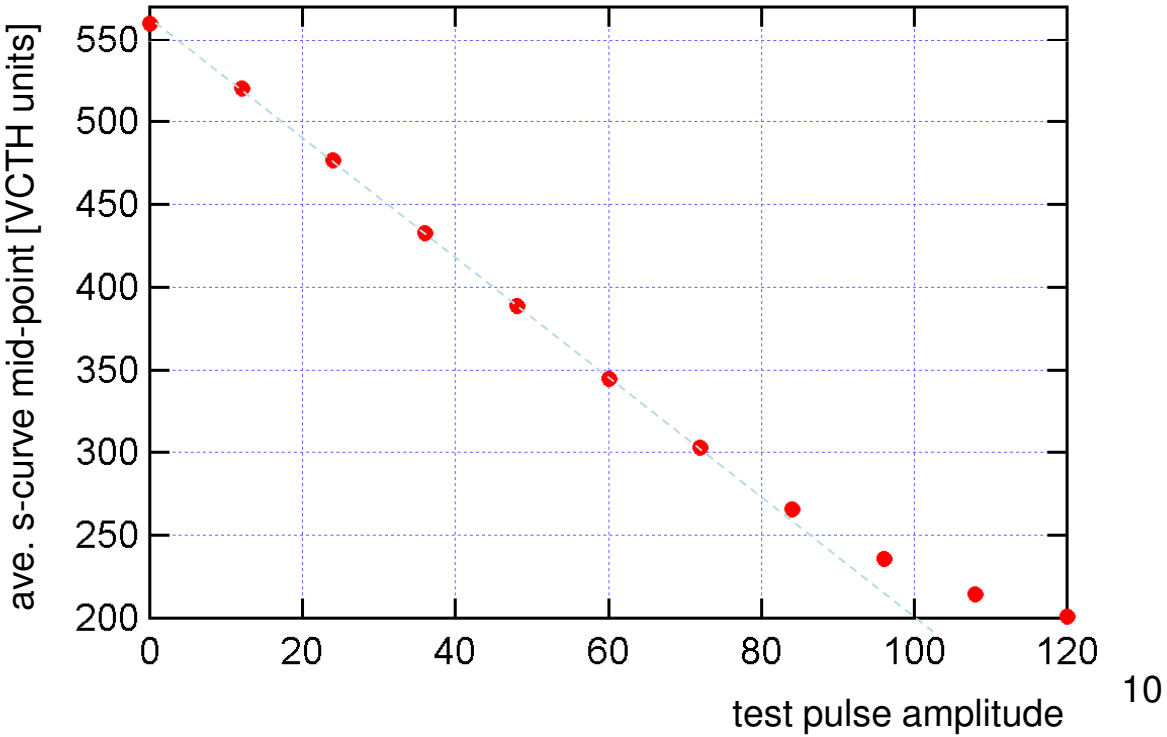


approximate calibration
1 fC = 12 TP units

(~ 15% uncertainty in charge injection capacitors)

get ~ 40 mV / fC

good linearity to ~ 6 fC



test pulse sweeps

use test pulse to look at comparator output signal duration

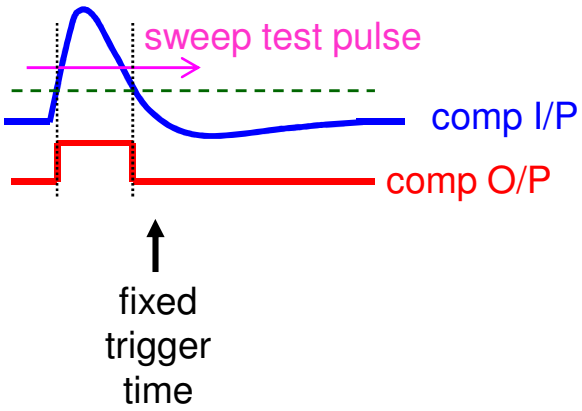
fix trigger time and sweep test pulse charge injection time - 1 nsec steps

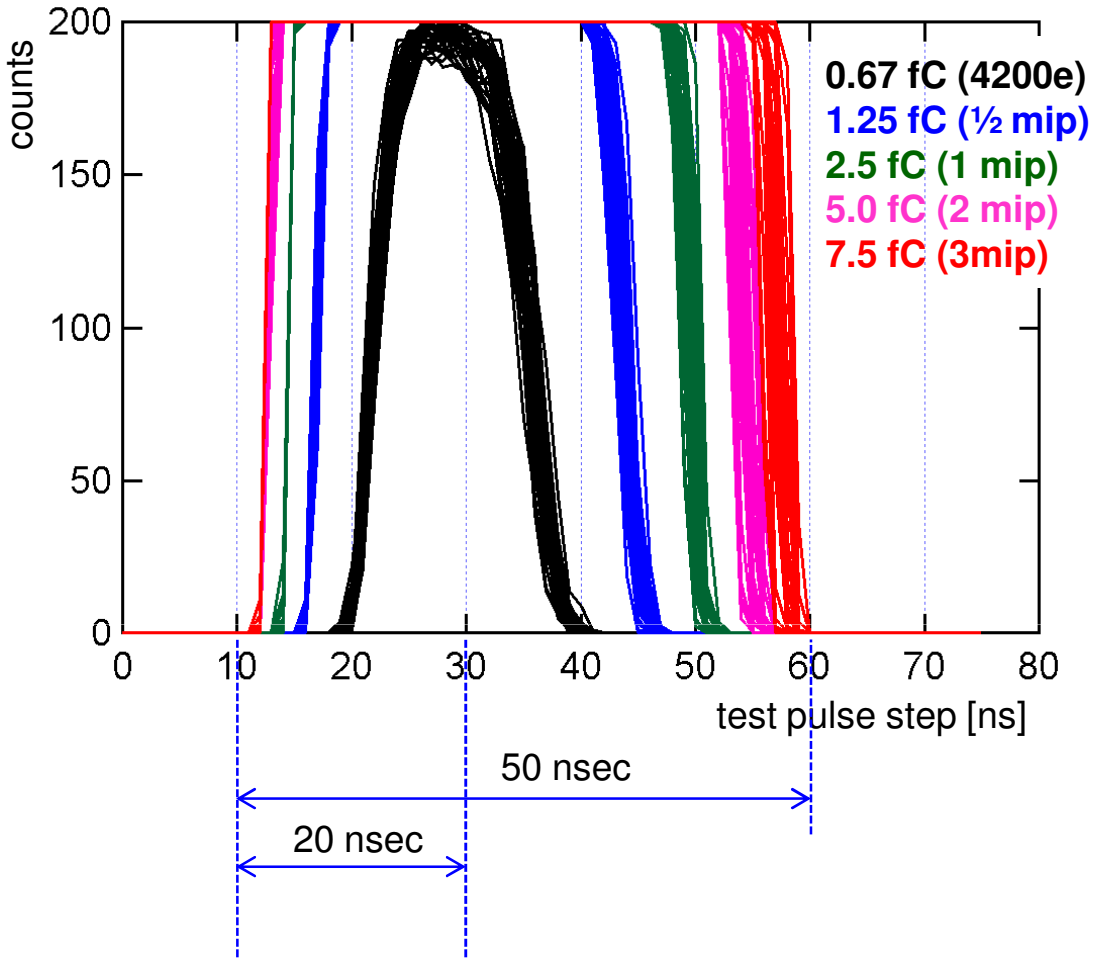
VCTH set to ~ 4000 e

pulse width < 50 nsec

=> signal confined to 1 BX

can deduce pulse peaking time < 20 nsec





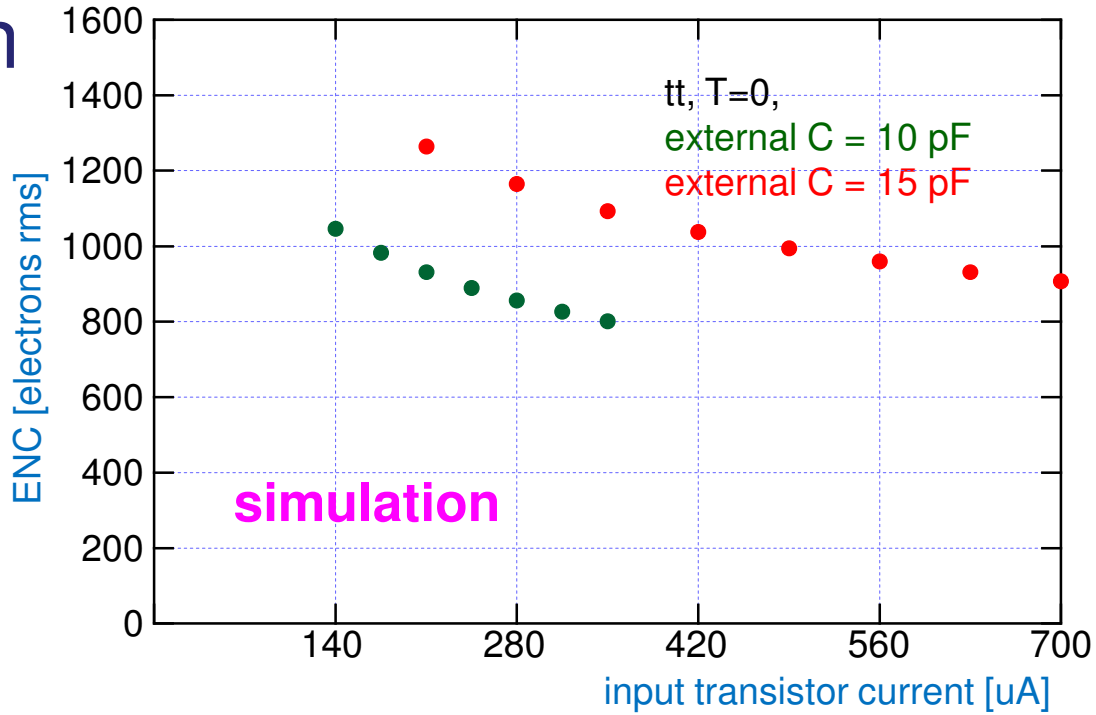
power consumption

analogue power depends on desired performance

noise depends on current in input FET

<1000e target can be achieved for
total analogue power of 350 uW / channel

(to be confirmed)



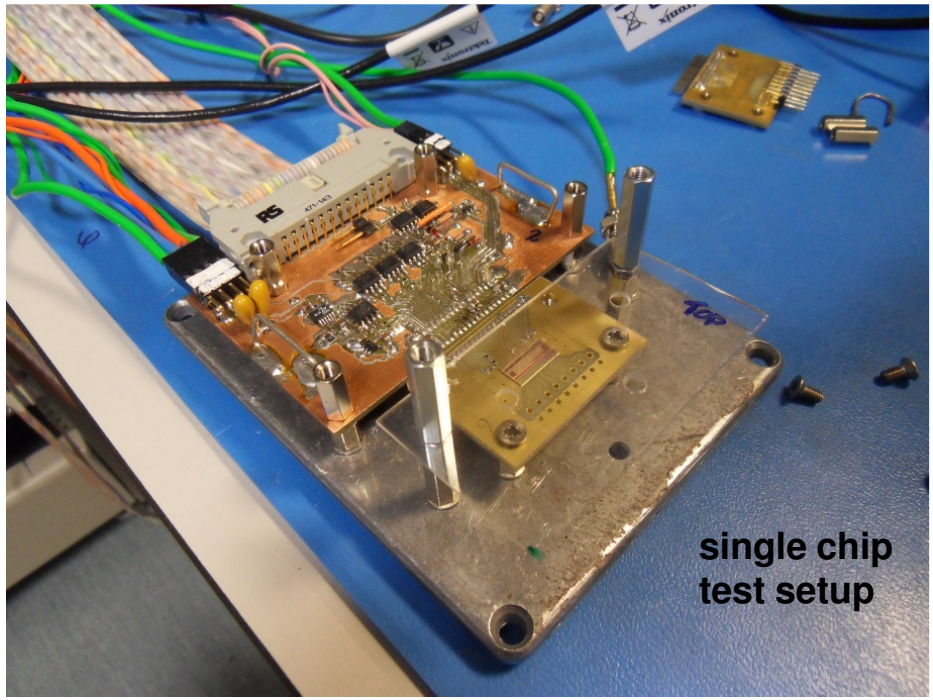
digital power

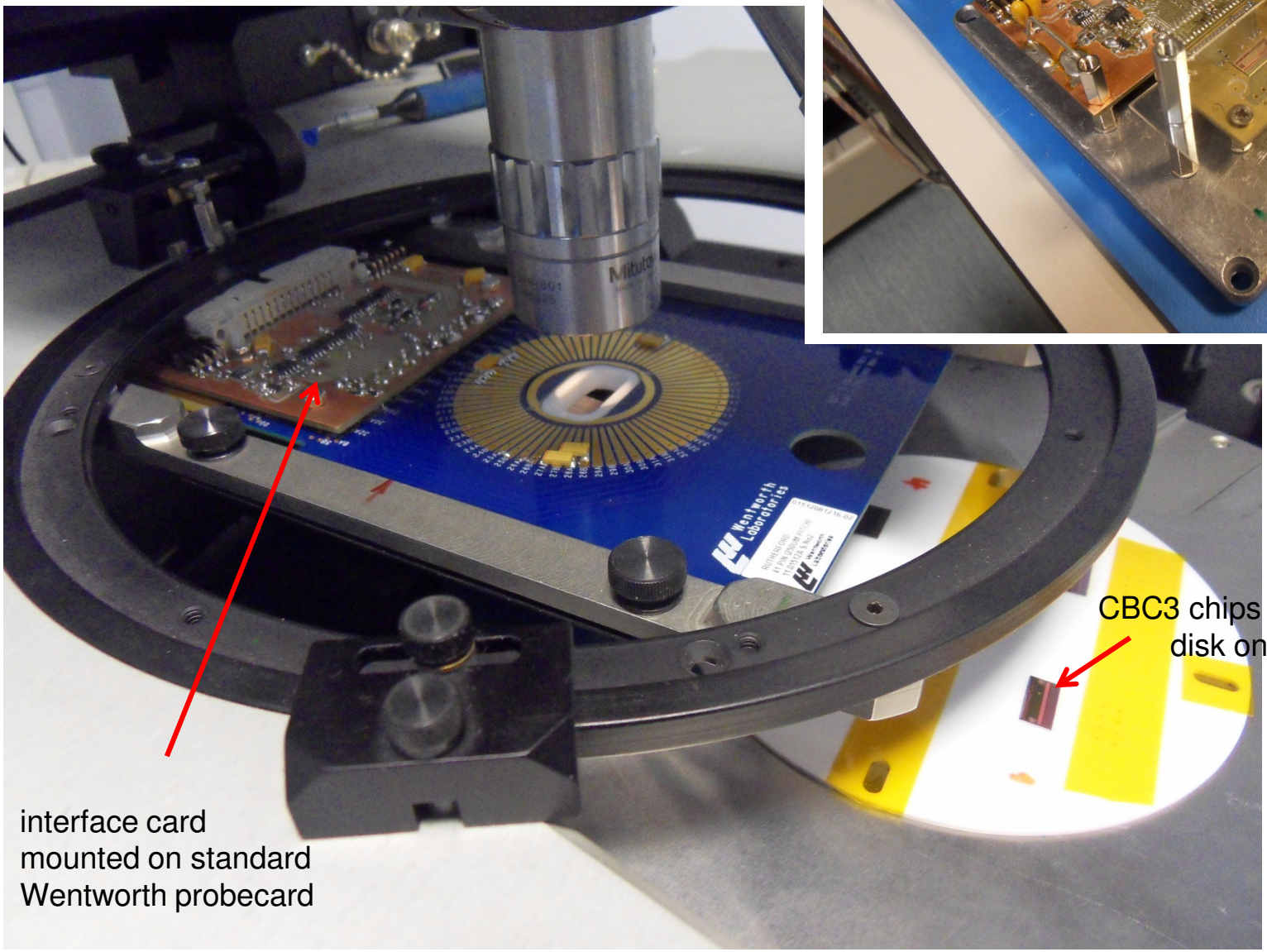
target: 100 uW / channel
(based on assumptions and guesswork - early on in design cycle)

measured: ~160 uW / channel
=> overall chip power goes to ~510 uW / channel (unless sacrifice some analogue power)

wafer probe test setup

320 MHz full speed running of chip via probe-card seems to work - good news



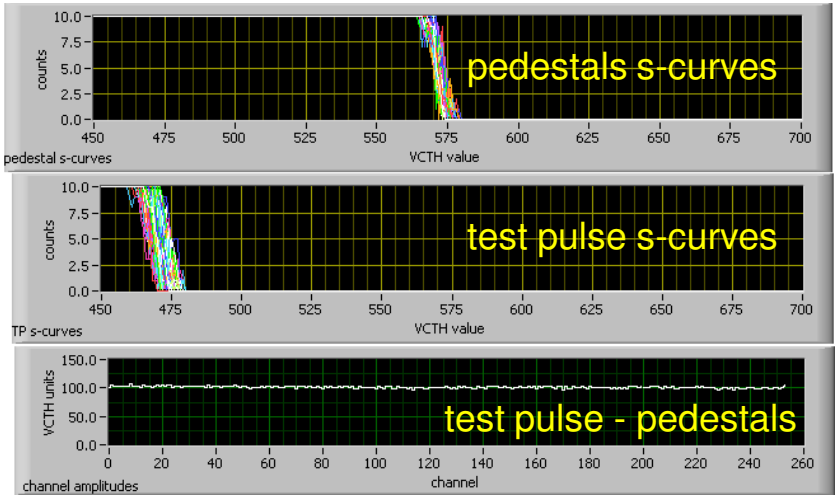


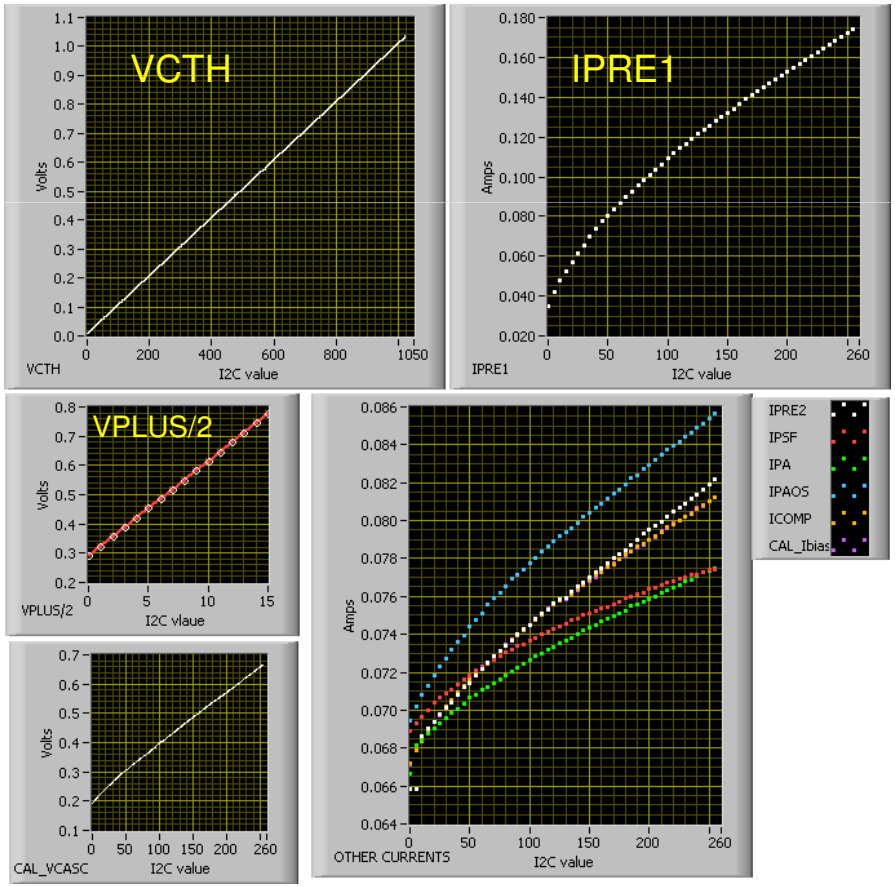
wafer probe tests(1)

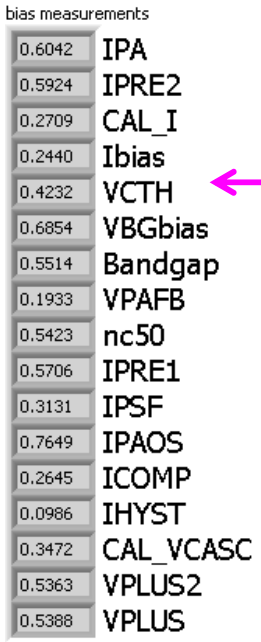
all I2C registers, pipeline & buffer ram locations checked for stuck bits

bandgap reference tuned (process dependent), unique chip ID programmed, efuses blown to fix values

offsets tuned, s-curves for pedestals and test pulse acquired
low or non-responsive channels can be identified







power consumption checked

bias generator voltages and currents measured - can look at chip-to-chip variations and reject significant outliers

wafer probe tests(2)

check all stub addresses and bend information correctly reported

set VCTH so all channels firing all the time, then use channel mask to generate specific clusters

sweep seed cluster across chip, sweeping window cluster throughout window

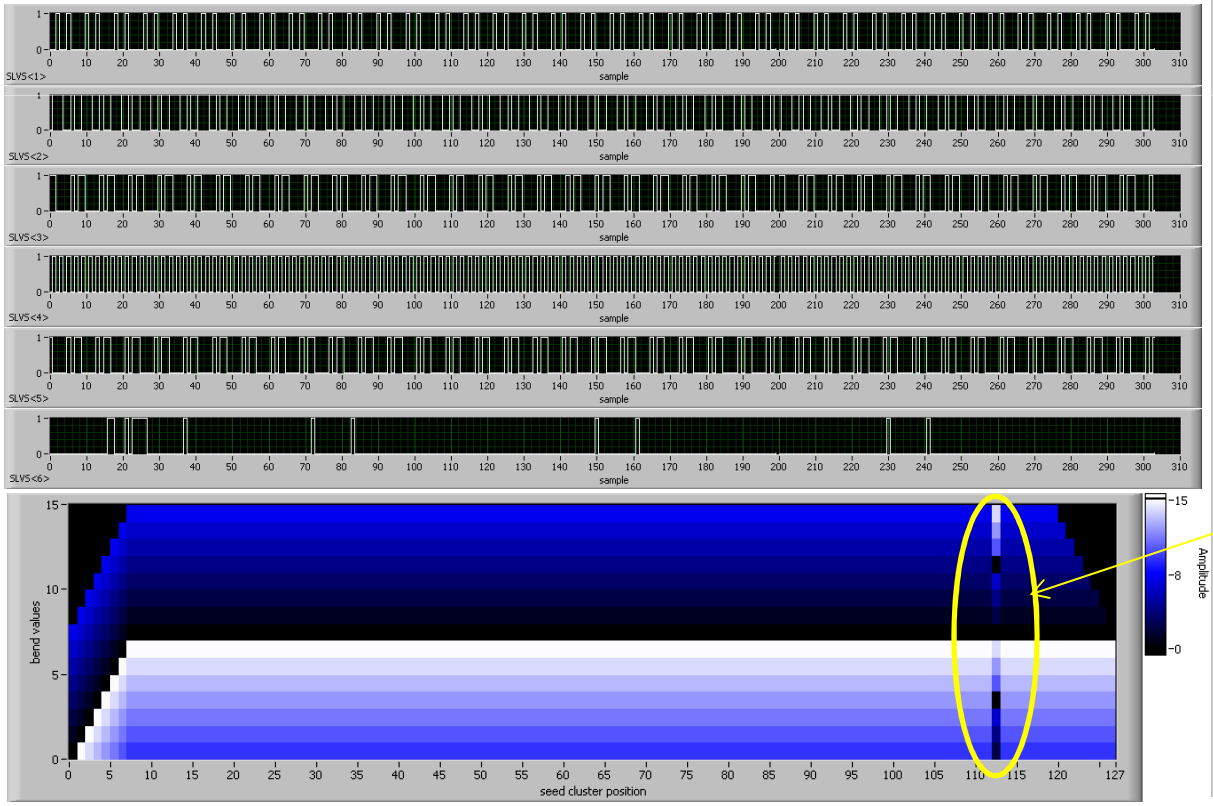
can use method to check:

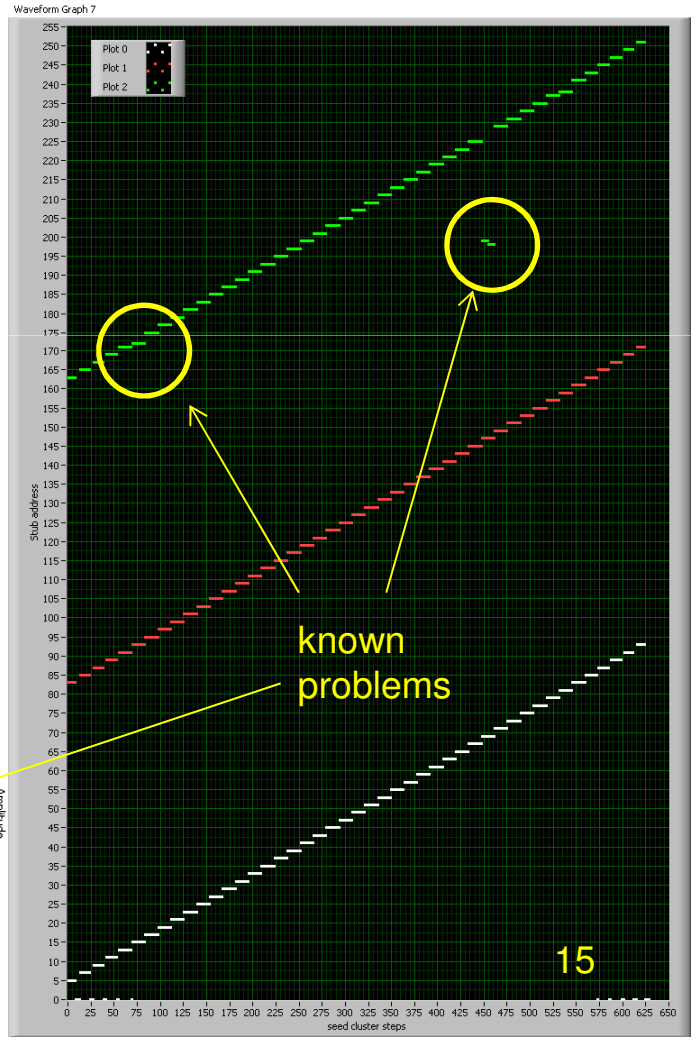
all combinations of seed and window cluster widths

all possible programmable pT window widths

all possible window offsets

can do 3 stubs at a time





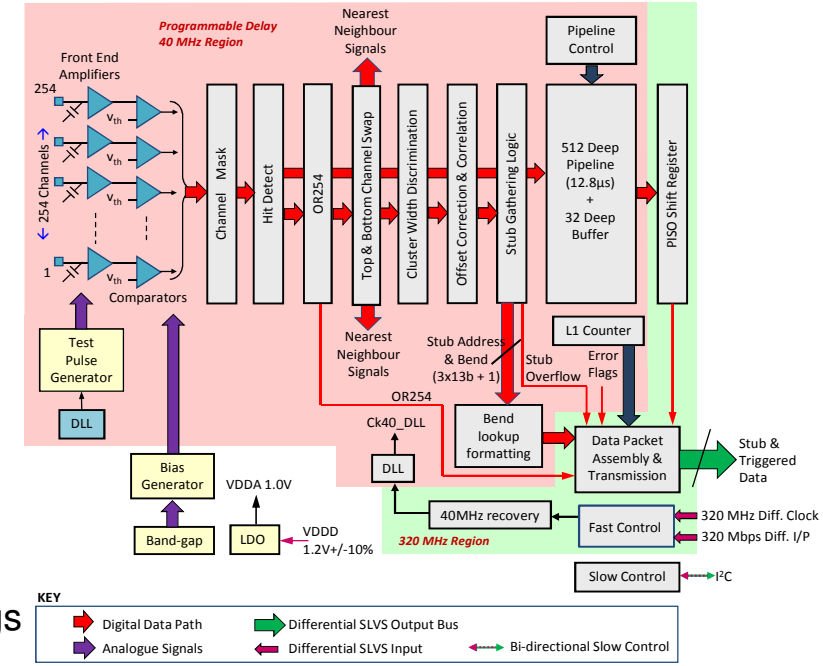
problems identified so far

some problems in the digital logic

1) a few stub addresses and bend info are incorrect

traced to mistakes in Verilog description files
(should have been caught)

easily fixed and not difficult to correct for



2) triggered readout data gets corrupted for some DLL settings

(DLL used to tune comparator output sampling in 1 nsec steps)

more serious problem - under investigation

only occurs if trigger occurs during readout period of data from a previous trigger

stub data unaffected

most DLL settings are OK - consistent across all chips tested so far

=> avoid the problem DLL values and should be ok

summary

CBC3 is working
- some digital issues to work around, but nothing to stop progress

analogue front end appears ok
- need to bump-bond and connect to sensors to get true performance
  - tests with 2CBC3 hybrid probably ~ 3-4 months away

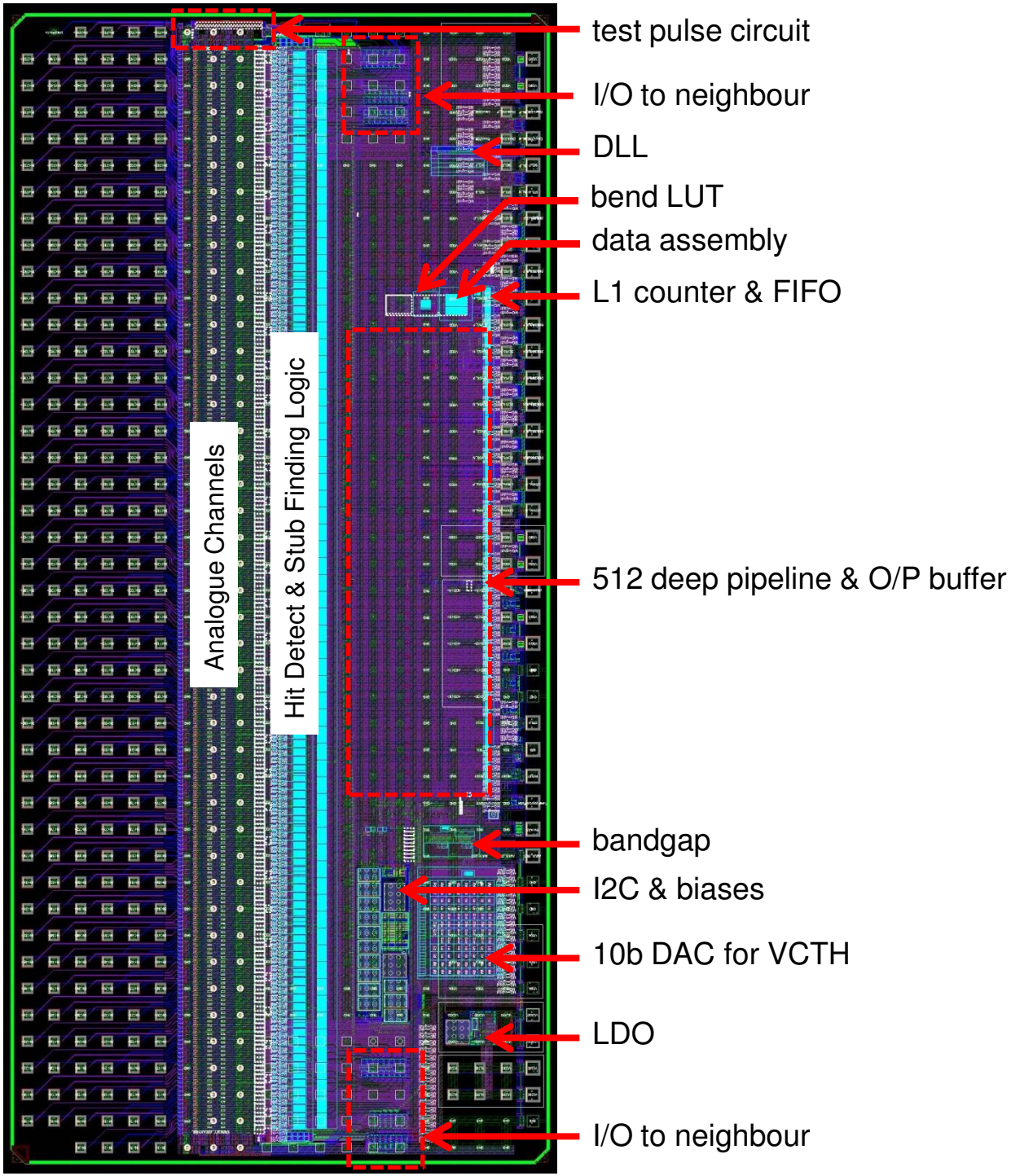
wafer probe test setup ready - probing at 320 MHz looks feasible
- 8 wafers currently in transit to IC
- should be able to ship tested wafers to bumping company ~ end March

ionizing irradiation test currently in progress

SEU test expected before Summer

extra

CBC3



final layout picture for reference

20 columns, 43 rows
(1 more column than CBC2)

5.25 mm x 11 mm

CBC3 digital interfaces

output data: up to 3 stubs data transmitted to CIC/BX
6 SLVS diff pairs @ 320 Mbps

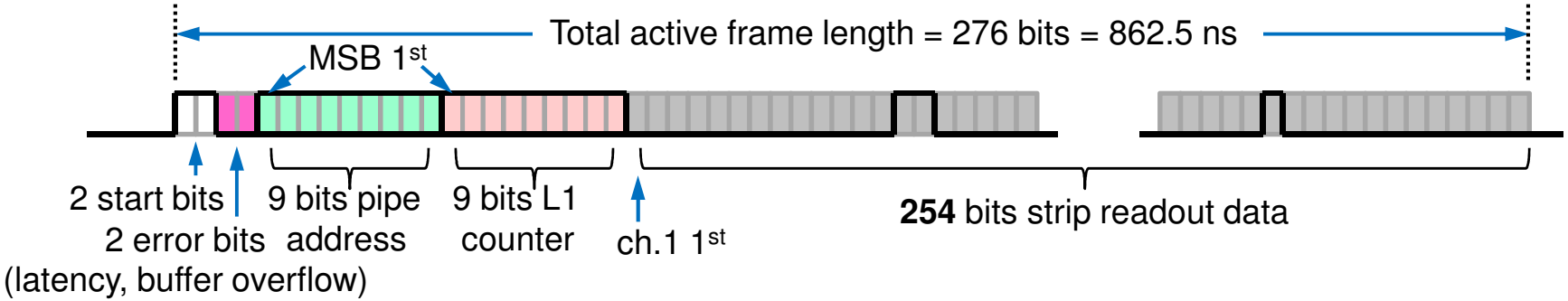
25 ns

S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**

R = L1 triggered readout data
time flow **top** to **bottom** (e.g. S1<7> output first)

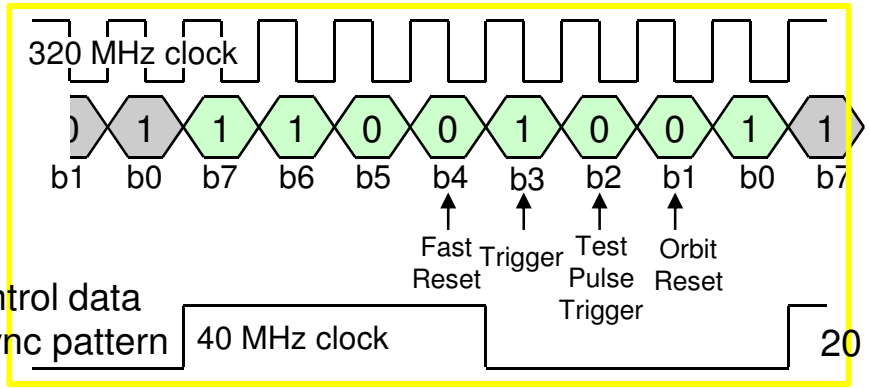
readout data

readout data frame length 950 nsec
=> up to 1 MHz L1 triggering capability



fast control

320 MHz clock
320 Mbps fast control line



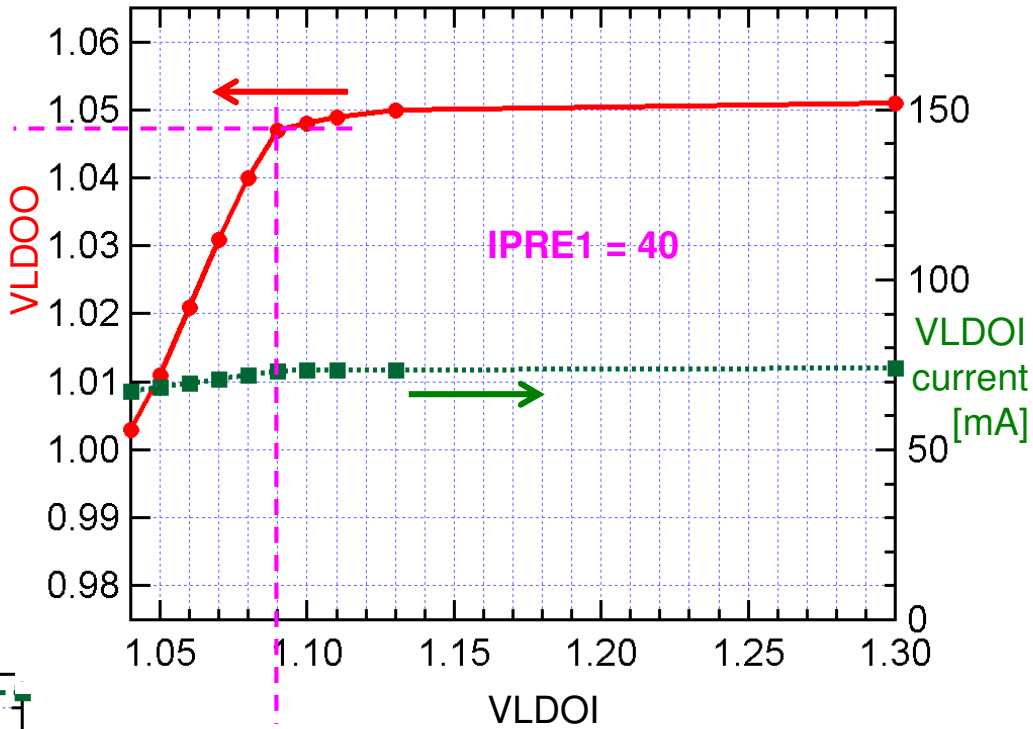
40 MHz generated from fixed sync pattern in fast control data
normal command structure can't be confused with sync pattern

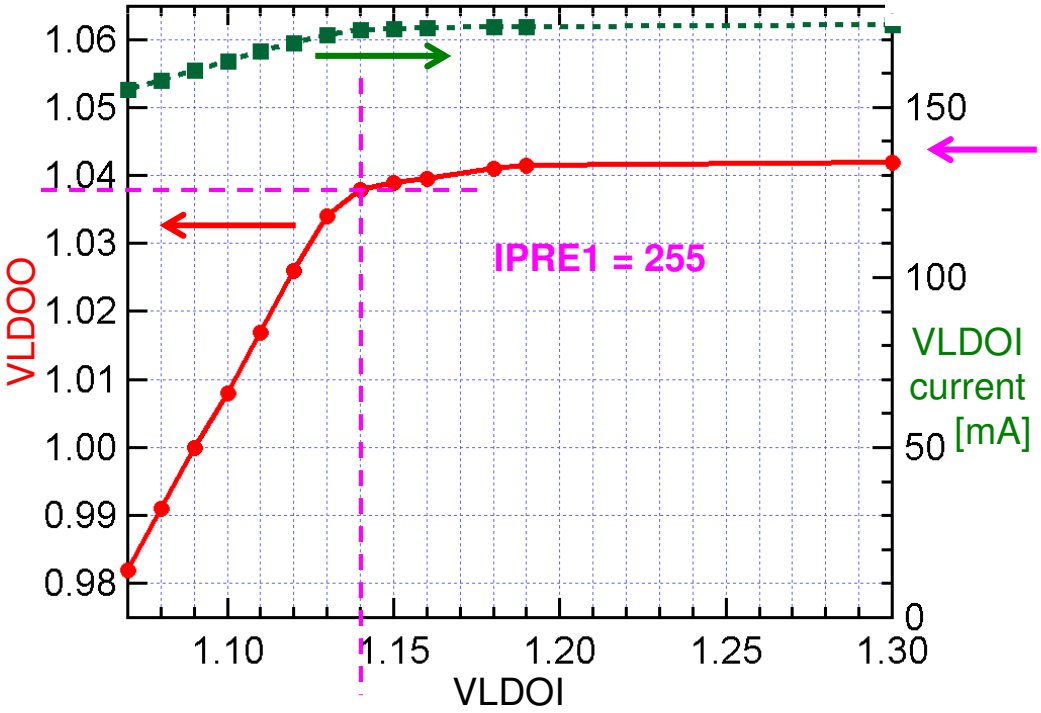
LDO measurements

IPRE1 I2C = 40 (~nominal)
dropout = 1.09 - 1.047 = 43 mV

if VDDA (=VLDOO) set at 1.05 V
then minimum VDDD (=VLDOI) that can be tolerated is

= 1.05 + .043 = 1.093 V





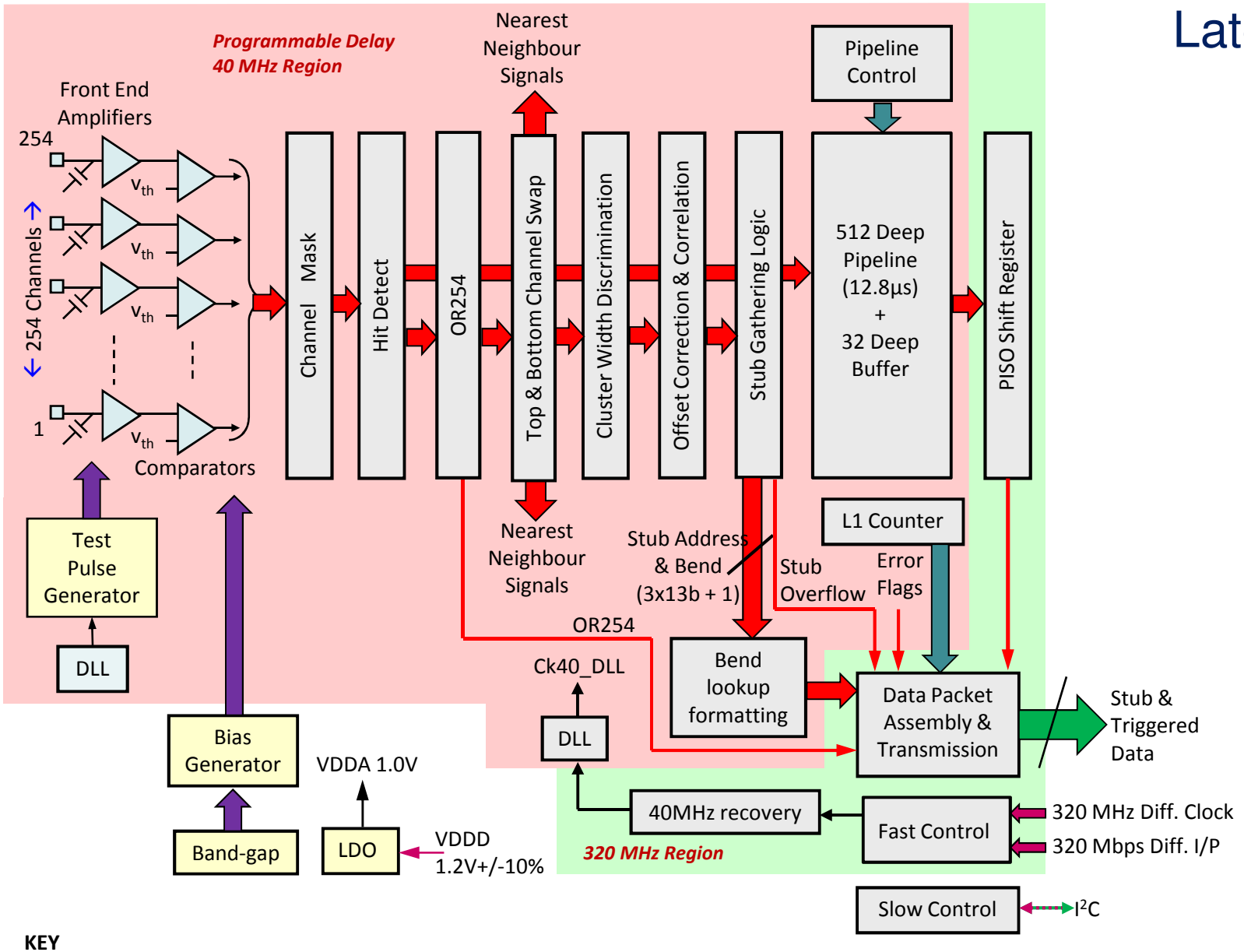
IPRE1 I2C = 255 (maximum)
dropout = 1.14 - 1.038 = 102 mV

if VDDA (=VLDOO) set at 1.05 V
then minimum VDDD (=VLDOI) that can be tolerated is

= 1.05 + .102 = 1.152 V

both results easily compatible with VDDD = 1.25 +/- 0.05

Latest Block Diagram



DLL problem

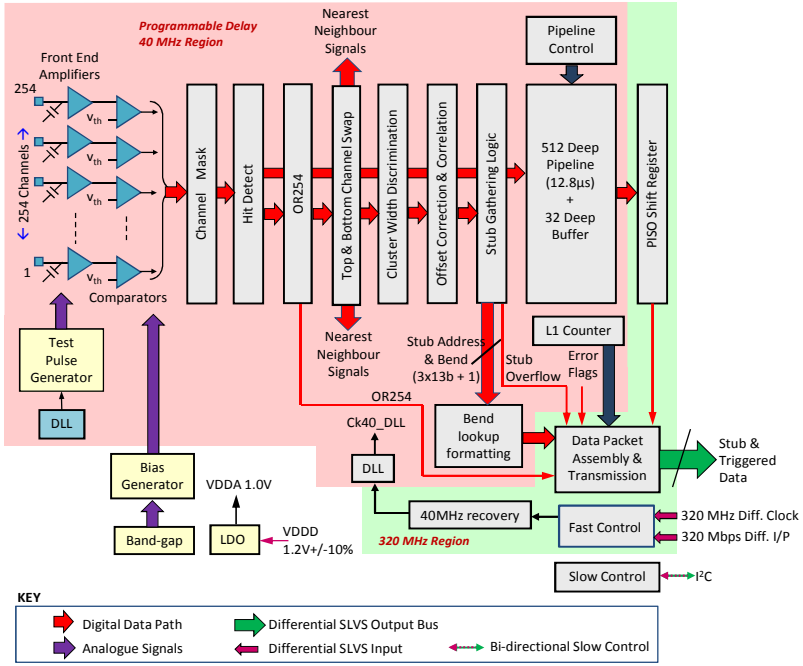
Programmable Delay 40 MHz Region uses Ck40_DLL

programmable in 1 nsec steps

320 MHz Region uses 320 MHz and Ck40_ref (the input to the DLL)

for some values of DLL setting (1 nsec resolution) the L1 data readout logic malfunctions if two (or more) triggers are applied

but only if the trigger spacing is less than 950 nsec



symptoms

frame separation reduces to 925 nsec.

data, including header, from 1st frame is repeated in 2nd frame

multiple frames appear, not corresponding to triggers

.... (not a completely exhaustive list, not all symptoms appear simultaneously)

example

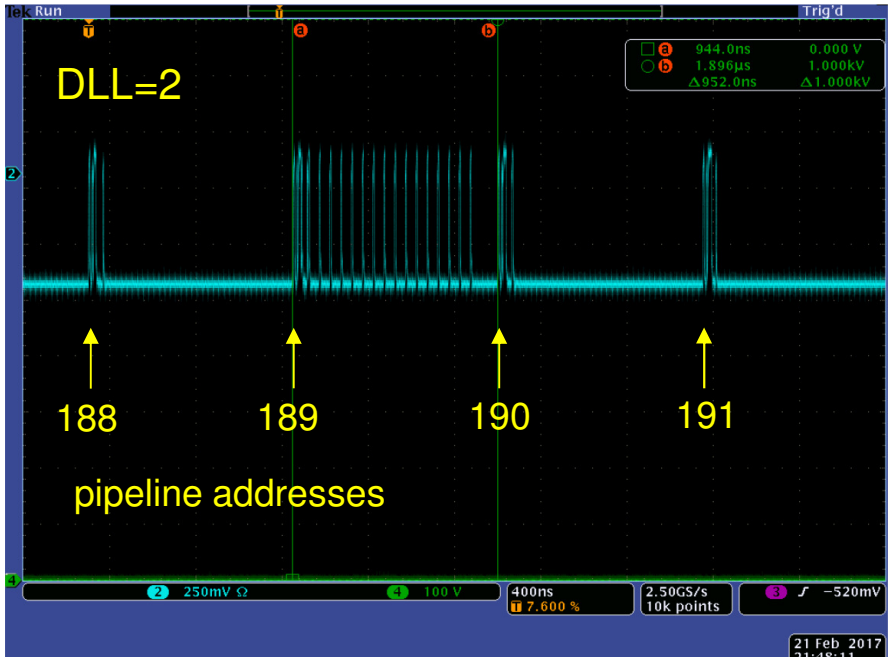
Ck40 DLL setting = 2

4 consecutive triggers sent

test pulse timed to be in 2nd frame

readout data looks ok

header spacing 950 nsec.



Ck40 DLL setting = 3

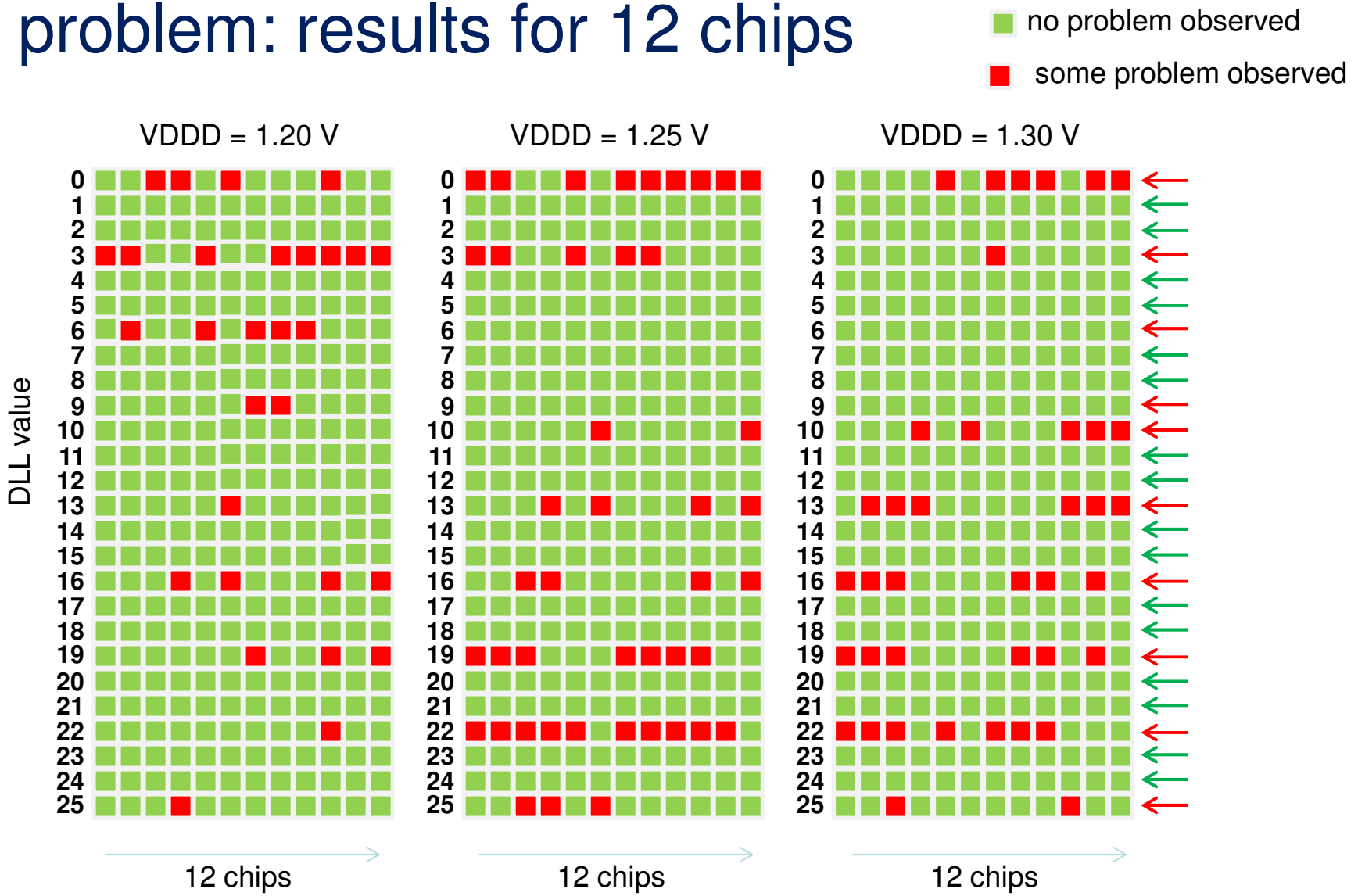
same triggering and test pulse conditions

header spacing reduced to 925 nsec.

2nd frame test pulse data only starts to appear ~ third way through second frame, and spills over into 3rd frame

more detailed look shows header pipe addresses not correct

the problem: results for 12 chips



observations

problem DLL values depend on VDDD, and are not the same for all chips
but appear to always occur at ~3 nsec spacings (probably related to 320 MHz clock)
DLL values in between the 3 nsec problem spacings show no problems