CBC3 testing status summary

Mark Raymond, Outer Tracker Electronics, 17th May, 2017

single chip tests

all CBC3 results so far from wire-bonded single chip setup

chips diced from first wafer

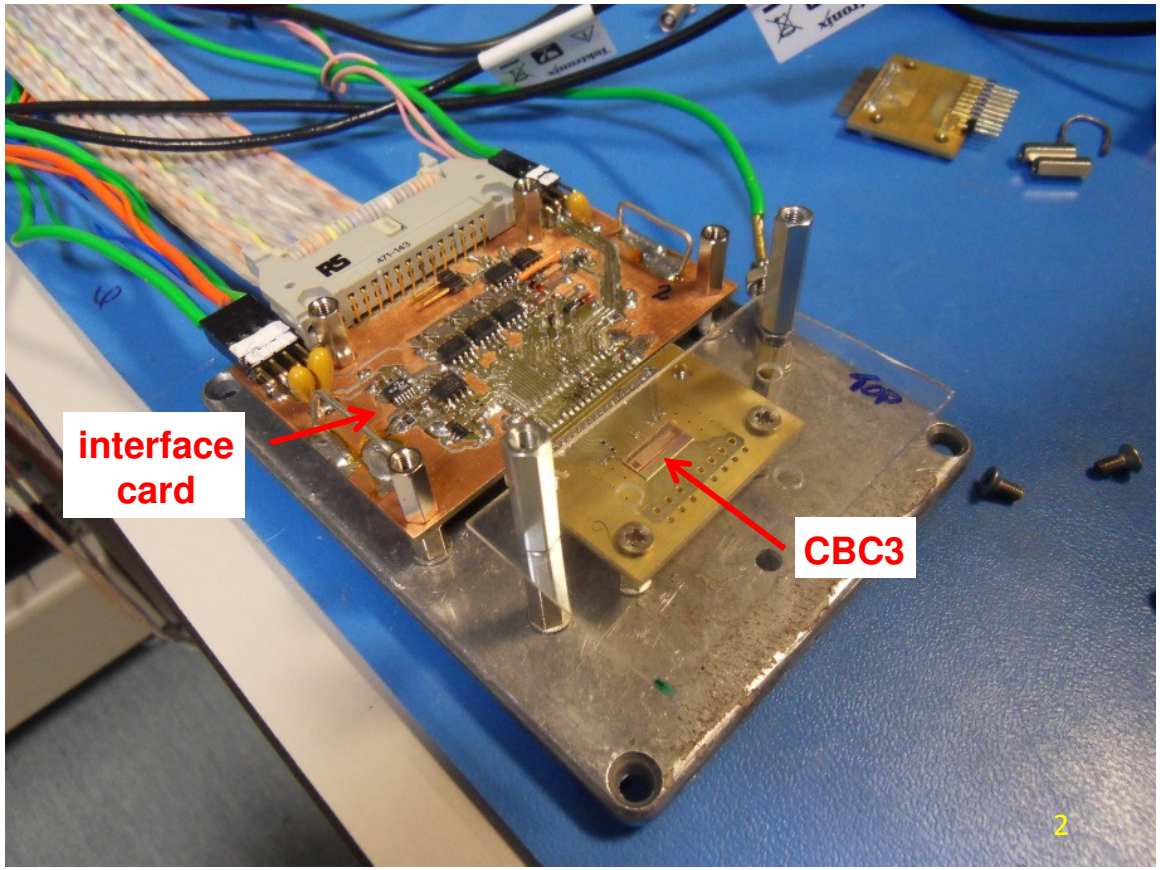
for lab measurements, see:

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2016/CBC3_first_results_Dec_2016.pdf
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_status_March_2017.pdf

same setup used for ionizing and SEU tests (status today)

also used to develop wafer probe tests

wafer probe results summary follows

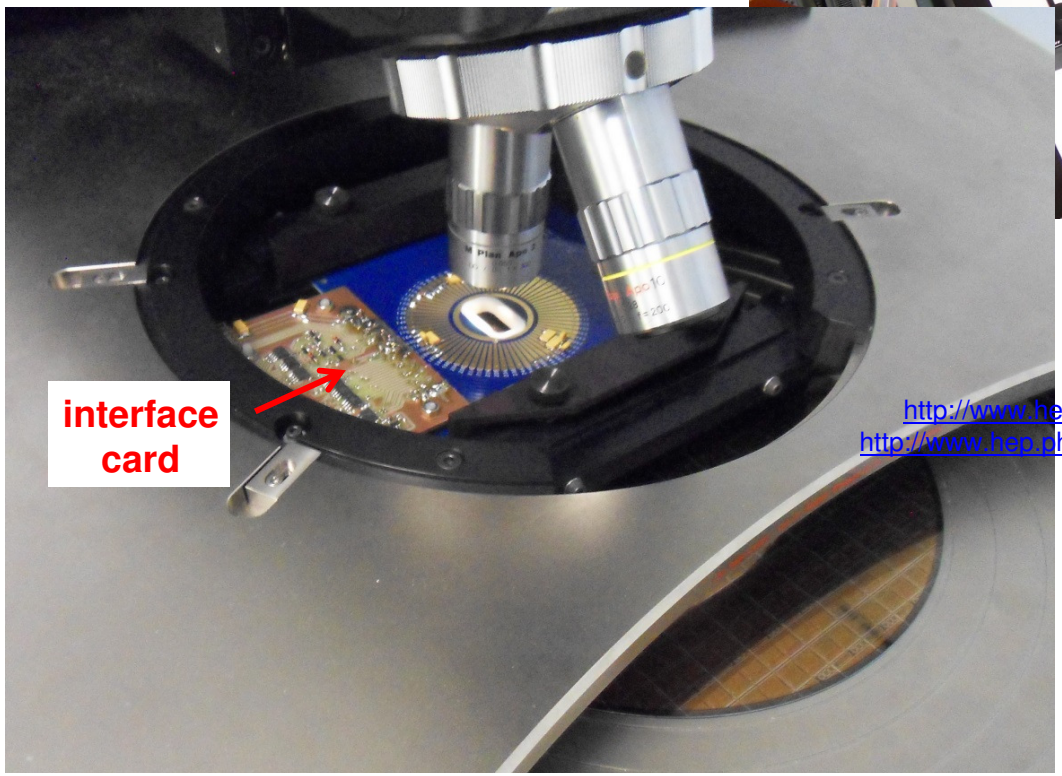


wafer probing

8 CBC3 wafers to be probed
186 chips per wafer

5 tested quickly and despatched beginning April to PacTech for bump-bond processing and subsequent dicing

3 remain at Imperial - also now tested



will summarise probe test results briefly here - for more details see:

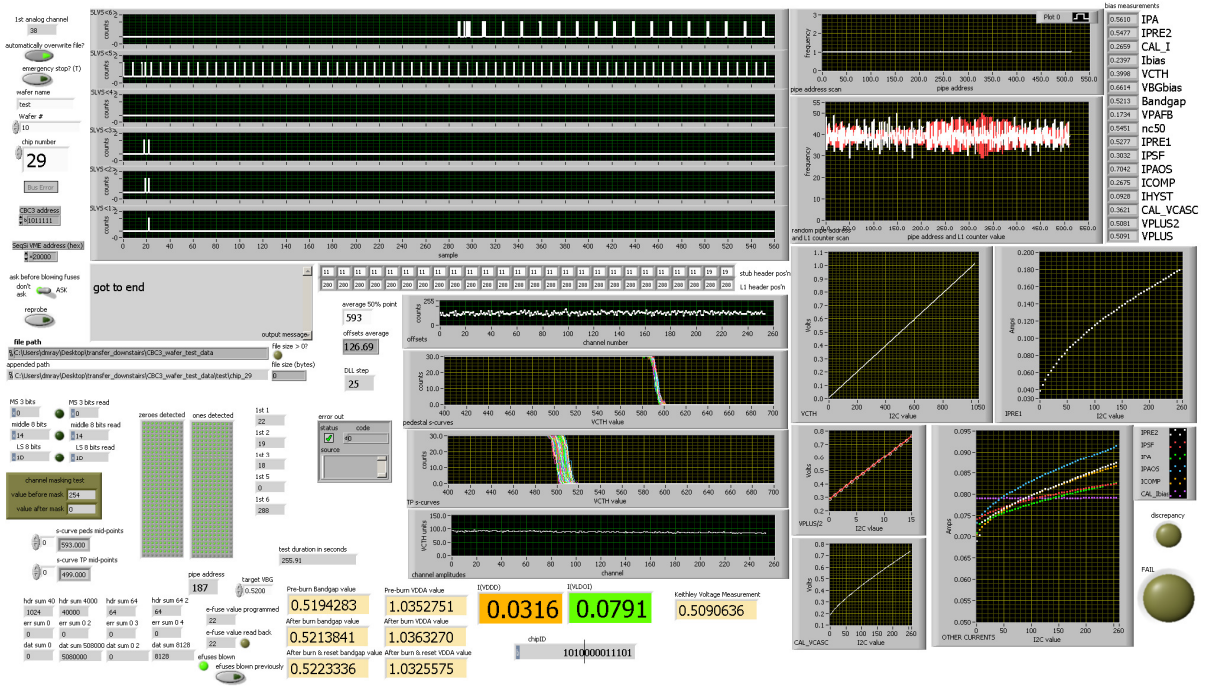
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2017/CBC3_status_Feb_2017.pdf
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2017/CBC3_wafertest_April_2017.pdf

wafer probe tests

all tests run at full speed (320 MHz)

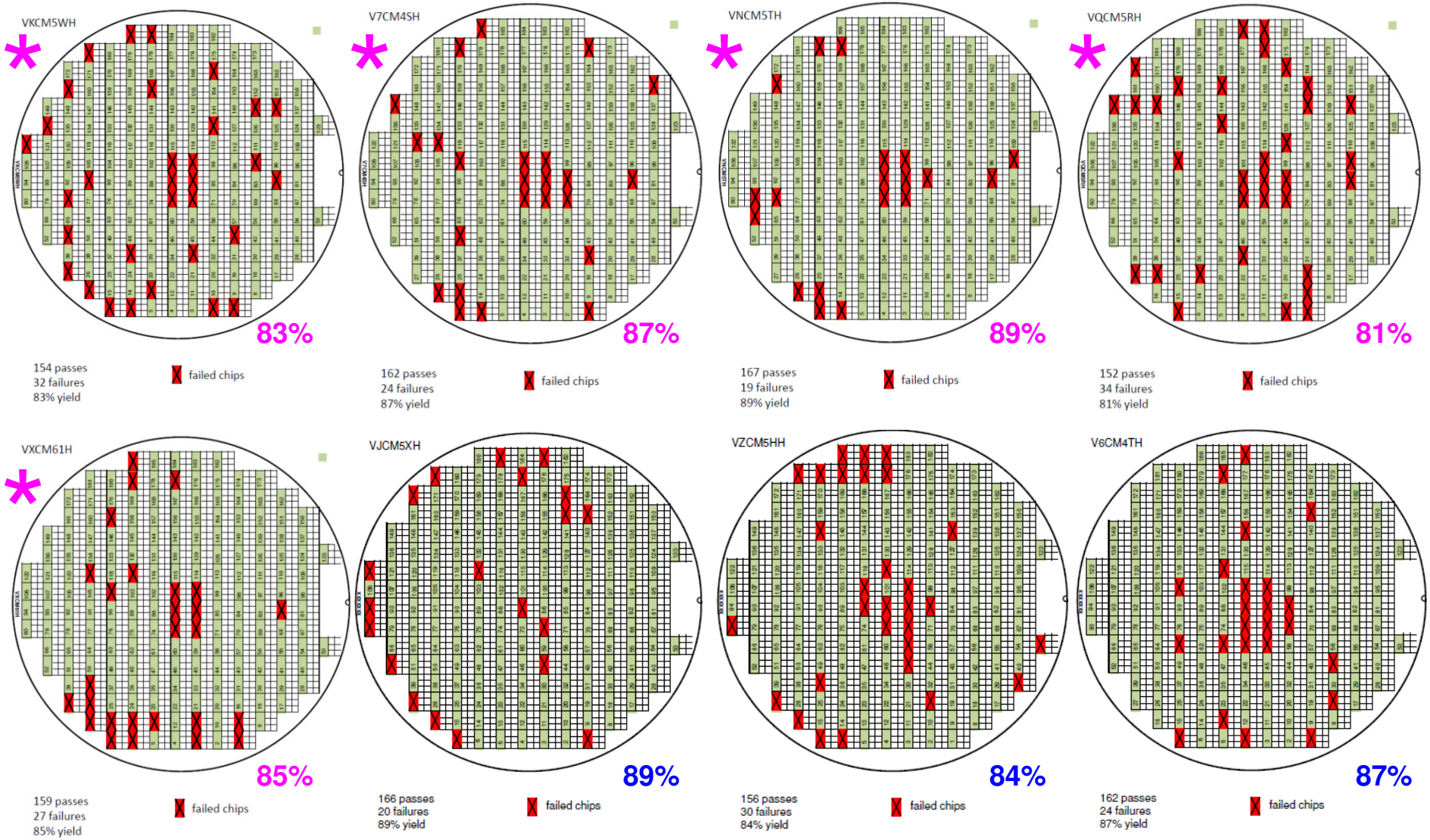
categorize failures as:

- I2C failure
  - no response
  - stuck bits in registers
- power
  - excessive current draw
- pipeline
  - any stuck bits
- stub logic
  - wrong address or bend info returned
- channel
  - high/low or non-uniform gain (one or more channels)
  - large spread on offsets after tuning
- other
  - DLL, physical damage noticed, file not written, ….



← chip failed immediately if any test failed up to here

results



* 5 wafers to PacTech for bump-bond processing

high average yield ~85%
some common failure patterns

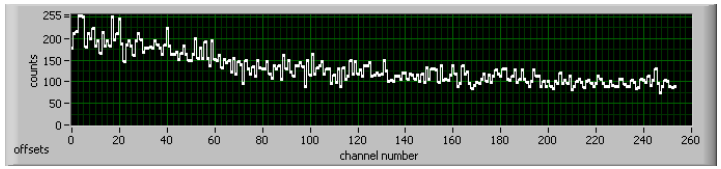
wafer probe failure summary

	VQCM5RH	VKCM5WH	VXCM61H	V7CM4SH	VNCM5TH	VJCM5XH	VZCM5HH	V6CM4TH
yield [%]	81	83	85	87	89	89	84	87
I2C failure	0	5	5	0	2	0	3	1
power	0	0	3	0	0	3	0	1
pipeline	5	4	0	0	3	1	2	1
stub logic	1	1	2	1	0	3	0	2
channel	20	18	14	19	14	8	13	18
other	8	3	2	4	1	7	12	1

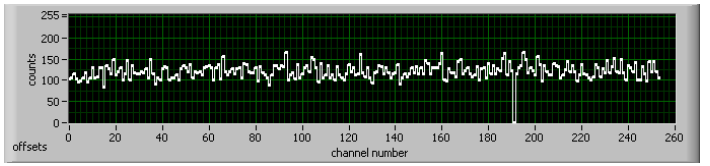
wafers to PacTech

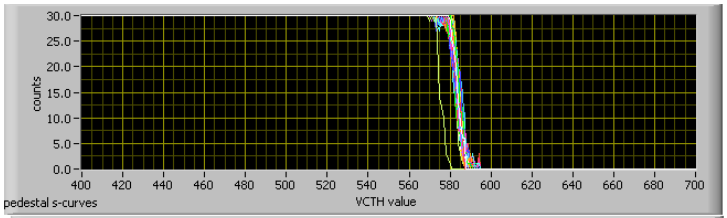
some chips fail in more than one category - first to occur is one listed in table
channel failure is largest category - some examples on next slide
channel failure if any channel shows gain > +/- 10% from the mean
or large offsets spread after tuning
most (~all) of failures in centre of wafers are channel failures

types of channel failure

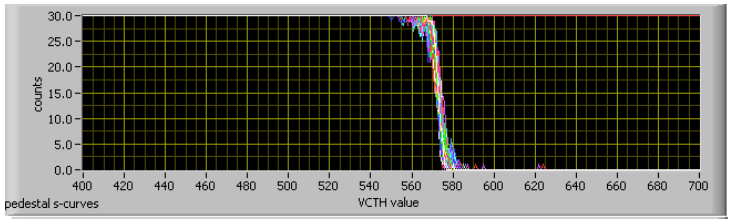


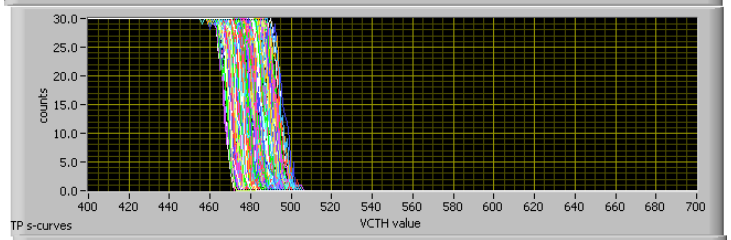
offset values after tuning



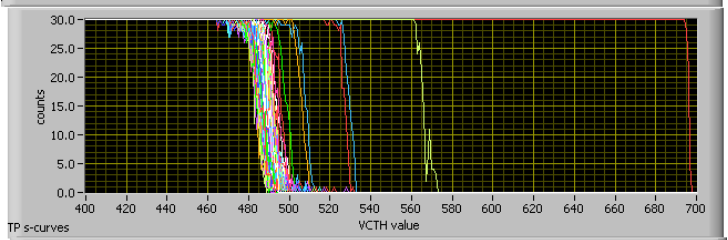


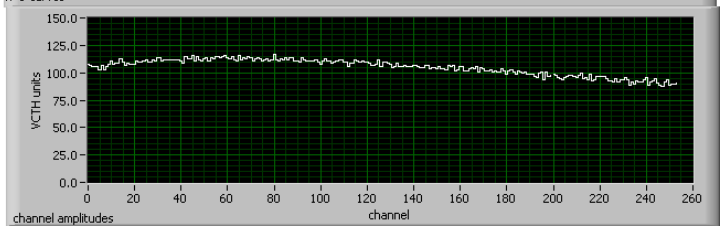
pedestal s-curves



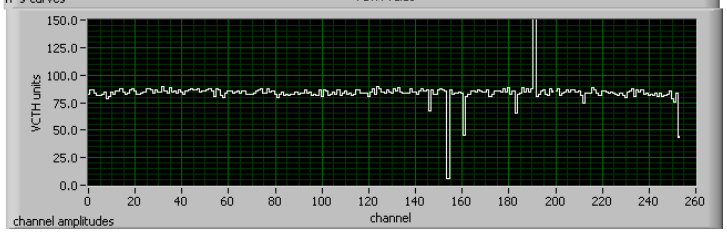


test pulse s-curves





test pulse - peds (= gain)



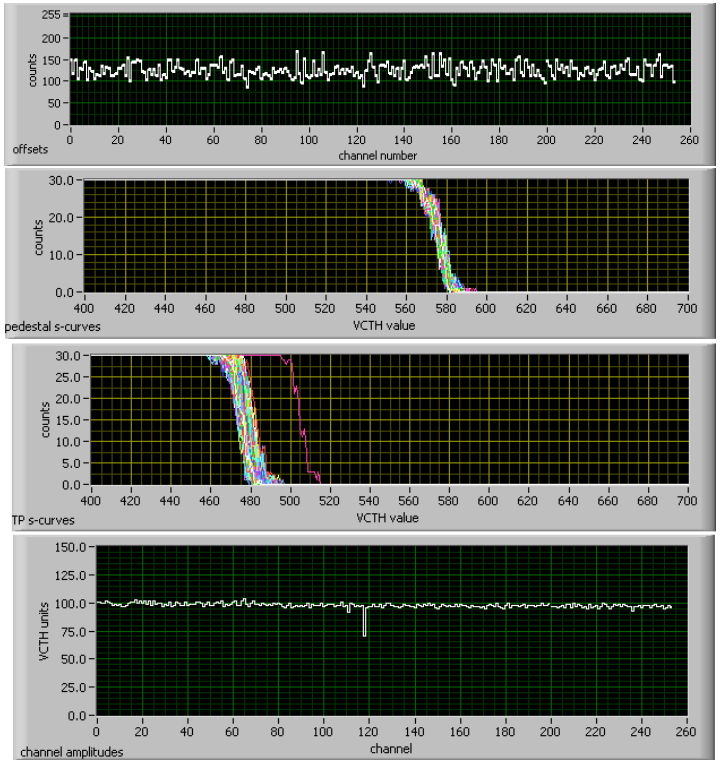
this chip shows an obvious trend across the chip in the gain picture, and also in the offsets after tuning

this problem more often observed on chips at the edge of the wafer

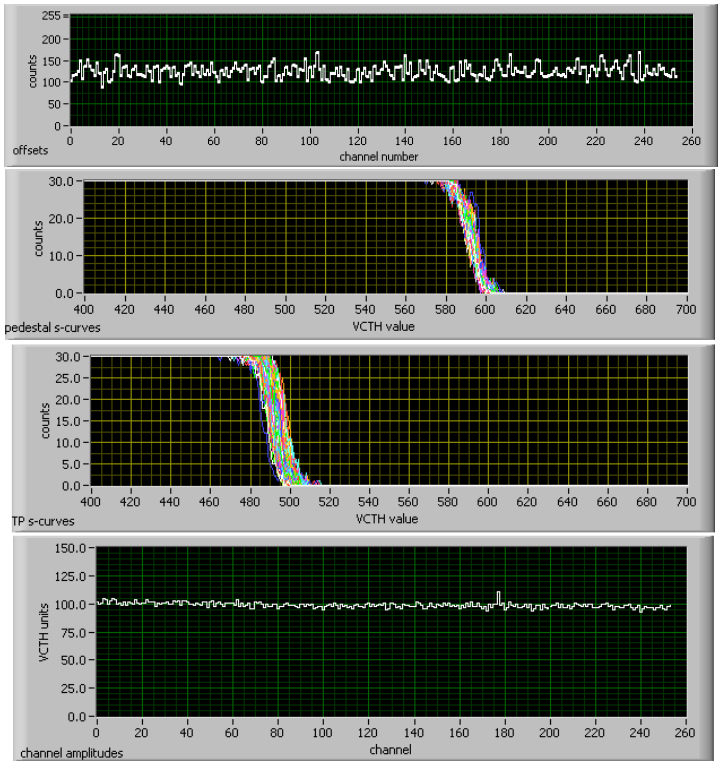
this chip shows a problem on several channels

problem typical of chip in centre of wafer

more types of channel failure



single channel with low gain



single channel with slightly high gain
but still a failure

summary

5 CBC3 wafers probed and now with bumping company

ability to probe wafers at full speed now confirmed

looking forward to bump-bonded chips on hybrids in the summer

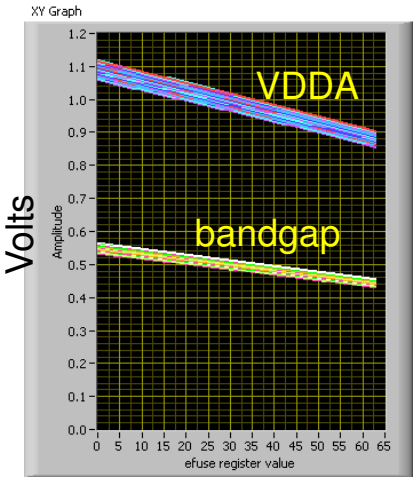
8 wafers probed altogether

average yield ~ 85% (high) but noticeable pattern of failures in centre of wafers

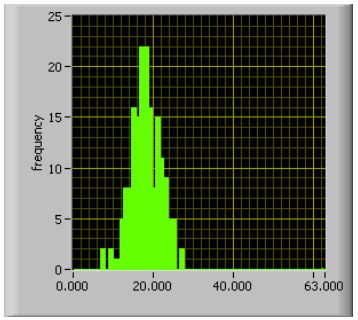
test data is retained, so individual chip ID will allow to check whether any performance issue observed on hybrid correlates with anything observed at wafer test time

extra

post test data analysis examples



e-fuse reg. value

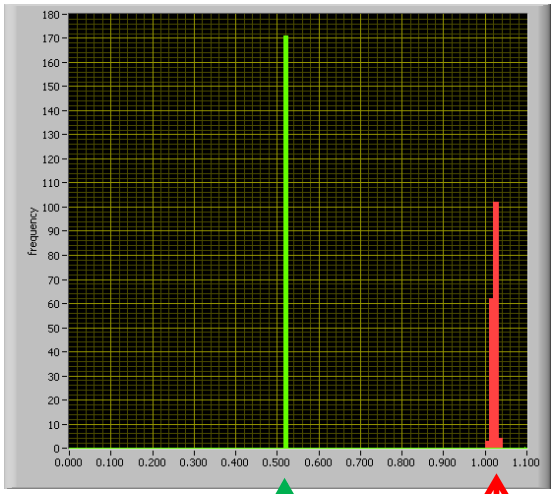


e-fuse reg. value after tuning

efuse register programmed (during test) to tune bandgap to desired value, and fuses blown

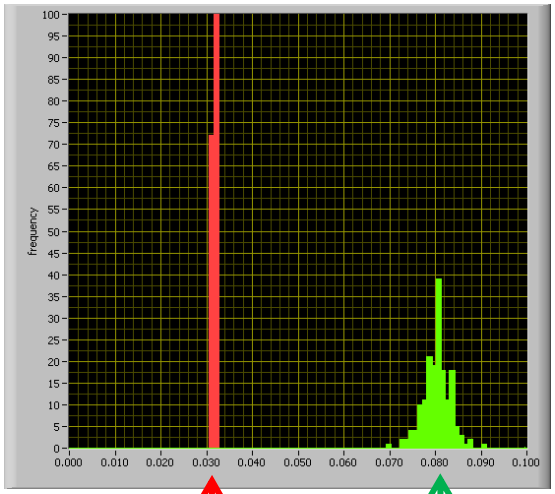
(chip ID efuses blown at same time)

voltages and currents can be histogrammed for all chips and outliers rejected



bandgap after tuning

VDDA after tuning



VDDD current

LDO input (VDDA) current

e-fuses

unique chip ID set by 19 bits:
- 10 bits wafer ID
- 9 bits chip position on wafer

CBC3 wafer numbers 1 -> 8
chips 1 -> 186

test results file kept for each chip

=> can check whether correct chips have been used, and if any anomalous behaviour on hybrid can be correlated with performance at probe test time

efuses also used to set bandgap voltage on chip