CBC3 design status

CMS Tracker Week, Phase 2 Electronics, 28th January, 2016

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introduction

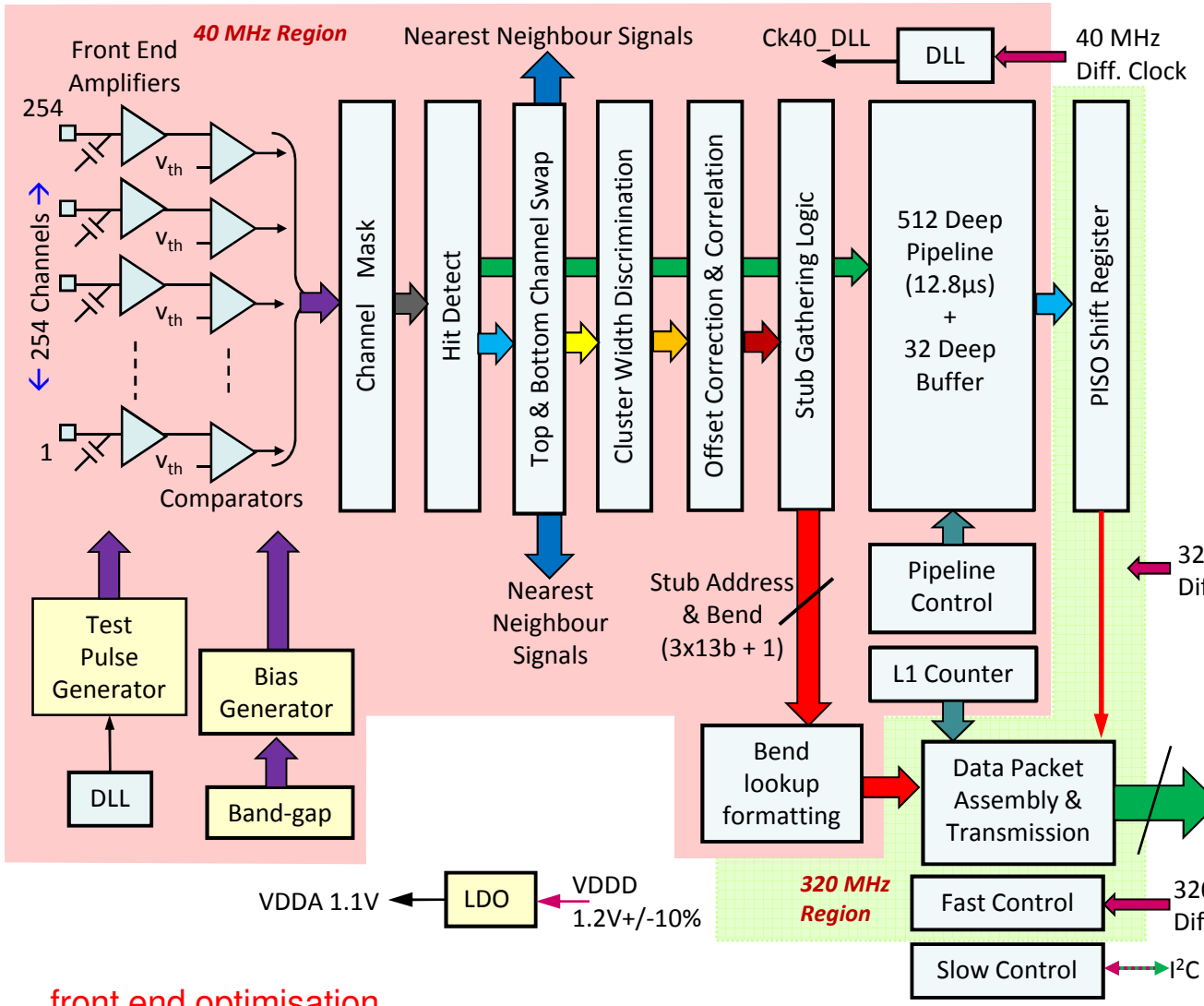
previous talks

- May 2016 tracker week: CBC3 specifications
  - http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_elec_CBC3specs_May_2015.pdf
- November 2016 tracker upgrade week: CBC3 design progress
  - http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3progress_Nov_2015.pdf

today

- brief reminder of CBC3 features
- progress update
  - threshold issues
- schedule

CBC2 -> CBC3



system issues addressed

- synchronization & timing
- data formats
- electrical standards
- powering

longer pipeline - 12.8 usec

higher L1 trigger rate capability: ~1 MHz

stub data transmission off-chip: address & bend info for up to 3 stubs

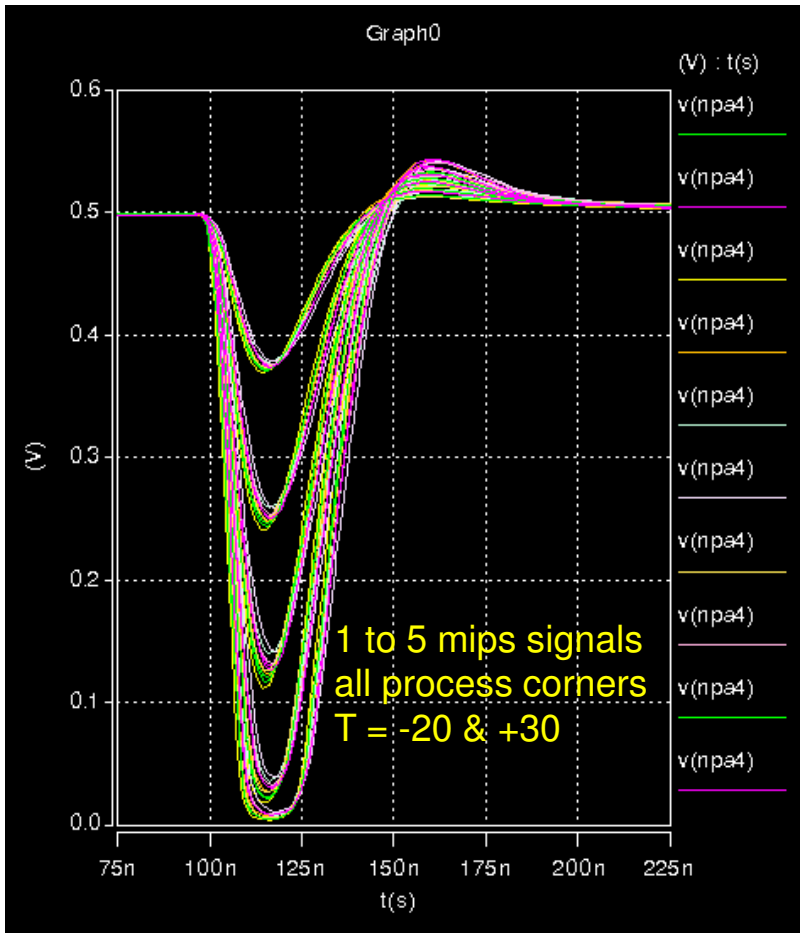
front end optimisation

shorter pulse shape, bug fixes, improved comparator threshold res'n, …

½ strip resolution for cluster width discrimination and correlation logic

CBC3 front end simulated performance

front end amplifier pulse shape

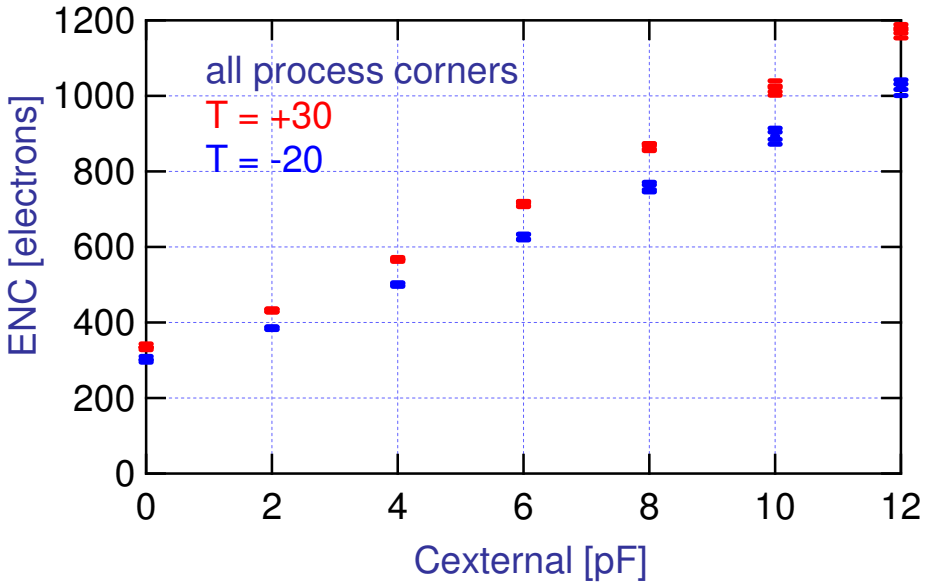


pulse shape width < ~50nsec

=> no dead time due to pile-up

robust to full range of simulation conditions

NOISE dependence on external capacitance



< 1000e achievable for Cexternal < 10pF

CBC3 digital interfaces

output data: up to 3 stubs data transmitted to CIC/BX
- 5 diff pairs @ 320 Mbps
- 8 bit stub seed address (1/2 strip resolution)
- 4 bit bend info (location of cluster in window layer)

up to 1 MHz L1 triggering capability
- 1 diff pair @ 320 Mbps
- readout data frame < 1 usec

single 320 Mbps fast control line

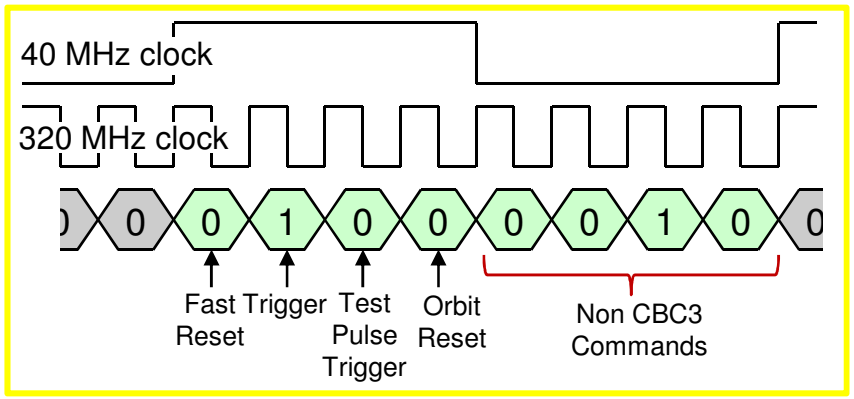
output data

25 ns

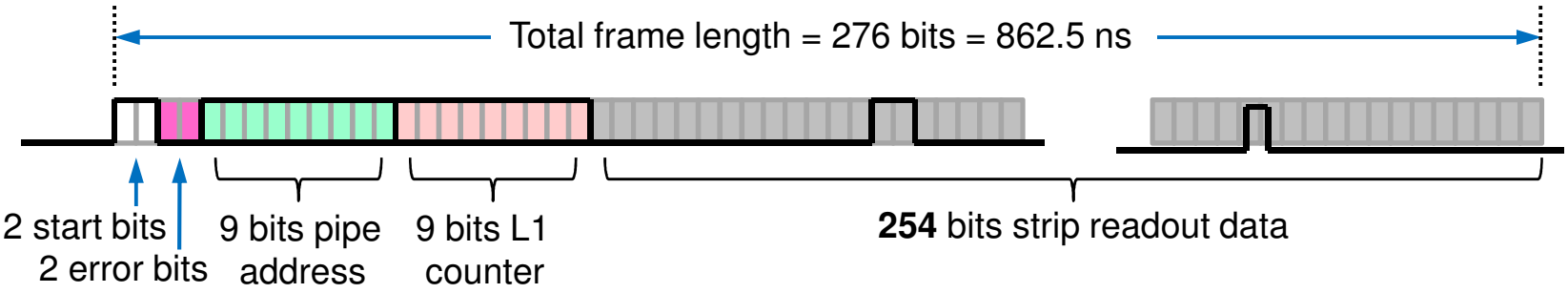
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	R
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	R
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	R
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	R
S1<4>	S2<4>	S3<4>	B2<0>	SoF	R
S1<5>	S2<5>	S3<5>	B2<1>	OR254	R
S1<6>	S2<6>	S3<6>	B2<2>	Error	R
S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	R

R = L1 triggered readout data
time flow top to bottom (e.g. S1<0> output first)

fast control



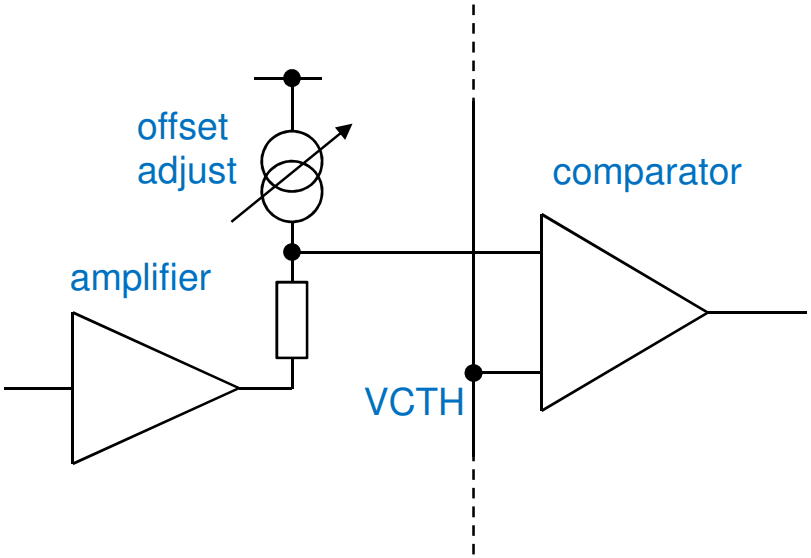
readout data frame



thresholds and offsets

I2C parameter VCTH programs comparator
global threshold (global = same for all channels)

8-bit offset adjustment at individual channel level

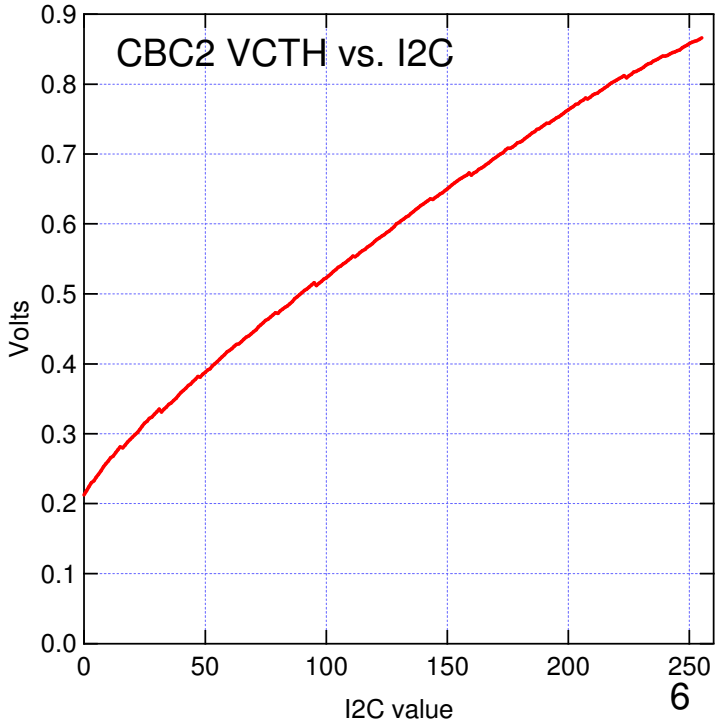


VCTH for CBC2 generated by mirroring adjustable current (8-bit res'n) into a resistor

not v. linear, and not monotonic

VCTH sweeps important diagnostic tool in binary system
used to measure efficiency, and noise

=> improve resolution and linearity for CBC3

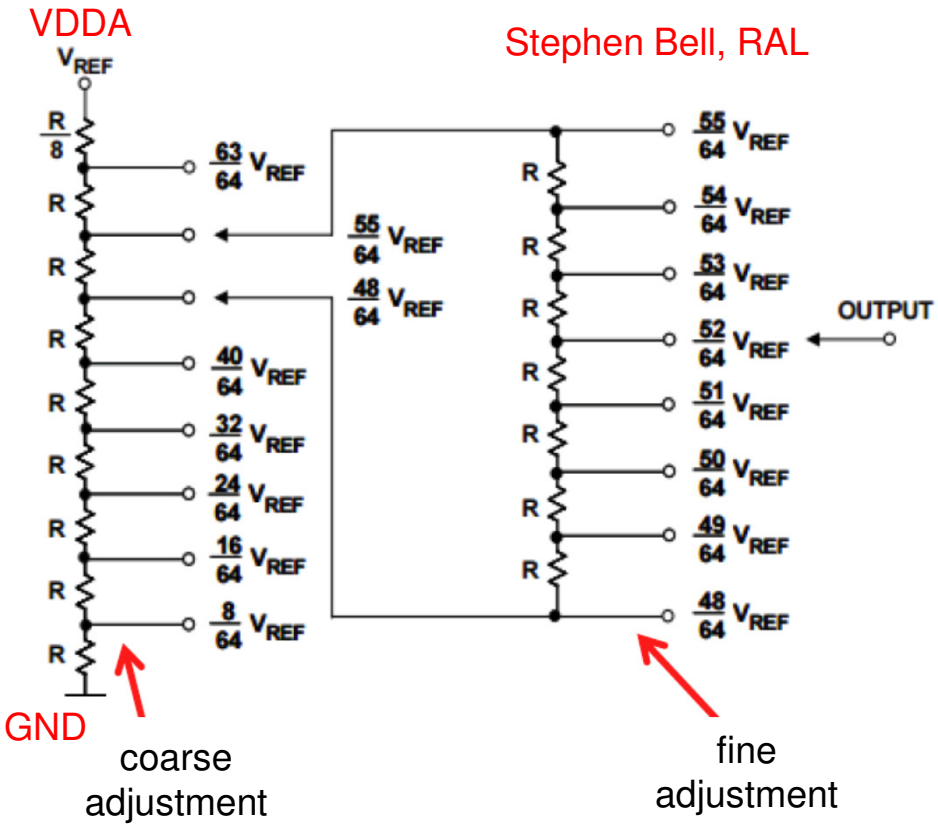


VCTH DAC for CBC3

VCTH in CBC3 implemented by
segmented resistor ladder DAC architecture
~108 resistors -> **10-bit** res'n

INL & DNL < 0.4 lsb
achieved for all simulation corners

=> global threshold res'n ~ **140e**

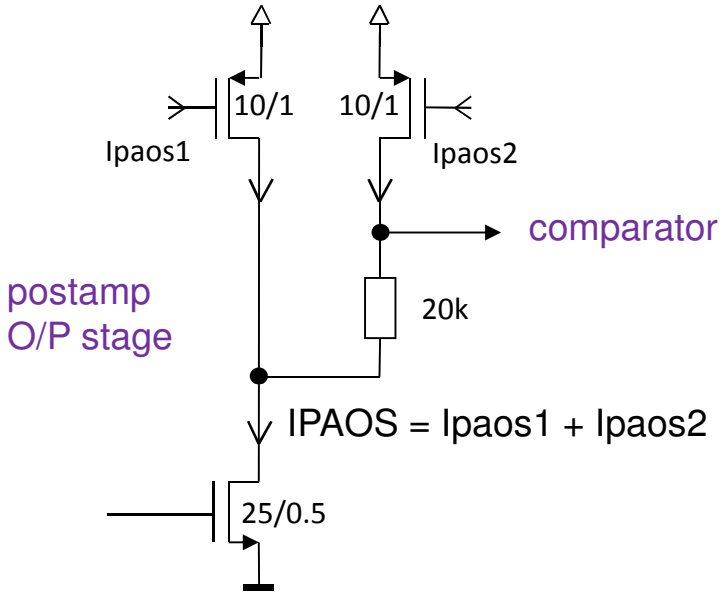


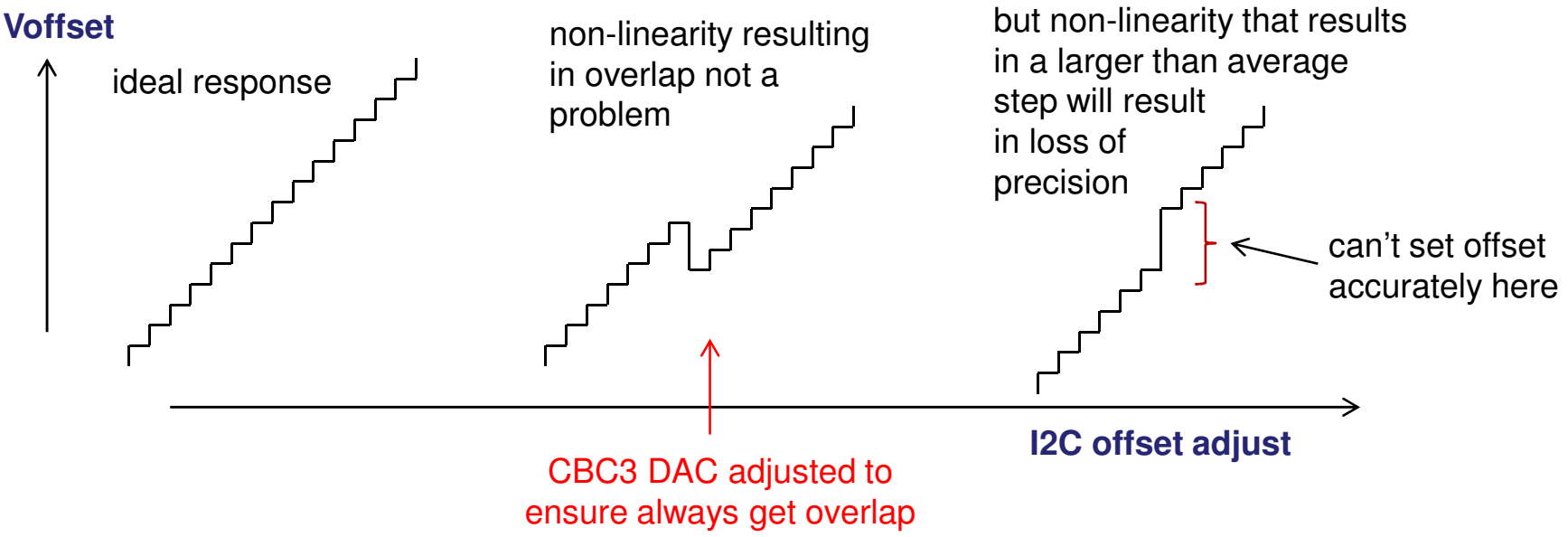
offsets tuning linearity

DC shift at postamp output (comp. I/P) produced by Ipaos2 current in 20k resistor

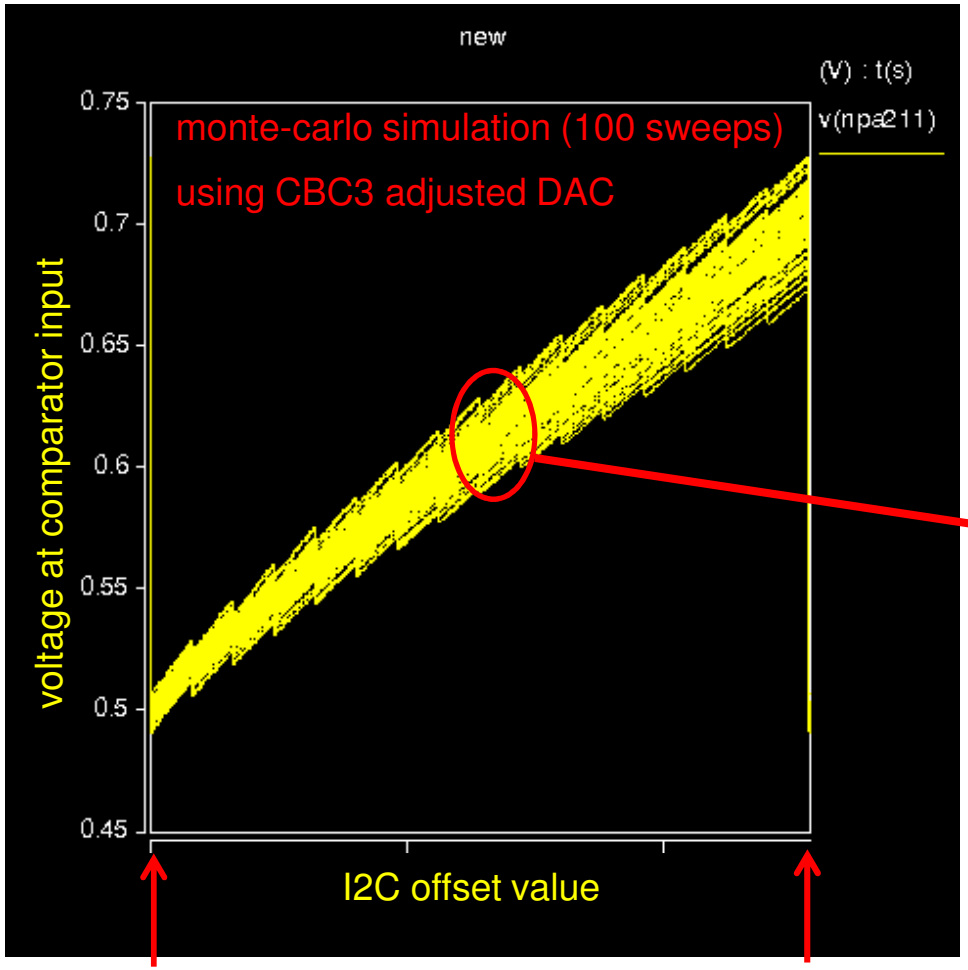
individual channel offsets adjust achieved by varying ratio of Ipaos1:Ipaos2 (total current IPAOS = constant)

8-bit adjustment for nominal Ipaos = 10uA
gives 0.8mV /bit offset adjustment precision **(~100e**)
(for ideal DAC functionality)



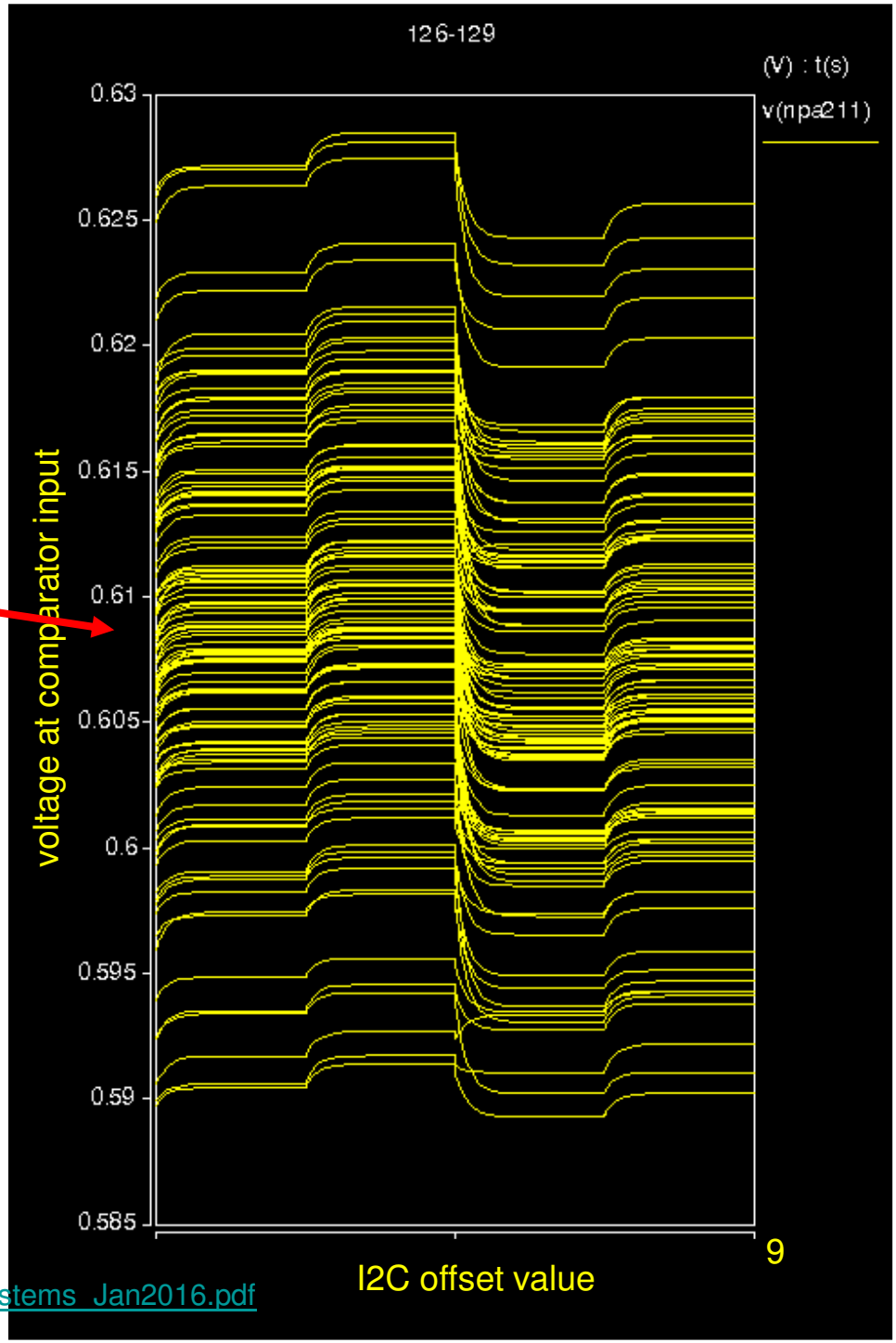


CBC3 non-linearity - but overlap



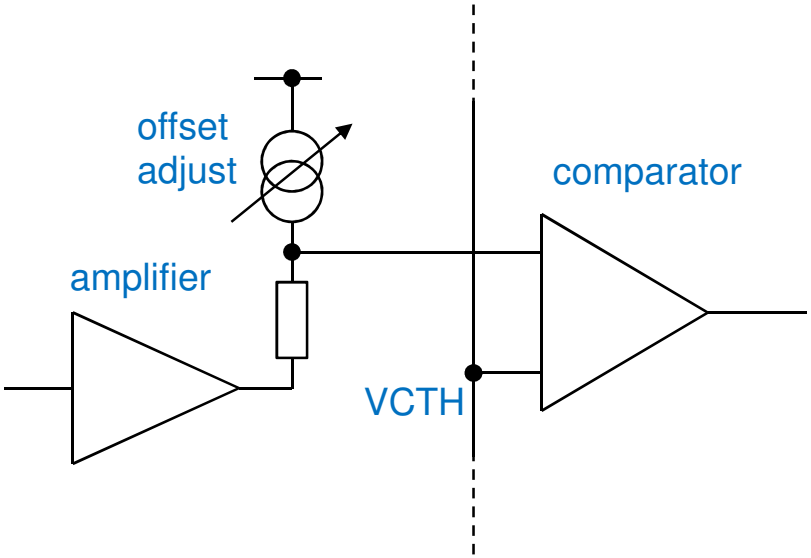
no current in
level shift resistor

maximum current in
level shift resistor



for more details see:
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2016/CBC3_systems_Jan2016.pdf

threshold & offsets tuning summary



global comparator threshold VCTH

10-bit resolution
linear: DNL (&INL) < 0.4 lsb
lsb ~ 140e

individual channel offset adjust (254 registers)

8-bit resolution
lsb ~ 100e

new tuning method + 1 MHz I2C -> offsets for complete chip tuned in ~ few seconds

see Kirika Uchida talk at 19/1/16 Electronics for 2S and PS-Pt modules meeting
https://indico.cern.ch/event/483130/session/1/contribution/35/attachments/1213273/1770477/20160119CBC.pdf

only these user adjustments should be required for CBC3 setup

front end simulations indicate all other I2C parameters can be fixed

(e.g. no pulse shape tuning required like for APV)

schedule

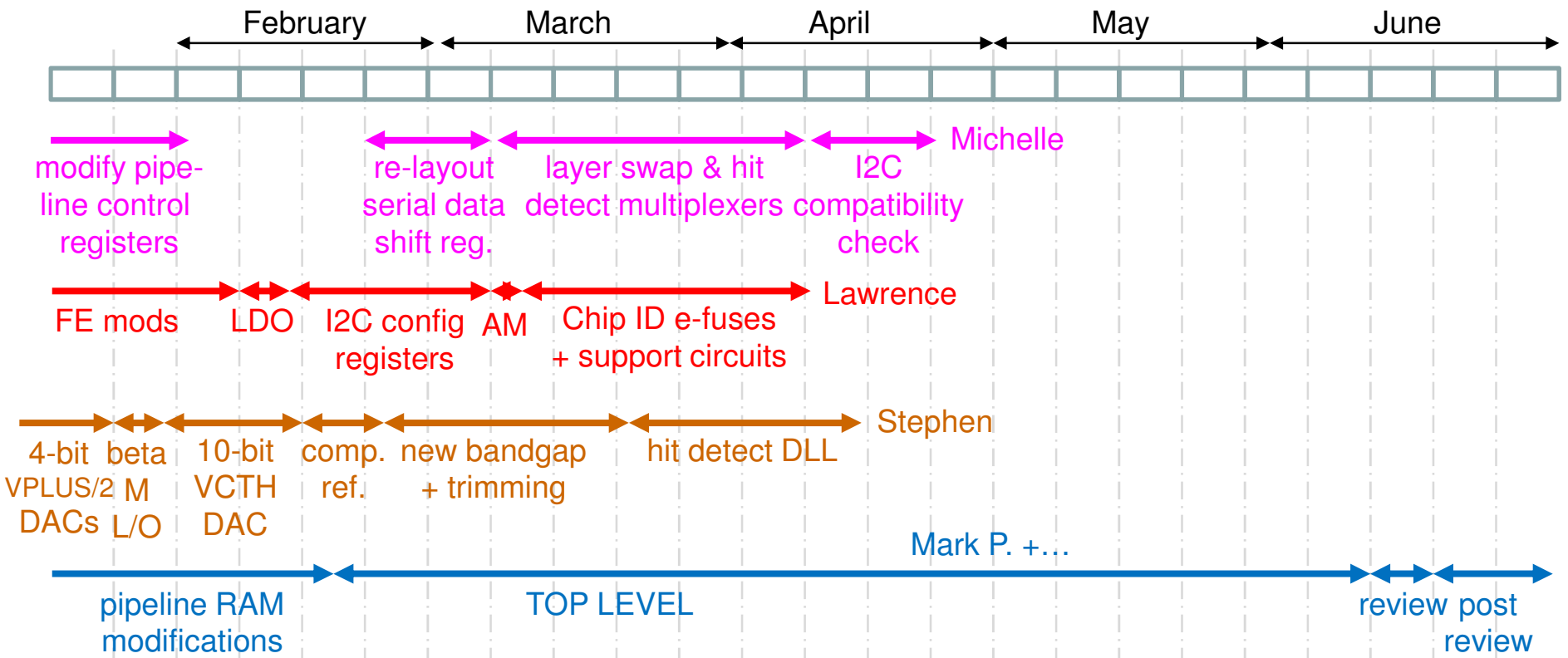
- original plan predicted ready for submission Q1 2016
- have suffered from staff loss at RAL (late 2015)

  Lawrence Jones and Stephen Bell now allocated to CBC3
- project schedule to completion has now been revised (Mark Prydderch)

  including a few previously unforeseen additions to the design

  (new bandgap+trimming, e-fuses, FE mods a bit more extensive than expected,..)

schedule



all design blocks complete by ~mid April
but TOP level work takes till June
(assembly of complete chip, connecting up, checking,..)
can probably provide information needed for reticle assembly earlier

final remarks

no major design left on CBC3, but still some work to do

some delay, but should be ready for submission ~ middle of year

still hoping to share wafer with GBT-SCA

new version (1.2) of CBC3 specification document available

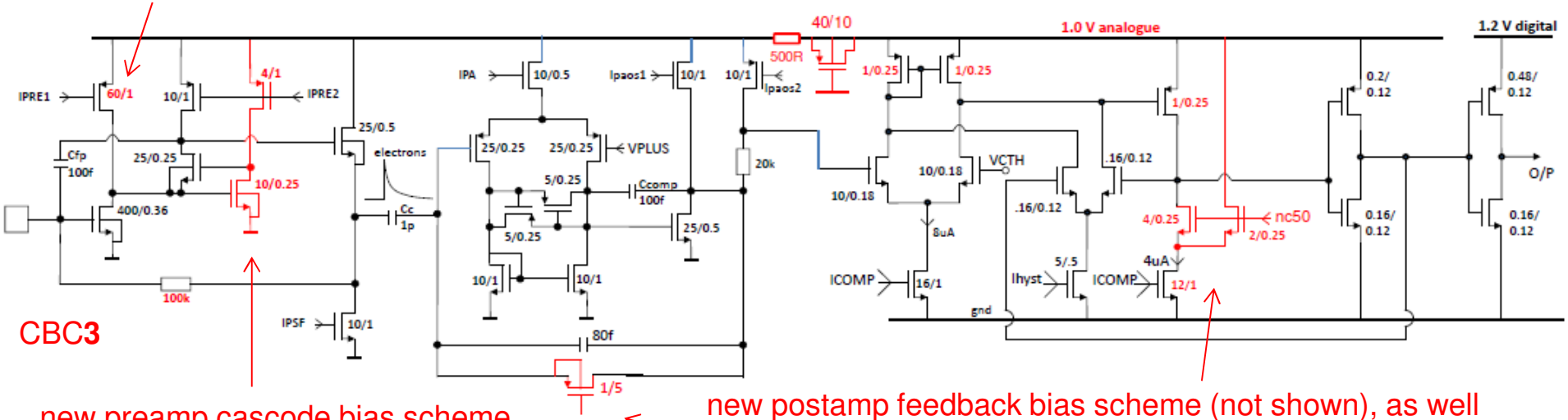
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p2.docx

(mostly corrections, clarifications and updates suggested by Francois)

extra

CBC2 vs. CBC3

increase in bias FET
allows higher currents

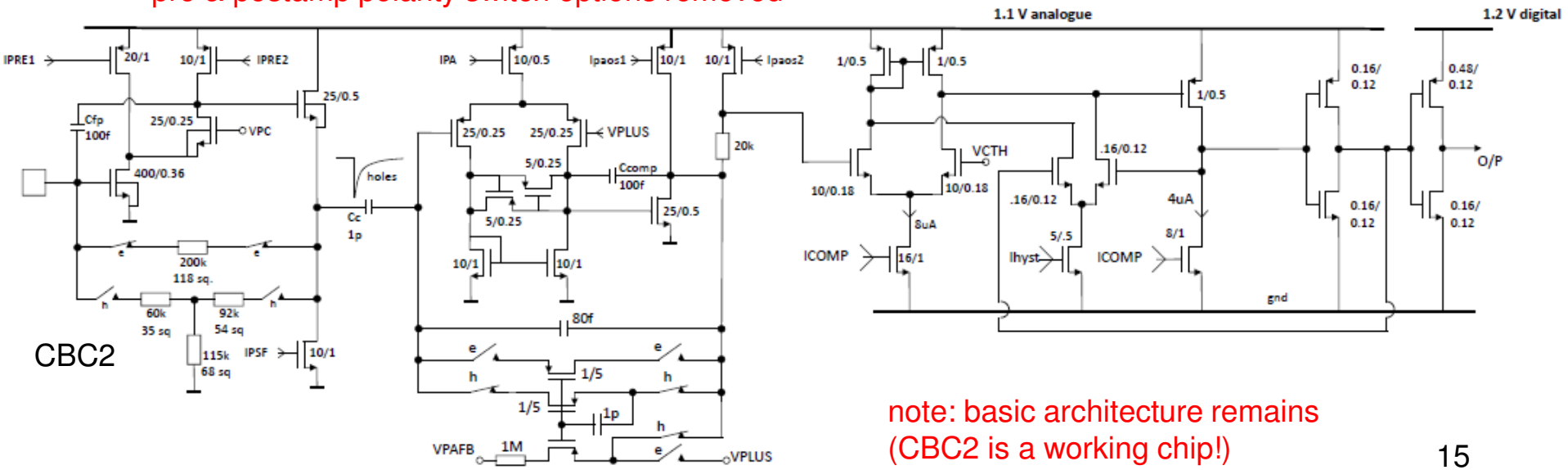


CBC3

new preamp cascode bias scheme
to eliminate “shadow effect”

new postamp feedback bias scheme (not shown), as well as current neutral comparator, addresses CM effects observed when many channels fire

pre & postamp polarity switch options removed



CBC2

note: basic architecture remains
(CBC2 is a working chip!)