CBC3 progress

Tracker Week, Phase 2 Electronics, 21st July, 2016

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introduction

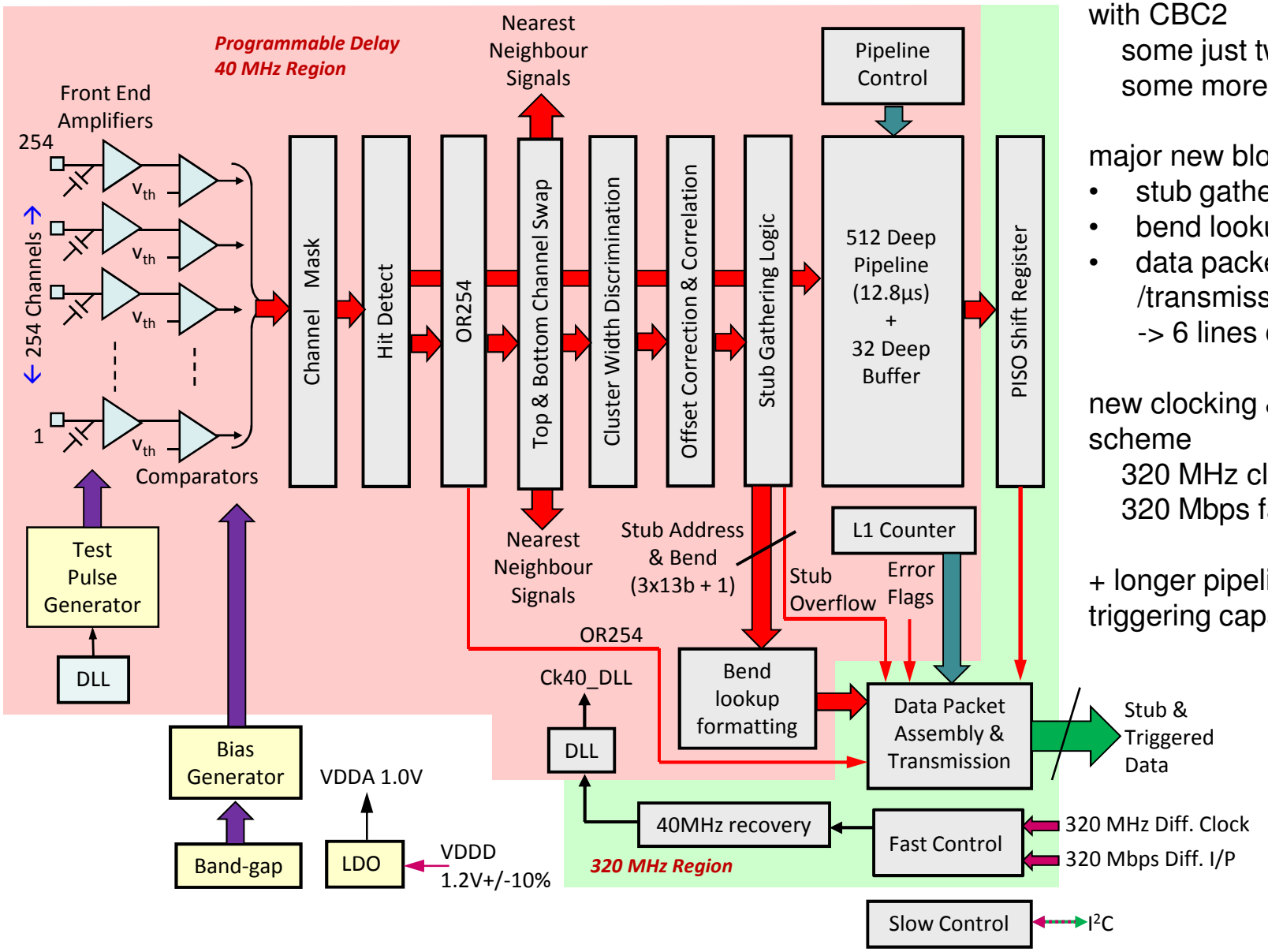
previous talks

May 2015 tracker week: CBC3 specifications
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_elec_CBC3specs_May_2015.pdf
November 2015 tracker upgrade week: CBC3 design progress
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3progress_Nov_2015.pdf
January 2016 tracker week: CBC3 design progress
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3progress_Jan_2016.pdf
May 2016 tracker phase 2 upgrade week week: CBC3 design progress
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3progress_May_2016.pdf

today

the chip is “finished”
summary of features & post-layout performance
preliminary thoughts on testing & test schedule

CBC3 block diagram



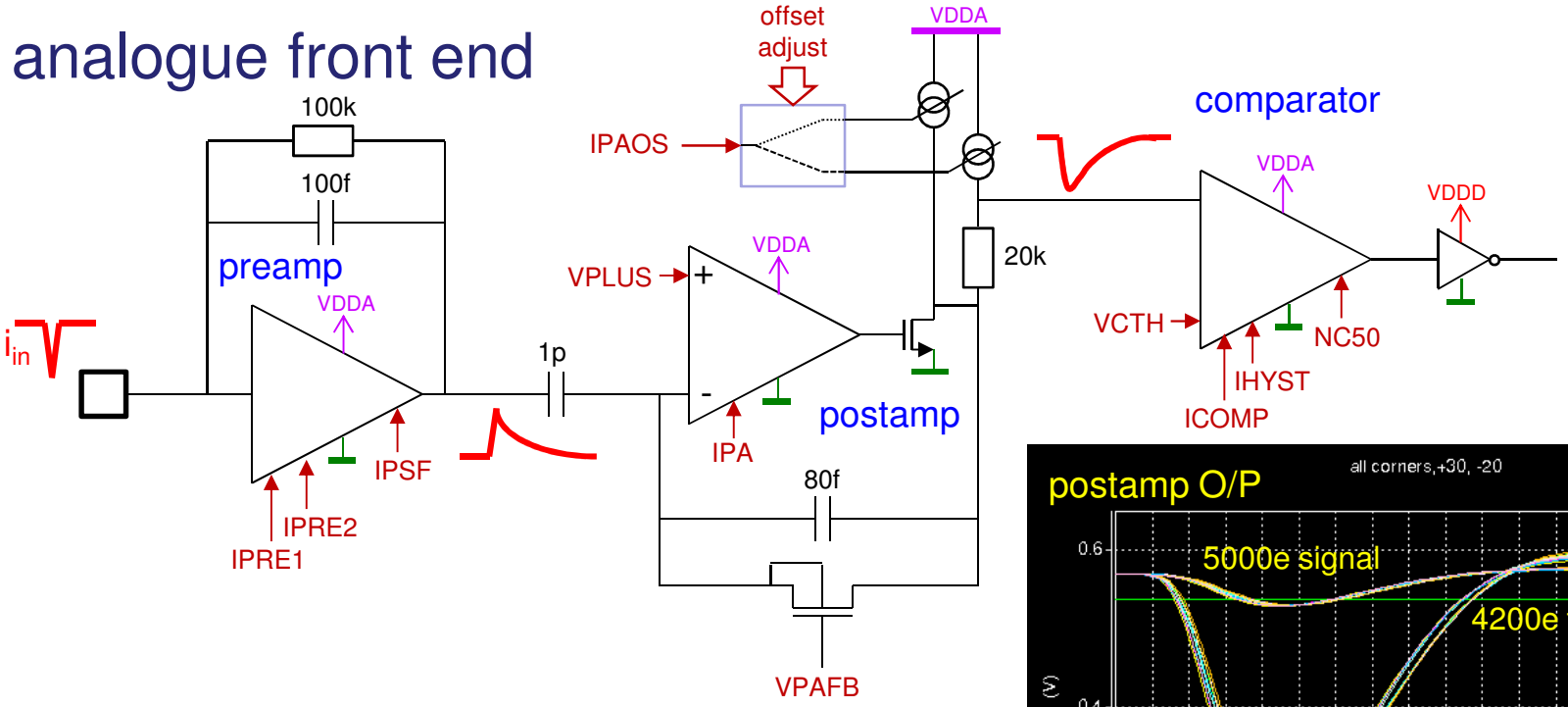
many changes compared with CBC2
- some just tweaks
- some more significant

major new blocks
- stub gathering logic
- bend lookup
- data packet assembly /transmission
  -> 6 lines @ 320 Mbps

new clocking & signalling scheme
- 320 MHz clock
- 320 Mbps fast control

+ longer pipeline, 1 MHz triggering capability, ….

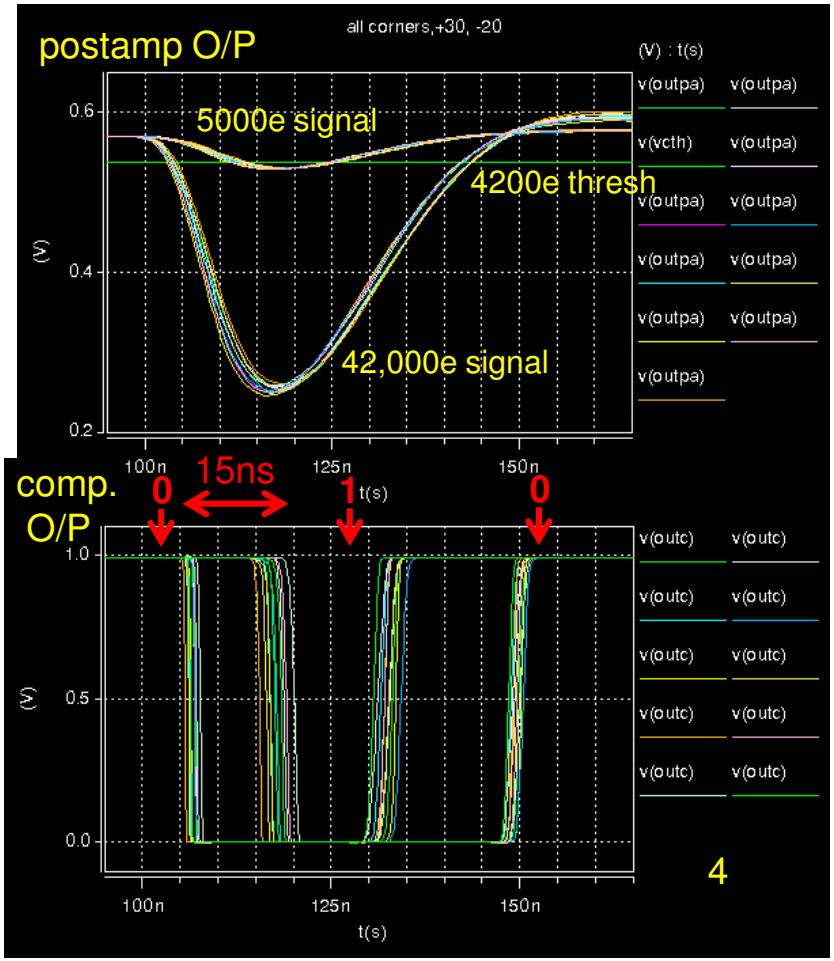
analogue front end



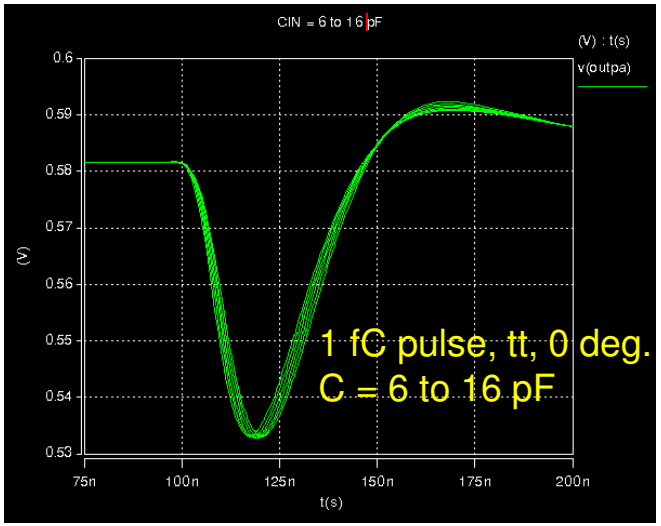
main design changes

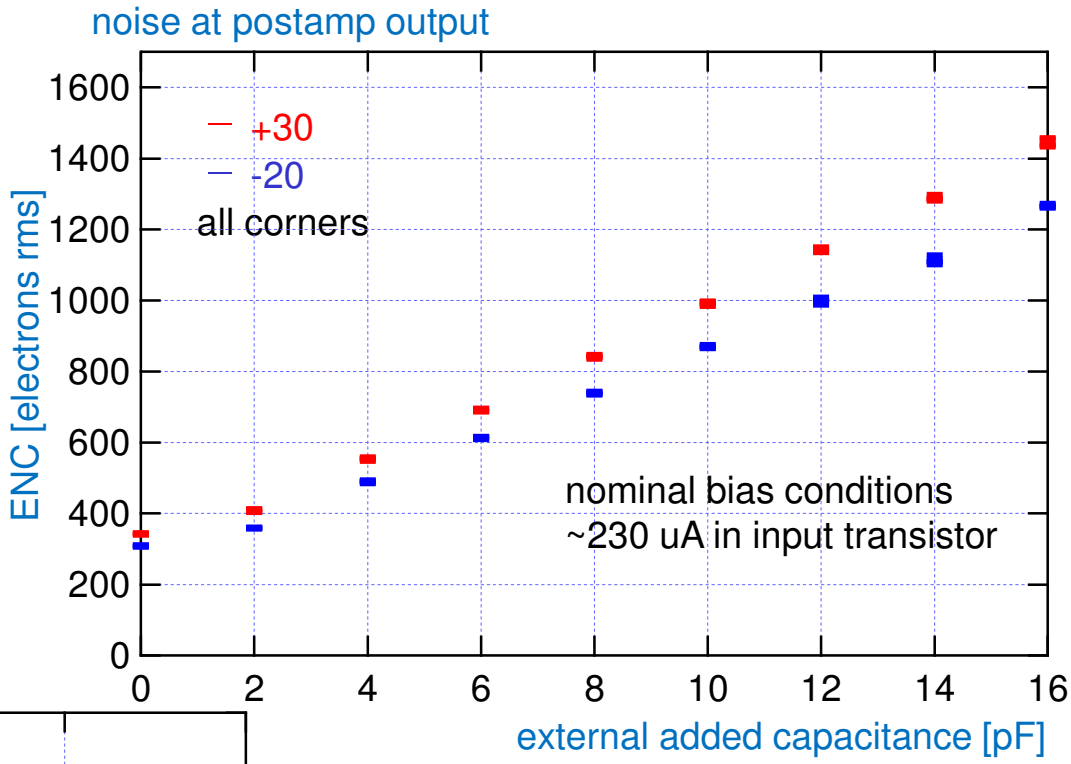
optimised for n-in-p sensors
faster shaping (return to baseline within 50 ns)
VCTH linear, monotonic and 10-bit
CBC2 “shadow” and CM effects addressed

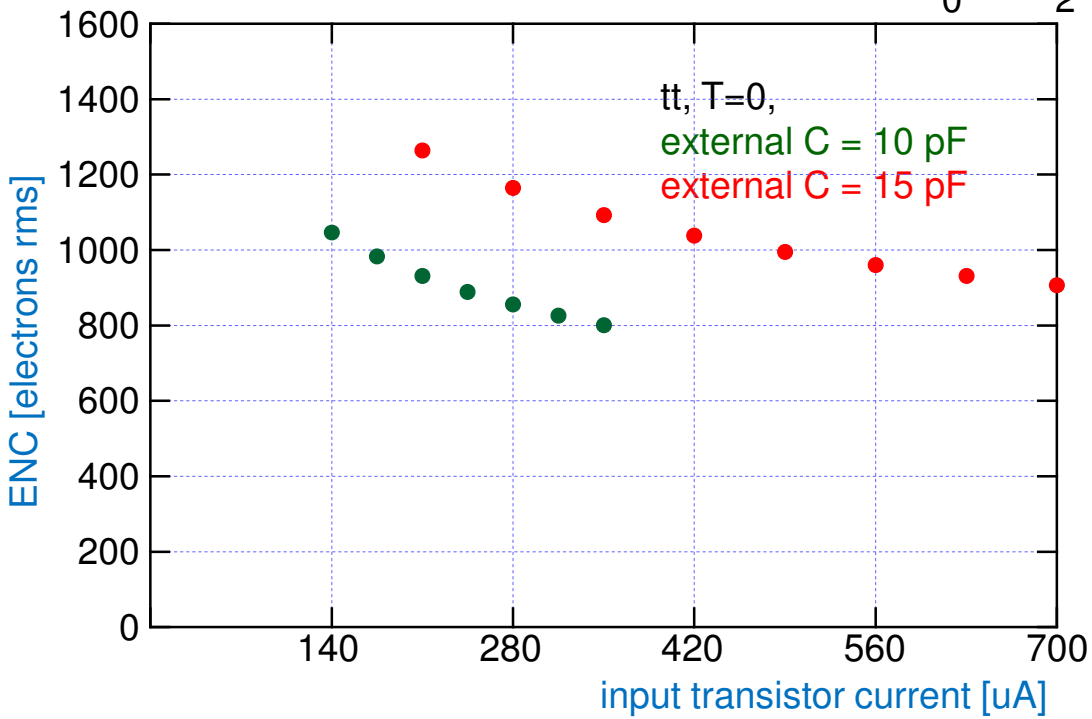
post-layout
timewalk
simulation



noise







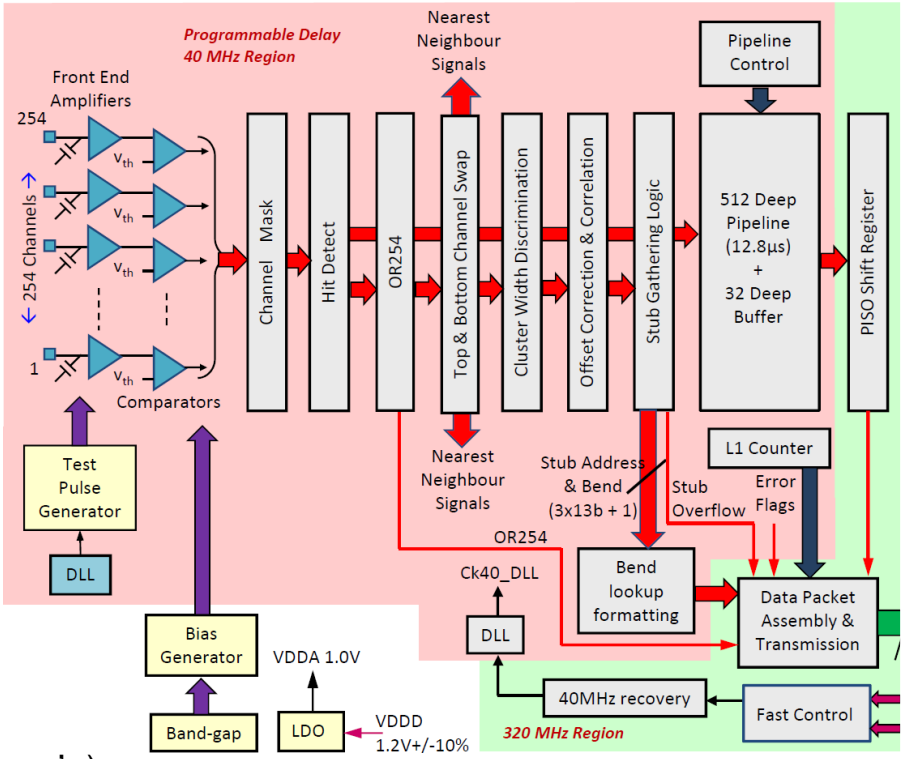
post-layout simulations

1000e achievable for external capacitance up to ~10 pF at preamp input (for acceptable power consumption)

no strong dependence on process corners

pulse shape/height varies not much over quite large input capacitance range

main digital functionality



Hit Detect

samples unmasked comparator outputs @ 40 MHz
(phase adjustable via DLL)

Top/Bottom Channel Swap

swaps seed/window layer to keep seed layer closest to beam for modules on both sides of rod

CWD

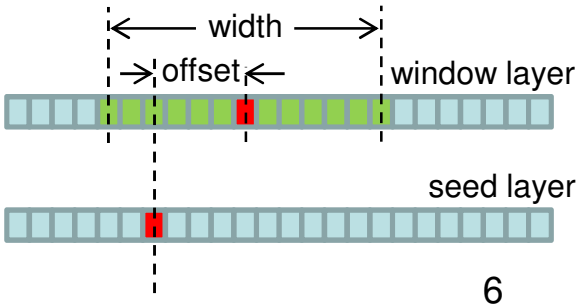
clusters up to 4 strips wide accepted
2 & 4 strip clusters assigned to mid-position
=> ½ strip resolution => 8-bit cluster address

Offset Correction & Correlation

window width programmable up to ± 7 strips (½ strip res'n)
window can be offset up to ± 3 strips (½ strip res'n) (4 domains / chip)
5-bit bend info indicates position of cluster in window

Stub Gathering Logic

up to 3 stub addresses + bend info passed to bend lookup formatting block every BX
- 1st 3 stubs only
- more than 3 -> Stub Overflow bit set in O/P data packet



Bend lookup formatting

5 bits bend info reduced to 4 bits using programmable lookup table

Data Packet Assembly & Transmission

6 SLVS differential pairs transmitted off-chip @ 320 Mbps
- 5 for stub data, 1 for L1 readout data

CBC3 digital interfaces

output data: up to 3 stubs data transmitted to CIC/BX
6 SLVS diff pairs @ 320 Mbps

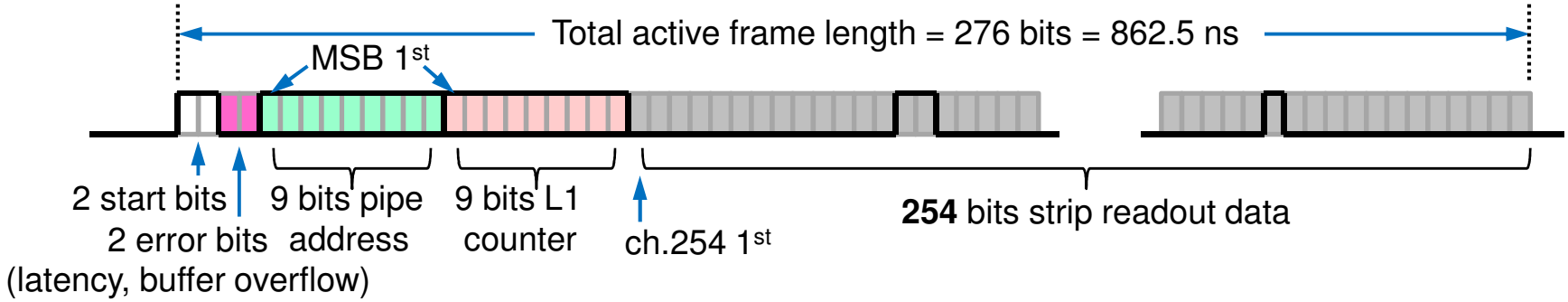
25 ns

S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**

R = L1 triggered readout data
time flow **top** to **bottom** (e.g. S1<7> output first)

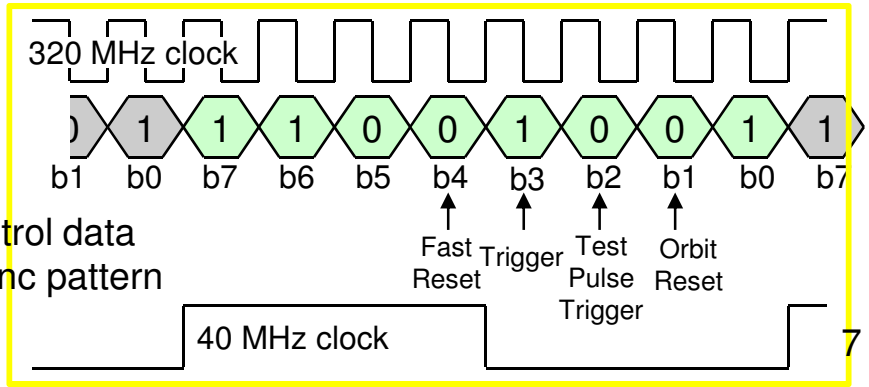
readout data

readout data frame length 950 nsec
=> up to 1 MHz L1 triggering capability



fast control

320 MHz clock
320 Mbps fast control line

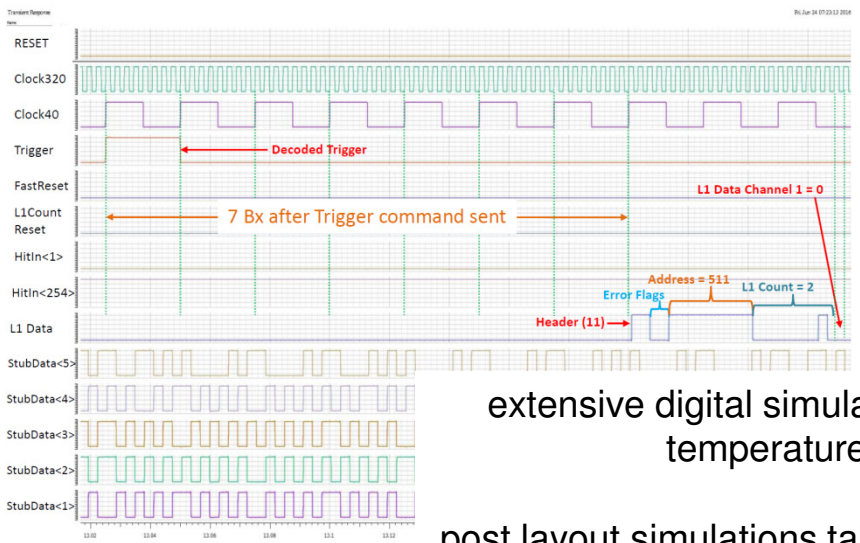


40 MHz generated from fixed sync pattern in fast control data
normal command structure can't be confused with sync pattern

digital simulations

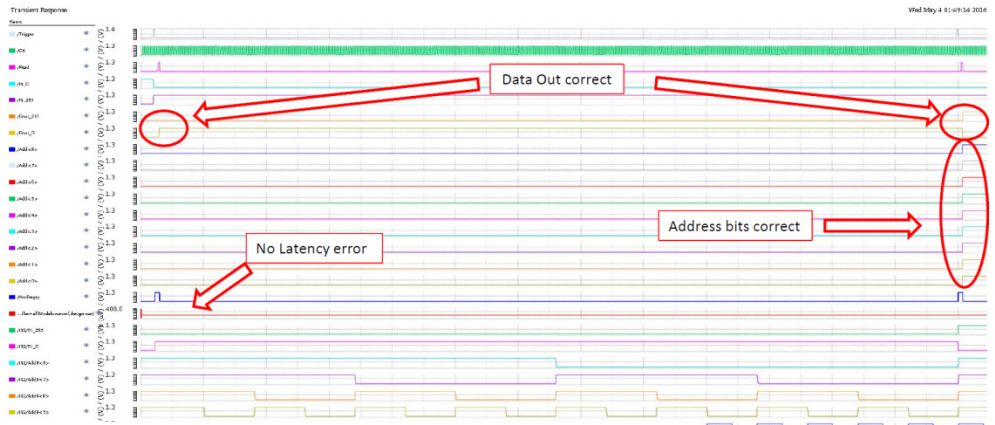
Back end schematic simulation: Start of L1 Data from 2nd Trigger. Corners ss & sf at 1.1V and 0C.

Write 1 to channel 1 and 0 to 254, then 0 to channel 1 and 1 to 254. 2 triggers, one for address 0, & one for address 511.



Schematic simulation of Stub Data

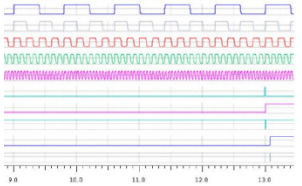
Pipeline & Buffer RAM simulation for cut down layout. Corner ssf at 1.2V, +30C



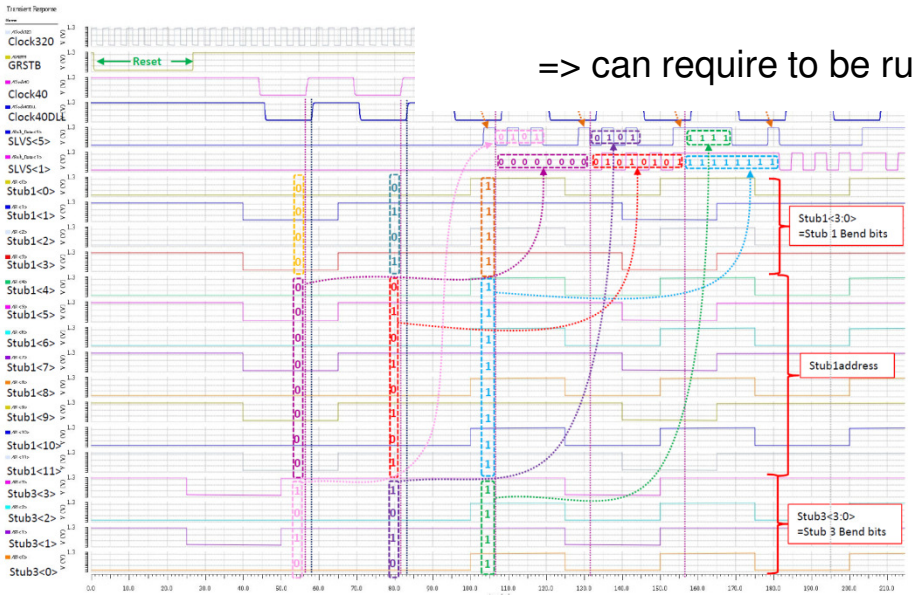
extensive digital simulations carried out at all process corners, temperature and power supply extremes

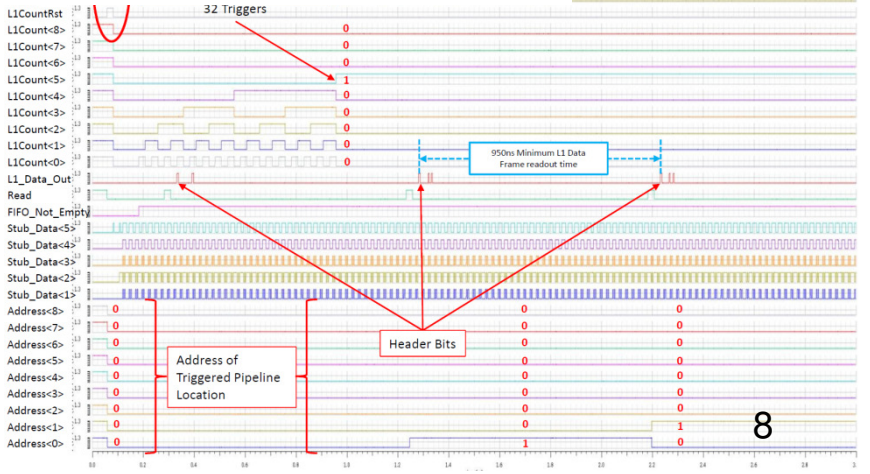
post layout simulations take days to run, even with heavily cut-down versions of the circuitry

=> can require to be run several times if problems found

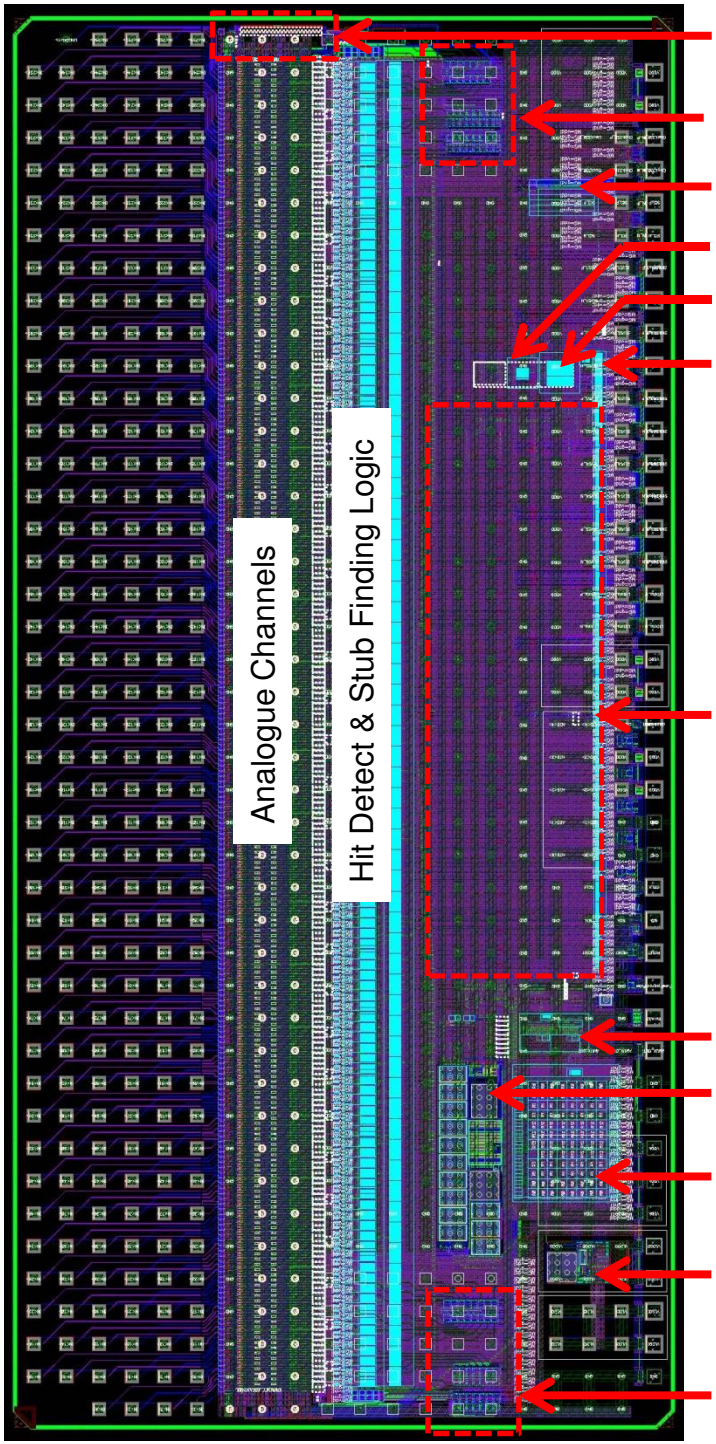


ve accuracy





CBC3 Top Level



test pulse circuit

I/O to neighbour

DLL

bend LUT

data assembly

L1 counter & FIFO

512 deep pipeline & O/P buffer

bandgap

I2C & biases

10b DAC for VCTH

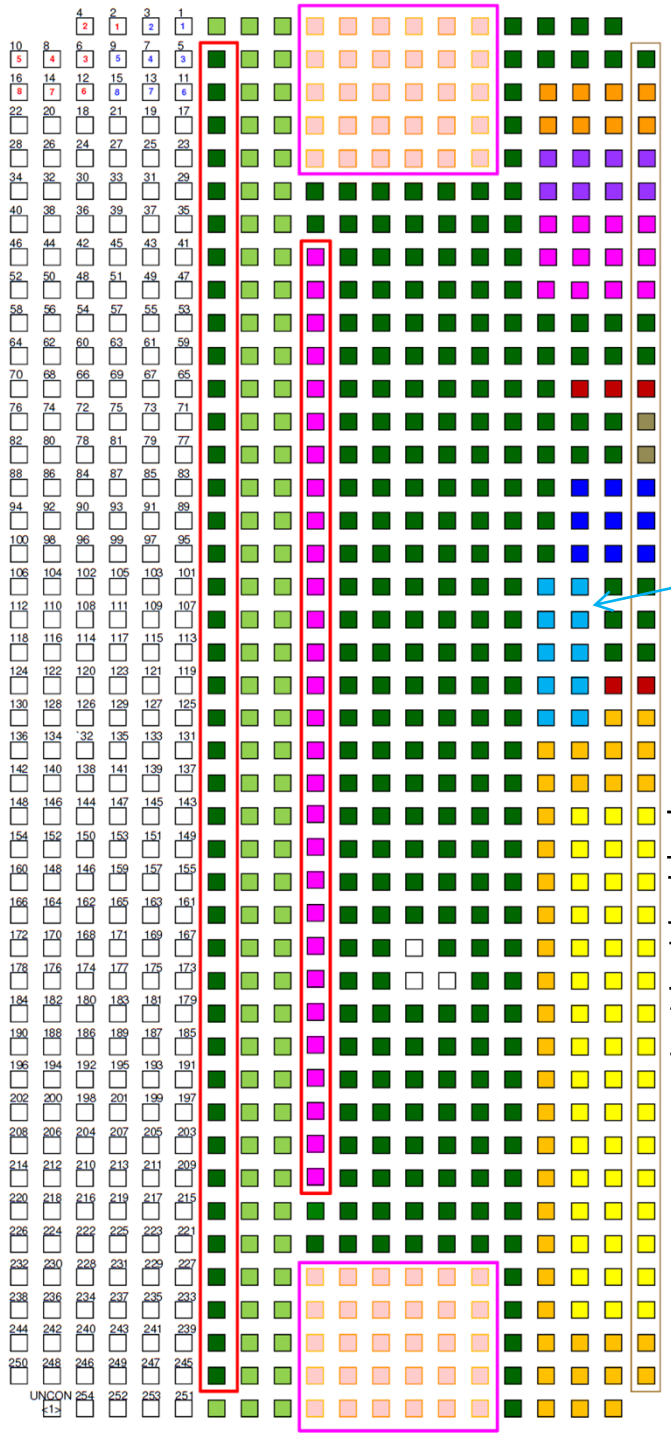
LDO

I/O to neighbour

20 columns, 43 rows
(1 more column than CBC2)

5.25 mm x 11 mm

pad allocations



some minor re-arrangement here since last time

pads as viewed on hybrid surface
(as if looking through chip)

right-most column for wire-bond / wafer probe

like CBC2 gives access to internal bias currents and voltages

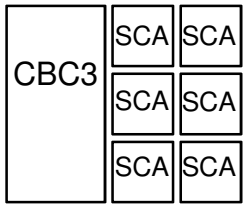
chip ID can be set by e-fuses (19 bits)
will be programmed at wafer probe time
every chip will have unique ID

CERN PMOS bandgap reference
also trimmed by e-fuses (6 bits)

CBC3 production

CBC3 sharing wafer with GBT-SCA chip

1 CBC3 : 6 SCA



SCA is wire-bond chip
CBC3 has one wire-bond column

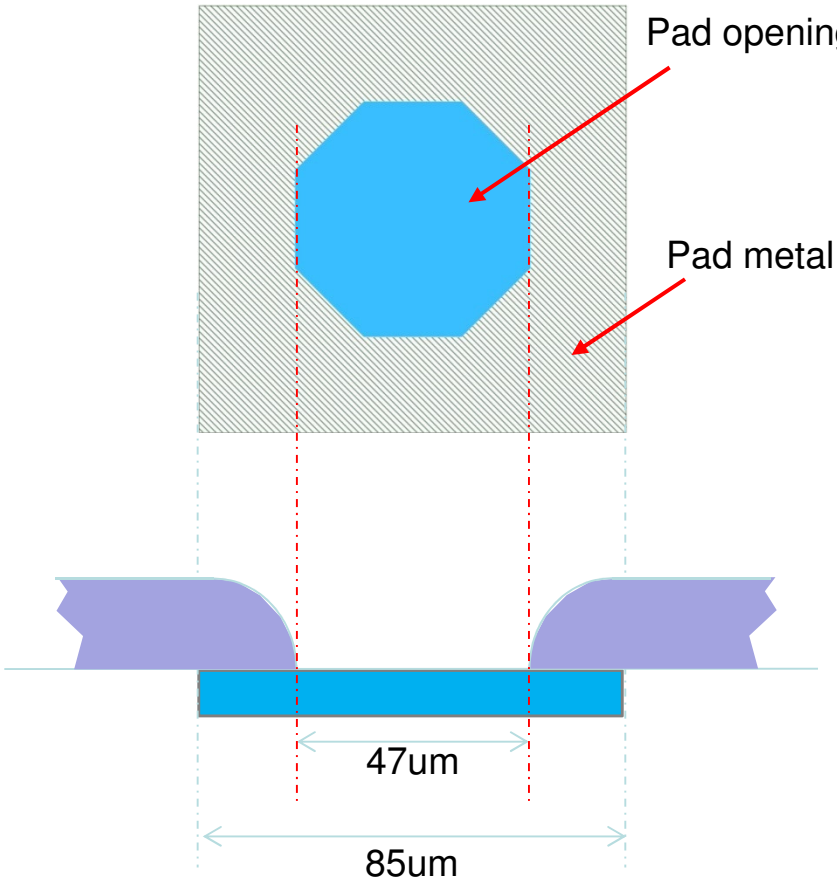
plan is to ask for all wafers to be delivered un-bumped
(Global Foundries out-sources wafer bumping anyway)

then look after getting bumping done ourselves
for the CBC3 dedicated wafers

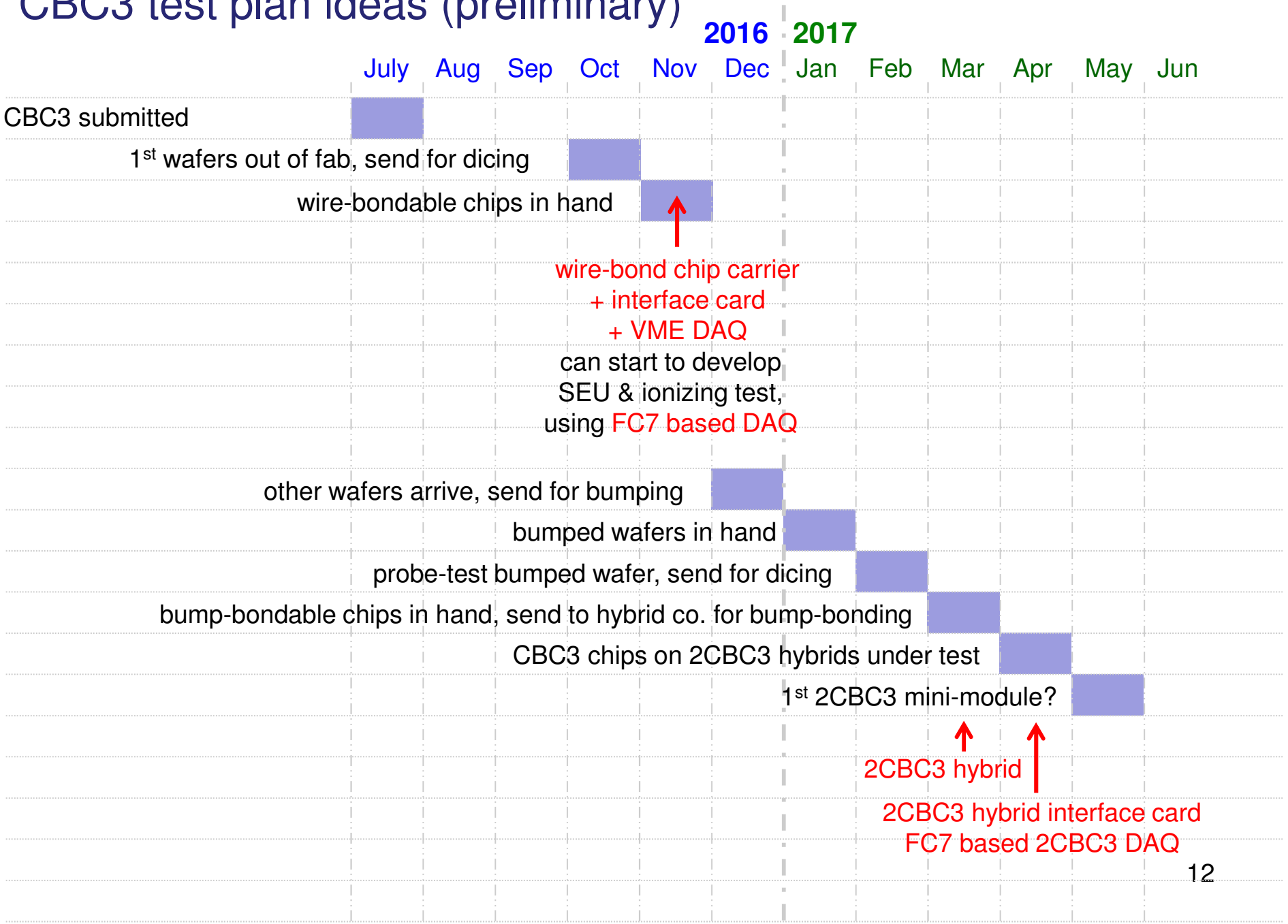
should be straightforward but important to get
bump-bond pad design correct

final pad design not yet resolved

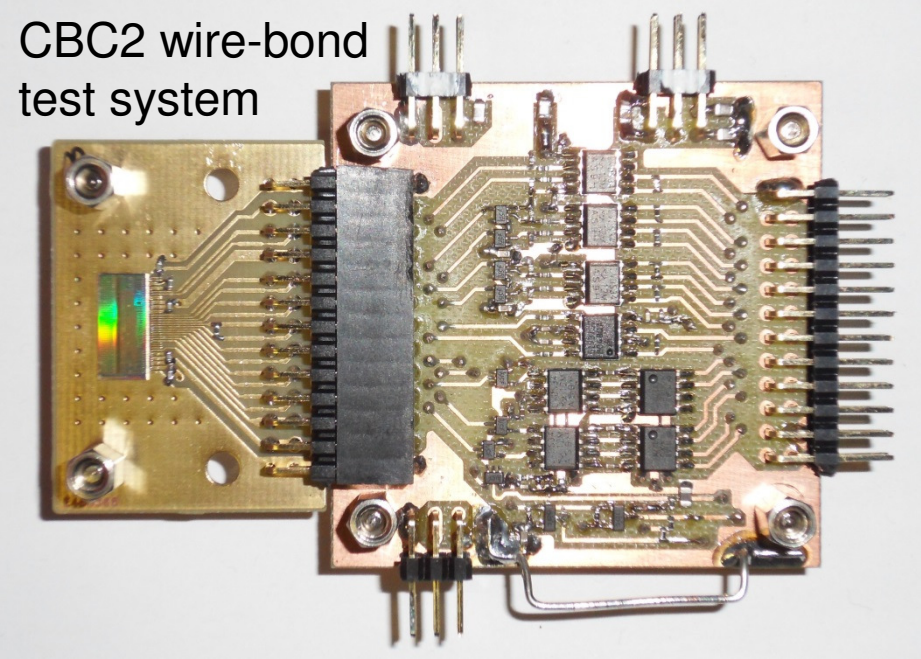
current design of CBC3 bump-bond pad (pad metal is the same as if it was actually a wire-bond pad)



CBC3 test plan ideas (preliminary)



1st tests



1st diced chips will be wire-bondable

can follow similar test procedures to CBC2

make single chip carrier + interface board

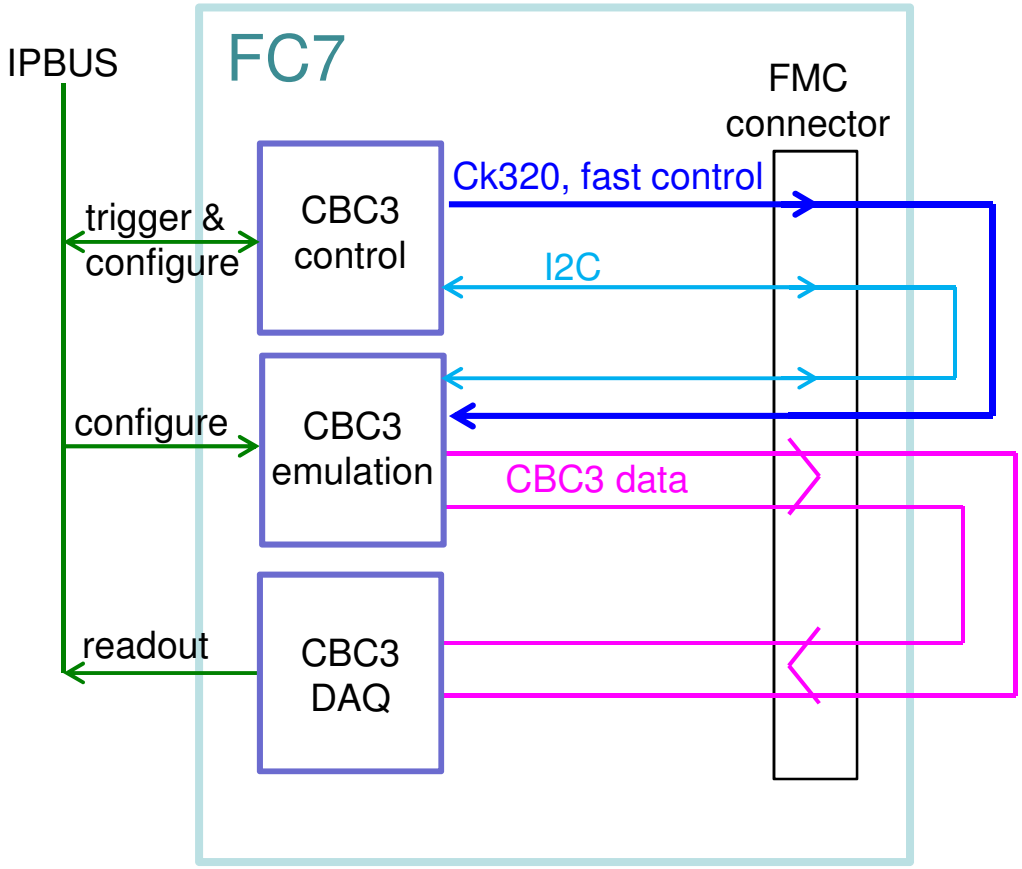
useful for:

- developing wafer probe tests
- ionizing tests
- SEU tests

need to adapt/develop DAQ hardware/firmware/software to deal with 6 x 320 Mbps data streams

CBC3 initial test system development: control & DAQ

Kirika Uchida



CBC3 control

generates 320 MHz clock
encodes control signals on fast control line
(fast reset, test pulse trig., L1A, orbit reset)
implements I2C interface

CBC3 emulation

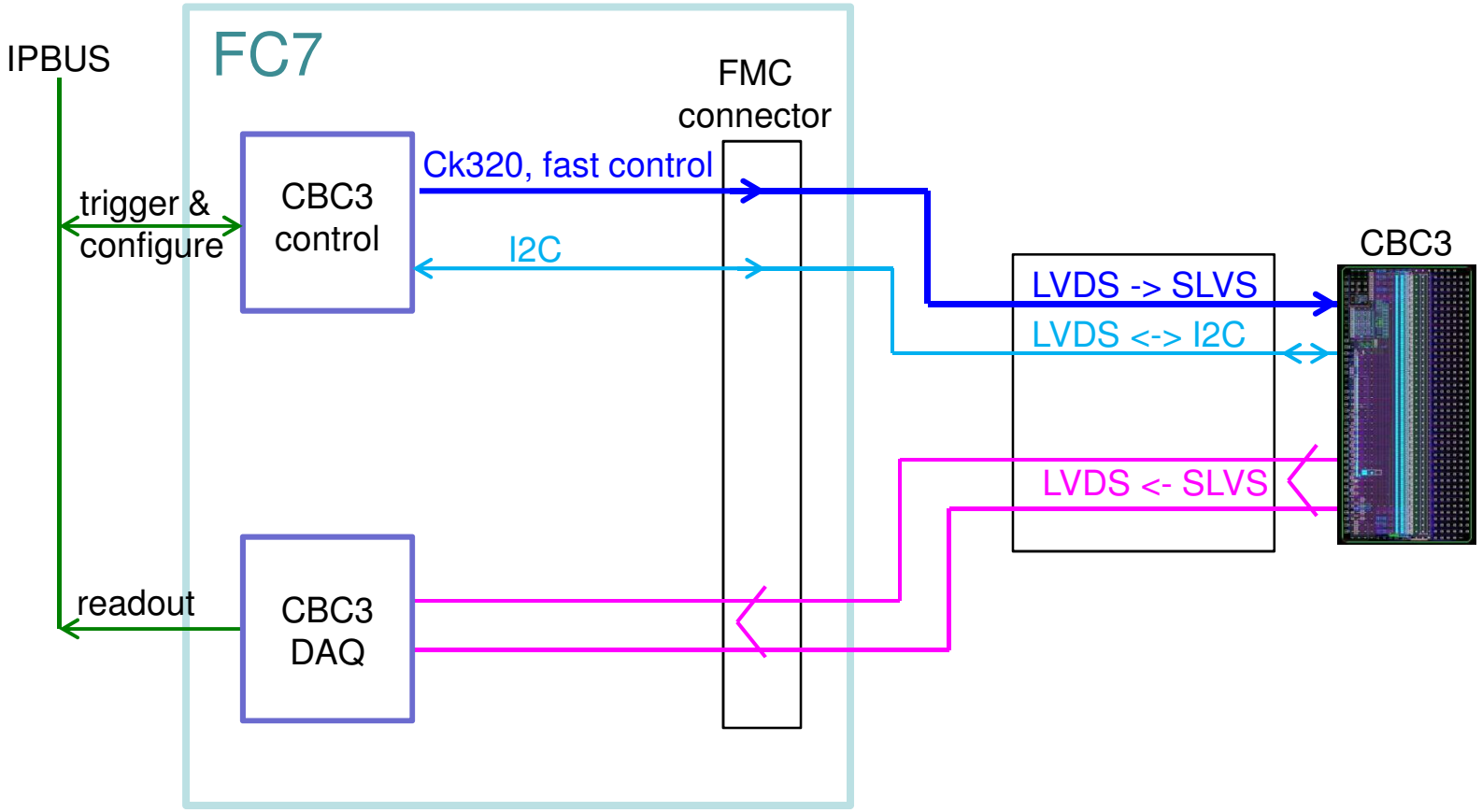
responds to fast control signals
for example
test pulse trigger produces stubs
L1A produces data frame
(data patterns can be configurable)

CBC3 DAQ

receives and processes the emulated data

CBC3 initial test system development: control & DAQ

Kirika Uchida



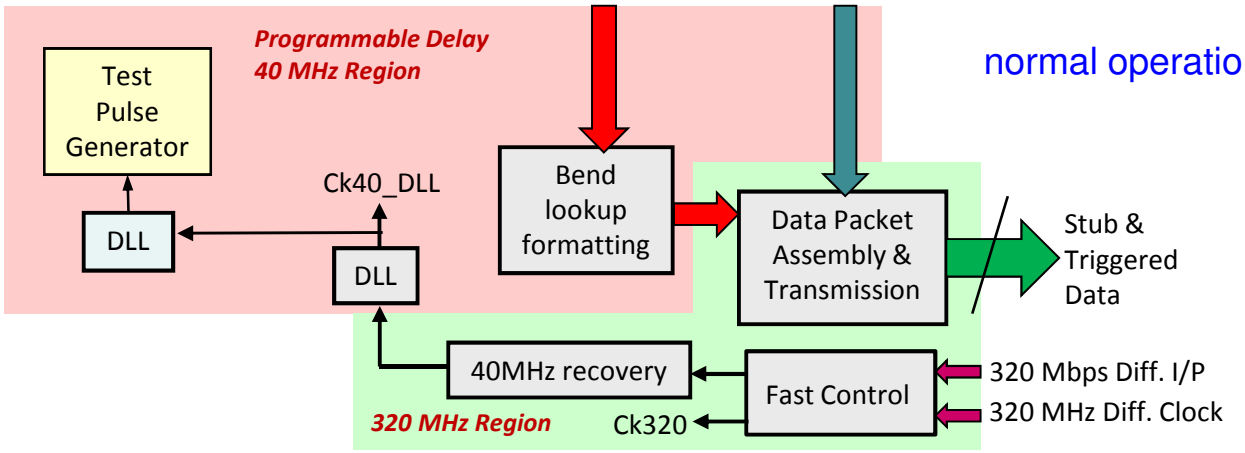
summary

- CBC3 is the final prototype of the 2S module front end chip
  - contains all the functionality required
  - post-layout simulations meet specifications
  - soon to be submitted for manufacture on 2 month turnaround
- next steps
  - write a user manual
  - prepare test setups
    - hardware, firmware & software

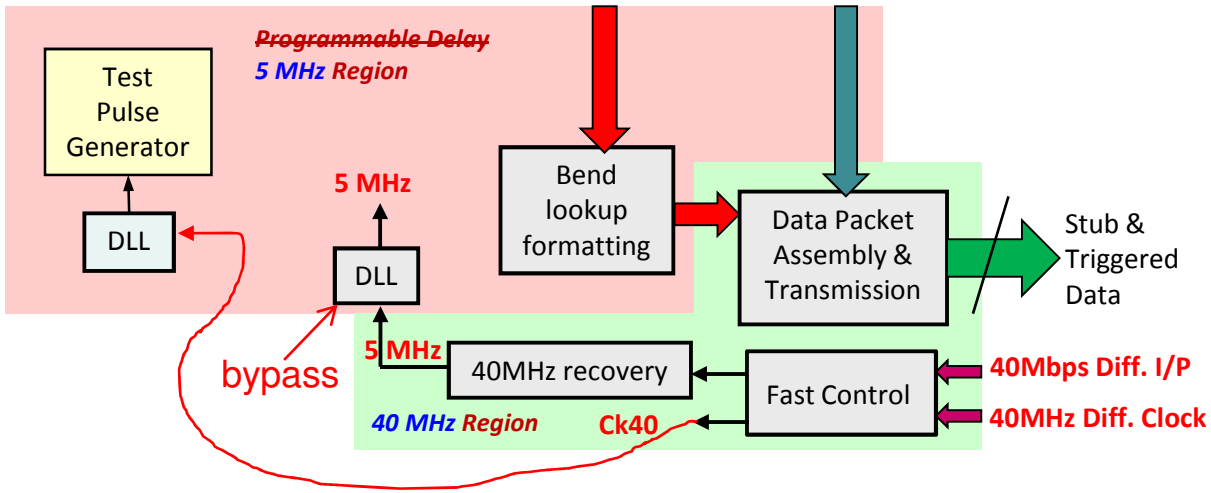
extra

40 MHz test mode

if necessary (e.g. for wafer probing) can run chip at 40 MHz



normal operation



40 MHz test mode

change 320 -> 40 MHz (Ck40)

run SCI at 40 Mbps

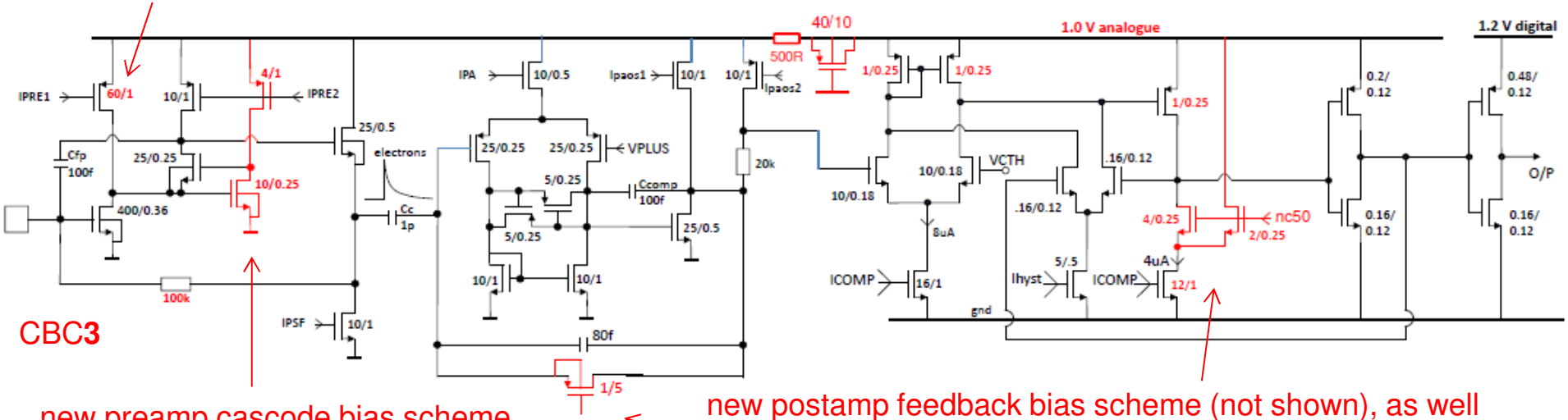
on-chip recovered clock is 5 MHz

bypass 40 MHz DLL
(have to - it will not capture)

feed Test Pulse DLL from Ck40

CBC2 vs. CBC3

increase in bias FET
allows higher currents

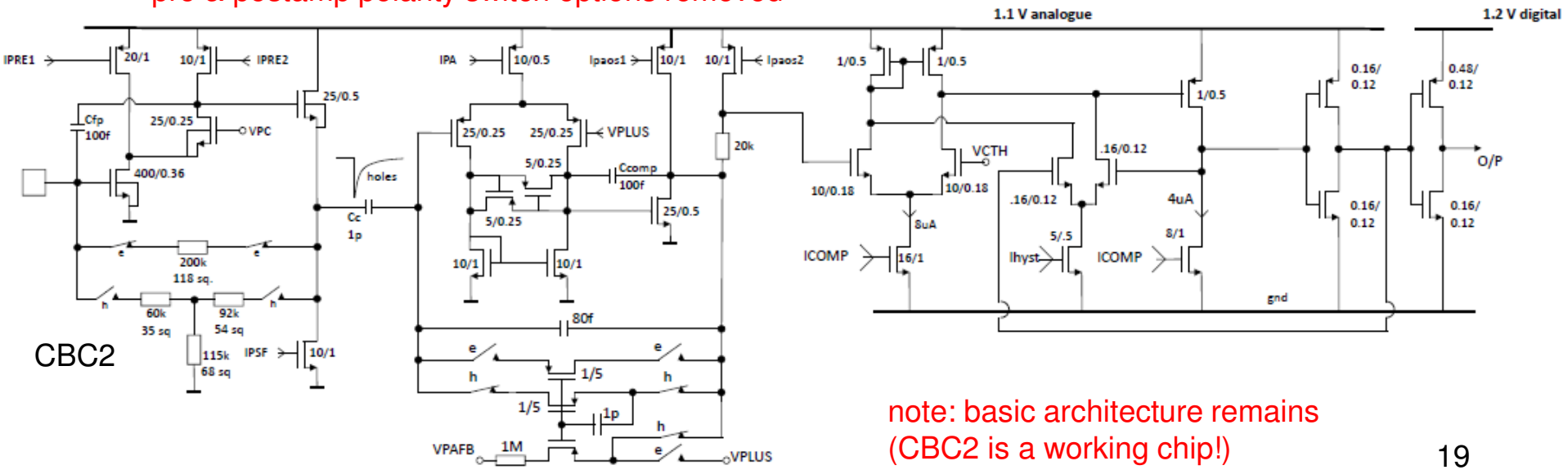


CBC3

new preamp cascode bias scheme
to eliminate “shadow effect”

new postamp feedback bias scheme (not shown), as well as current neutral comparator, addresses CM effects observed when many channels fire

pre & postamp polarity switch options removed



CBC2

note: basic architecture remains
(CBC2 is a working chip!)

top & bottom channel swap

modules mounted above and below support structure will be flipped (probably)

=> seed and window layers will also be flipped unless do something about it

(expect lower efficiency when seeding from outer layer because of scattering and conversions -> more hits in outer layer which don't correspond to valid stub)

simplest thing is to swap channels on chip

1<->2, 3<->4, 5<->6,…..