CBC3 progress

Tracker Phase 2 Upgrade Week, Phase 2 Electronics, 12th May, 2016

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introduction

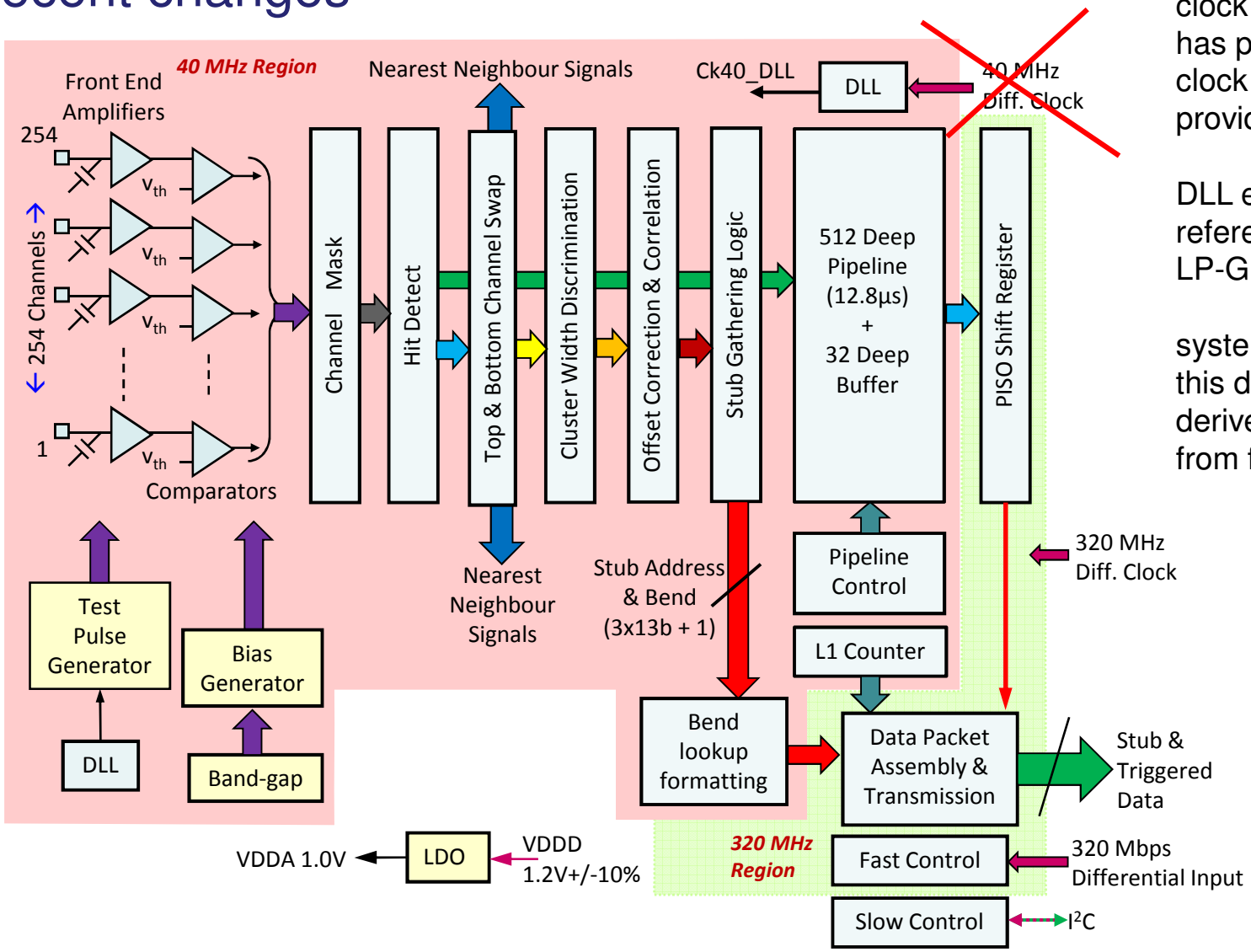
previous talks

May 2016 tracker week: CBC3 specifications
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_elec_CBC3specs_May_2015.pdf
November 2016 tracker upgrade week: CBC3 design progress
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3progress_Nov_2015.pdf
January 2016 tracker week: CBC3 design progress
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3progress_Jan_2016.pdf

today

progress update
recent design changes
schedule

recent changes

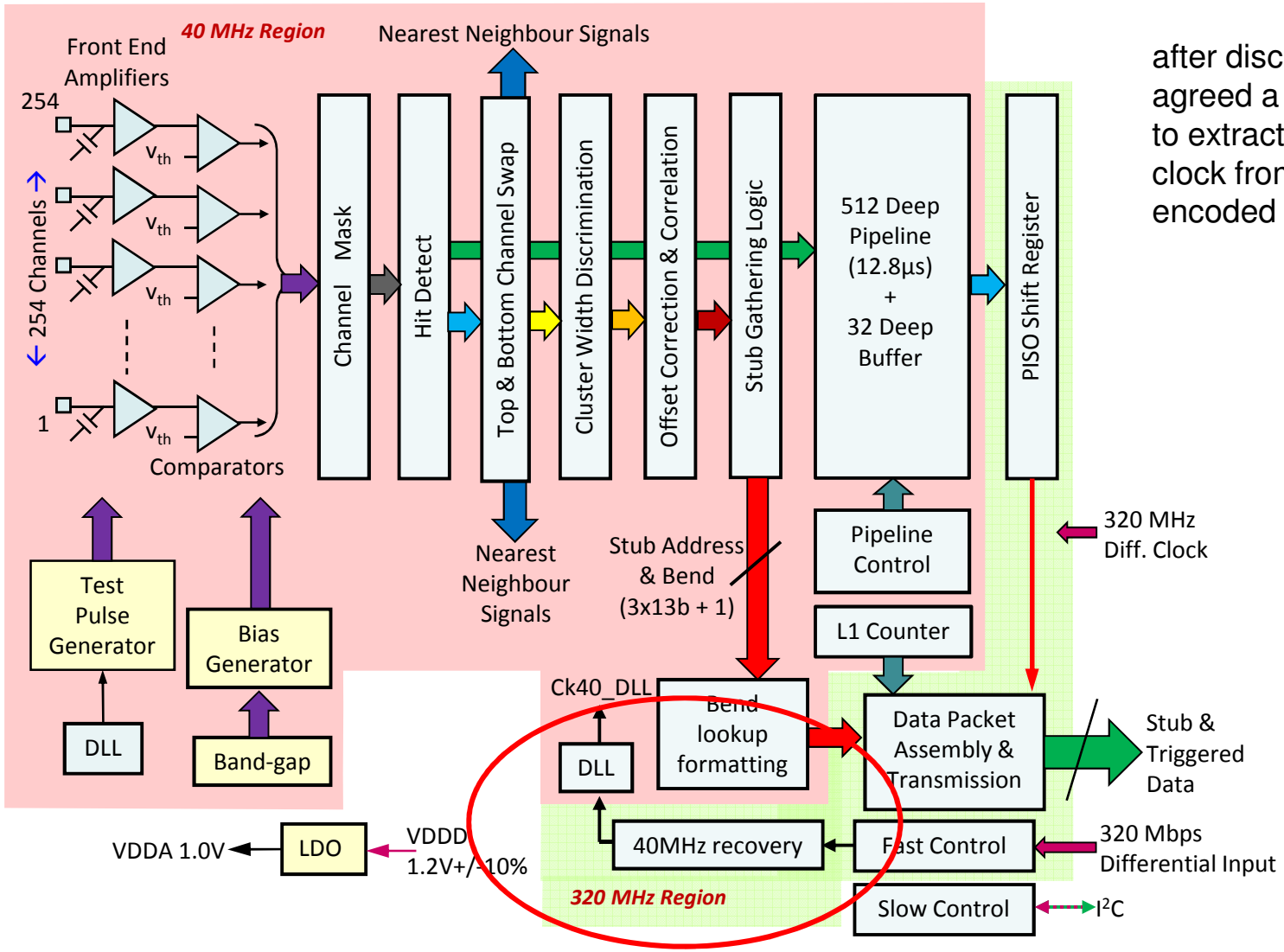


clock to 40 MHz region has programmable clock phase (1 ns res'n) provided by DLL

DLL expecting 40 MHz reference input from LP-GBT

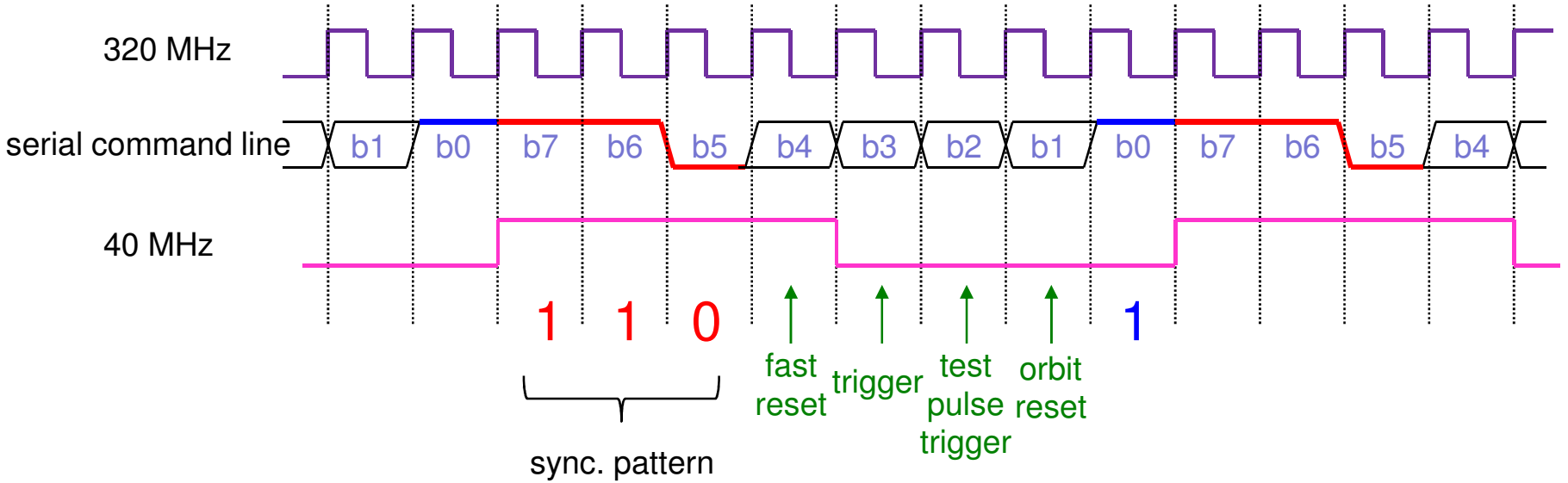
system decision to scrap this dedicated clock and derive reference clock from fast control input

recent changes



after discussion, have agreed a coding scheme to extract 40 MHz reference clock from fixed pattern encoded on fast control line

40 MHz encoding scheme



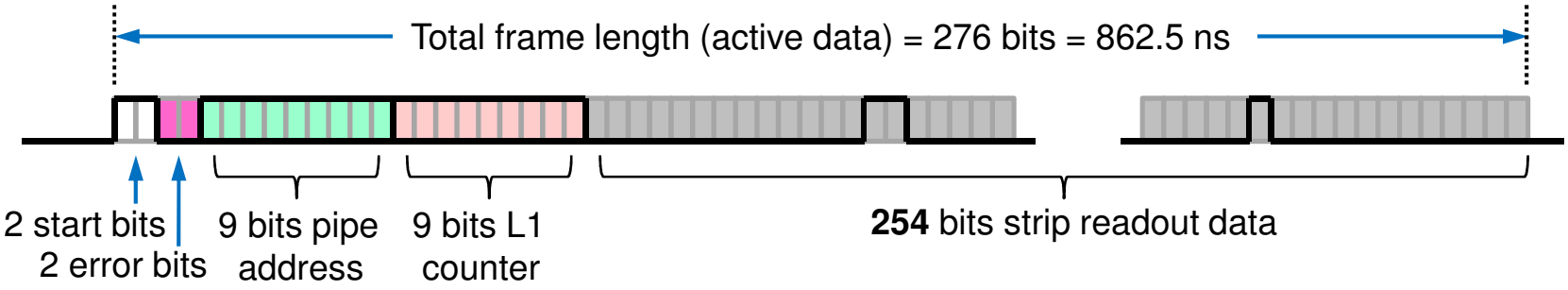
normal command structure cannot be confused with ‘110’ sync. pattern

would never send fast reset at same time as trigger

would never send trigger at same time as test pulse trigger

final ‘1’ ensures test pulse trigger coincident with orbit reset does not produce ‘110’

output data frame format



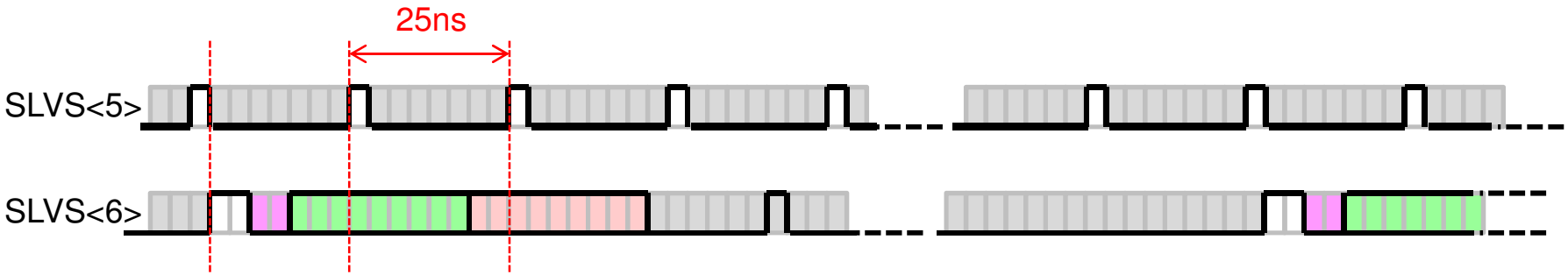
pipe address and L1 counter fields will not be swapped

(as was suggested in recent systems meeting)

strips readout data order will be reversed w.r.t. CBC2

254, 253,….., 2, 1 (instead of 1, 2, 3,…)

output data frame timing



SLVS<5> contains sync pulse
SLVS<6> is triggered readout data

output data frame header will start in 1st bit of 25 nsec block

(not previously specified)

i.e. no gap between sync pulse and 1st bit of header (also discussed recently)

overall output data frame length padded with '0's to exact multiple of 25 nsec

now stands at 950 nsec

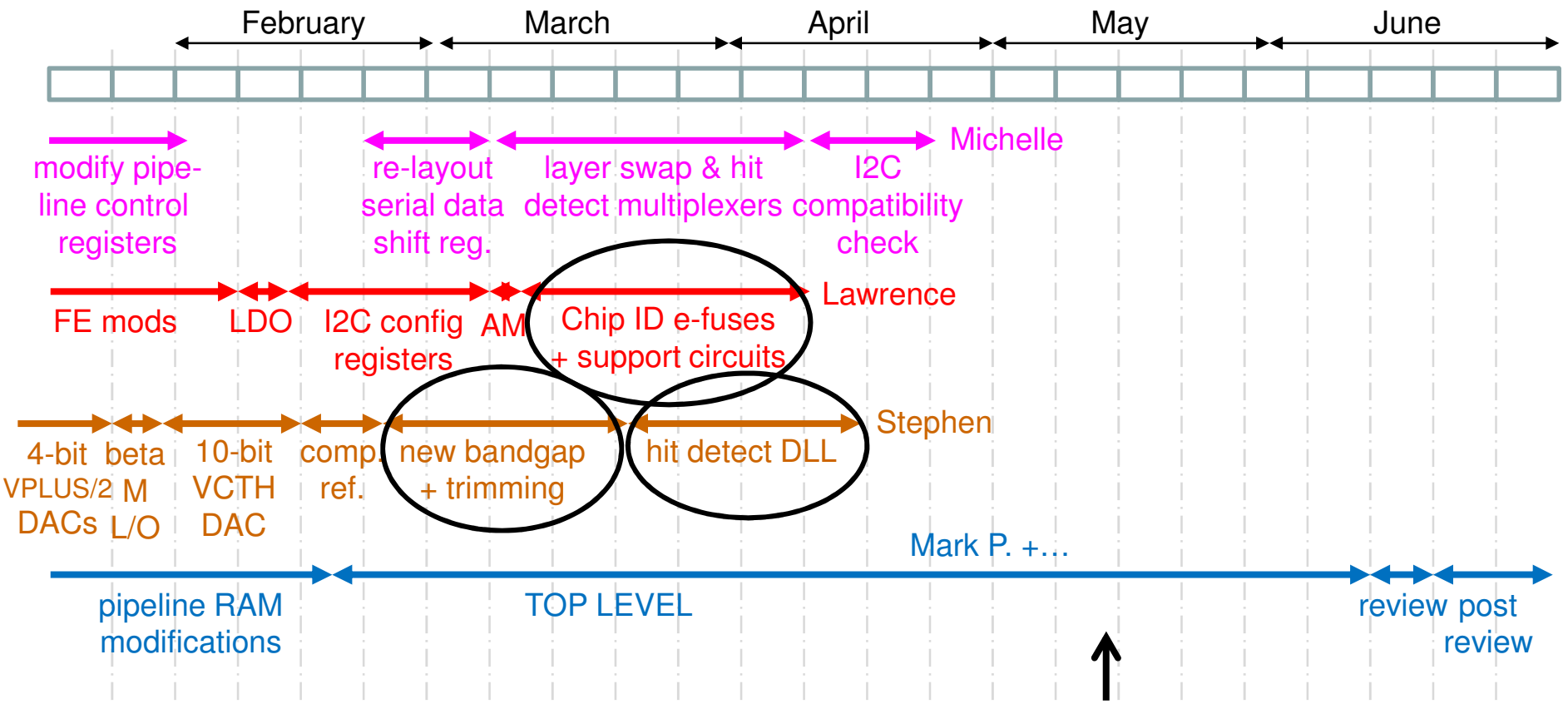
output data block

SLVS<1>	SLVS<2>	SLVS<3>	SLVS<4>	SLVS<5>	SLVS<6>
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**

25 ns

R = L1 triggered readout data
time flow top to bottom (e.g. S1<0> output first)

schedule



schedule as presented last time (extra tasks Ck40 and some I2C mods absorbed)
Top Level tasks now underway (all designers involved)
individual design blocks assembled, connected up, lots of checking
(progress on circled blocks will be covered in next slides)

Chip ID and bandgap trim e-fuses

e-fuses used to set 19 bit individual chip ID at wafer probe time

10 bits for wafer ID, 9 bits for pos'n on wafer

can be read back via I2C

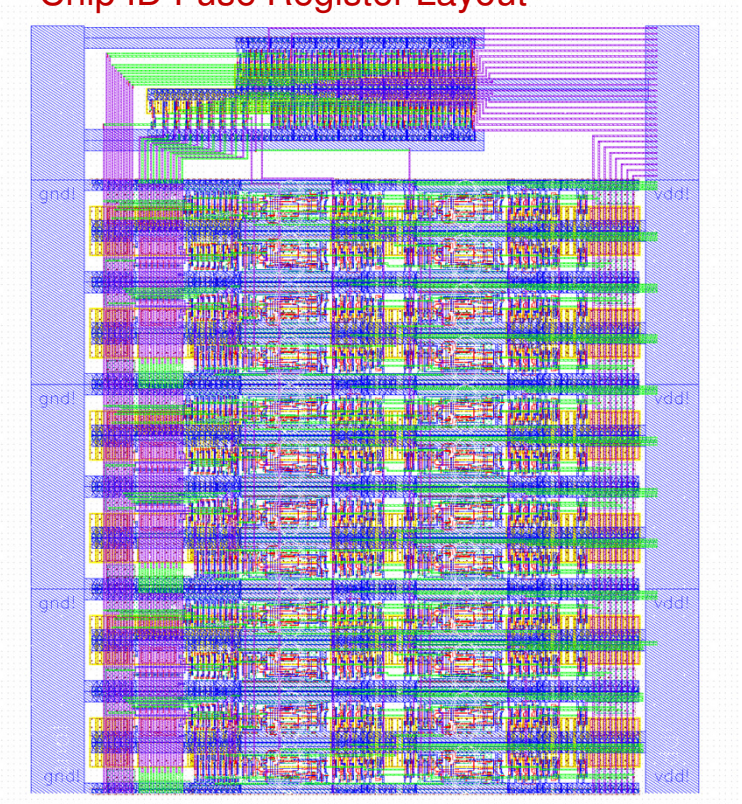
e-fuses also used for 6-bits Bandgap Trim

new CERN bandgap has good stability to radiation
but will vary with process

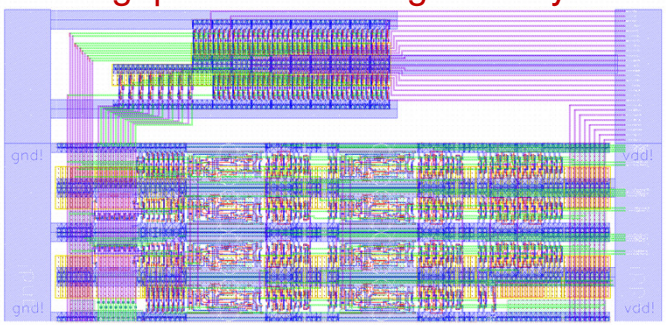
fuses set default (reset) value in I2C register

can be read back or overwritten if so desired

Chip ID Fuse Register Layout



Bandgap Trim Fuse Register Layout



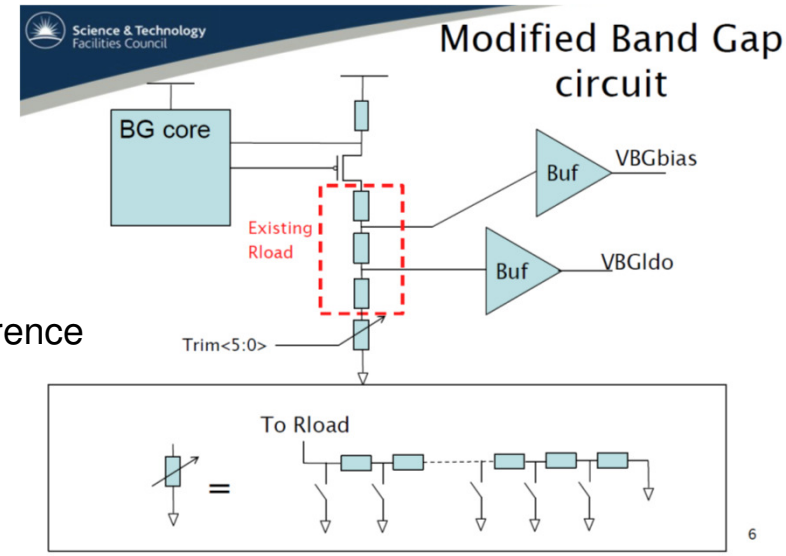
bandgap and trimming

using CERN PMOS based bandgap for radiation stability

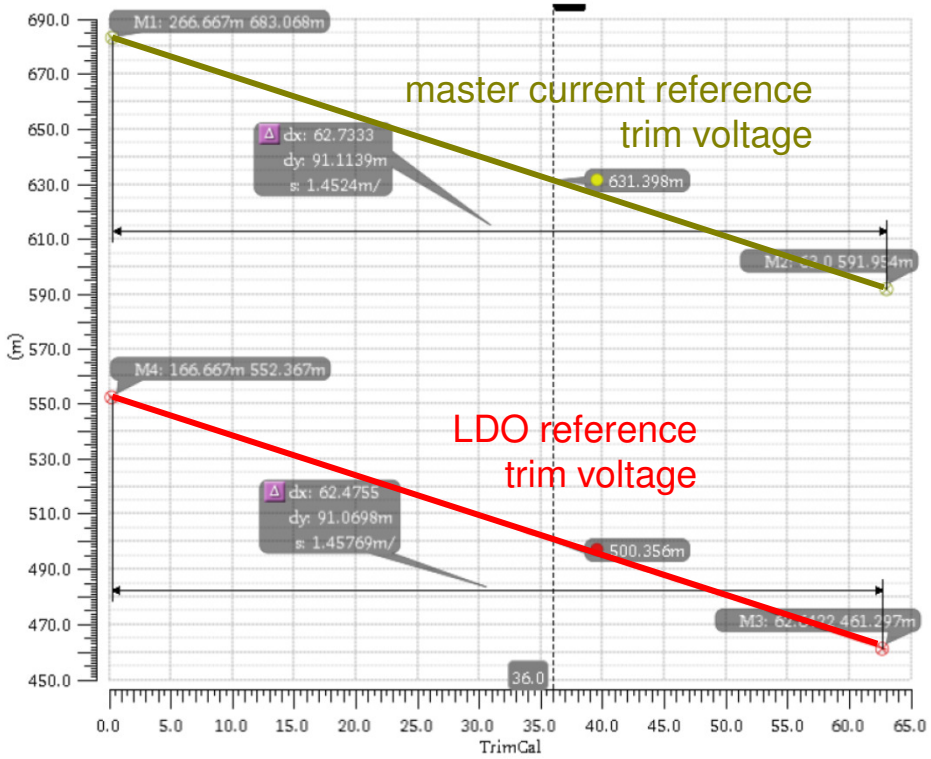
requires trimming for process variations

need 2 voltages, one for LDO and one for master current reference

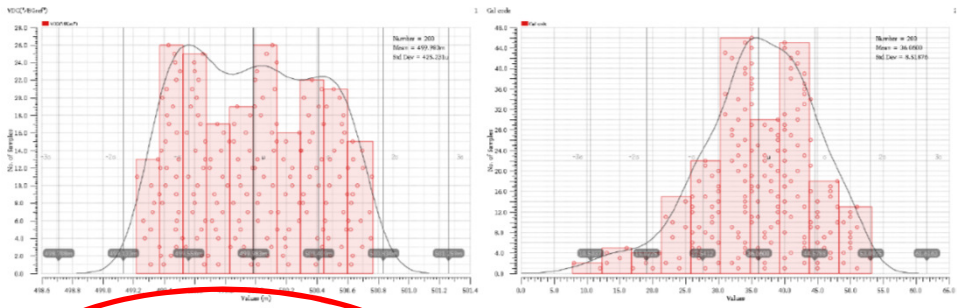
6-bit trim enough to cope with process with good accuracy



6bit trim range



Trimming of MC process variation



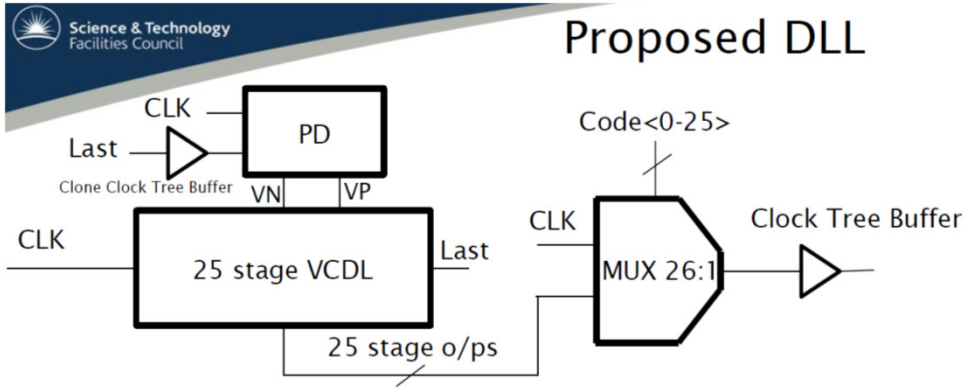
- VBGldo after trimming for process variation
  - Mean= 500mV
  - Range 499.2mV -> 500.8

- Trim code used for process compensation
  - Mean= 36
  - Range 8 -> 51

DLL for front end sampling

CBC2 DLL deviates slightly from 50:50 mark: space ratio (not an issue for test pulse)

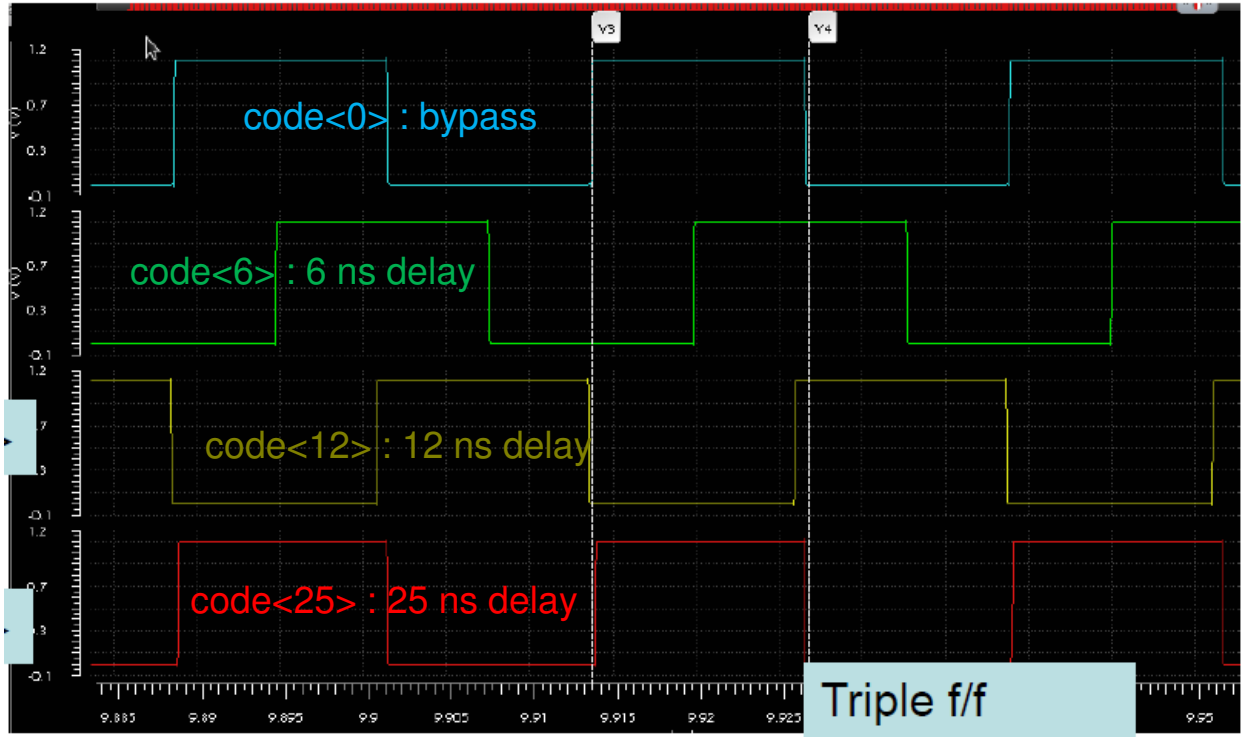
using improved version for CBC3



- Existing delay stages from CBC2
- Uses a new phase detection circuit
  - Two charge pumps
  - Muller C gate

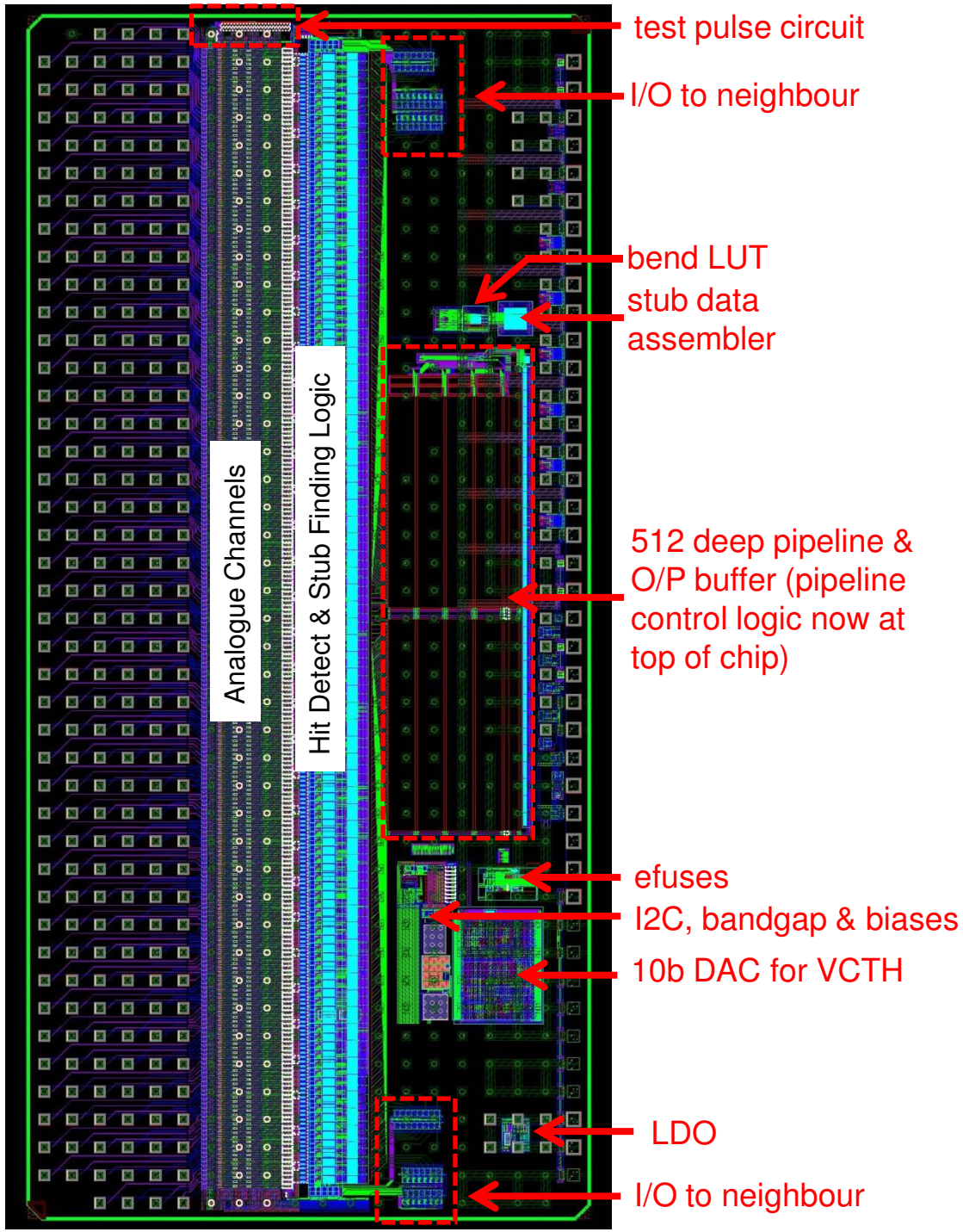
- Fixed width delay pulses
- Synced to both edges of the clock
- Delay in steps of 1ns
- 25 step control with bypass option
- Code<0> = bypass
- Code<1-25> = <1-25>*1ns increments

post layout simulation of delay stages



Triple f/f
-30C, 1.1V, sf

Top Level



congested in bottom right hand corner

all the blocks located there naturally want to be in close proximity

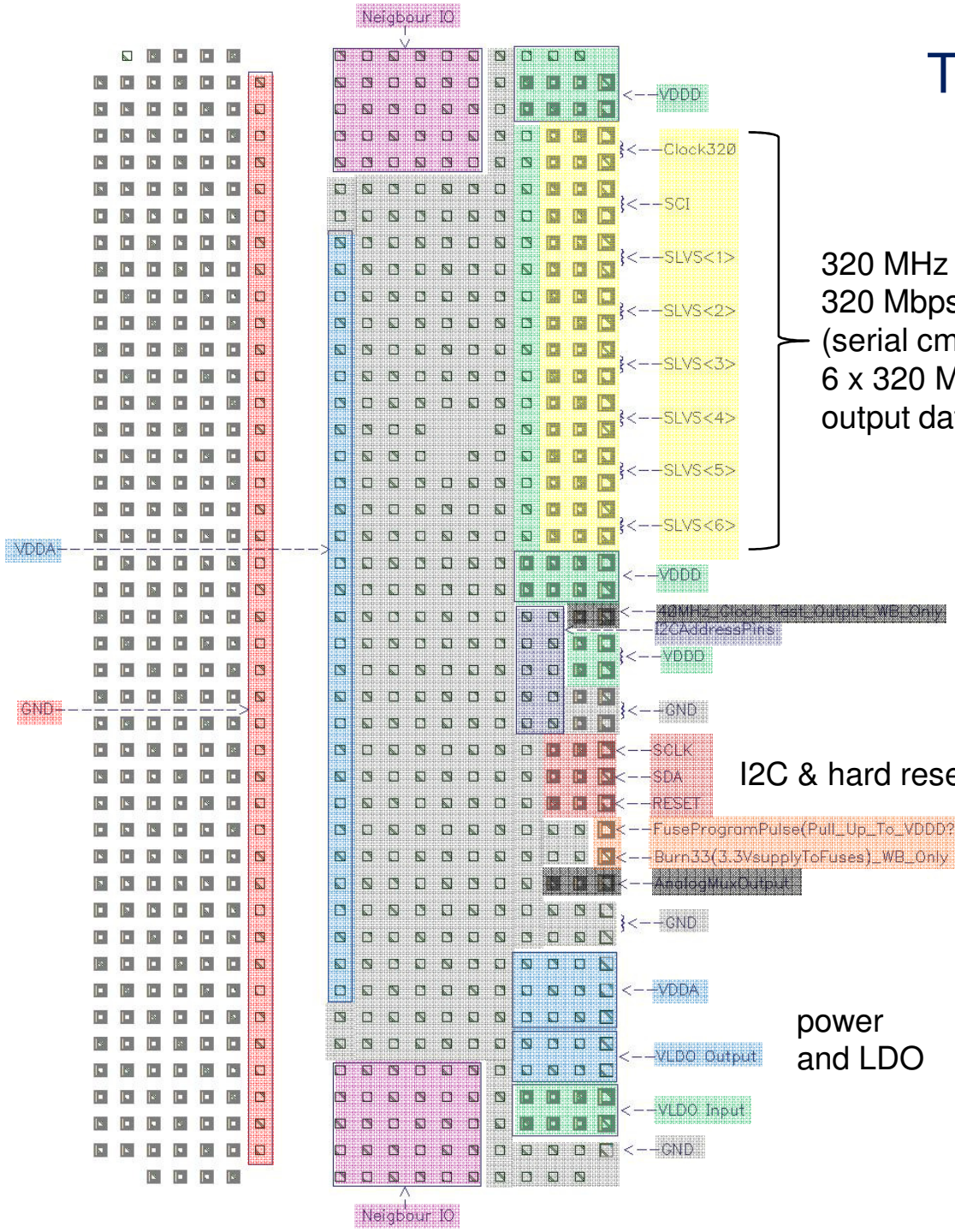
note that pipeline and buffer ram have been flipped vertically so that control logic is at top of chip

helps with congestion

consequence is that channel order in triggered output data frame will be reversed

width of chip has increased by one column (250 um) cf. CBC2

Top Level - pad allocations



320 MHz clock
320 Mbps SCI
(serial cmd I/F)
6 x 320 Mbps
output data

I2C & hard reset

e-fuse
programming

power
and LDO

pads as viewed on chip surface
43 rows, 20 columns

(may not yet be completely final)

extra power provision (GND
and VDDA) to front end

tracking to neighbour IO pads
now only 5 pads deep into chip

(6 cols of 5 rows instead of
5 cols of 6 rows)

summary

recent changes (Ck40 and I2C mods) incorporated into design and complete

top level chip assembly now underway

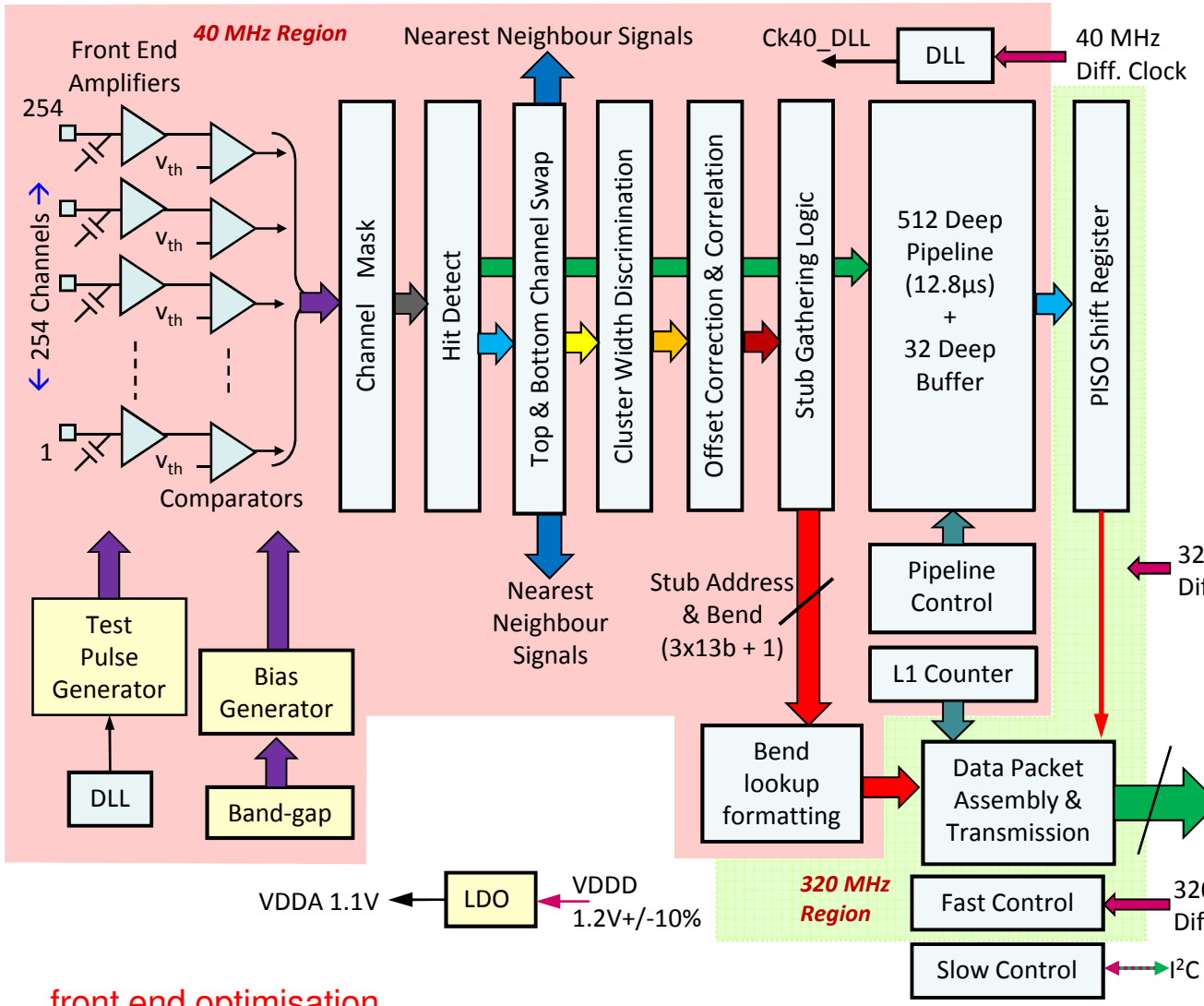
- chip width has to grow by at least 1 column (250 um)
  - should be possible to keep it to one column only
- channel order in CBC3 triggered output data frame will be reversed cf. CBC2

still expecting to be finished by end June

- combined production run with SCA asic

extra

CBC2 -> CBC3



system issues addressed

- synchronization & timing
- data formats
- electrical standards
- powering

longer pipeline - 12.8 usec

higher L1 trigger rate capability: ~1 MHz

stub data transmission off-chip: address & bend info for up to 3 stubs

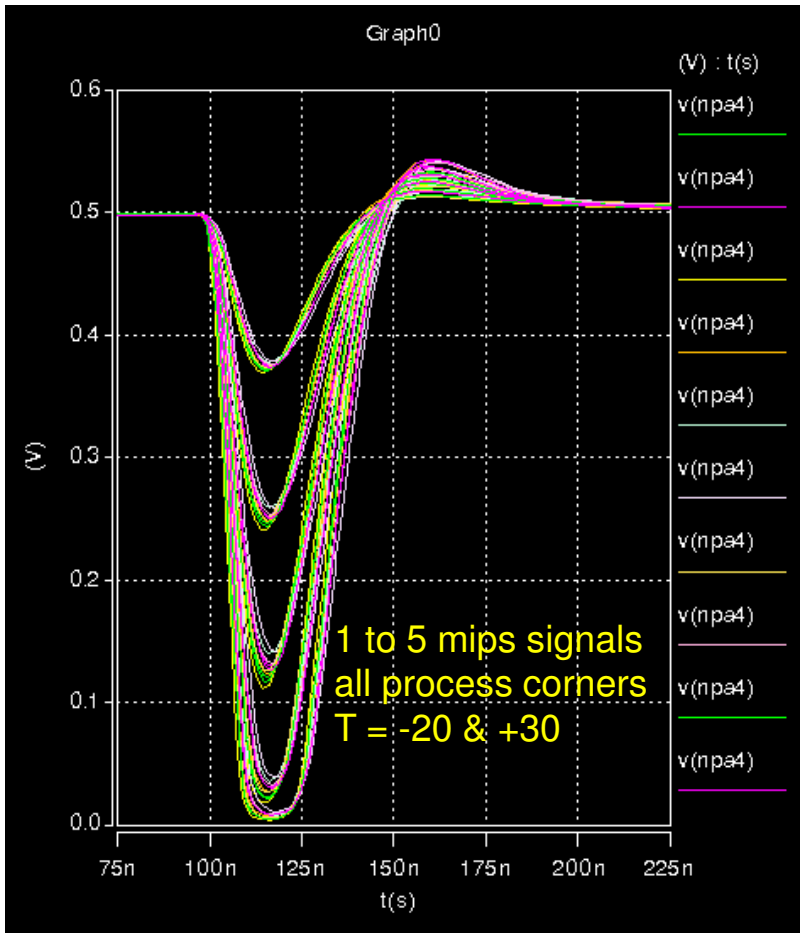
front end optimisation

shorter pulse shape, bug fixes, improved comparator threshold res'n, …

½ strip resolution for cluster width discrimination and correlation logic

CBC3 front end simulated performance

front end amplifier pulse shape

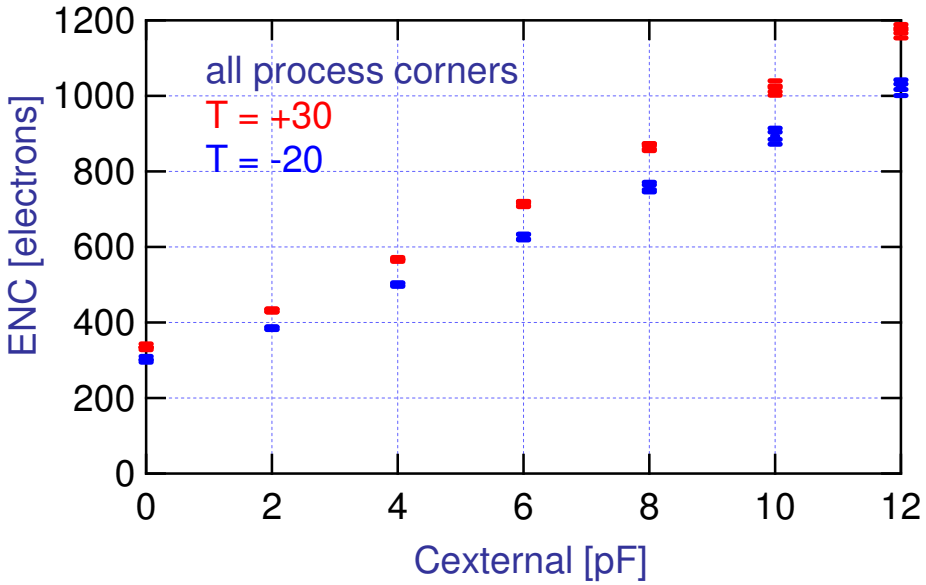


pulse shape width < ~50nsec

=> no dead time due to pile-up

robust to full range of simulation conditions

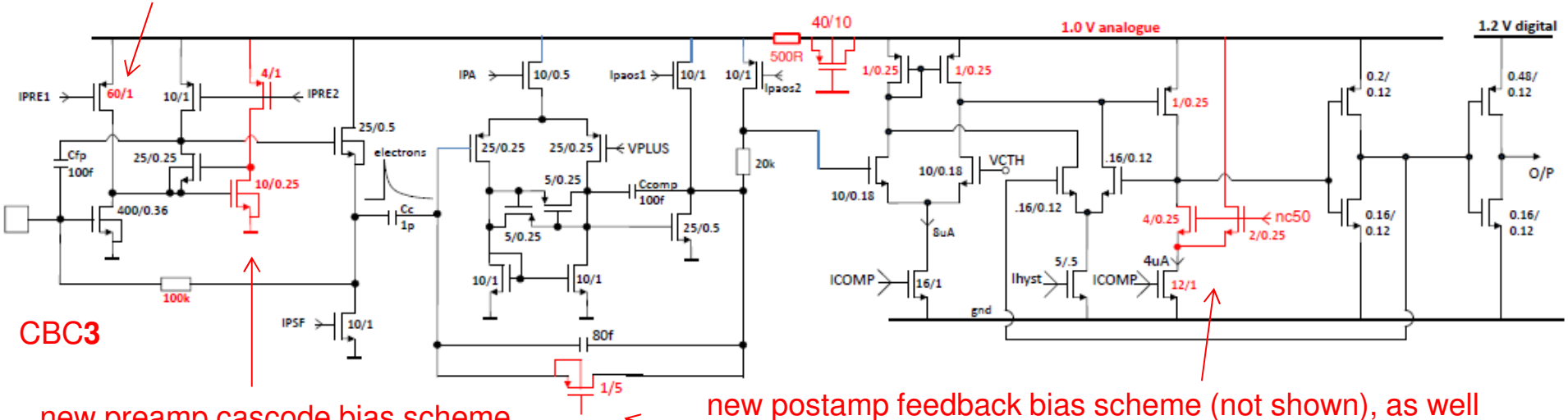
NOISE dependence on external capacitance



< 1000e achievable for Cexternal < 10pF

CBC2 vs. CBC3

increase in bias FET
allows higher currents

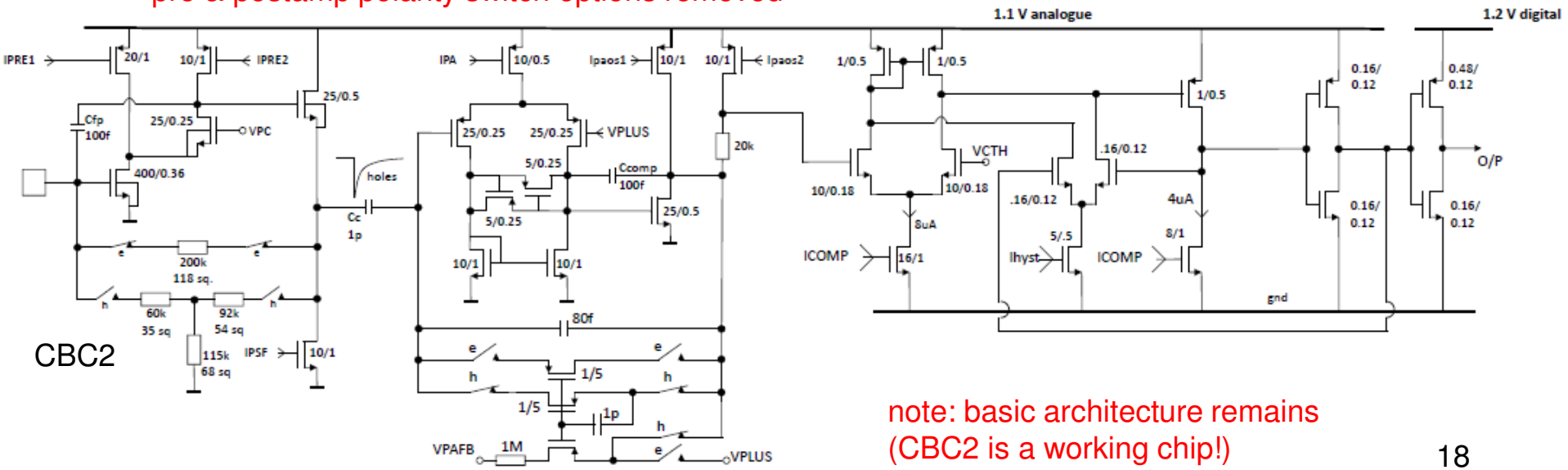


CBC3

new preamp cascode bias scheme
to eliminate “shadow effect”

new postamp feedback bias scheme (not shown), as well as current neutral comparator, addresses CM effects observed when many channels fire

pre & postamp polarity switch options removed



CBC2

note: basic architecture remains
(CBC2 is a working chip!)