CBC3 design status

CMS Tracker Upgrade Week, Phase 2 Electronics, 12th November 2015

Mark Raymond, Imperial College
Mark Prydderch, Michelle Key-Charriere, Lawrence Jones, RAL

introduction

CBC3 intended to be final version for 2S-pT system
- based on CBC2, but:
  - front end optimization, bug fixes, …
  - produces stub addresses and bend info
  - longer pipeline: 256 -> 512 (12.8 usec latency)
  - higher L1 trigger rate capability (up to ~1 MHz)

previous talks
- January tracker week: early design status and plans
  - http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Architecture_and_Plans_29_01_15.pdf
- May tracker week: CBC3 specifications
  - http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_elec_CBC3specs_May_2015.pdf

today
- design status (now well advanced)
  - mainly front end design changes & performance

CBC3 design and simulation constraints

simulation conditions

chip power supply VDDD = 1.2V (on-chip DC-DC conversion dropped)

on-chip LDO provides VDDA

require front end operation at VDDA = 1V minimum

allows headroom for LDO dropout and VDDD tolerance

operational temperature ~ 0 deg.

require good functionality @ -20 and +30

maintain performance for all manufacturing process corners

sensor constraints

n-in-p (electrons), AC coupled, 5 cm strip length (possibly longer)

=> can simplify FE design for one polarity only

(helps to achieve satisfactory operation at VDDA=1V)

performance requirements

pulse shape

peaking time <20 nsec., return to baseline within 50 nsec

noise

target ENC <1000e

things to fix

- leakage current in pipeline at low ionizing doses
  http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_TID_Davide_Nov_14.pdf
  enclosed NMOS devices now implemented

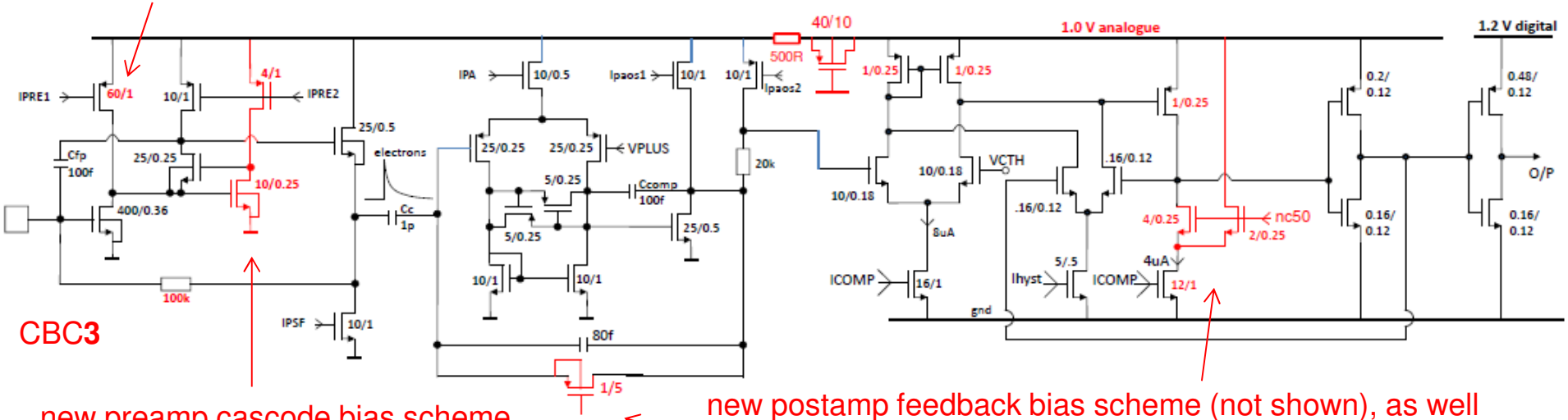
- I2C register SEU immunity could be better
  http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_SEU_Kirika_Nov_14.pdf
  now using Whitaker cells for registers

- CM effect in electrons polarity mode
  shows up when threshold low and many channels firing
  traced to supply current fluctuations when many comparators firing coupling to postamp feedback FET biasing
  http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC2_CM_systems_Jan2015.pdf
  a new method for biasing the feedback FET has been implemented

- so-called “shadow effect”
  when signal injected into many channels, other channels fire, but ~50ns later
  traced to coupling through preamp cascode bias
  http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC2_shadow_effect_Apr_2015.pdf
  can be solved using regulated cascode circuit in the preamp

CBC2 vs. CBC3

increase in bias FET
allows higher currents

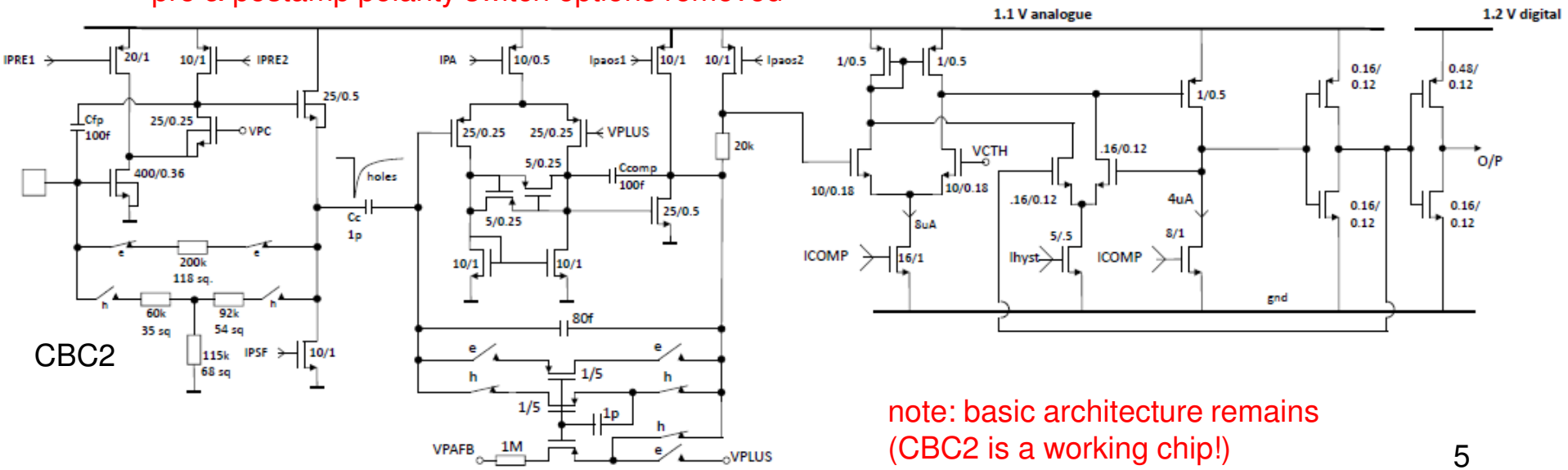


CBC3

new preamp cascode bias scheme
to eliminate “shadow effect”

new postamp feedback bias scheme (not shown), as well as current neutral comparator, addresses CM effects observed when many channels fire

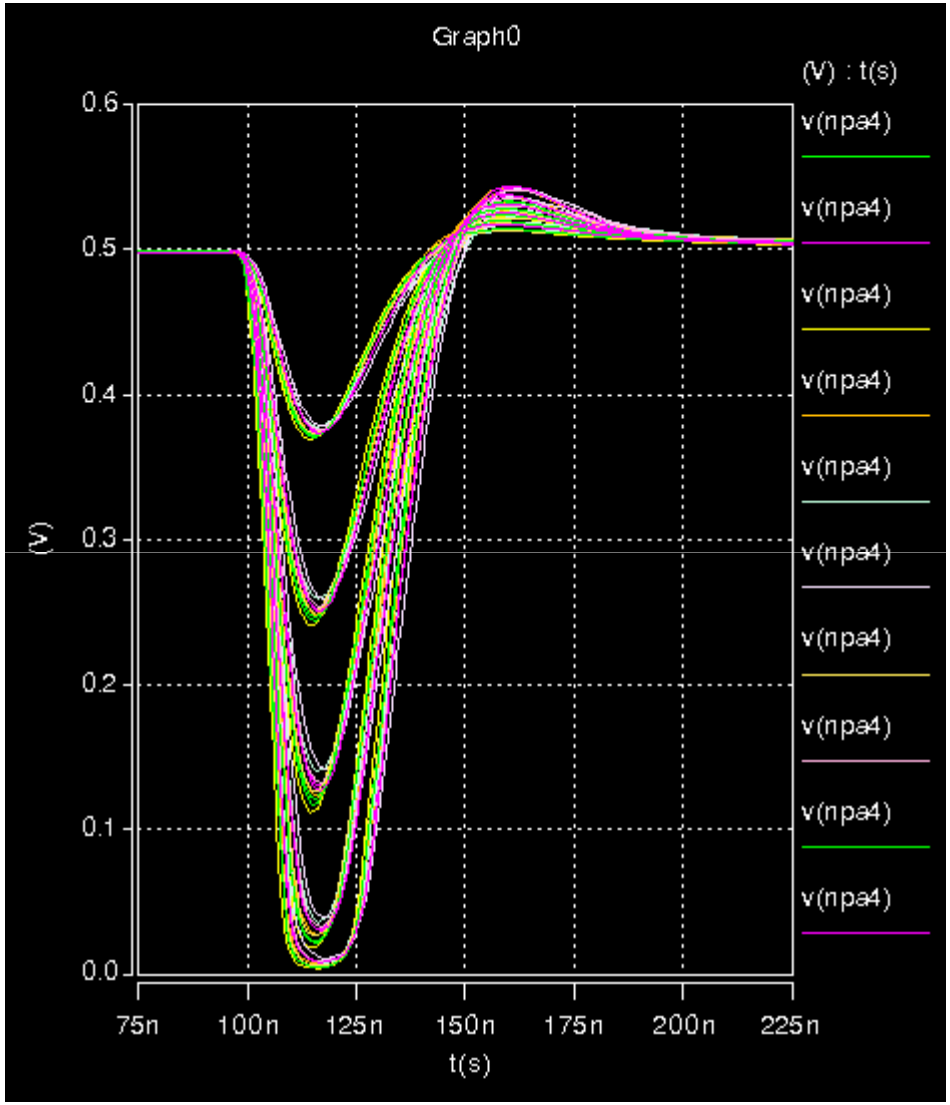
pre & postamp polarity switch options removed



CBC2

note: basic architecture remains
(CBC2 is a working chip!)

CBC3 amplifier performance: pulse shape



pulse shapes at postamp output

2.5 fC to 12.5 fC, 2.5 fC steps
(one to five mips)

preamp Cin = 10p

all process corners, T = -20 & +30, VDDA = 1V

pulse shape robust to wide range of simulation conditions

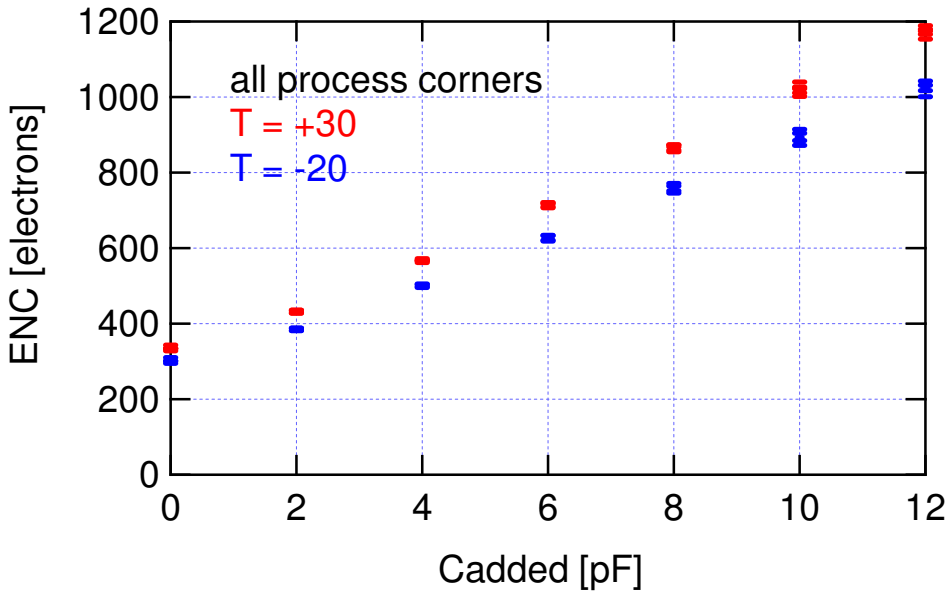
width < ~50 nsec

worth noting: ~ no adjustment needed to cope with process or temperature variations

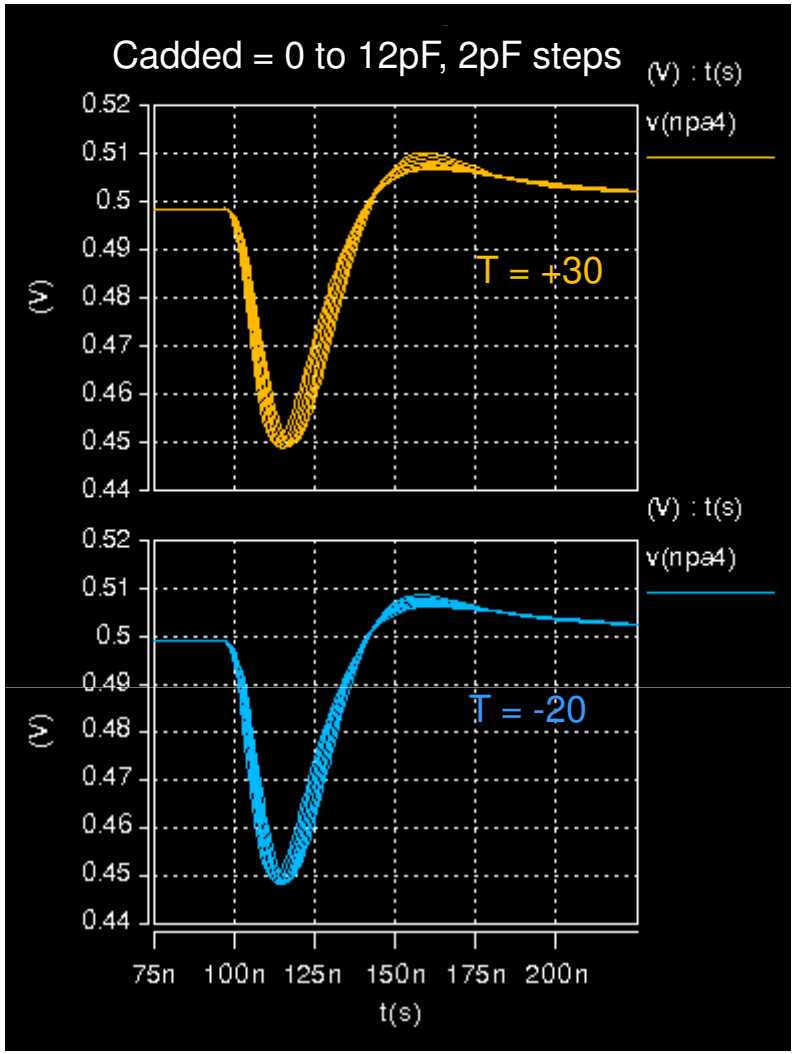
noise performance vs C

dependence on added external capacitance for
fixed 200uA current in I/P FET (240uW)

total front end power ~350uW (preamp+postamp+comp)



< 1000e achievable for Cadded < 10pF



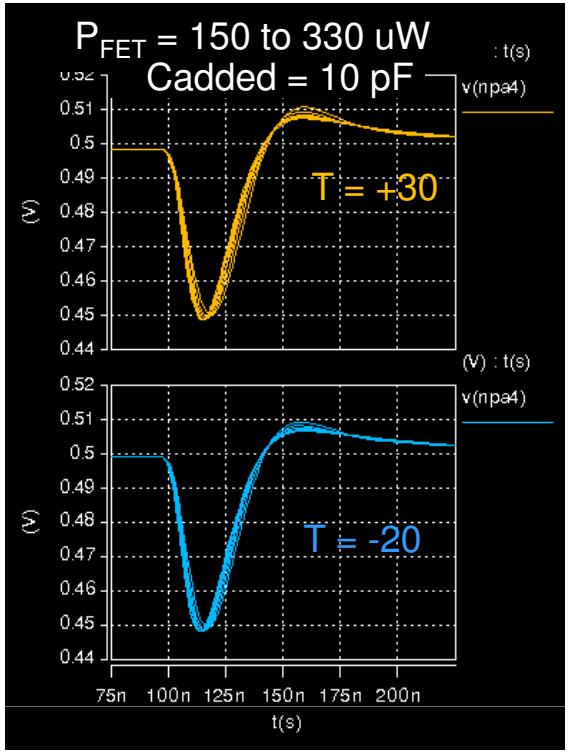
noise vs power

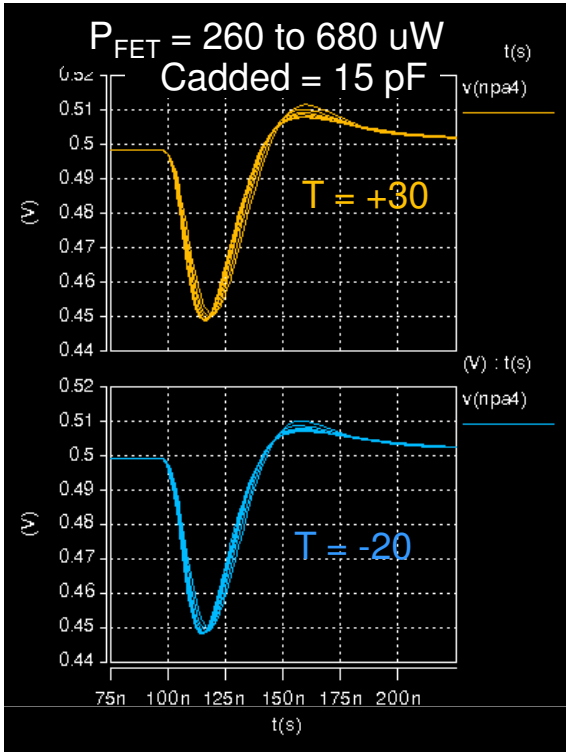
dependence on power for fixed values of Cadded

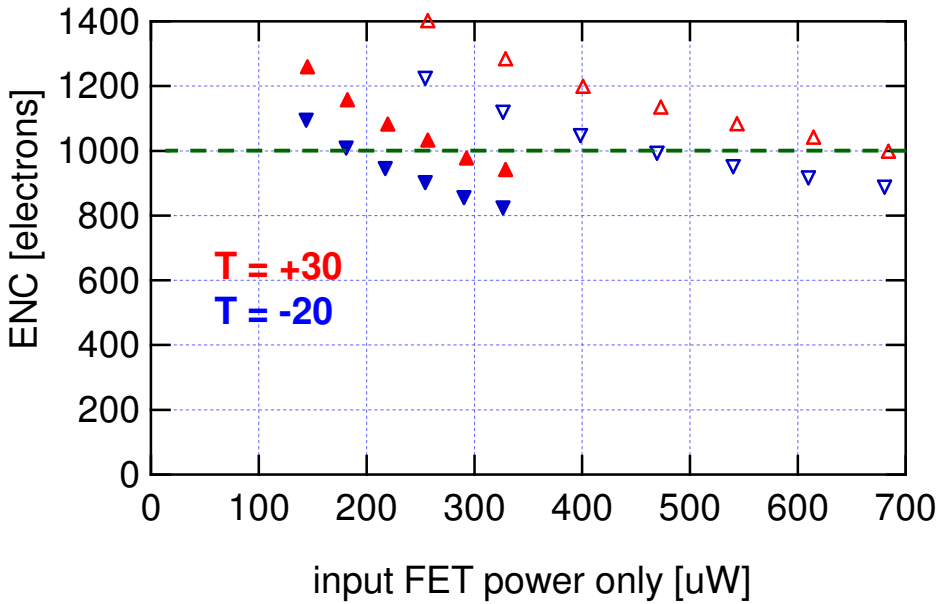
varying current in input FET
($P_{FET} = I_{FET} \times 1.2$)

choose 2 input capacitance values
10 pF and 15 pF

simulations for typical process params only, T = +30 and -20







closed symbols
Cadded = 10 pF total (2 stray + 8 sensor)
<1000e for ~250uW in I/P FET (for T~0)

open symbols
Cadded = 15 pF total (2 stray + 13 sensor)
<1000e for ~600uW in I/P FET for (T~0)

(must add ~100uW for rest of front end
+ digital as well)

CBC3 digital functionality

reminder of main changes/new features

stub gathering logic, address and bend transmission
- 8 bit stub seed address (1/2 strip resolution)
- 4 bit bend info (location of cluster in window layer)

up to 3 stubs data transmitted to CIC /BX
- 6 diff pairs @ 320 Mbps

pipeline cell modifications and length increase (12.8usec)

single 320 Mbps fast control line

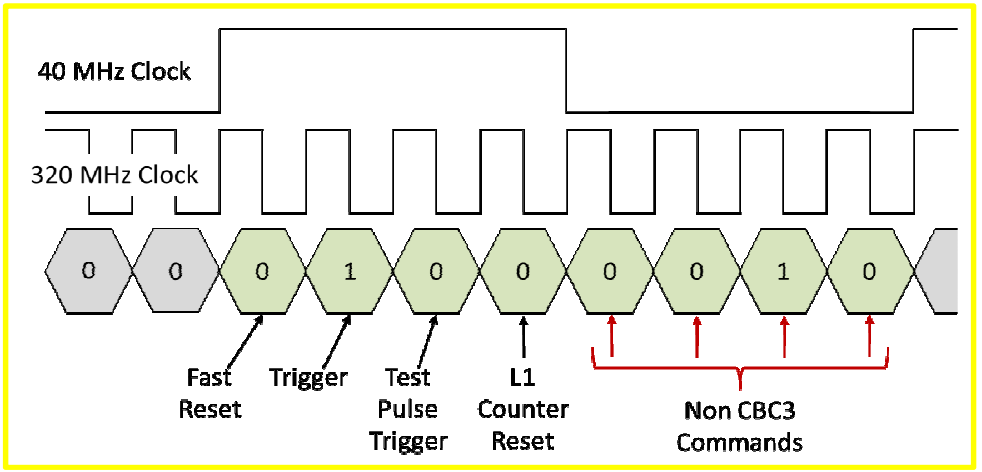
up to 1 MHz L1 triggering capability
- readout data frame < 1 usec

output data

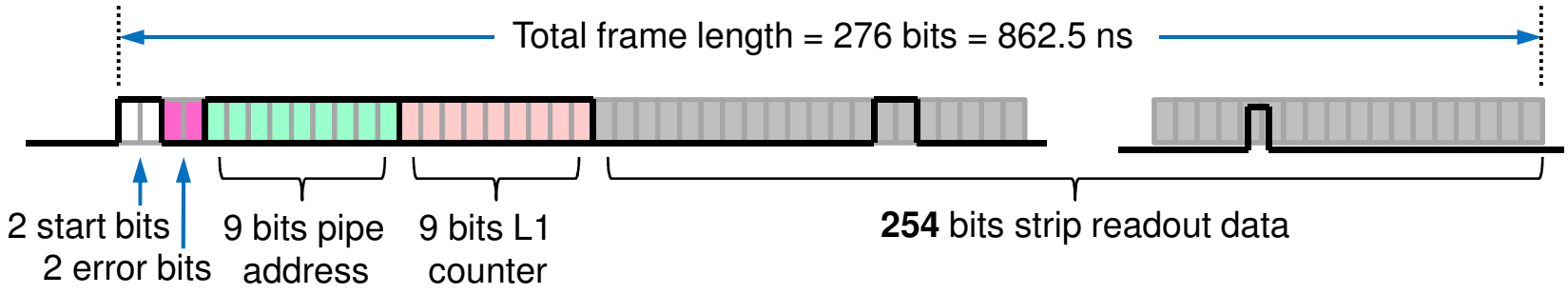
25 ns

S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	SoF	**R**
S1	S2	S3	B2	OR254	**R**
S1	S2	S3	B2	Error	**R**
S1	S2	S3	B2	**Sync**	**R**

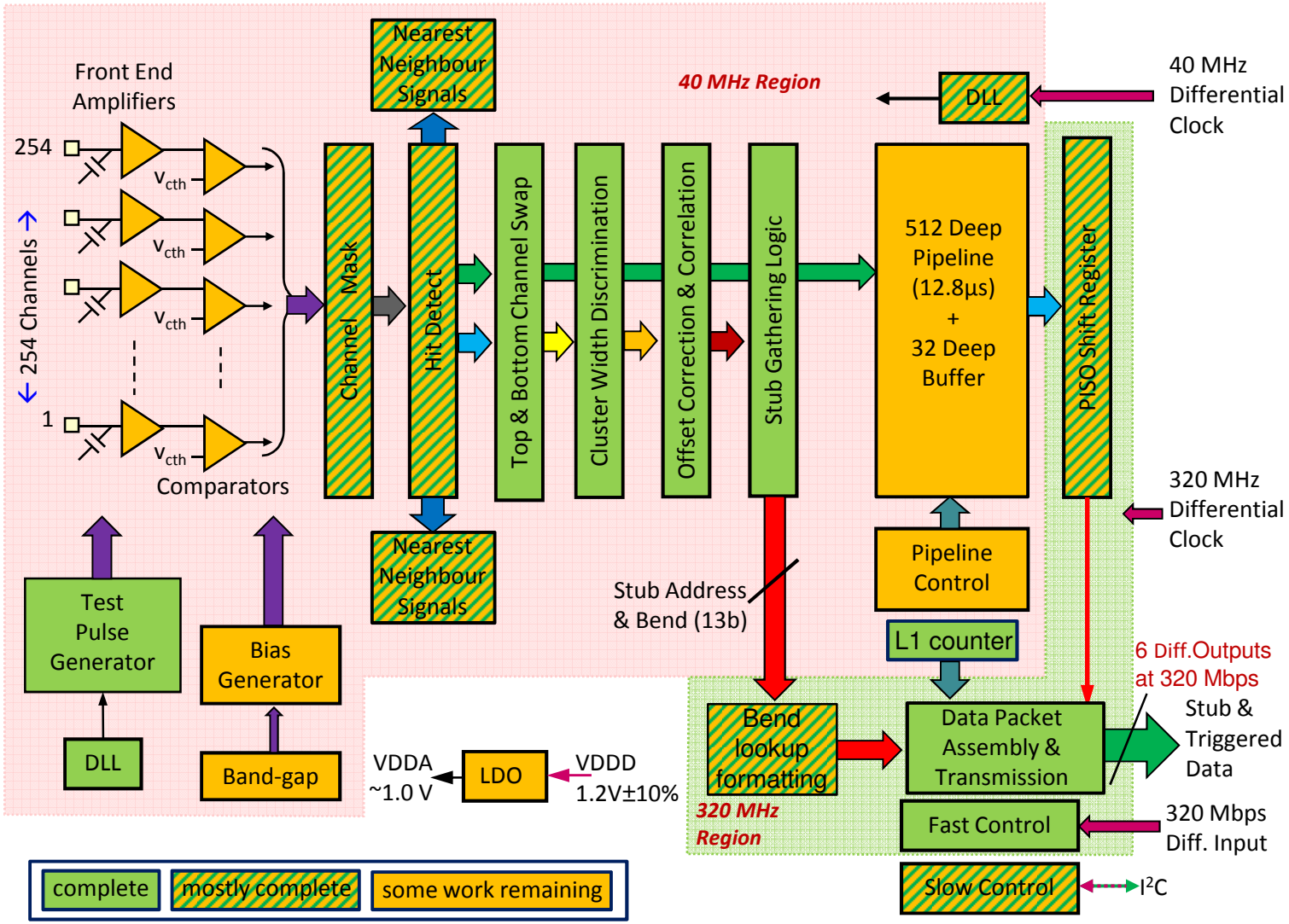
(R = L1 triggered readout data)



Readout data frame



digital blocks progress



CBC3 powering: bandgap & LDO

planning to use PMOS based bandgap design (CERN - Jan Kaplon)

good radiation hardness
ionizing and displacement

but stronger process dependence
=> need mechanism to trim

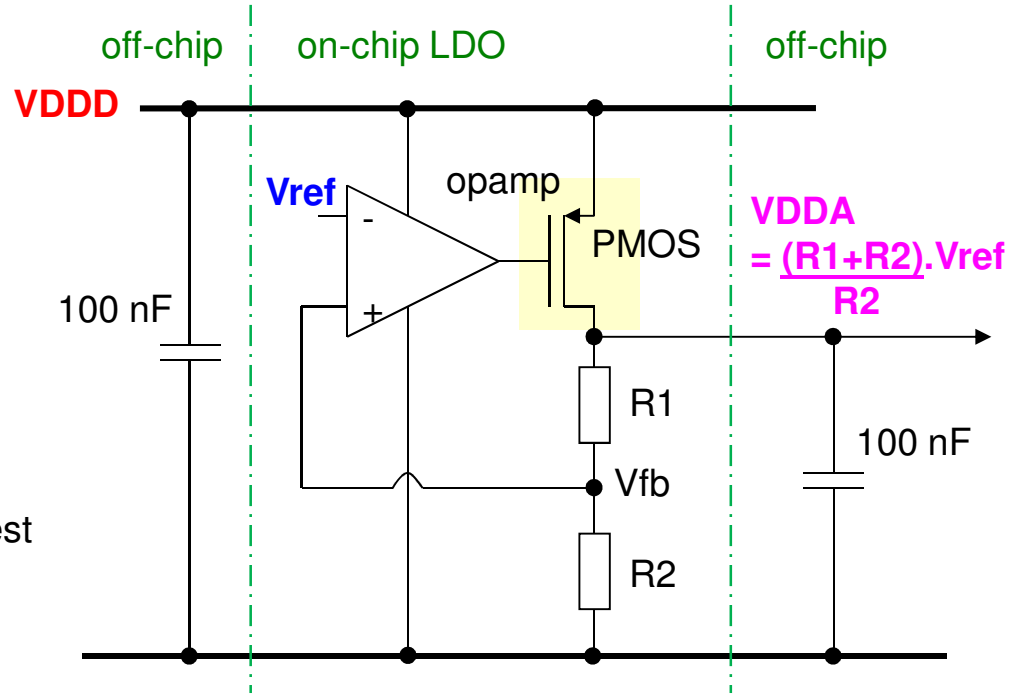
can use e-fuses
electrically programmable during wafer test

procedure

take Vref for LDO from PMOS bandgap

use I2C register to trim VDDA to desired value during wafer test

use e-fuses to fix default register value (default = value after power-on or hard reset)



also plan to use e-fuses to program unique chip identifier at wafer test

further details

CBC3 specs

http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_elec_CBC3specs_May_2015.pdf
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p12.docx

front end design and performance

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_FE_status_June2015.pdf
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_systems_Sept2015.pdf

more detail on digital blocks

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_systems_July2015.pdf

simulated multi-channel hips response

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_systems_Sept2015.pdf

summary

front end amplifier & comparator design complete

- design meets specifications
- layout and post-layout simulation still to be done

digital and other design blocks

- no major design outstanding, but still some work to do

expect to submit in February

- plan now to share wafer with other projects on separate run (not through MOSIS)
- will get many more chips this way
- hope for chips in hand in middle of year