CBC progress report

CMS Binary Chip

130nm CMOS chip for short strip readout at sLHC

contents

- introduction and status
- test results
- future directions

CMS Upgrade week, May 2011.
Mark Raymond, Imperial College.

CBC introduction

key features

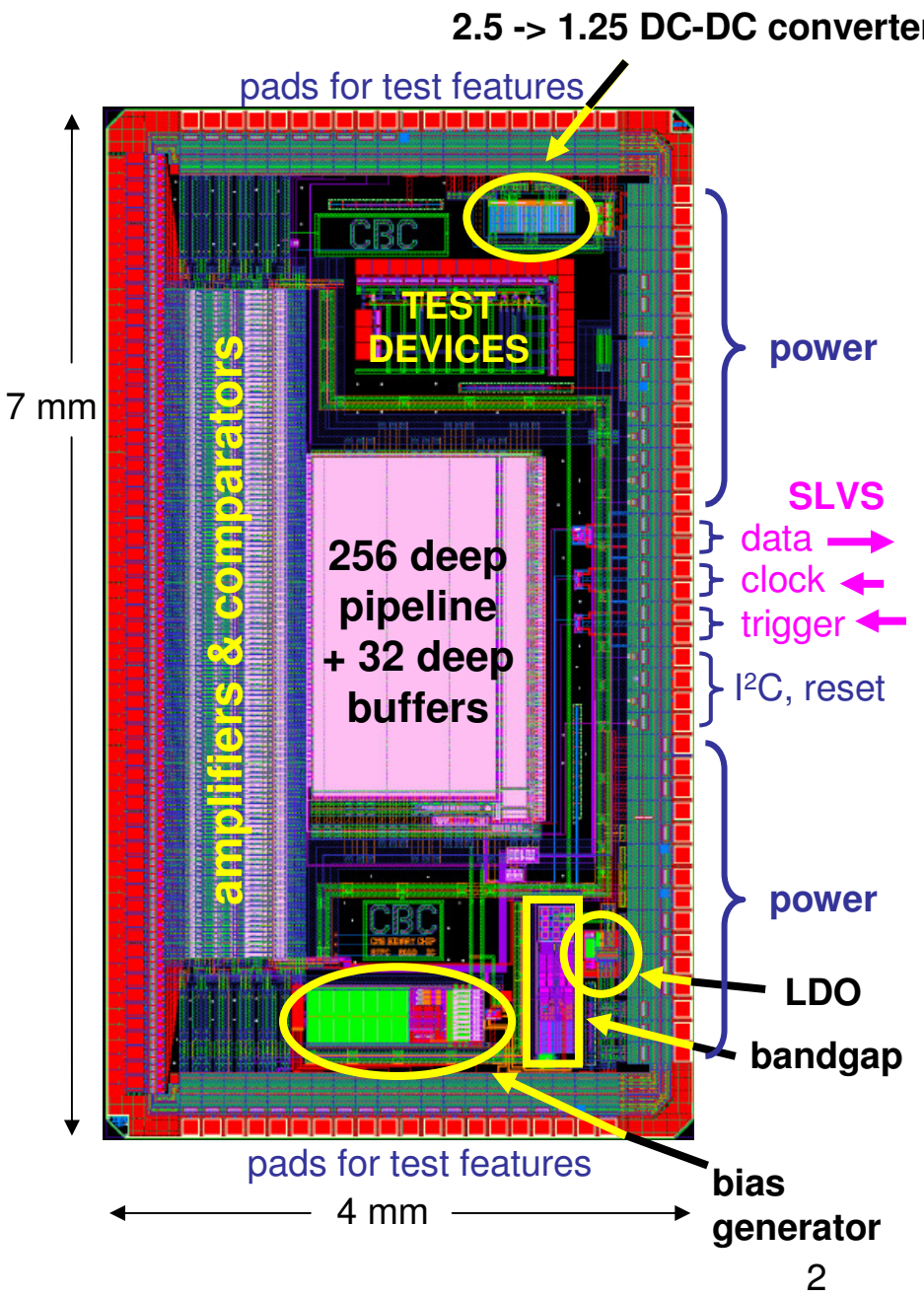
- designed for short strips, ~2.5–5cm, < ~ 10 pF
- full size prototype - 128 channels (50 μm pitch)
- not contributing to L1 trigger
  (could be adapted to 2-in-1 type triggering)
- binary un-sparsified readout
  chip & system simplicity, low power
- powering test features
  2.5 -> 1.2 DC-DC converter
  LDO regulator (1.2 -> 1.1) feeds analog FE

main functional blocks

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- output shift register and SLVS driver
- fast (SLVS) and slow (I2C) control interfaces

some target specs

- DC coupling to sensor – up to 1 uA leakage
- can be used for both sensor polarities
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  < 0.5 mW/channel for C_{SENSOR} ~ 5 pF



status

chip design begun ~ March 2009 in 130nm IBM CMOS
lead engineer: Lawrence Jones, RAL

submission: July 2010, expected turnaround ~ 3 months (~ end October)

unexpected delays - foundry busy, Christmas,..

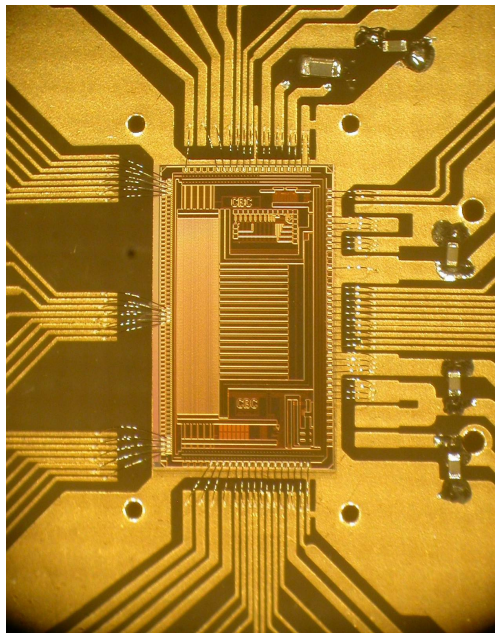
=> chips under test since 14th February

testing status

early test results presented ACES workshop - March 10th

testing status now more mature
will present some new results today
all features functionality looked at
.. but some in more detail that others

test setup



dummy channel
interface board
fast & slow control
& data out interface
test
charge
injection
CBC test board
~ 22 x 22 mm²
bias generator
test board

basic functionality

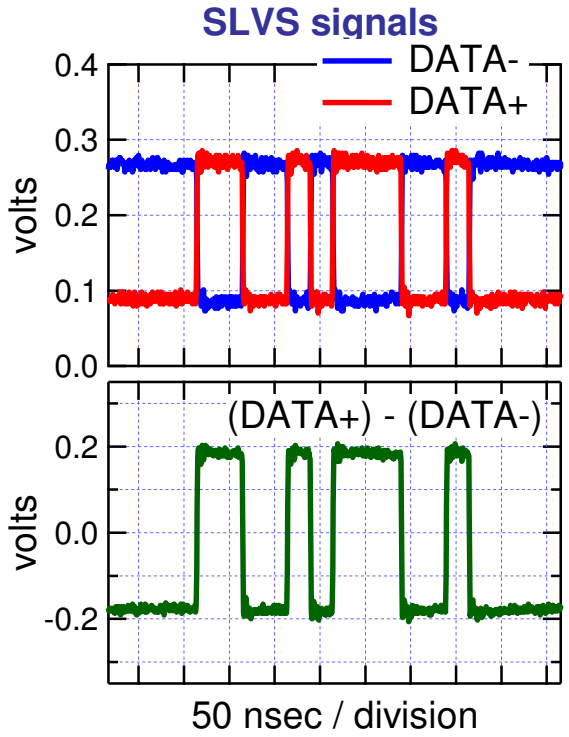
communication interfaces

fast: SLVS (Scalable Low Voltage Signalling)
SLVS circuits provided by CERN (S. Bonacini, K.Kloukinas)
used for 40 MHz clock I/P, L1 trig and data out

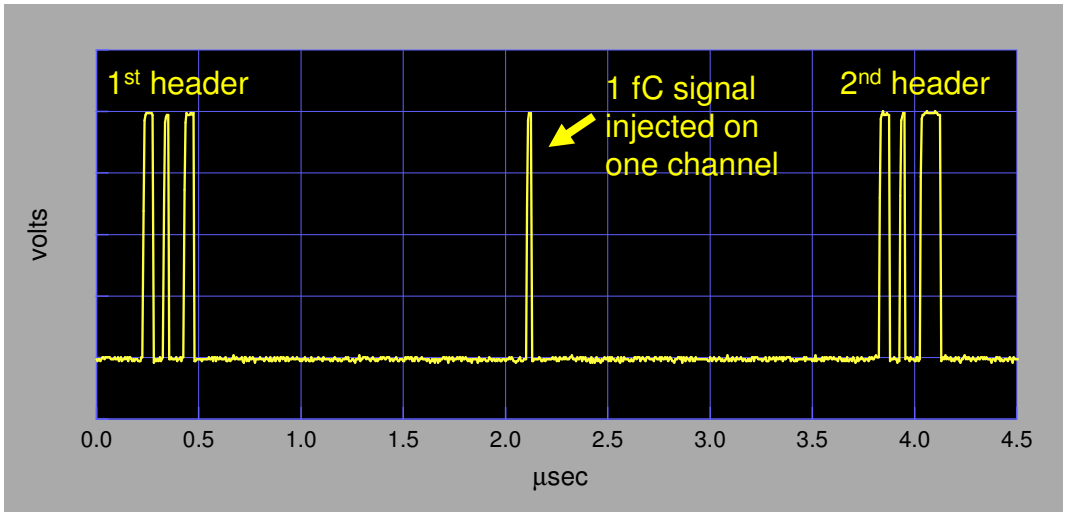
slow: I2C - used to programme
bias generator
operational modes, latency,..
128 comparator threshold trim values

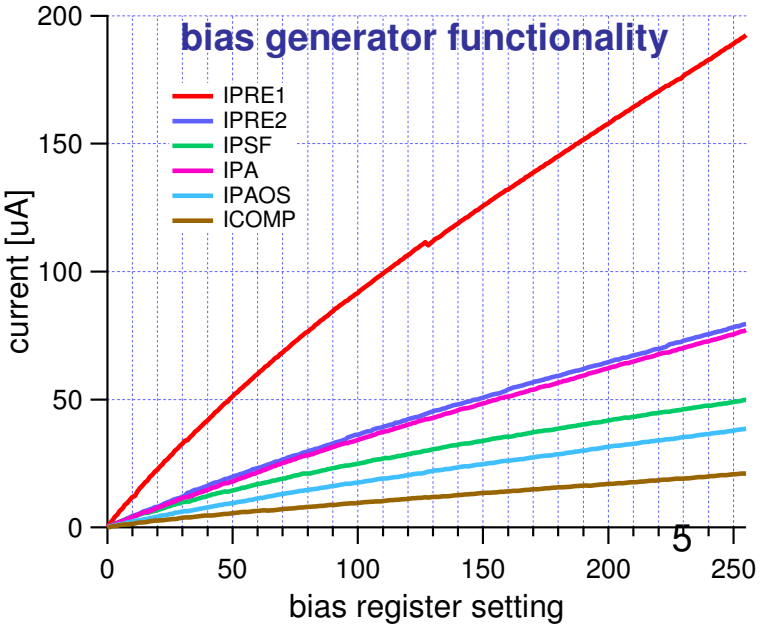
output data frame

following trigger get 12-bit header
2 start bits, 2 error bits (latency, fifo overflow), 8 bit pipe address
followed by 128 channel bits



e.g. 2 consecutive data frames (2 triggers)



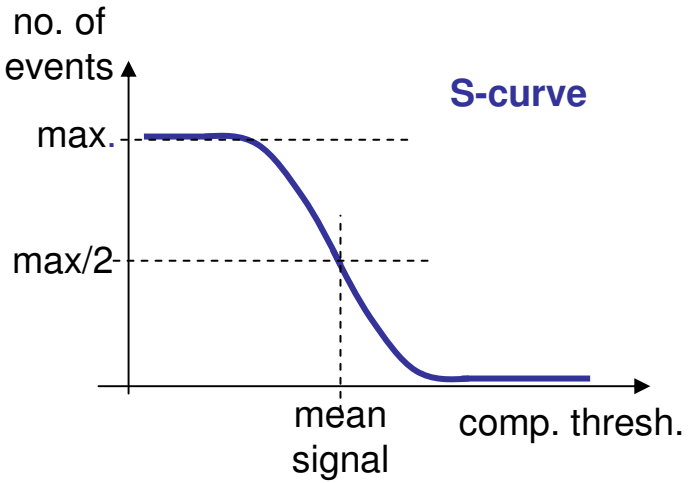


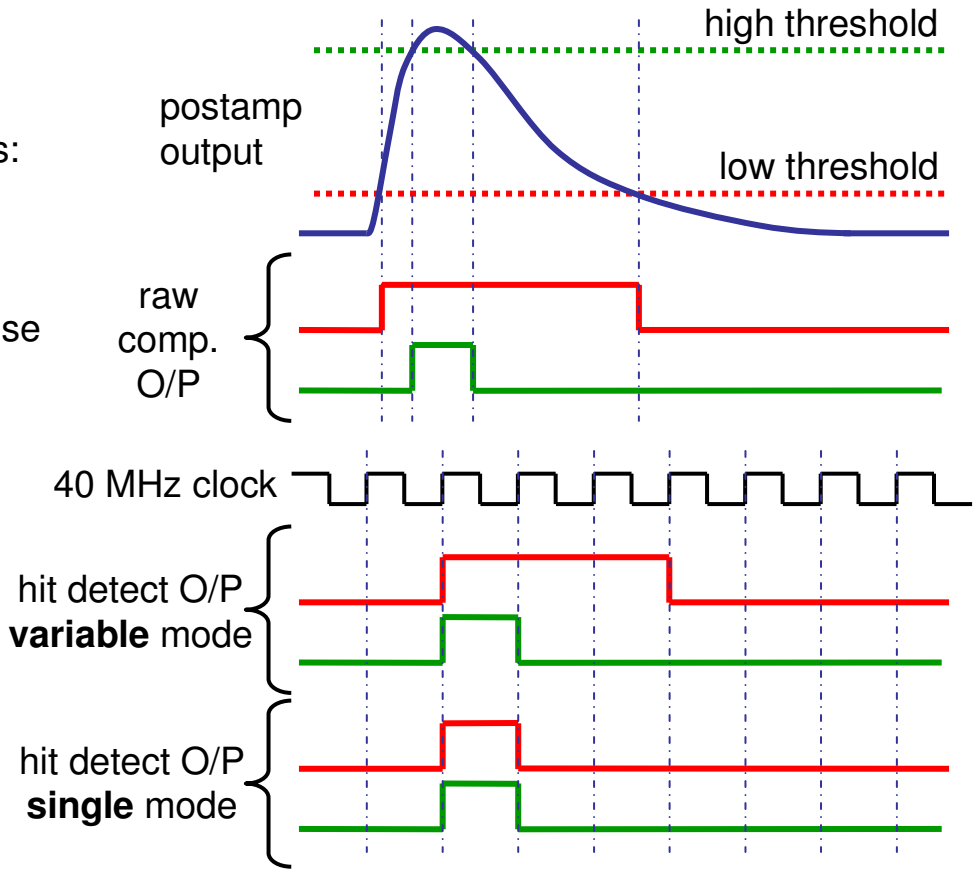
testing front end performance using comparator

can learn a lot about front end performance by varying:
- comparator threshold
- time and magnitude of injected charge

CBC has “hit detect” circuit which operates in 2 modes:
- ***variable*** - raw comp. O/P sampled into pipeline
  consecutive pipeline samples high as long as comp. O/P stays high
- ***single*** - comp. O/P shortened to single 25ns pulse
  only one sample in pipeline however long comp. O/P stays high

can look at S-curves
- no. of events vs. threshold value
  -> noise and gain studies





hit detect functionality

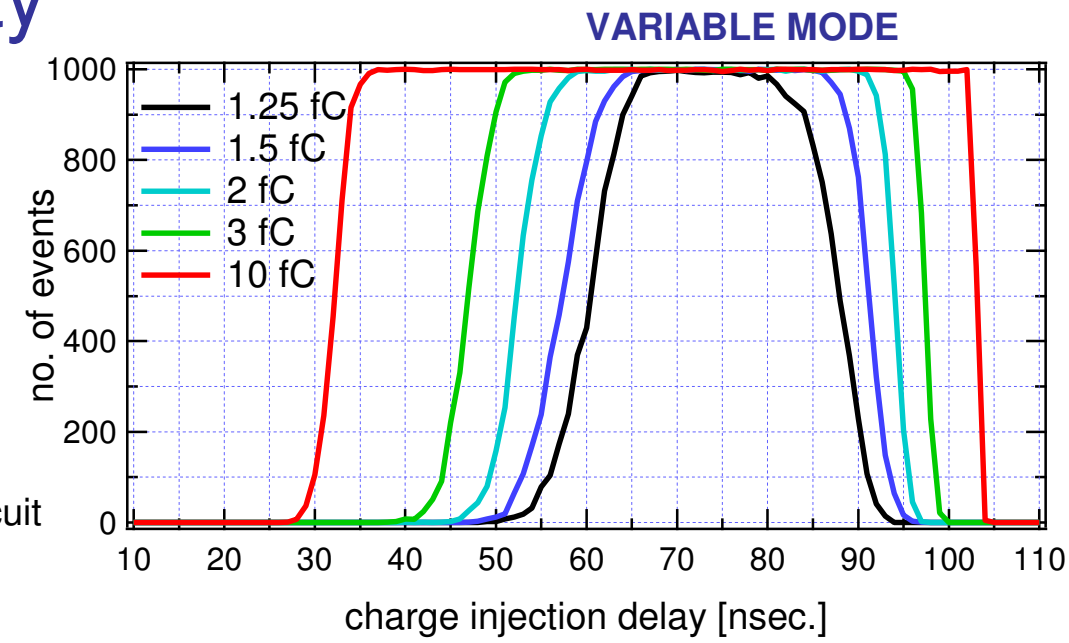
sweep signal charge injection time for both modes of operation

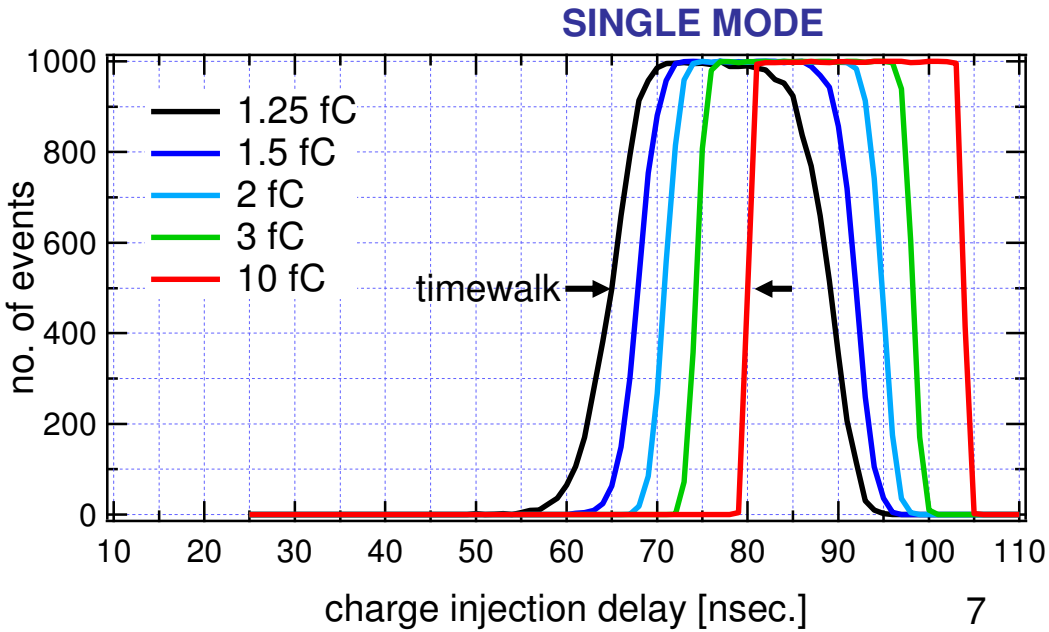
comparator threshold fixed at 1 fC

VARIABLE mode picture shows pulse width increasing as signal amplitude increases

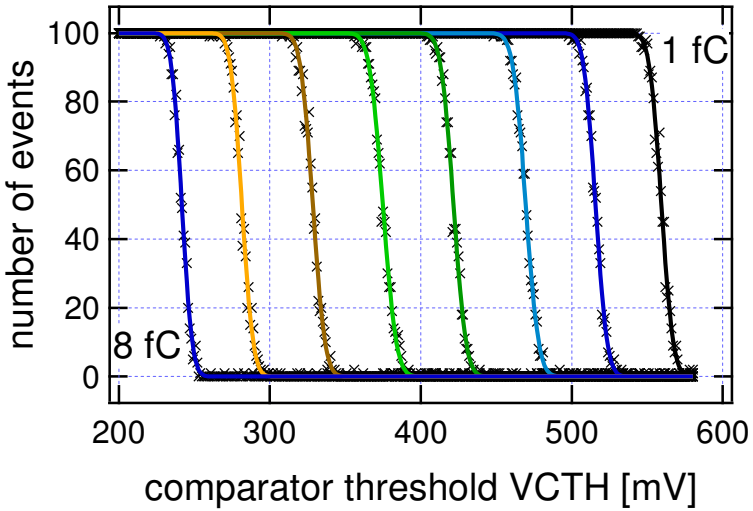
SINGLE mode picture shows *hit* detect circuit keeps pulse width at 25 ns

timewalk ~ 15 ns
(just within spec.)



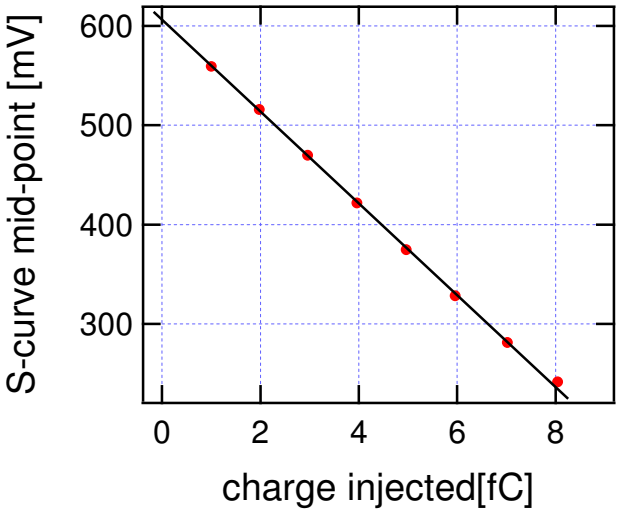


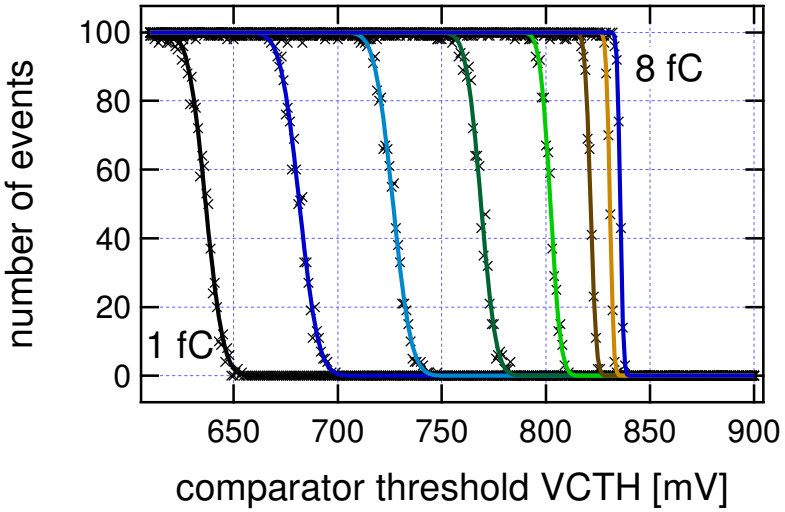
S-curves and gain



electrons mode

gain ~ 50 mV / fC
signals in range 1 - 8 fC
in 1 fC steps

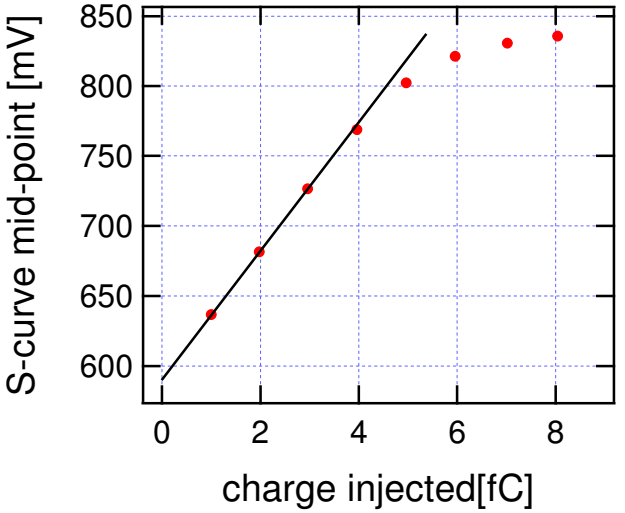




holes mode

gain ~ similar

dynamic range more limited - but still linear in region where normal comp. threshold will be set



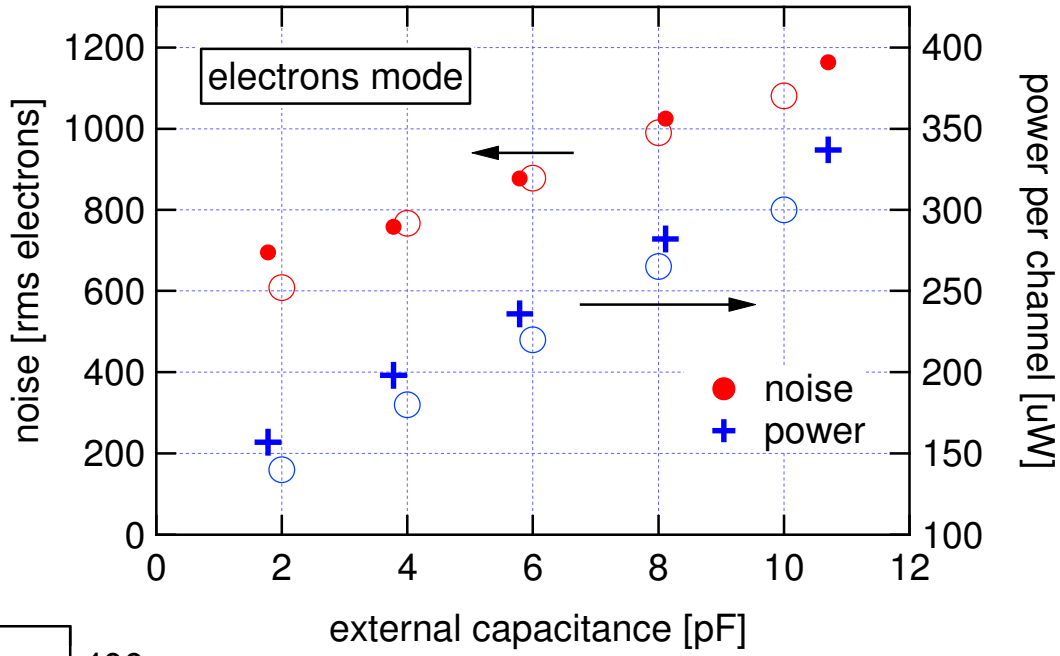
noise

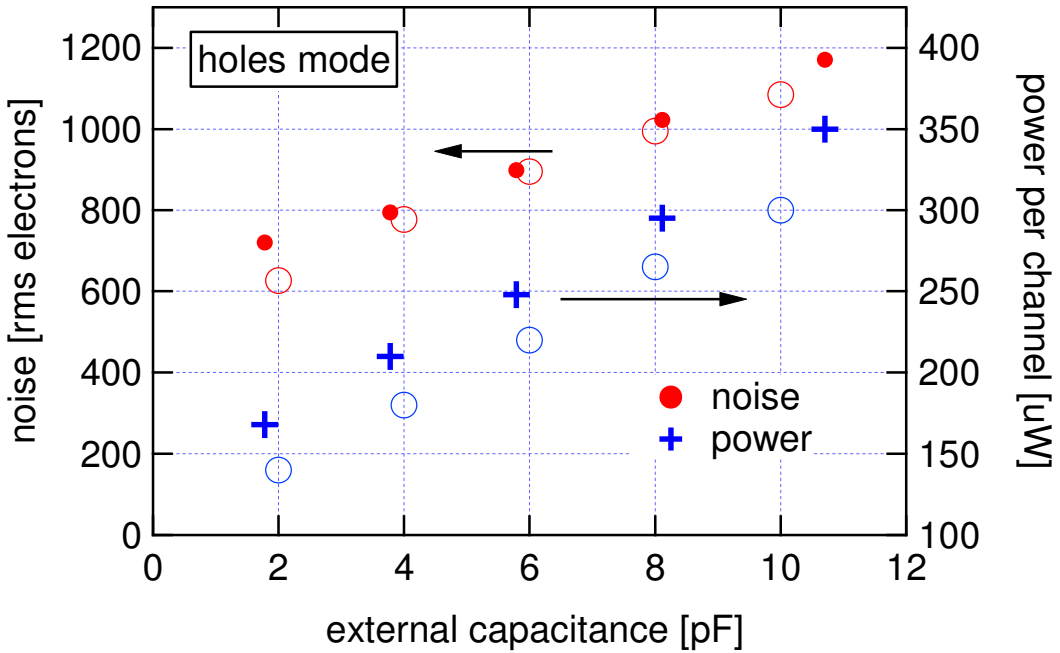
plots show dependence on external added capacitance in both operational polarities

current in input transistor adjusted to maintain pulse shape - so overall analogue power varies

results very close to simulation (open circles)

target spec. < 1000e for 5 pF sensor





power consumption

target 0.5 mW / channel based on:

analogue: 150 - 300 uW - sensor capacitance dependent simulation

digital: ~ **300 uW** - rough estimate (including 150 uW contingency)

measured

digital

I_{VDDD} = 2.8 – 4.5 mA for whole chip (depending on SLVS bias setting)

< 50 µW / channel

no measurable dependence on L1 trigger rate (0 – 100 kHz)
digital circuitry functions correctly down to V_{DDD} = 0.9V

analogue

depends on sensor capacitance (see noise slide)

130 + (21 x C_{SENSOR}[pF]) uW

total

180 + (21 x C_{SENSOR}[pF]) uW

e.g. < 300 uW for 5 pF sensor capacitance

(c.f. APV25 ~3.6 mW / chan. (for long strips))

comparator threshold uniformity

all channels have same
comparator global threshold (VCTH)

individual channel tuning achieved by
introducing programmable offset on the
comparator input signal

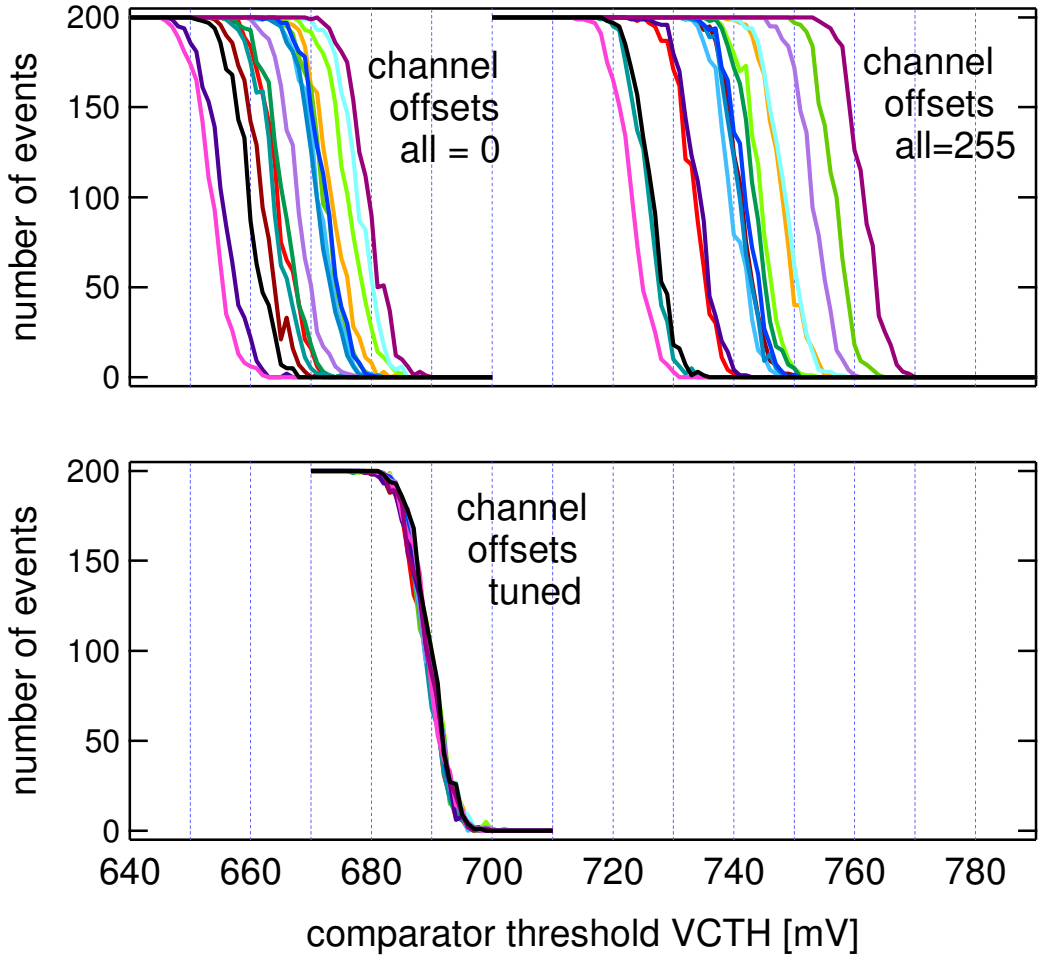
128 registers, 8-bit precision

peak-to-peak threshold spread ~ 30 mV

< 1 fC before tuning

pictures demonstrate effectiveness of
tuning to achieve comp. threshold matching

~ mV precision achievable



power features

CBC incorporates powering features

DC-DC switched capacitor converter
(CERN - M.Bochenek et al)

converts 2.5 -> ~ 1.2

clearly functioning

effect of switch noise needs careful study

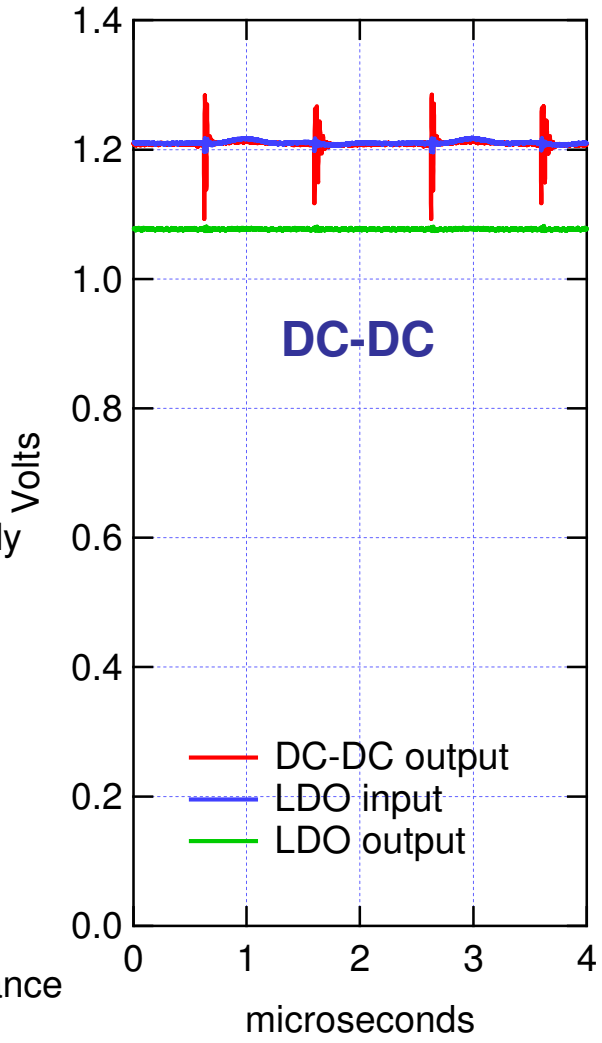
LDO linear regulator
regulates ~ 1.2 -> 1.1

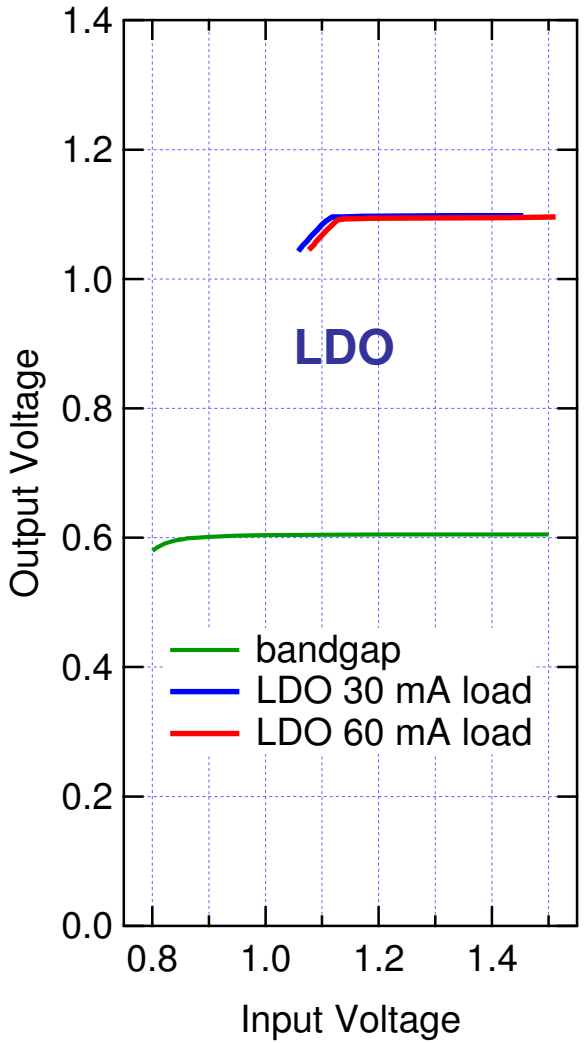
uses CERN bandgap (0.6 V)

“clean” 1.1 rail feeds analogue front end

DC measurements show good performance

dropout < 40 mV for 60 mA load





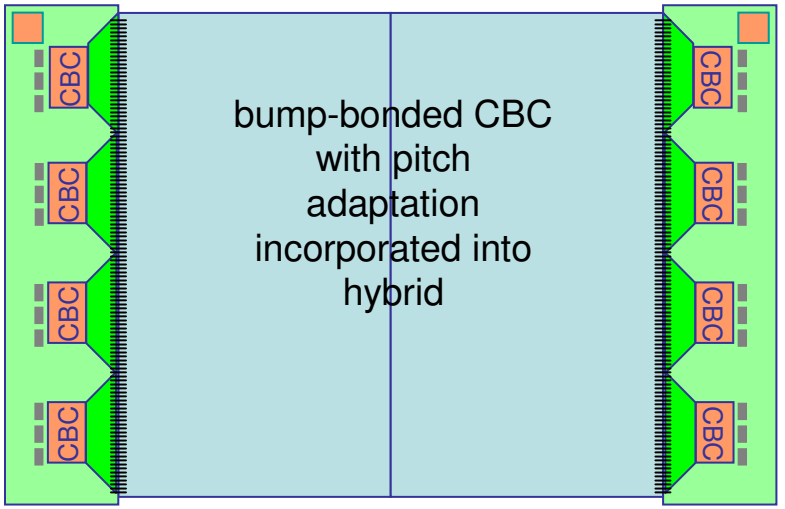
detailed evaluation of AC behaviour (power supply rejection) underway

future directions

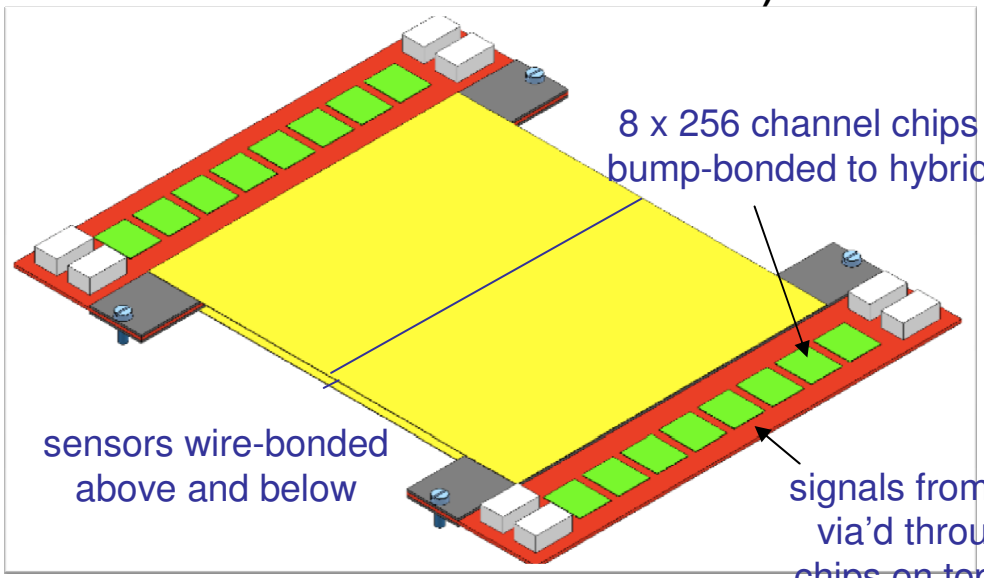
currently looking at:

1) bump-bonded version

allows to integrate pitch adaption to sensor on hybrid
hybrid has to be “hi-tech” substrate
fine pitch bonding (C4 ~ 250 μm) and tracking
chip layout should proceed in parallel with substrate design
things to learn about hybrid technology and impact on chip
plenty of scope for collaboration here



2) 256 channel version with 2-in-1 triggering capability



existing CBC L1 triggered short strip chip can be adapted to provide 2-in-1 type trigger data for CMS outer tracker

need

cluster width discrimination
offset and correlation
trigger formation and transmission

summary

130 nm CBC prototype working quite well

already providing valuable information

e.g. performance achievable and power budget required

long testing programme ahead, including

powering options studies - supply sensitivity with/without various on-chip options

temperature effects

tests with sensors

radiation: ionizing & SEU sensitivity

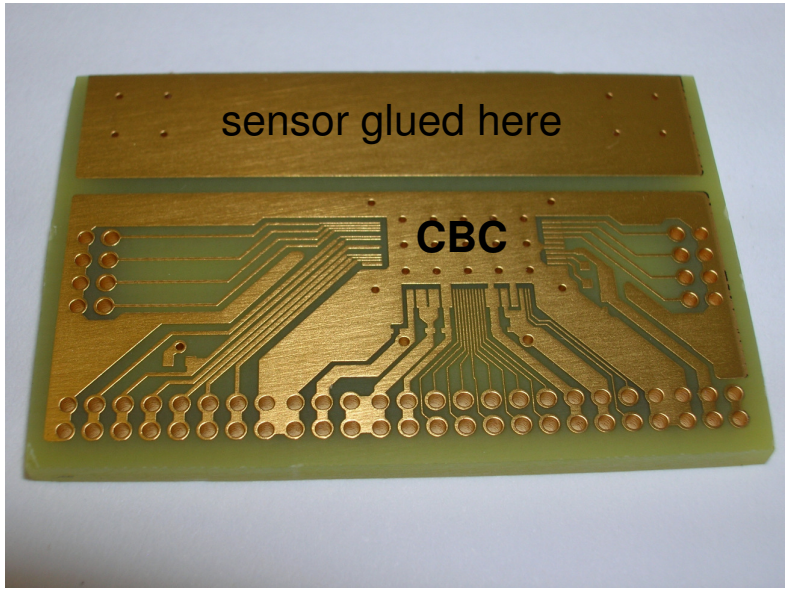
test beam

CBC documentation:

http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/

user manual and detailed test report will appear soon

single CBC + sensor test board



EXTRA

testing programme

baseline performance (conventional (clean) powering scheme)

- **digital functionality**
  - fast (Ck/T1 - SLVS) & slow control (I2C) interfaces setup and operation
- **analogue functionality**
  - amplifier
    - pulse shape, noise, linearity,..
      - C_{IN} dependence, signal polarity dependence, across chip & chip-to-chip uniformity
    - leakage current tolerance
- **comparator**
  - timewalk, threshold tuning and uniformity, hysteresis

all above will depend on bias generator settings
=> large parameter space to cover

power consumption

lots to study
have only scratched the surface so far

powering options studies

supply sensitivity with/without various on-chip options

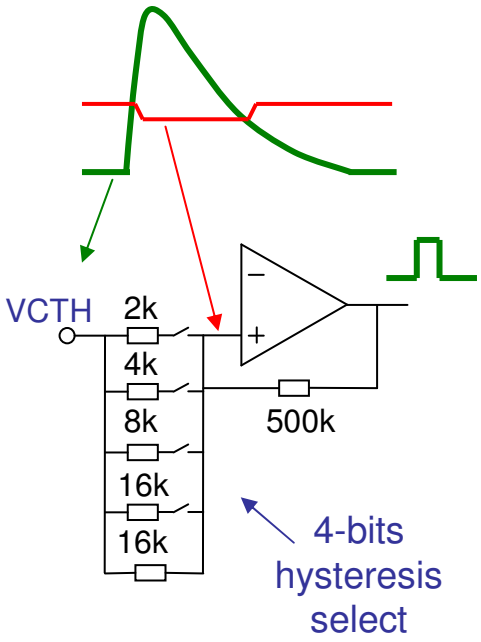
longer term

temperature effects (~ all of above vs. T)
tests with sensors
radiation: ionizing & SEU sensitivity
test beam

problems so far

not everything perfect – a couple of things have shown up so far

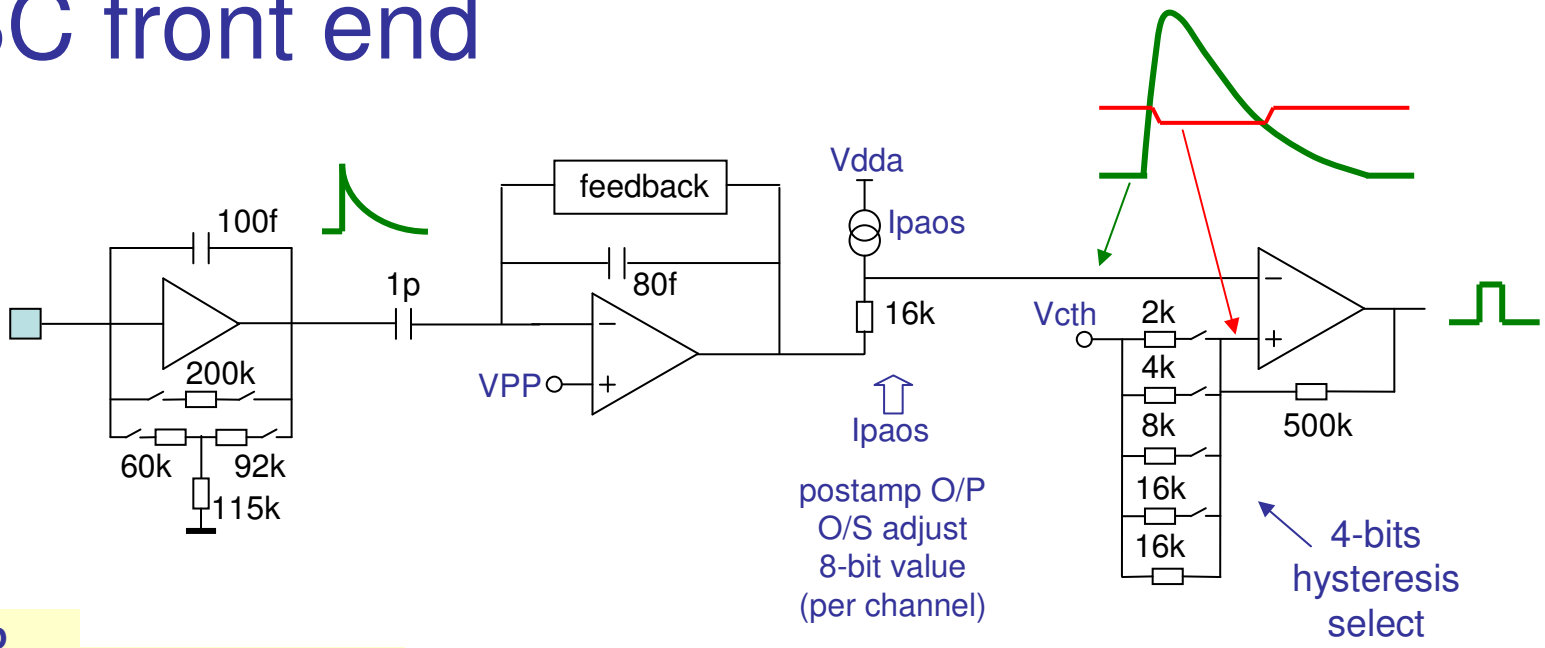
1) global comparator threshold voltage output (VCTH)
    get interaction between multiple channels and VCTH
        comparator has 500k feedback resistor (for hysteresis)
        but 128 x 500k resistors in parallel -> 4k (not so big)
        so VCTH gets pulled around if many channels switch at once
    would not have shown up on test chip with just a few channels
    can be fixed by providing external voltage
    probably not difficult to fix by design



2) another of the bias generator outputs needs external decoupling
    ~ similar effect associated with postamplifier

2) dummy analogue channel doesn't provide clean signals
    can be used to study DC behaviour, but transient response shows ringing
        may be due to test board layout – coupling between outputs and inputs
            will investigate further
    (not really an issue – but would have been if chip had not worked so well)

CBC front end

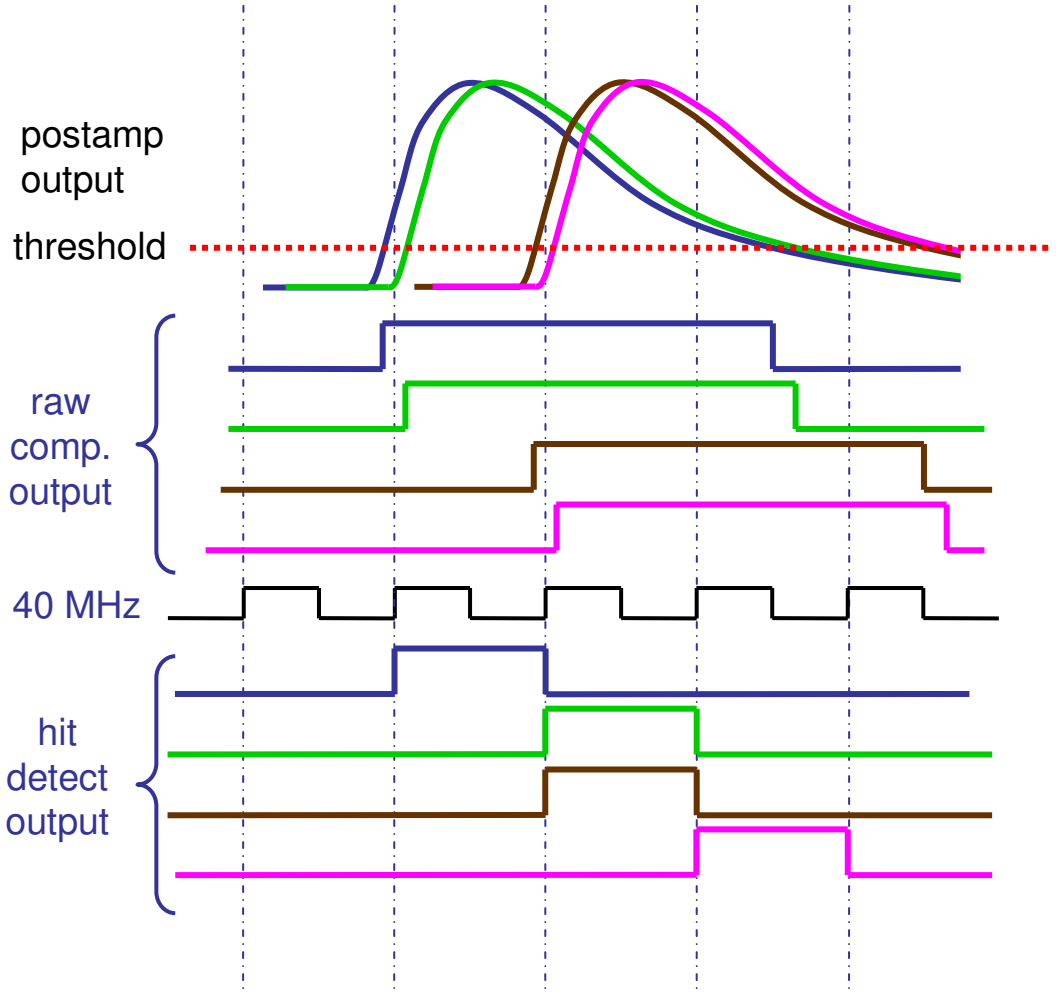


preamp
resistive feedback absorbs I_{leak}
T network for holes
Rf.Cf implements short
20ns diff. time constant
(good for no pile-up)

postamp
provides gain and int. time constant
~ 50 mV / fC
AC coupling removes I_{leak} DC shift
individually programmable O/P DC level
implements channel threshold tuning
8-bits, 0.8 mV / bit, 200 mV range

comparator
global threshold
(indiv. tuning at postamp O/P)
programmable hysteresis)

sweeping charge injection time



hit detect output for a specific timeslice requires the comparator to be triggered within the previous 25 nsec period (e.g. **green** and **brown** signals)

if comparator fires **earlier** or **later** then hit will be in **earlier** or **later** timeslices in the pipeline