CMS Binary Chip status

Outline

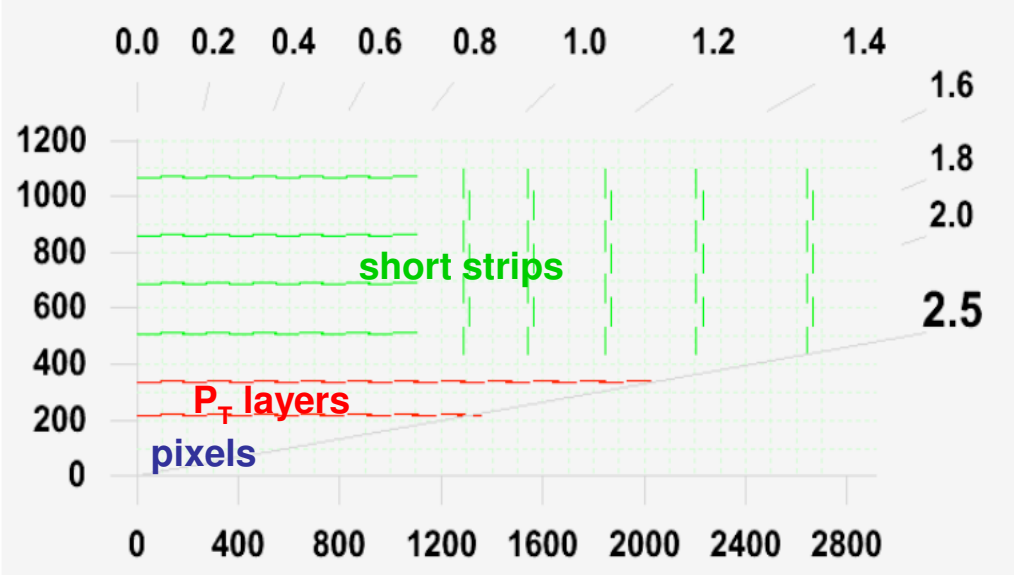
- intro & current status
- brief reminder of architecture, specs and simulated performance
- layout pictures
- testing plans
- future developments
- summary

introduction

CBC targeted at phase II outer tracker region
r > ~ 50 cm

assumed instrumented by short strips
~ 2.5 / 5 cm

assumed not contributing to L1 trigger
separate development for PT layers



environment

sLHC CMS tracker will operate at low T
~ -30 -> -40 degrees
=> important to meet specs at low temperatures
(but will still want to test and run chips and modules at room temperatures)

chip design begun March 2009 in 130nm IBM CMOS
Lawrence Jones (RAL engineer)

current status

MPW data to IBM this week

=> chips back ~ October

CBC design transmission to CERN was delayed by ~ 1 month, to 5th July

extra time needed to finish layout, top-level simulation, final design review, ..

CBC architecture

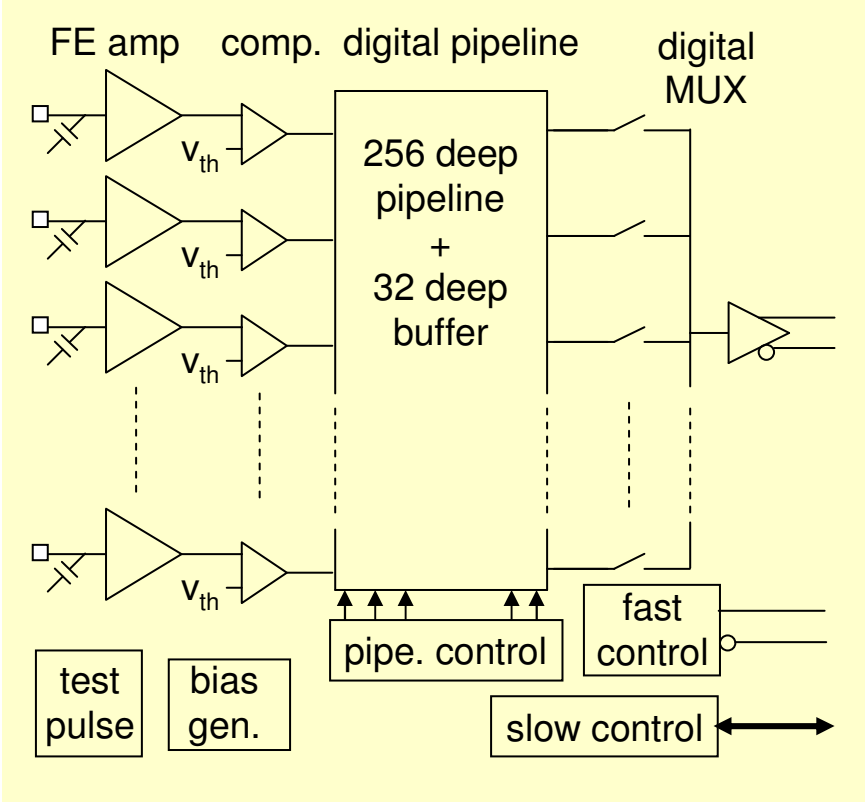
binary un-sparsified architecture
simplicity/robustness, lowest power

main functional blocks

- fast front end amplifier – 20 nsec peaking
- comp. with individually programmable threshold
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- output mux and driver (SLVS)
- fast (SLVS) and slow (I2C) control interfaces

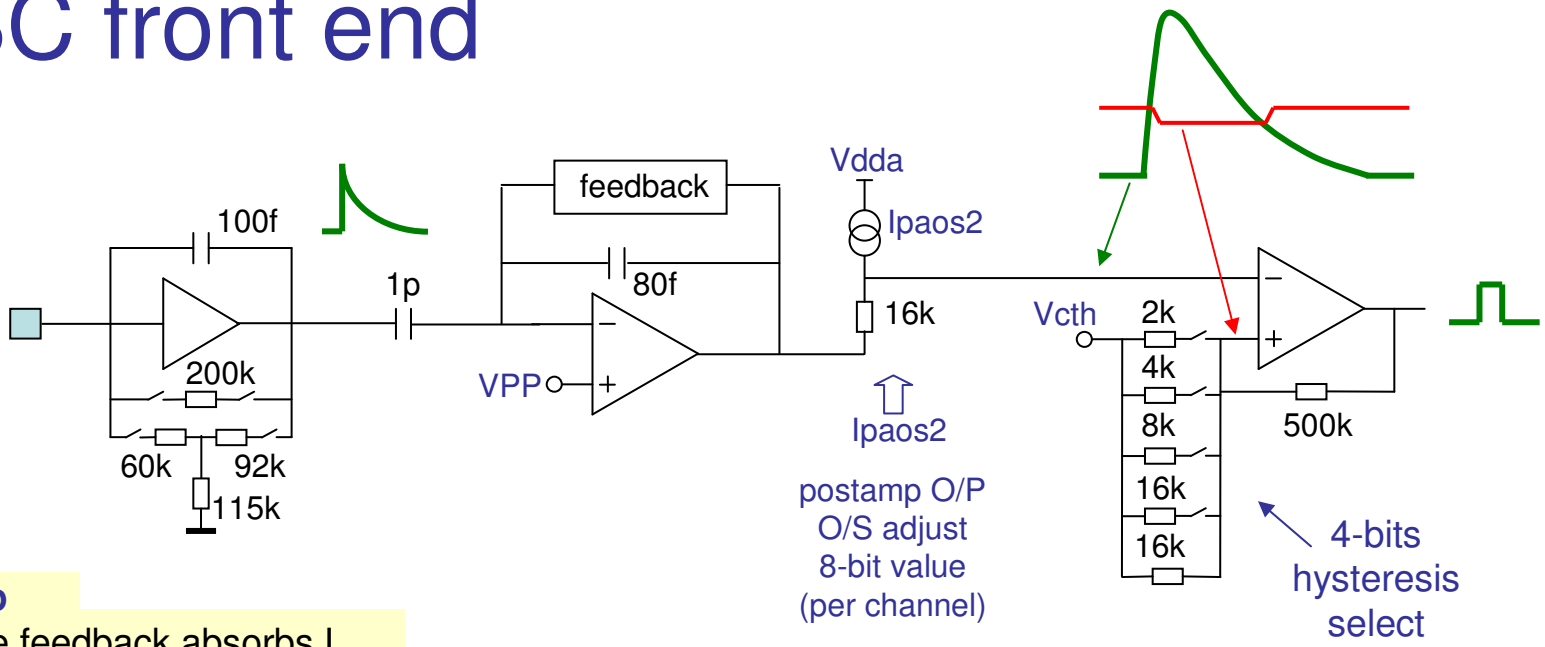
some target specs (see * for full list)

- both signal polarities
- DC coupled to sensor – up to 1 uA leakage
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  < 0.5 mW/channel for C_{SENSOR} ~ 5 pF



* *http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_specifications.pdf*

CBC front end



preamp
resistive feedback absorbs I_{leak}
T network for holes
Rf.Cf implements short
20ns diff. time constant
(good for no pile-up)

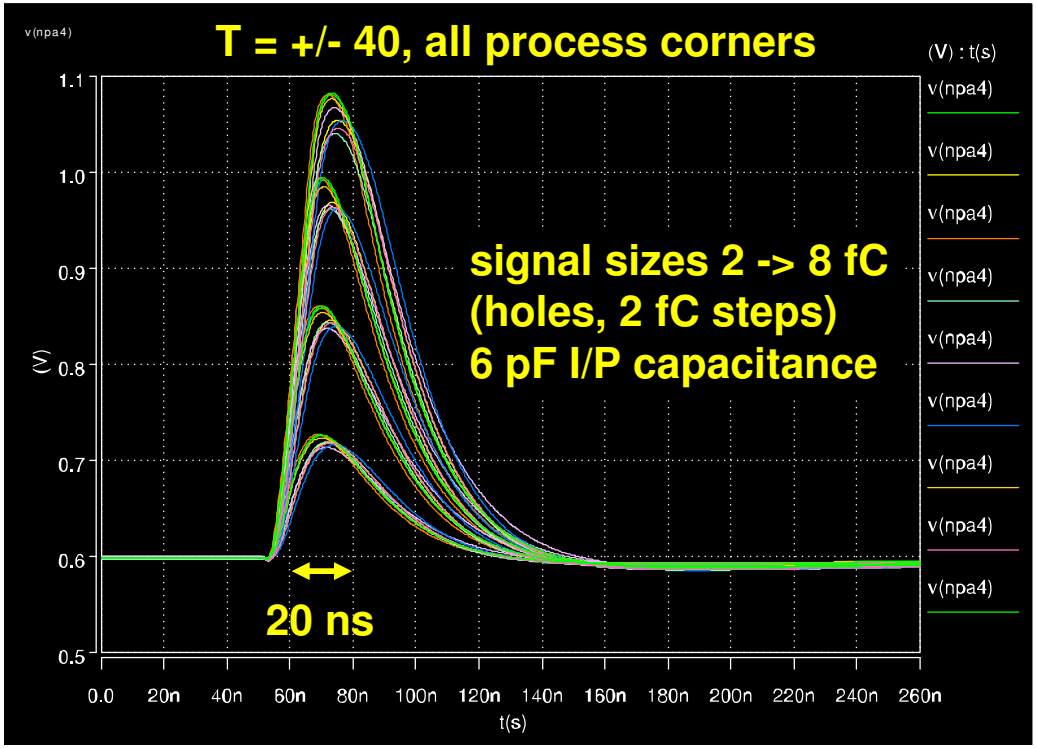
postamp
provides gain and int. time constant
~ 50 mV / fC
AC coupling removes I_{leak} DC shift
individually programmable O/P DC level
implements channel threshold tuning
8-bits, 0.8 mV / bit, 200 mV range

comparator
global threshold
(indiv. tuning at postamp O/P)
programmable hysteresis

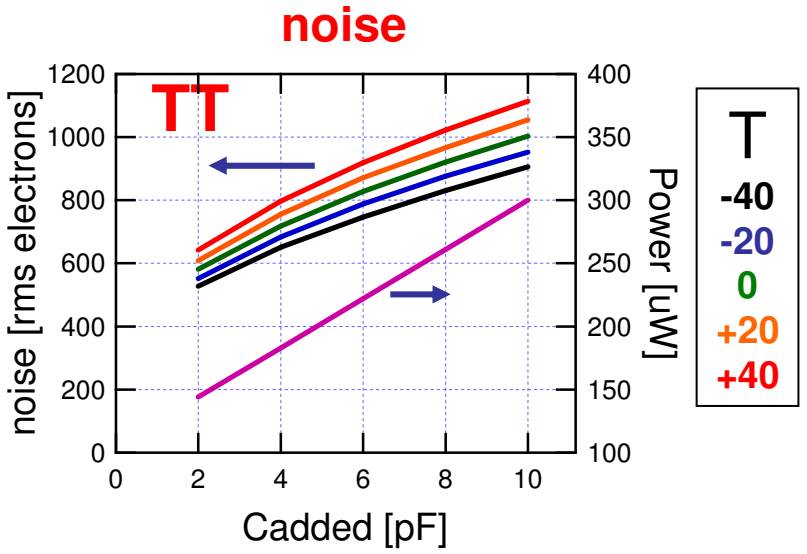
will show just simulated pulse shape and noise performance
for much more detail see design review talk:

http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/frontend_design_review_Oct_09.pdf

postamp output pulse shape & noise



~ 20 nsec peaking, ~ 50 mV / fC
robust to temperature (-40 -> +40) and process variations
electron signal gives opposite polarity



preamp input device power varied with Cadded (added input capacitance) to maintain constant pulse shape

(otherwise preamp risetime increases with Cadded and overall pulse shape affected)

for 1 uA leakage current add 440e in quadrature

layout

actual submission size 7 x 4 mm^2

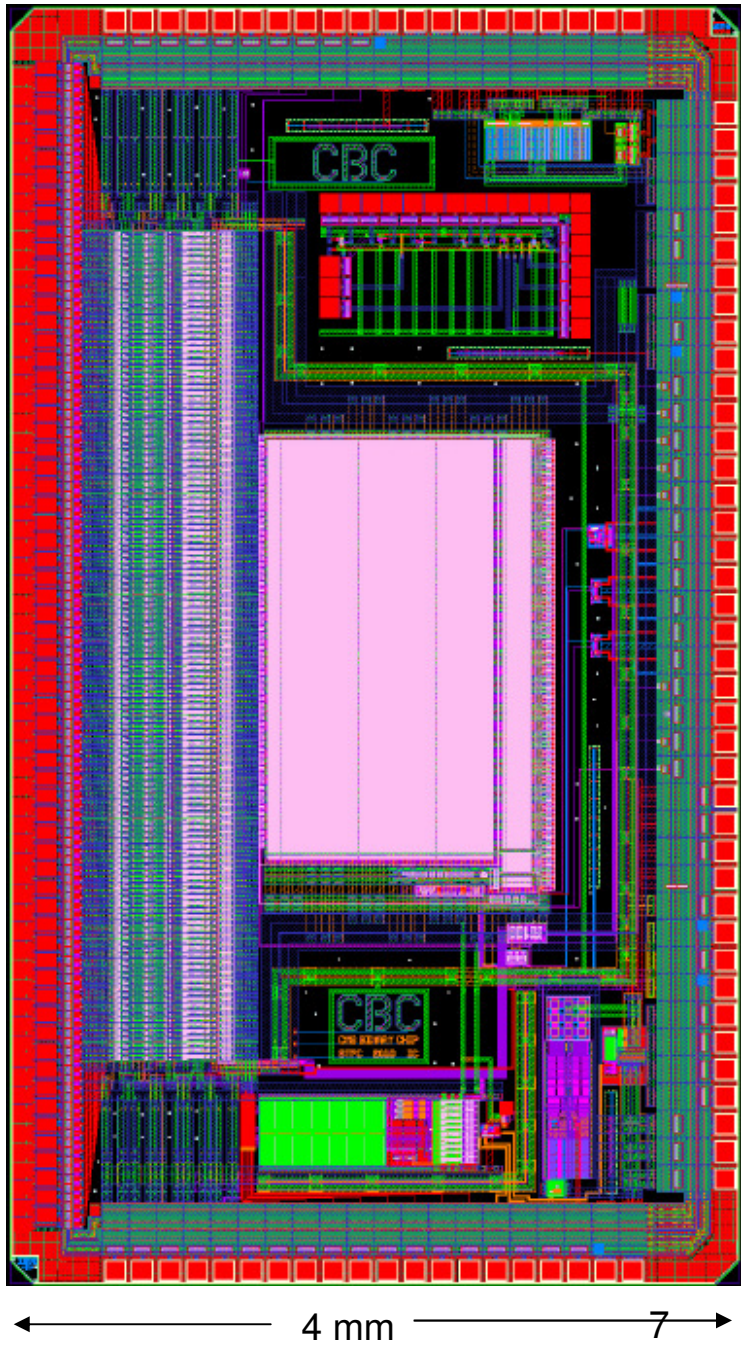
for MPW dicing reasons – 7 x 3.5 possible

input pads on 50 um pitch

2 staggered rows on 100 um pitch

note: no power pads on front edge

all other pads (top, bottom, right hand side) on 150 um pitch



some blocks

128 preamp/postamp/comparator channels
including DAC for individual postamp O/P offset

256 long pipeline (RAM)

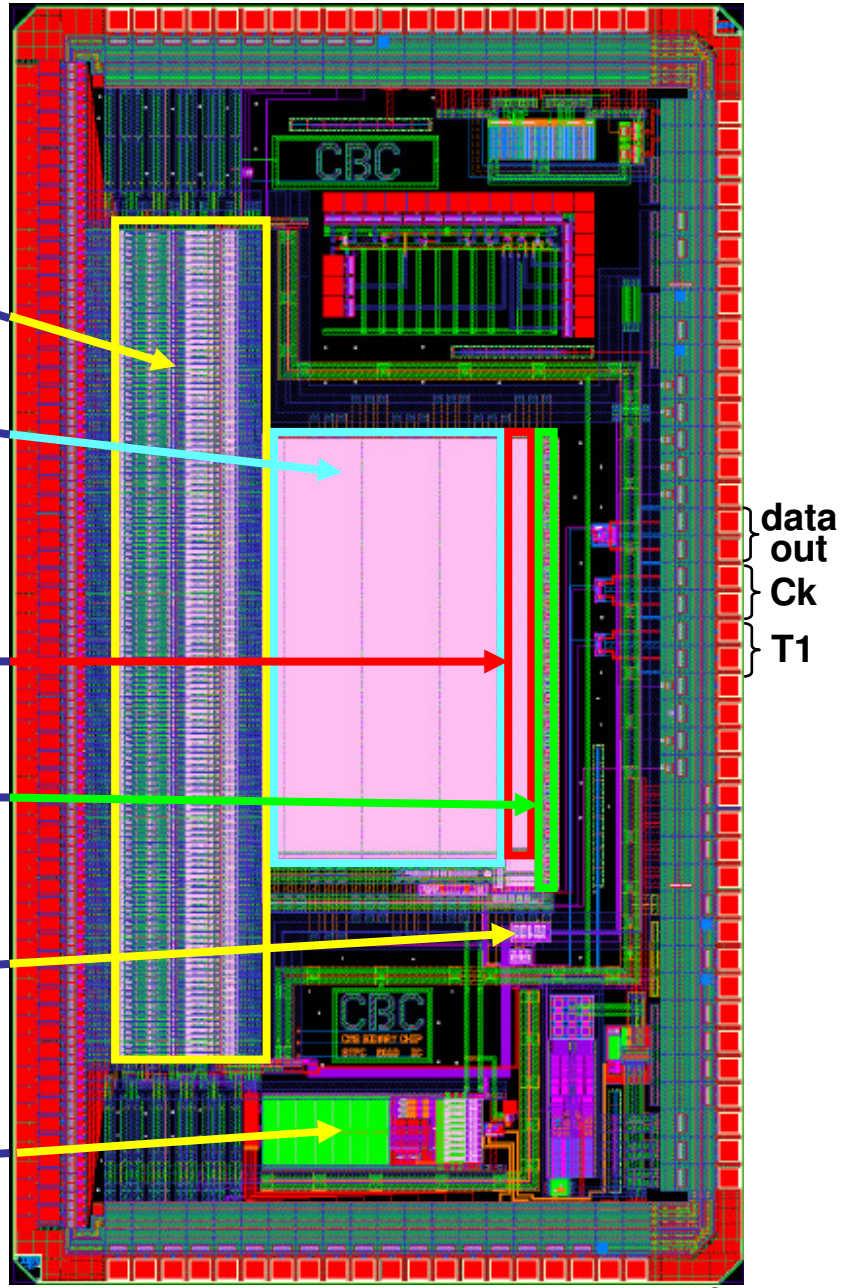
pipeline control logic (underneath pipeline)
"write" and "trigger" counters separated by programmed latency – decoded beneath pipeline columns to control read/write access

32 deep buffer for events awaiting readout
data transferred to this buffer on receipt of L1 trigger

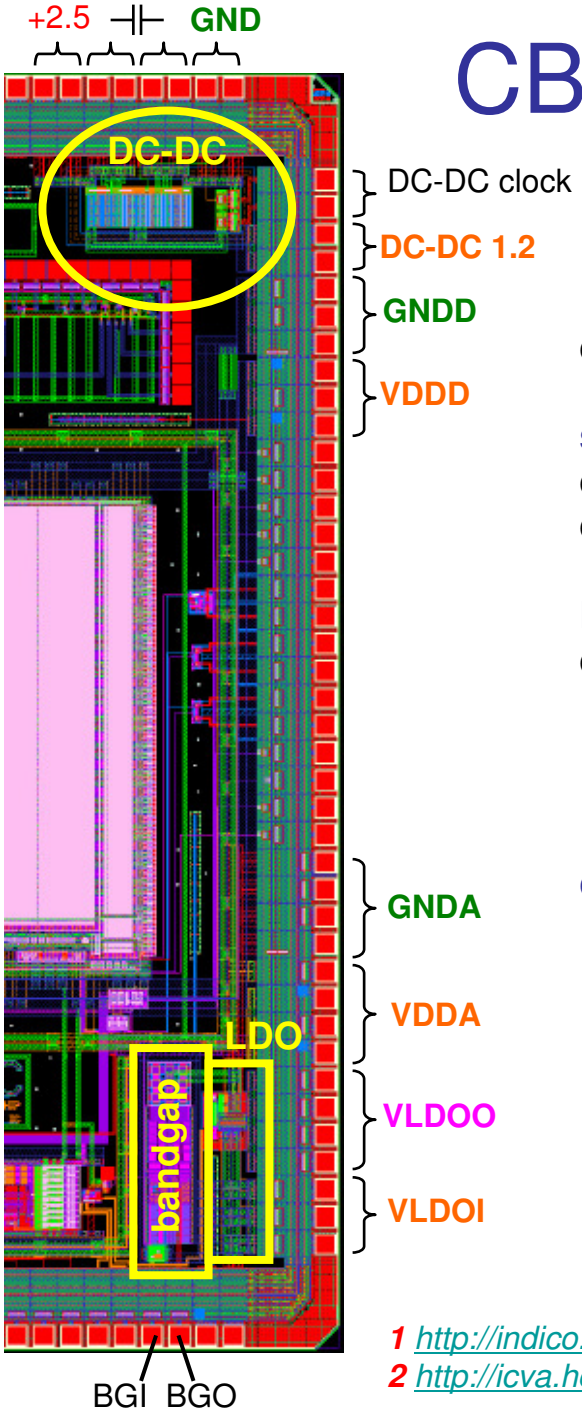
output shift register
triggered data shifted serially off-chip (channel order)
preceded by digital header
(includes triggered pipeline column address)

I^2C interface
for programming bias registers, 128 channel 8-bit offsets, latency, polarity select register, …

bias generator
7 currents, 3 voltages



CBC powering options

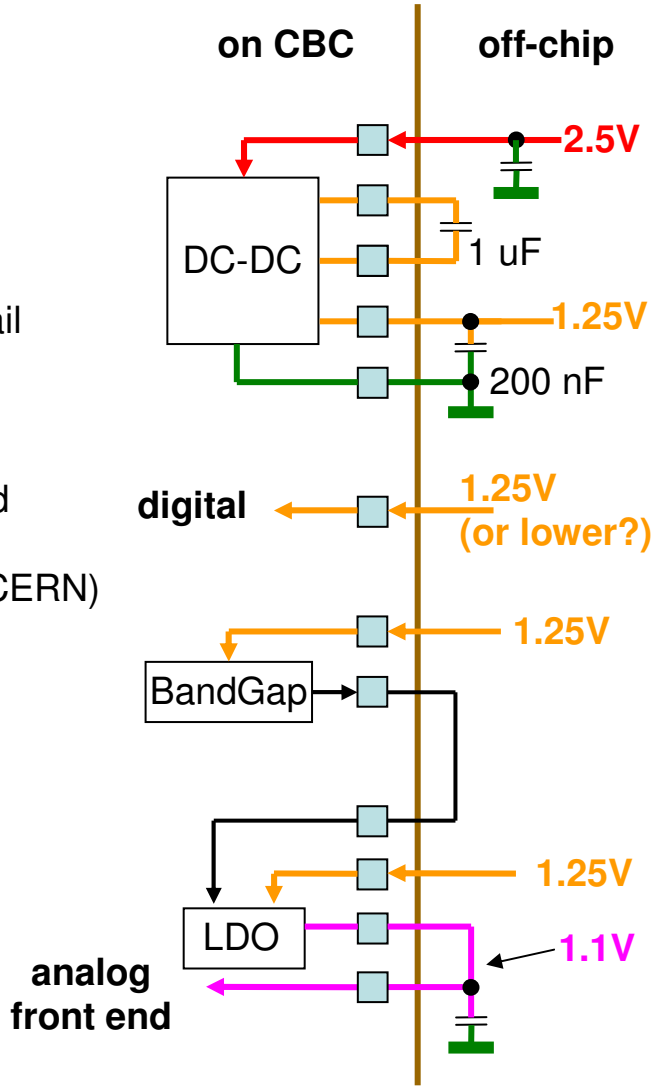


can explore some powering options

switched capacitor DC-DC (CERN) [1]
converts 2.5 -> 1.25
could use 1.25 to provide CBC digital rail

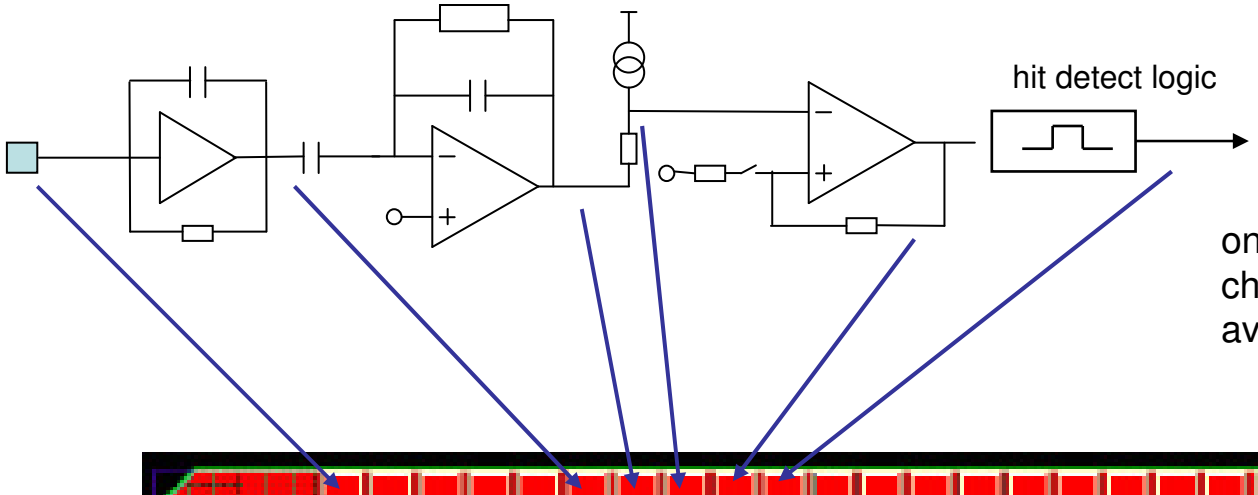
LDO (low drop-out) linear regulator
converts 1.25 -> 1.1
- provides regulated rail to front end
- giving supply noise rejection [2]
- needs bandgap reference input (CERN)

can incorporate without risk
- can be overidden
- all pads accessible

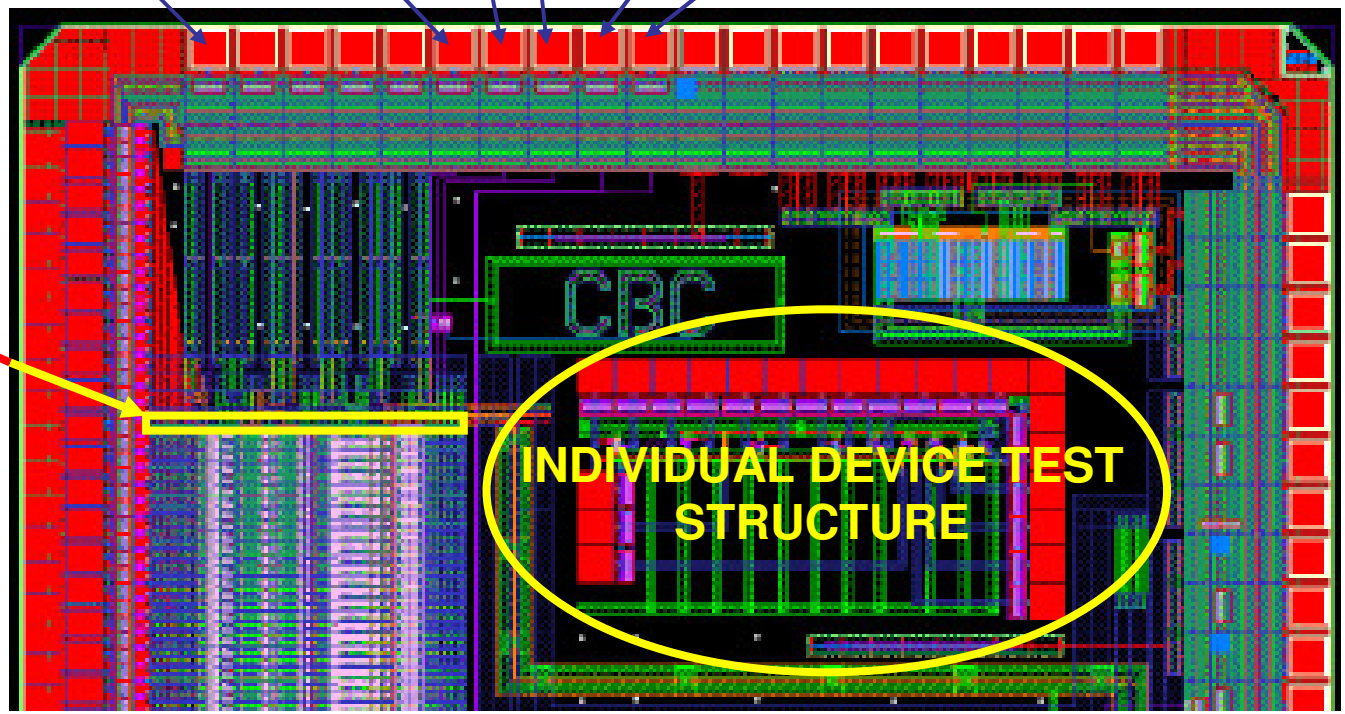


1 http://indico.cern.ch/getFile.py/access?contribId=3&resId=0&materialId=slides&confId=85278
2 http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/LDO_PWG_Sep09.pdf

test features (1)

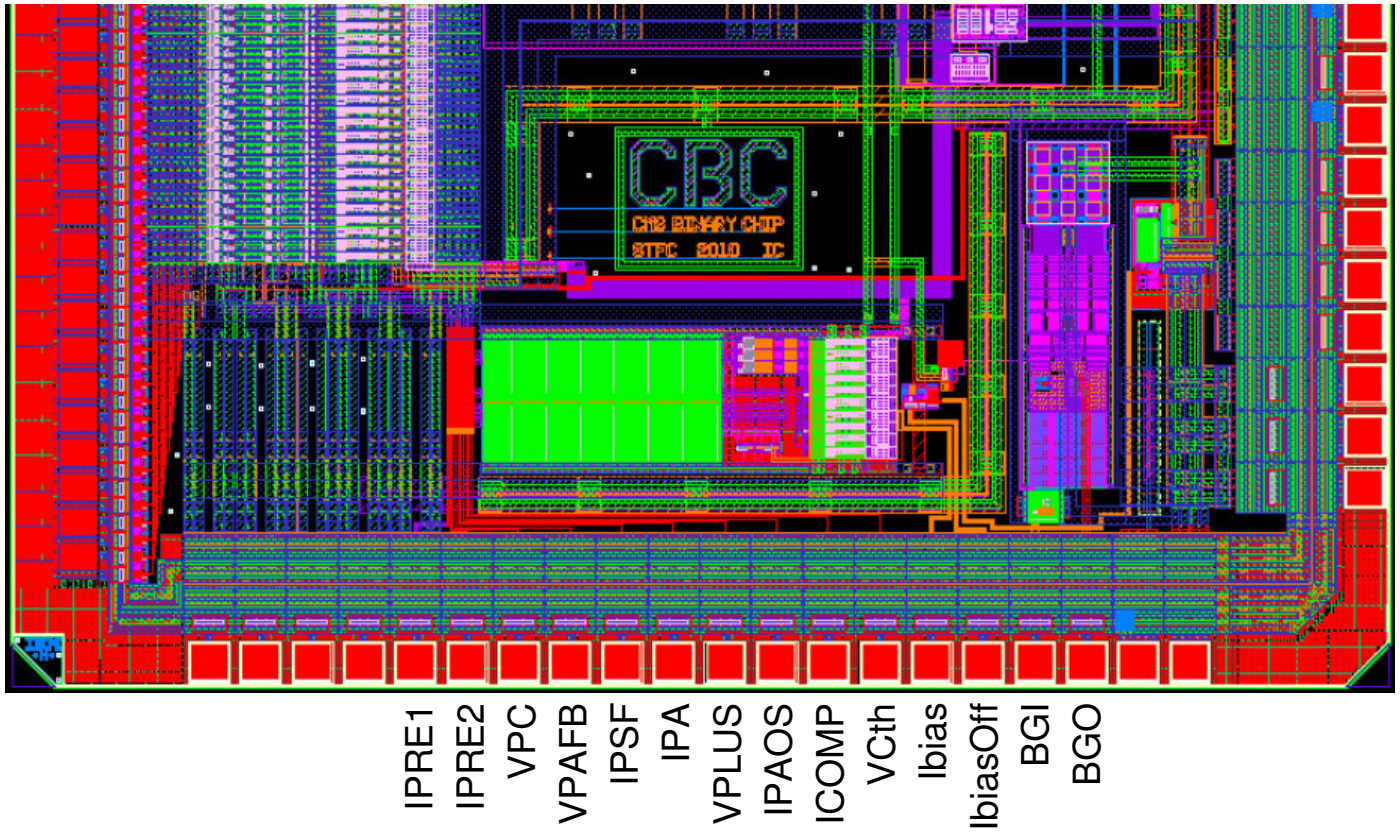


one complete dummy front end channel with buffered signals available along chain



dummy channel

test features (2)



access to all bias generator outputs to allow study/fault diagnosis/overide

test pulse

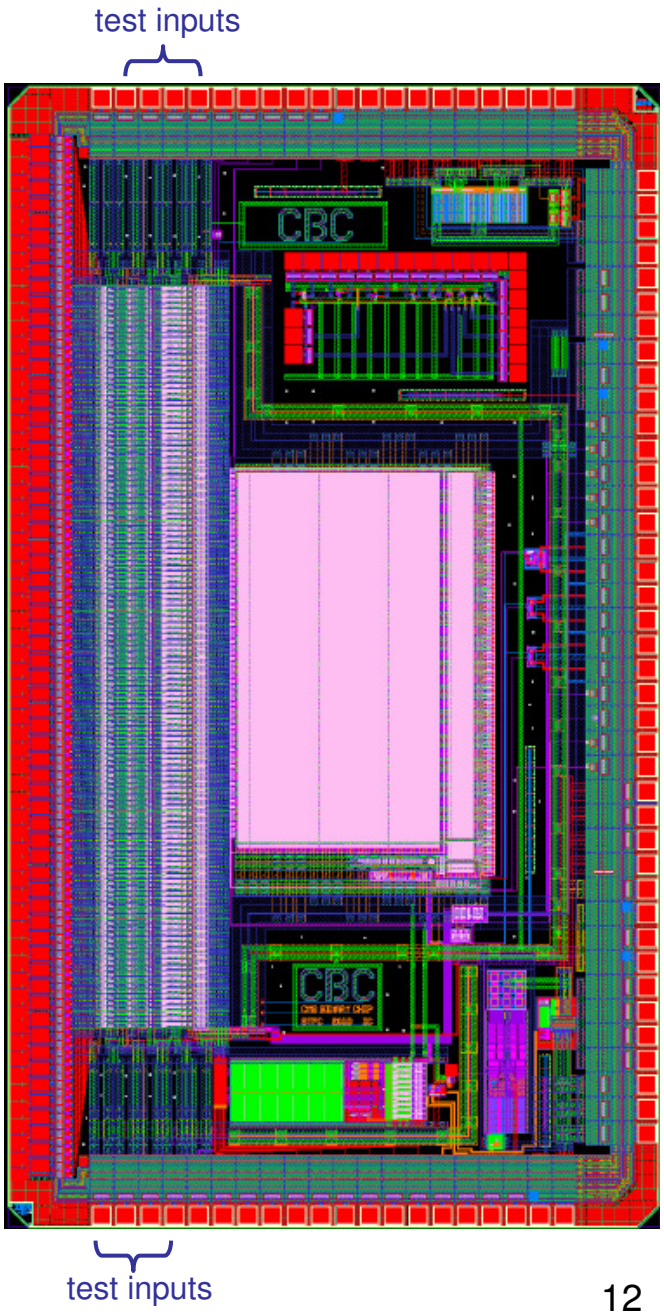
no time to implement complex circuit

e.g. DLL based charge injection to allow to sweep time of charge injection

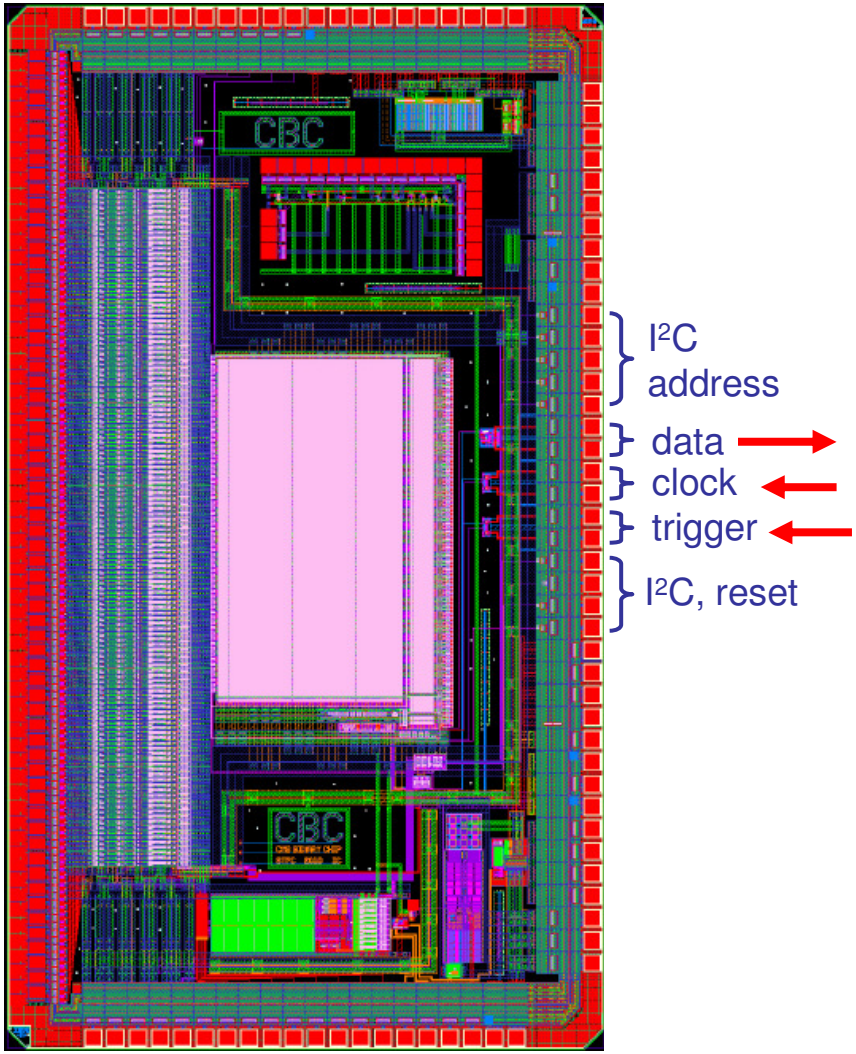
(but expect to include in future version)

just 8 pads, each one connected to 16 channels though small capacitor

allows to quickly verify functionality of all channels



running the chip

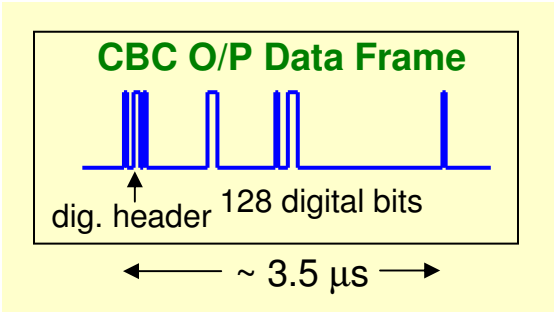


procedure very similar to APV

I²C for programming operational state
bias values, channel offsets, polarity, latency,…

SLVS fast control signals
40 MHz clock
trigger line
single 1 => L1 trigger
101 => fast reset (reset101 like APV)

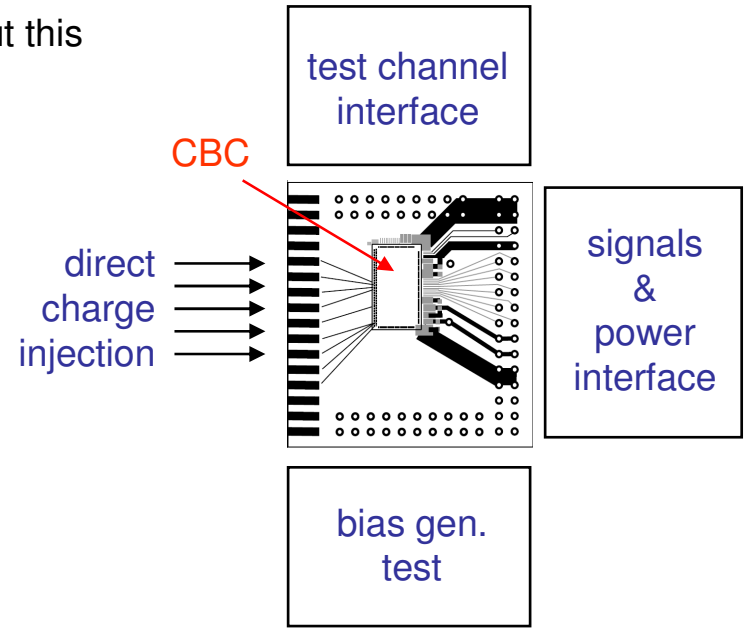
output frame at 40 Mbps
(no other bit-rate available on this version)



testing plans … only just begun thinking about this

at IC will want to verify detailed chip functionality and performance

will probably make something like this
fineline chip carrier board (chip + capacitors only)
+ interface boards for signals and power



may need different versions to test different functionalities
e.g. with/without different powering options

for DAQ can use old APV system – VME based/Labview interface

CERN VI2C card for I2C
digital pattern generator to provide clock/trigger
ADC to acquire output data (even though just binary)

Bristol plans

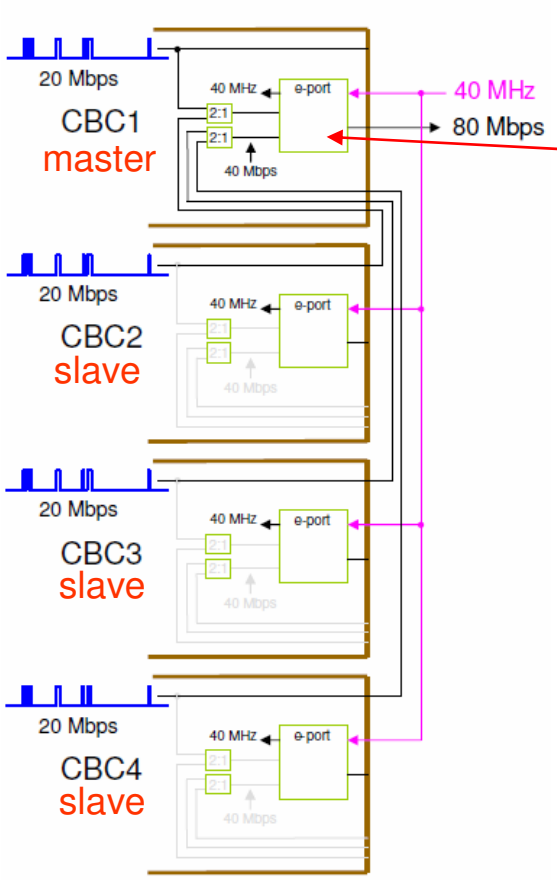
will focus on module and system tests using daughter board on FPGA development platform

see talk by David Cussans (16th June 2010 Power Working Group)
http://indico.cern.ch/getFile.py/access?contribId=3&resId=0&materialId=slides&confId=97972

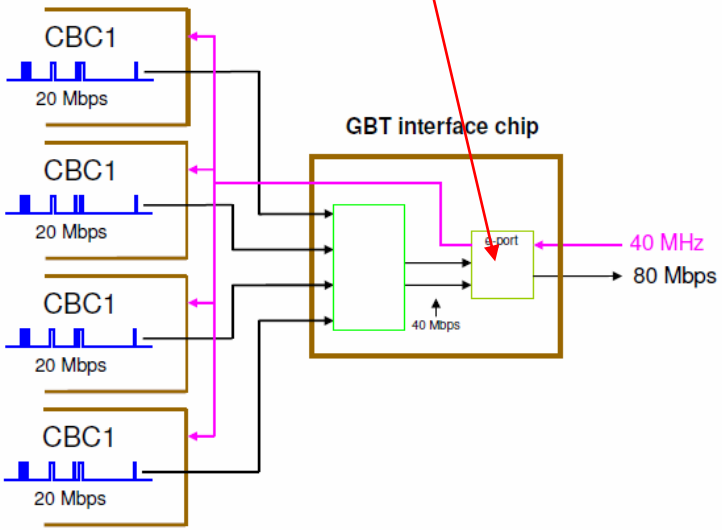
future chip developments (1)

CBC prototype designed to be complete working readout chip
but some system functionalities not yet present

system aspects have been discussed in TUPO meetings
e.g. how to combine data and interface to GBT
discussions will continue, but more than one viable option exists

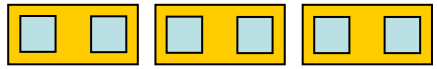


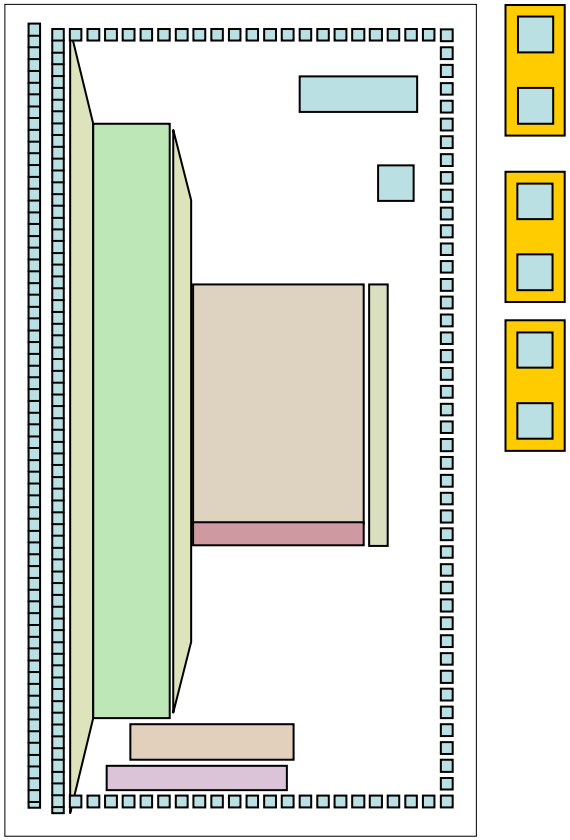
e.g. e-port (GBT interface circuit block)
either inside master CBC
or in separate chip

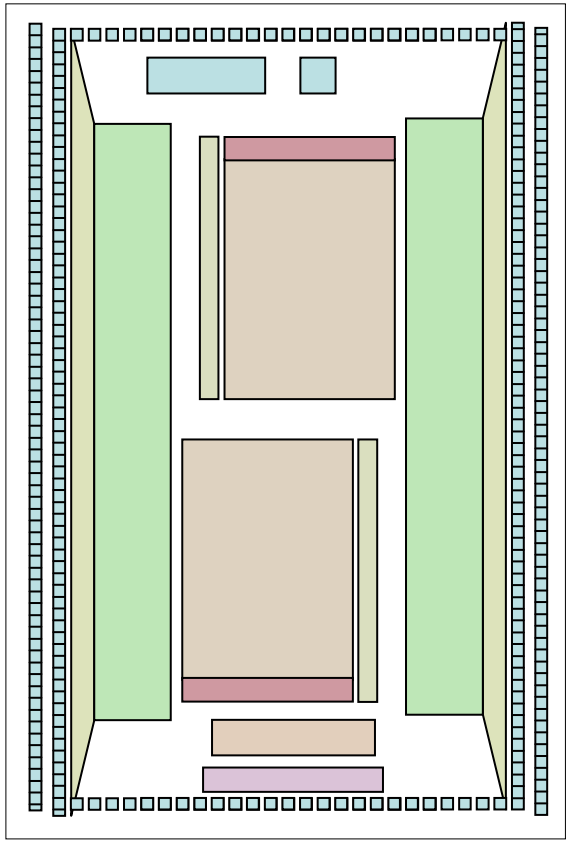


future chip developments (2)

0201 capacitors







128 -> 256 back-to-back

can share some functionality
- e.g. power, control
- but not much else

reduced area, cheaper

less pads available on 256 version

less flexible

overall power consumption
probably not much different

conclusions

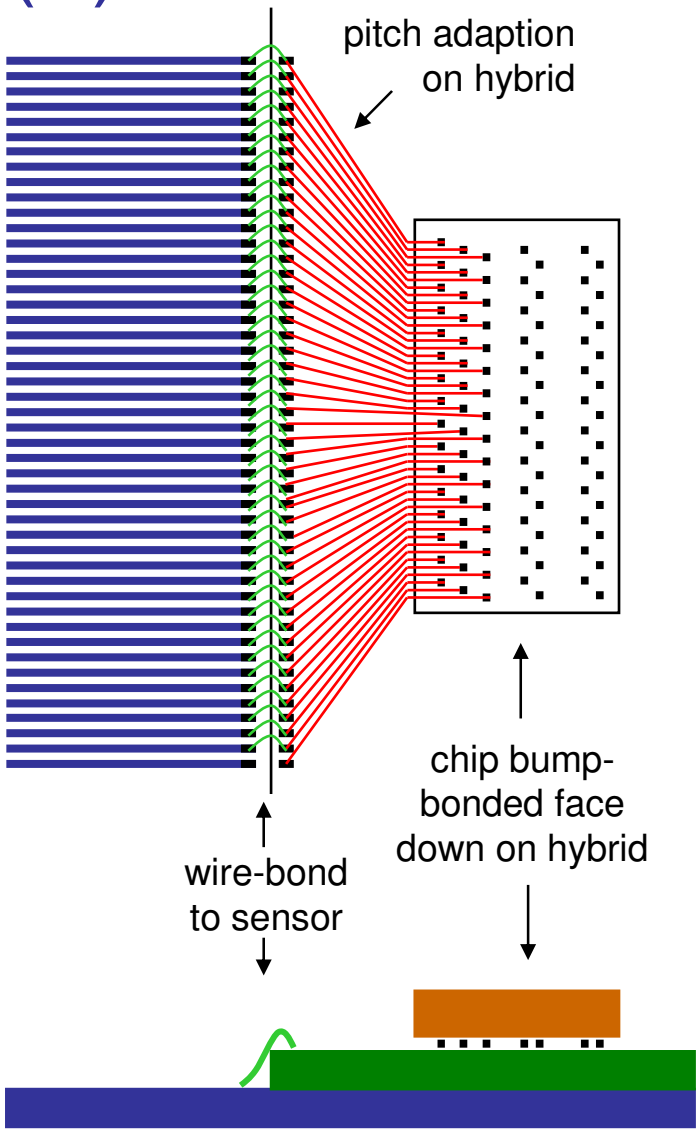
256 back-to-back probably not impossible
- but more detailed study may yet reveal difficulties
- e.g. hard to see where DC-DC conversion can fit without causing problems
  - (interference & room for external capacitors)

future chip developments (3)

bump-bonding?

removes ½ of the wire-bonds
pitch adaption on hybrid

significant changes to layout
hybrid & wire-bond to sensor still required
else where to put passives, route power, …



summary

CBC prototype designed to be complete working readout chip
- functionality and performance issues to study
  - noise, power, powering, radiation (SEE),….
- useful information for future chip and system developments

some system functionalities not yet present
- but current design compatible with future anticipated options

chips expected back in October

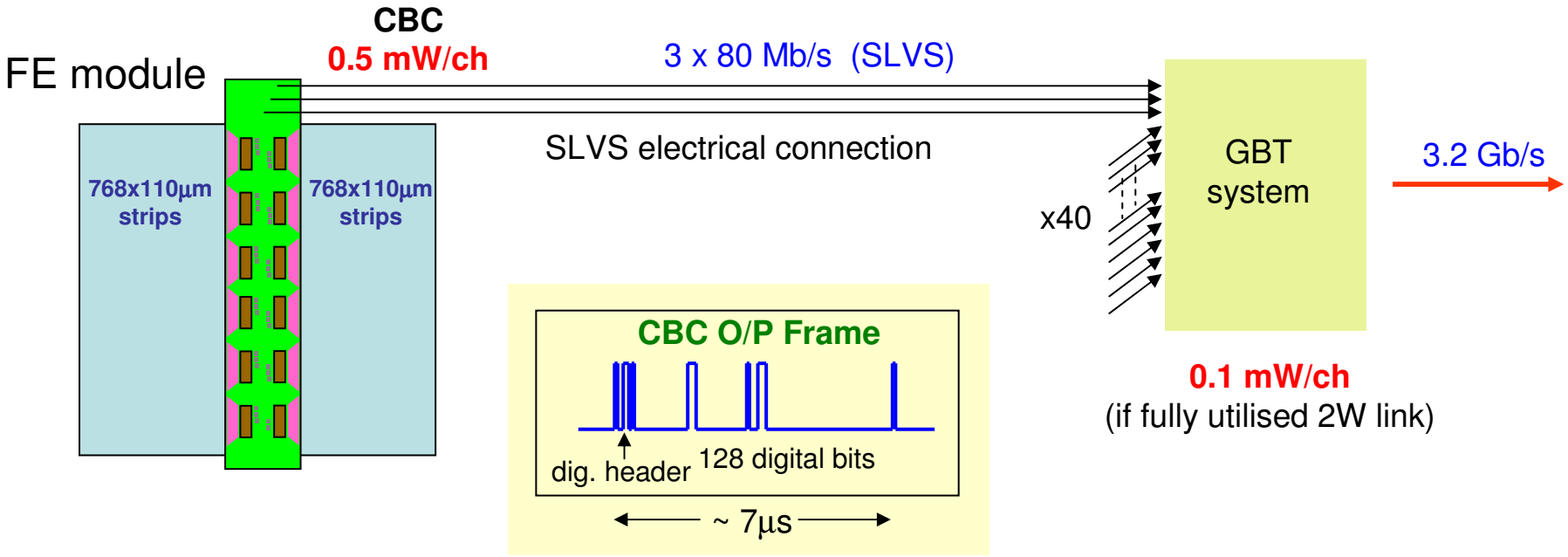
detailed documentation under development
- will appear eventually on:
  - http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/

plans for testing underway
- will concentrate initially on detailed functionality and performance at IC
- Bristol looking at module and system test stand

future developments
- some system options need to converge (GBT interface)
- need to study and make decisions on alternative layouts
  - 256 back-to-back, bump-bonding

EXTRA

sLHC strips readout system



binary unsparsified output frame format similar to APV (just hits, not analog values)

keep data frame ~7 µs (must be less than average L1 separation)

=> 128 channel CBC provides output data at 20 Mbps

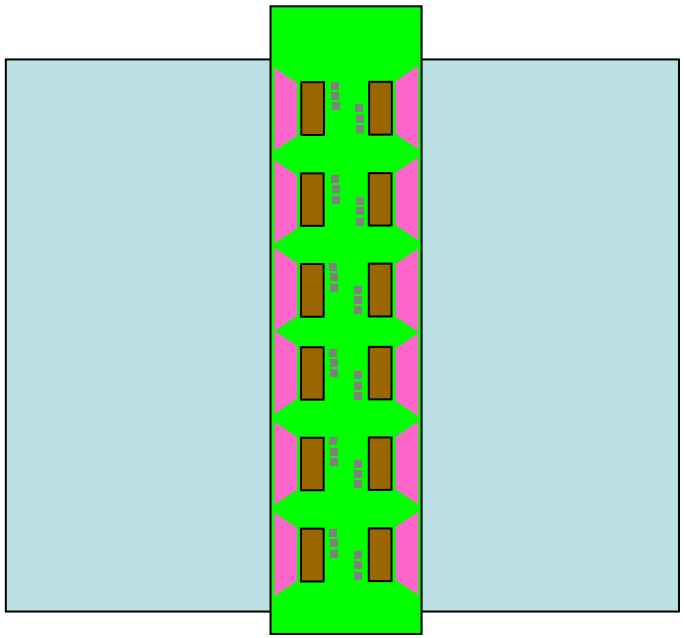
=> 4 CBCs data combined onto one 80 Mbps link to GBT input

plan to use GBT e-link (e-port IP block in chip)

takes care of data transfer synchronization

but not on this CBC version

module concepts



hybrid, bonding, PA issues

CBC prototype uses “conventional” layout

128 channels, effective pitch 50 um, wire-bondable
no special test setup preparations & generally easier to test

but 50 μm not well matched to sensor pitch ~ 100 μm

=> pitch adaption somewhere - where?
(would like to avoid separate PA’s in future system)

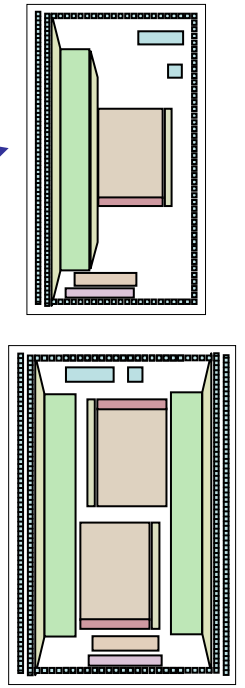
hybrid? - possible but uses space for fanout

would help if CBC input pad pitch better matched to sensor ~ 100 um pitch

other issues

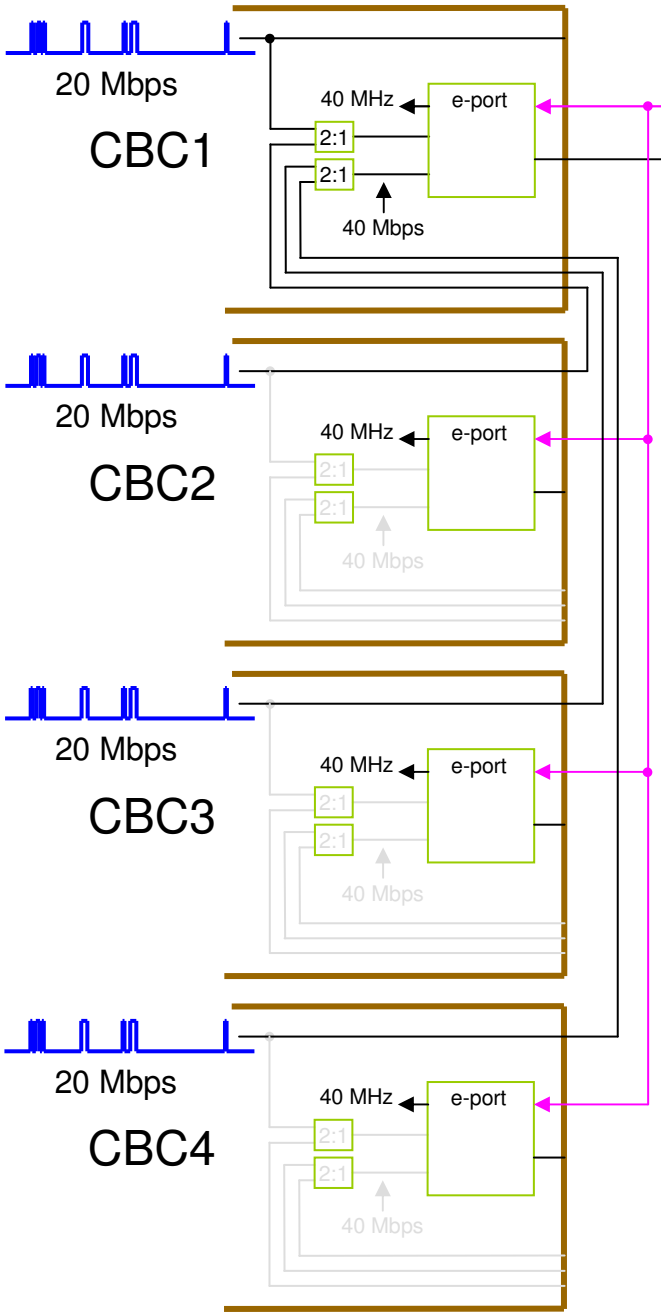
would module design benefit from 256 (2 x 128 channels back-to-back)?
(not impossible - but detailed study may yet reveal difficulties)

should we be looking at bump-bonding for chip/hybrid/sensor connection?



=> a number of issues to re-examine for a subsequent iteration

combining chips output data using CERN e-port IP core



single lines shown outside chips but assume all differential SLVS
using CERN SLVS interface driver/receiver

use e-port (e-link) to communicate with GBT (CERN IP core)
automatically takes care of synchronization
also has receive data path but we will probably not use
(plan to use I^2C bus for slow control)

all FE chips produce 20 Mbps output data frame

CBC1 programmed to be master
combines pairs of CBC data streams into 2 x 40 Mbps
(compatible with e-port requirements)
e-port combines 40 Mbps streams to produce 80 Mbps

will probably not implement e-port in CBC May '10 submission
some aspects still under development

but nevertheless a clear route to provide the CBC->GBT system interface in the future

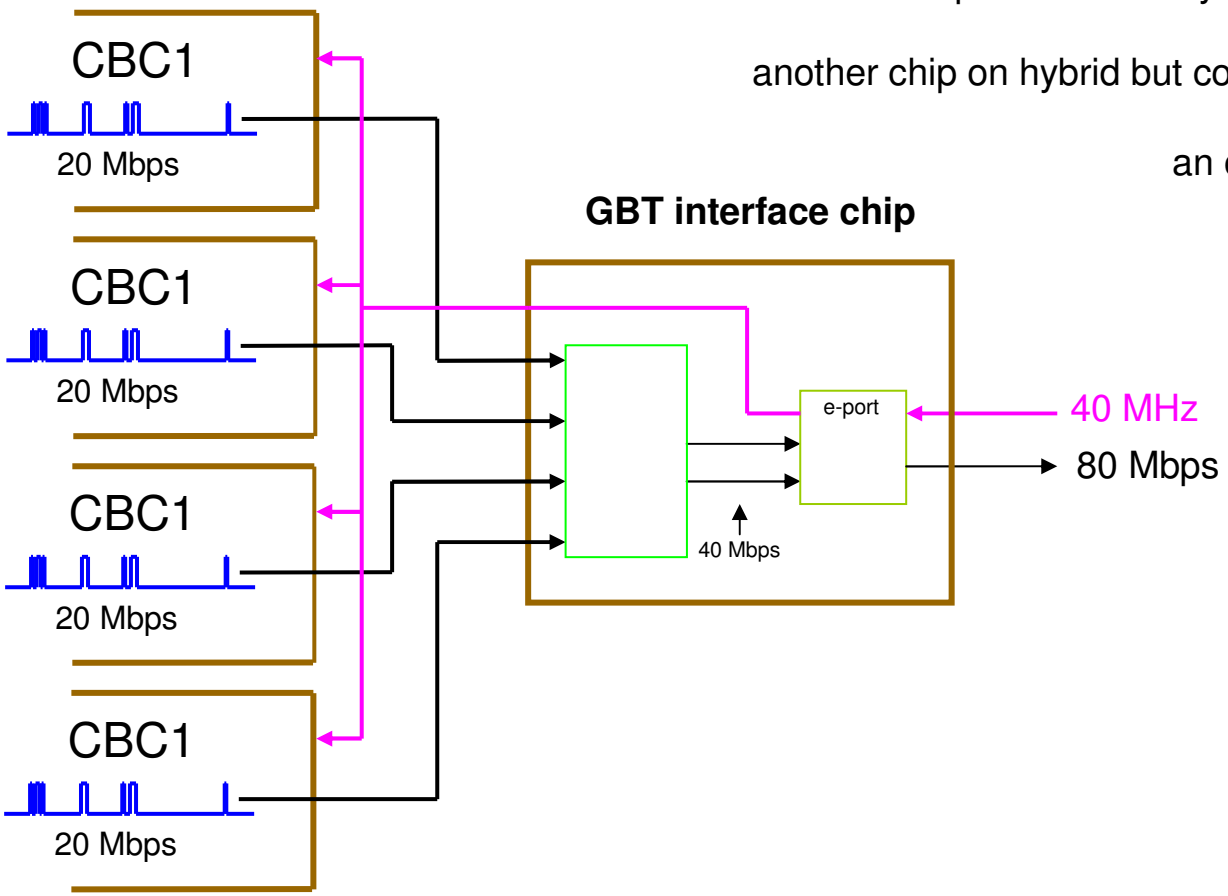
alternative scheme

put e-port in separate GBT interface chip

incorporates circuitry to combine CBC data streams

another chip on hybrid but could offer some future flexibility

an option to consider in the future



CBC power

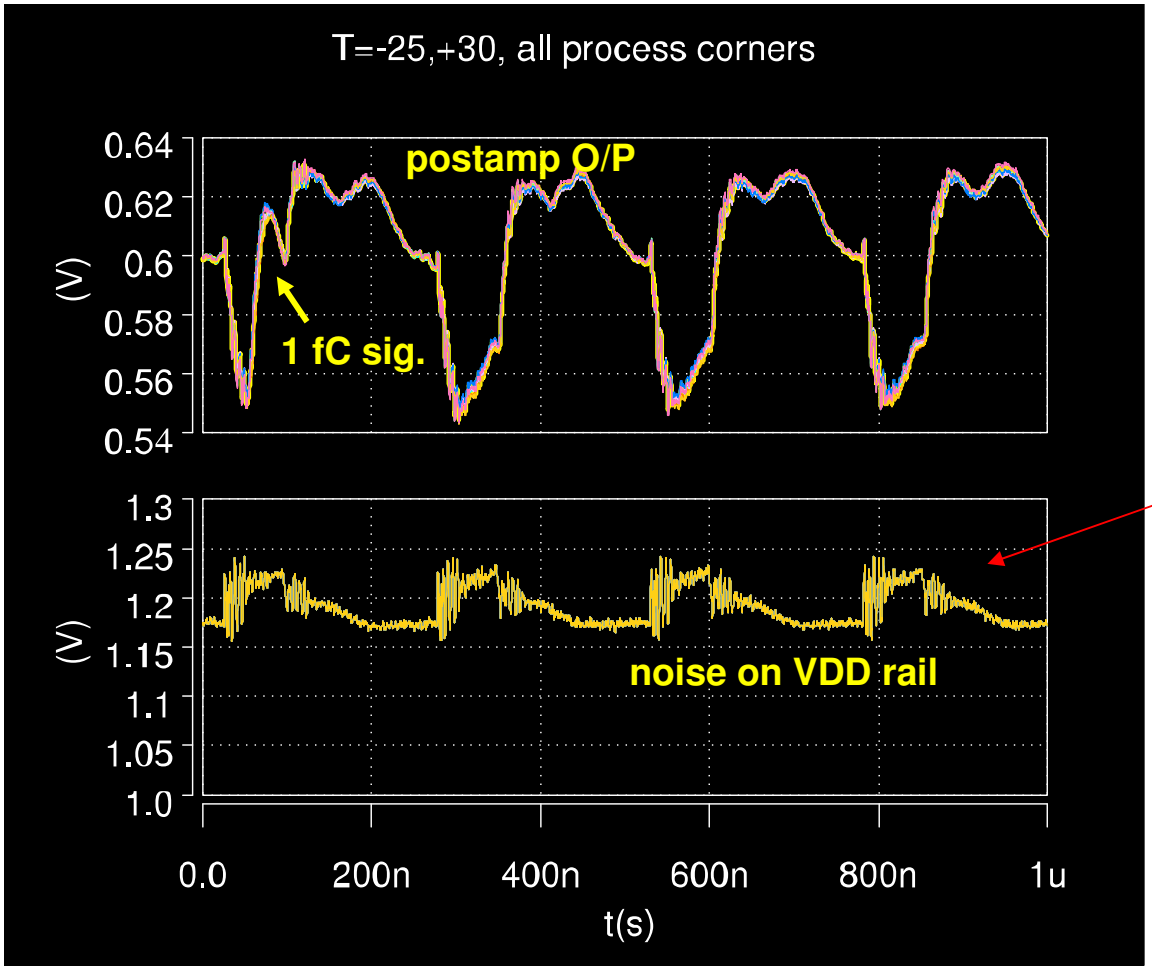
	power/FE chan.	
preamp/postamp		
20 nsec peaking time, short strips C_{SENSOR} ~ 5pF (~ 100 + (20 x C_{SENSOR}))	200 μW	~ 200 μW analogue
comparator	14 μW	
digital		
take 0.25μm APV25 (digital 400 μW) /10 for technology, x3 for SEU (pessimistic? CBC logic should be simpler)	120 μW	~ 300 μW digital
output		
LV differential ~ few mW / 128 chans.	30 μW	
contingency		
just guess nominal figure to bring overall power to 0.5 mW	150 μW	

0.5 mW / channel seems like an achievable target (c.f. 2.7 mW for APV25)

digital is biggest uncertainty, and maybe largest contributor
hope to improve estimate as design progresses
can consider running at lower voltage (dig. power ~ V^2) => extra contingency
e.g. 1.2 -> 0.85 power consumption halved
will keep power rails separate on chip to keep option open

using numbers above: 128 chan. chip needs ~ 20 mA analogue, ~30 mA digital

front end PSR without LDO supply



time domain picture

measured noise waveform added to VDD rail supplying FE circuit

sampled scope data for Enpirion "quiet" converter provided by Aachen

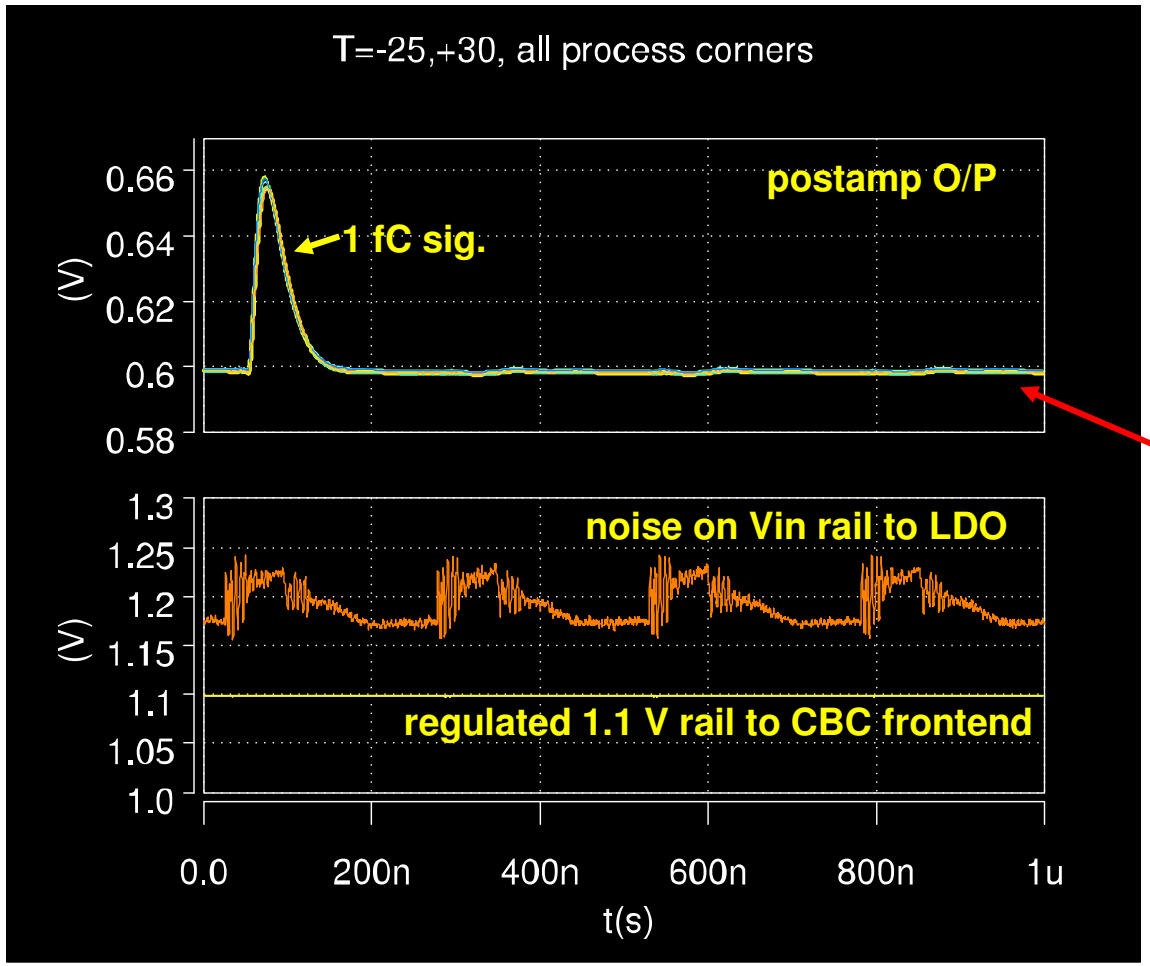
but x10 to (artificially) make it noisier

~ 80 mV pk-pk

1 fC normal signal completely swamped by noise

Ref: *http://indico.cern.ch/getFile.py/access?contribId=24&sessionId=0&resId=0&materialId=slides&confId=47293*

front end PSR **with** LDO supply



measured **x10** (80 mV pk-pk) noise waveform now added to LDO Vin

LDO loaded by single CBC frontend + 25 mA extra dummy load

1 fC signal at postamp O/P now appears

postamp O/P noise just visible

~ 125e pk-pk