CBC chip: status and plans

Outline

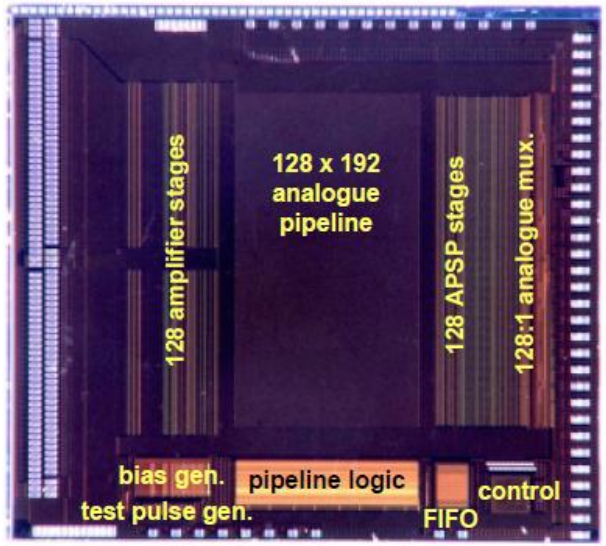
CBC1: first prototype and results summary

current status: CBC2

future plans

LHC -> HL-LHC

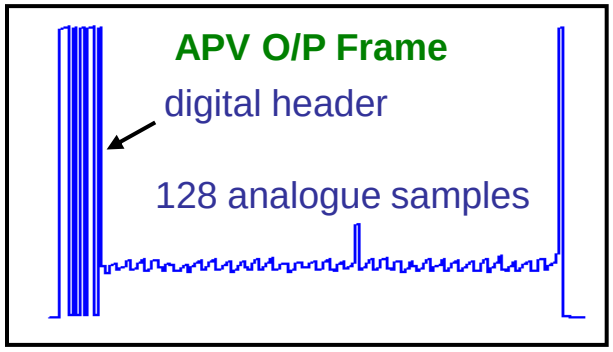
APV25



7.1mm

8.1 mm

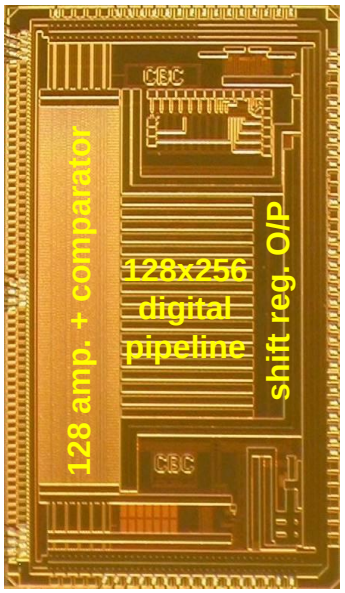
rad-hard 0.25um CMOS
unsparsified analogue readout
~ 3 mW / chan for 10-20 cm strips
analogue off-detector transmission



20 Ms/s readout -> 7 μs

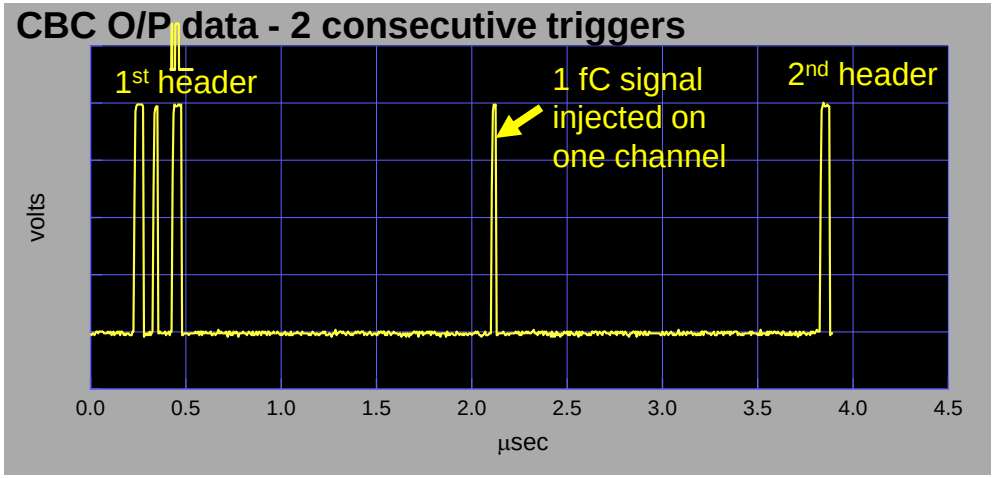
- digital off-detector links
- many more channels -> power becomes the big issue

CBC1



4 mm

130 nm CMOS
unsparsified binary readout
(retain system simplicity but give up analog info)
target low-power for short strips



CBC1

features

- designed for short strips, 2.5 – 5cm, < ~ 10 pF
- full size prototype - 128 channels
  50 μm pitch wirebond
- binary un-sparsified **triggered** readout only
- powering test features
  2.5 -> 1.2 DC-DC converter
  LDO regulator (1.2 -> 1.1) feeds analog FE

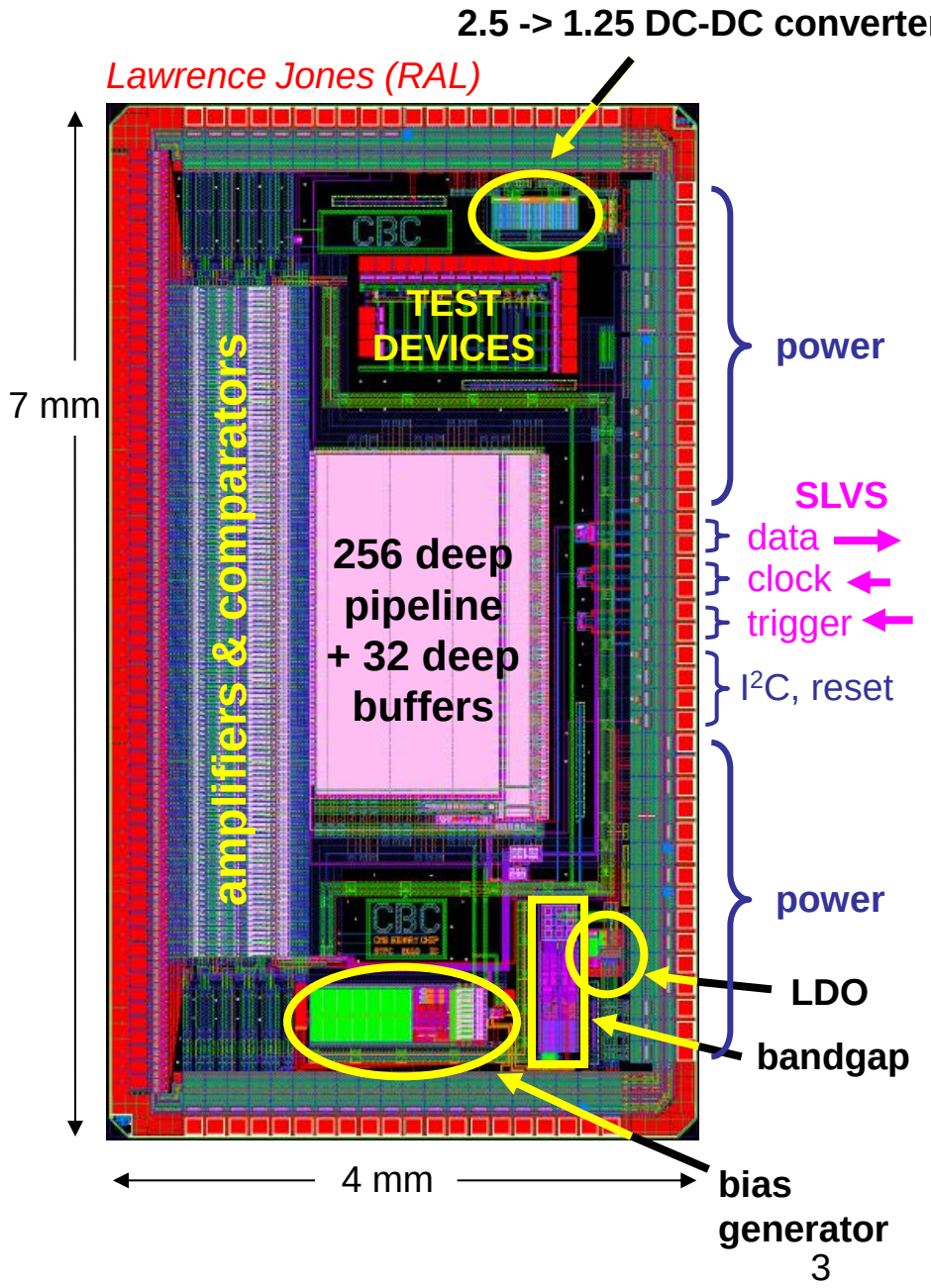
main functional blocks

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- fast (SLVS) and slow (I2C) control interfaces

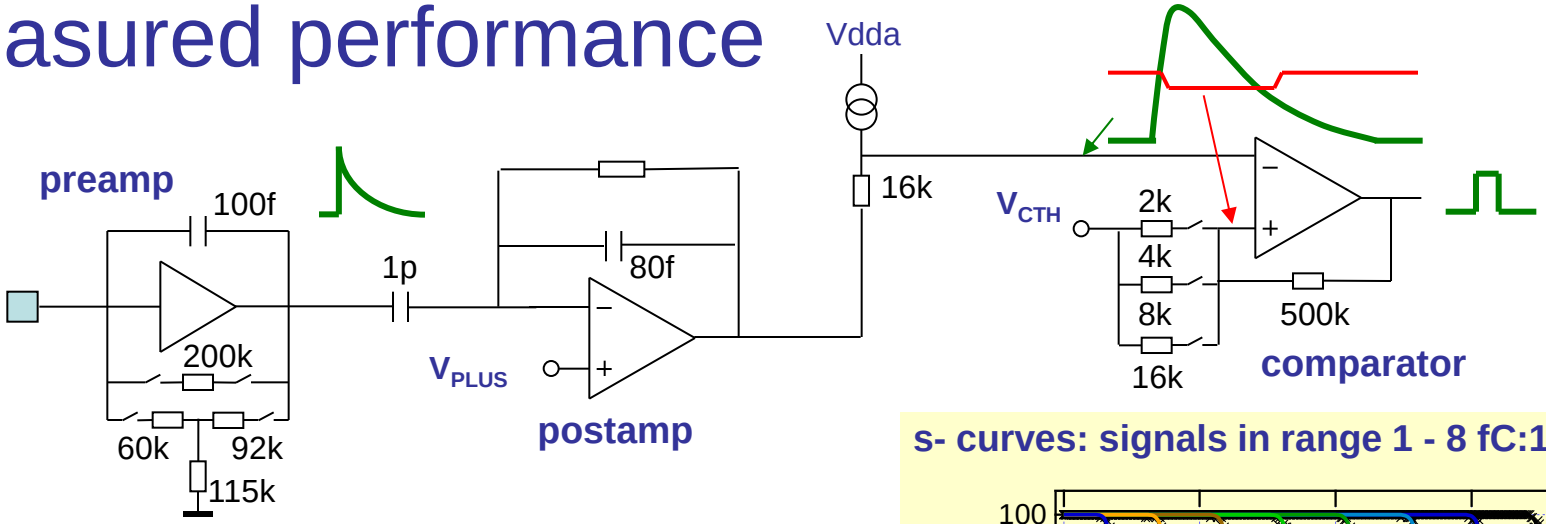
some target specs

- both signal polarities
- DC coupled to sensor – up to 1 uA leakage
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  < 0.5 mW/channel for C_{SENSOR} ~ 5 pF

first chips received Feb. 2011



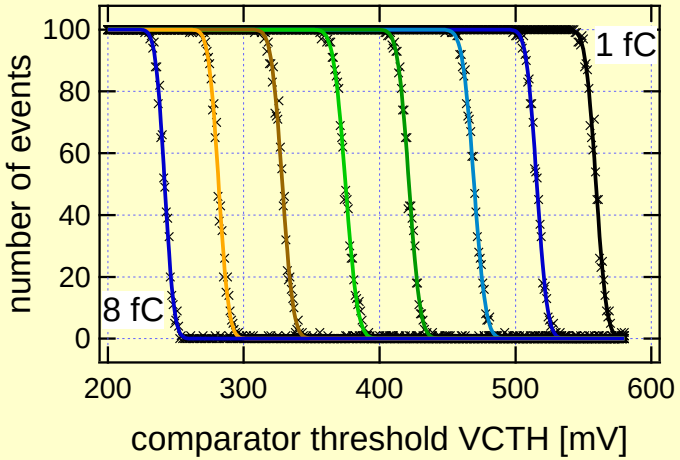
measured performance



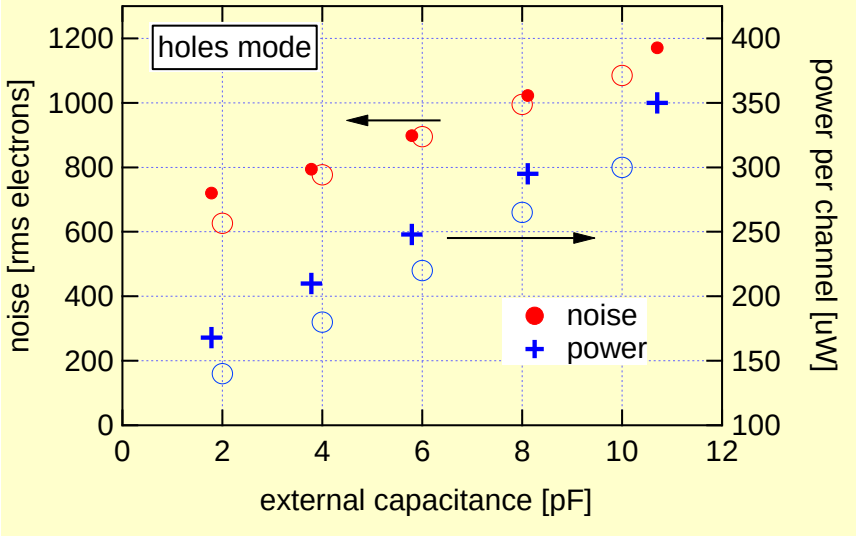
preamp: leakage tolerance 1μA verified, both polarities

postamp: gain: ~ 50 mV / fC

s- curves: signals in range 1 - 8 fC:1 fC steps



noise



noise dependence on external C

vary current in input device

=> pulse shape independent of C

e.g. for C_{SENSOR} ~ 8 pF (~ 5 cm strips)

~ **1000e** achievable for

~ **350 uW** tot. power/chan. (incl.digital) 4

comparator

thresholds

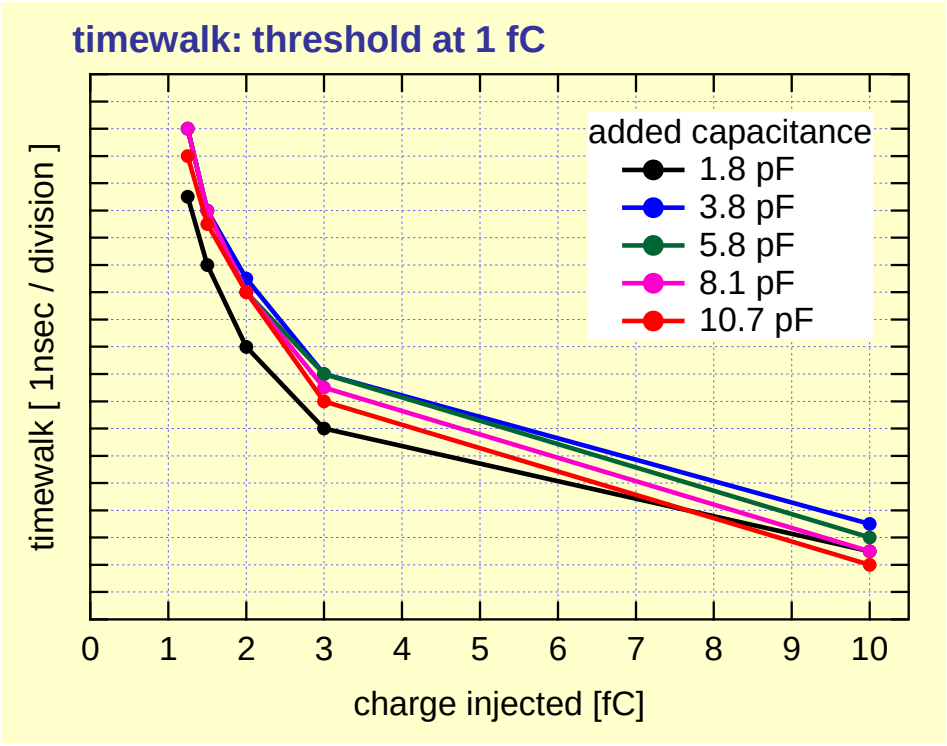
before tuning pk-pk threshold spread ~30 mV (~ 0.6 fC)

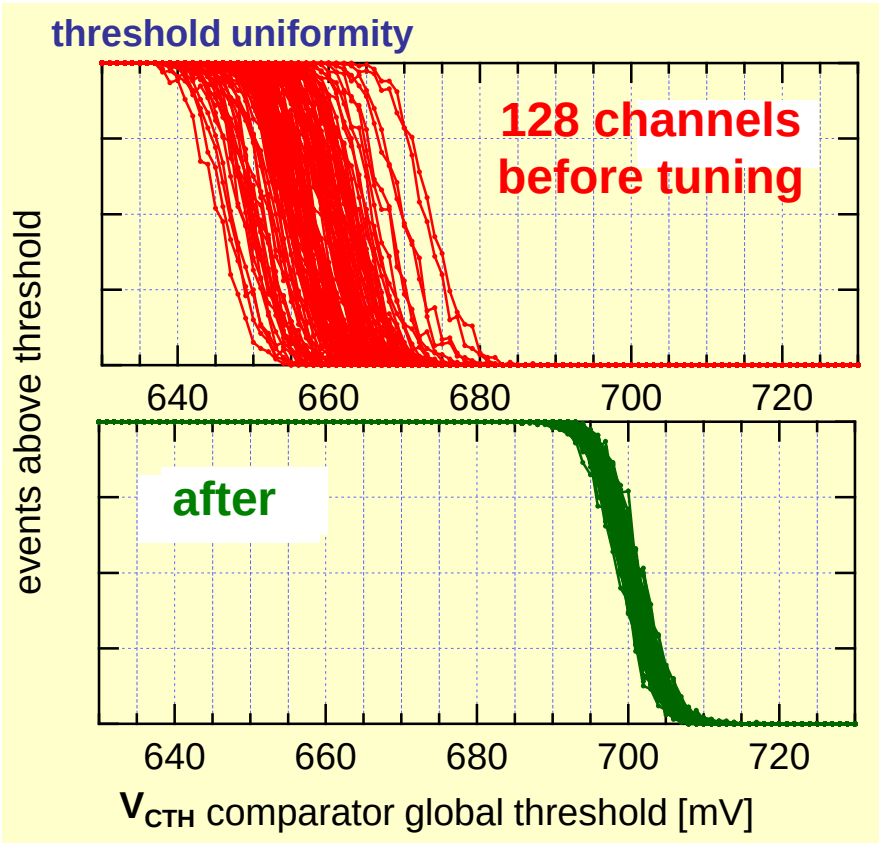
tuning reduces spread to ~ mV level

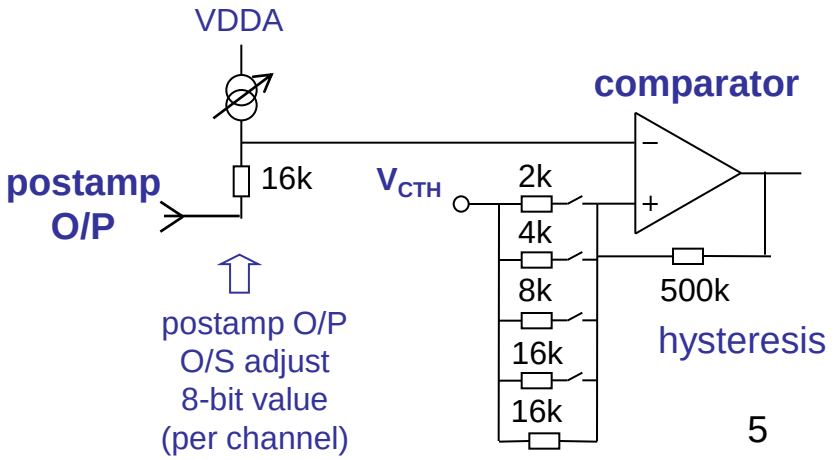
timewalk

timewalk spec.: < 16 ns between 1.25 and 10 fC signals, with comp. threshold set to 1 fC

measurements just within spec.







power features

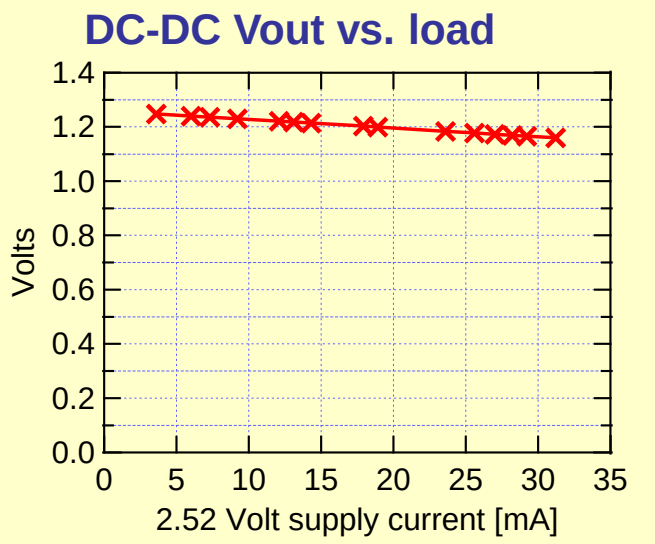
DC-DC switched capacitor converter (CERN)

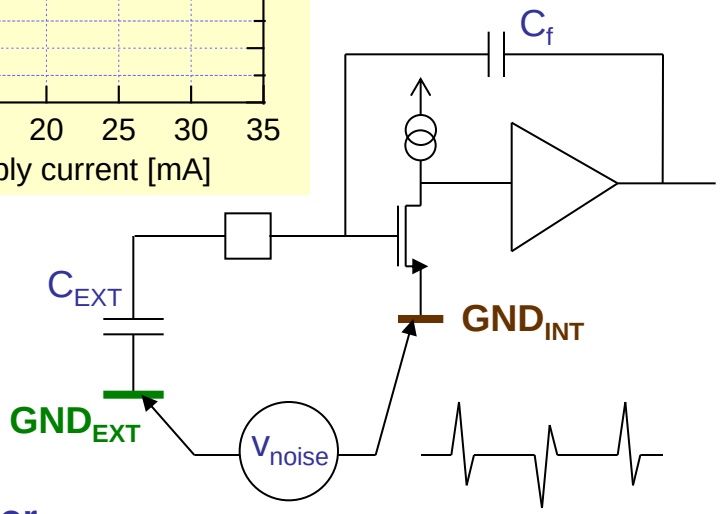
converts 2.5 -> ~ 1.2
works well: ~ 90% efficiency

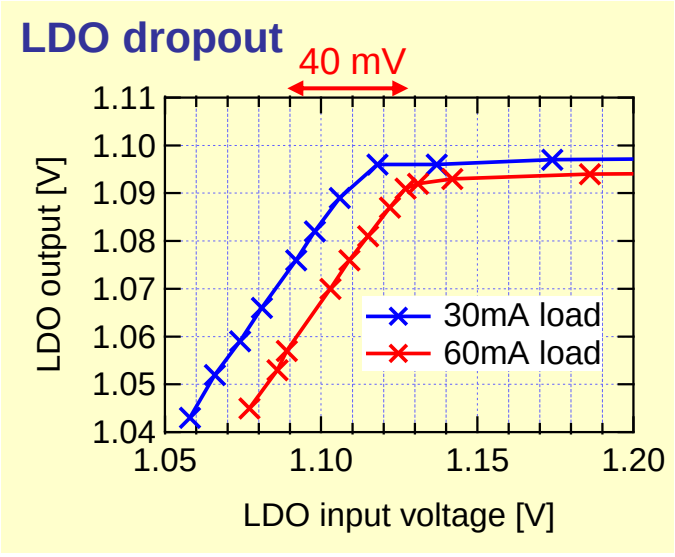
but switch noise produces difference between internal and external grounds

=> interference depending on C_{EXT}

improved circuit on CBC2, and bump-bonding should help







LDO linear regulator

provides clean, regulated rail to analog FE (uses CERN 130 nm bandgap)

~ 1.2 Vin, 1.1 Vout

dropout ~ 40 mV for 60 mA load

provides > 30dB supply rejection up to 10 MHz

CBC1 summary

- successful first prototype in 130 nm

  most things worked - some bugs needed workarounds (front end CM stability issues)

- learned some valuable information

  e.g. performance vs. power trade-offs

  <1000e achievable for < 5 mW / channel (target specifications achieved)

- performance verified in test beam

- in the meantime... (2011 - 12)

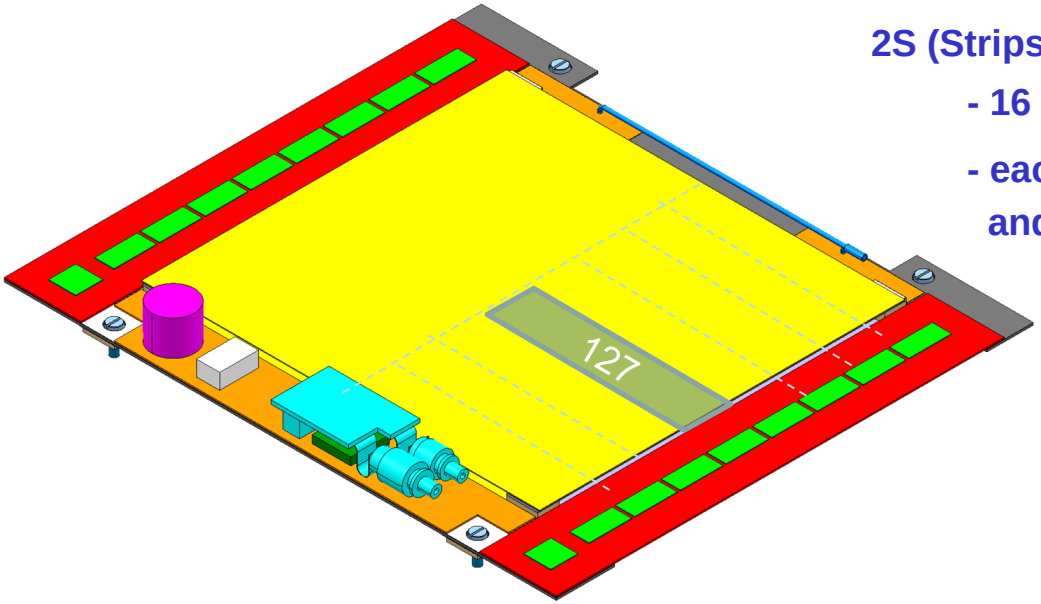
  2S-pT module concept developing

  ideas for implementing triggering functionality from strips in outer tracker

  ideas on simplifying module construction (bump-bonding)

-> CBC2

CBC2 for 2S-Pt module



2S (Strips-Strips) module

- 16 readout chips

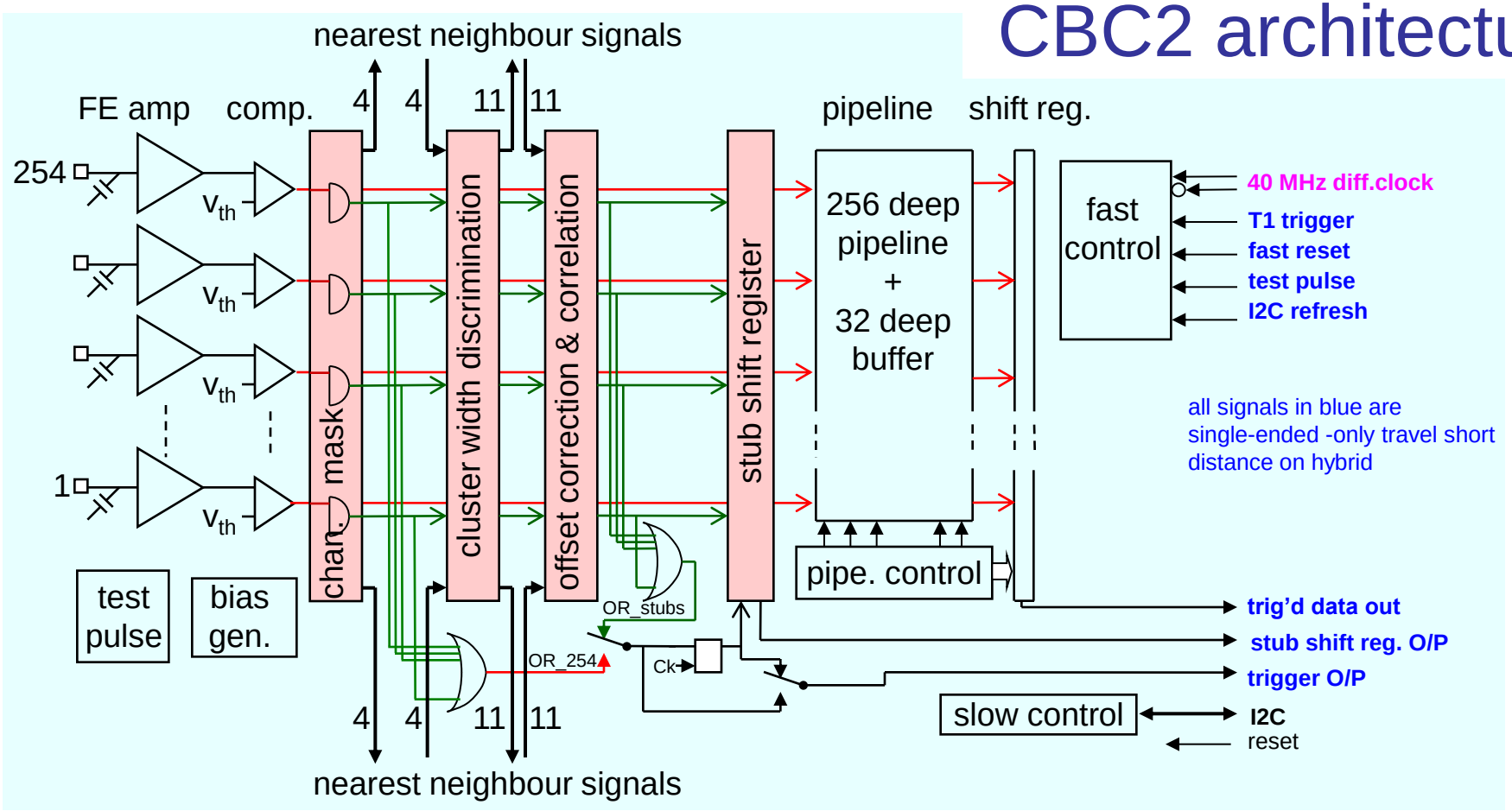
- each reads 127 strips from bottom sensor and 127 from top

CBC2

bump-bond chip, brings signals from 2 sensor layers in 1 chip (254 channels total)
provides L1 triggered readout data as in prototype
also performs cluster correlations to identify high Pt stub
positive correlation produces trigger output

=> functionality required to construct and evaluate prototype 2S-Pt module

CBC2 architecture



front end, pipeline, L1 triggered readout, biasing

~ same as prototype (some bug fixes) twice as many channels

new blocks associated with Pt stub generation

channel mask: block problem channels (not from L1 pipeline)

cluster width discrimination: exclude wide clusters > 3

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

trigger O/P: in normal operation 1 bit per BX indicates presence of high Pt stub

test pulse

charge injection to all channels (8 groups of ~32), programmable timing and amplitude

stub finding logic

cluster width discrimination (CWD) logic

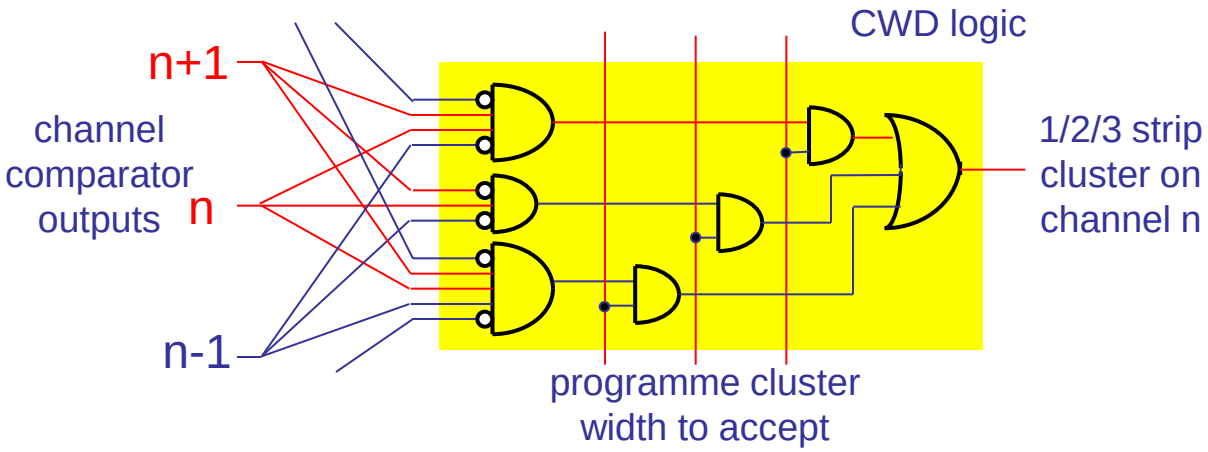
exclude clusters with hits in >3 neighbouring channels
wide clusters not consistent with high pT track

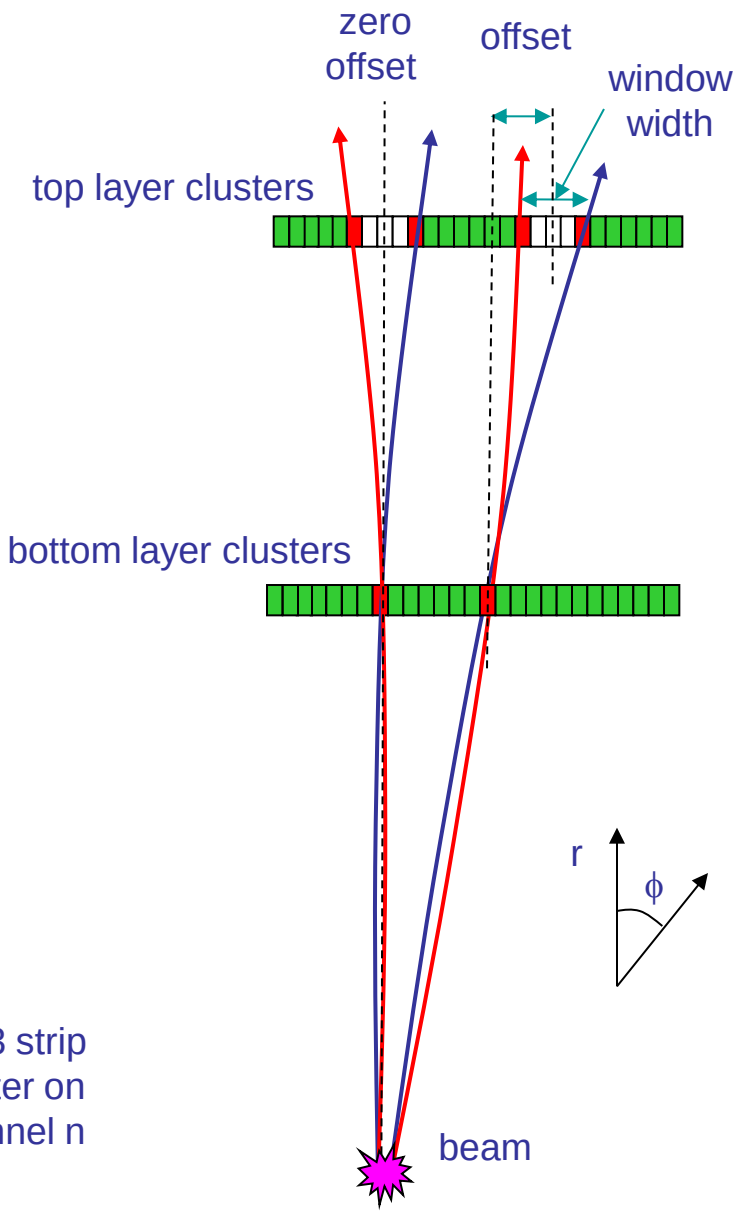
offset correction & correlation logic

for a cluster in bottom layer, look for correlating cluster occurring in window in top layer

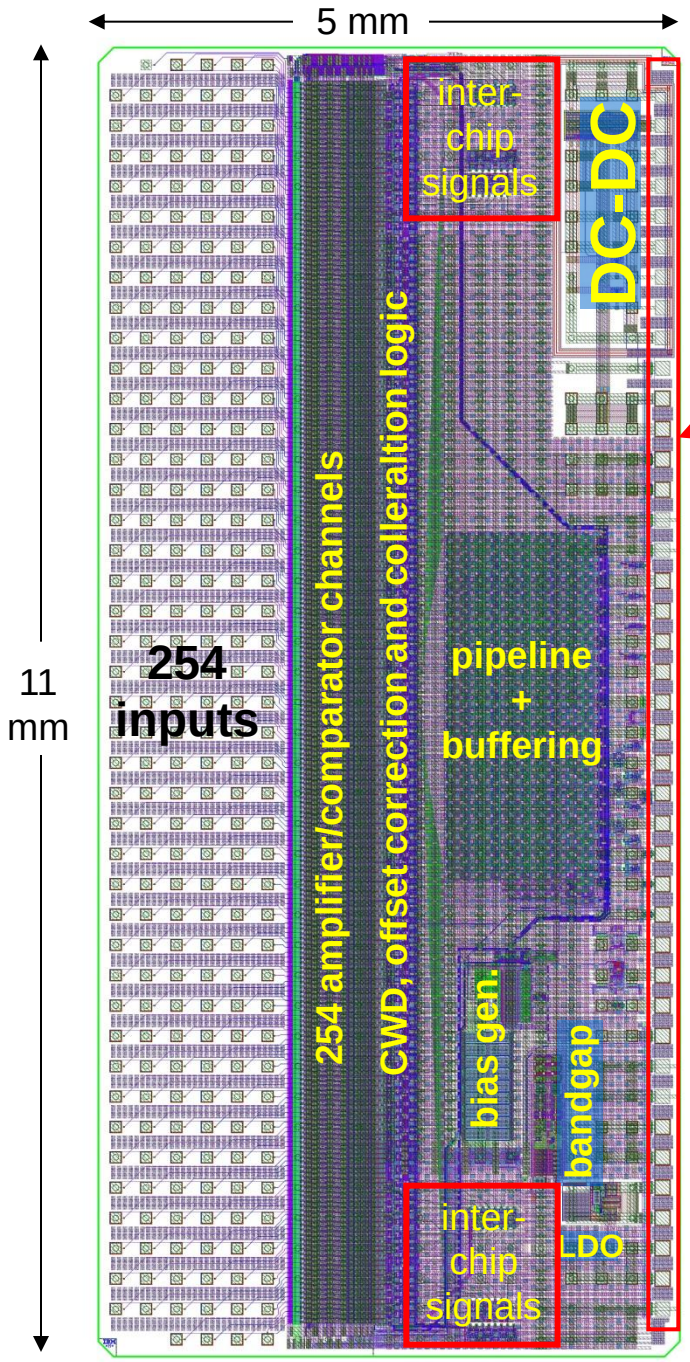
window width controls pT cut
stub found if cluster in bottom layer corresponds to cluster within window in top layer
window width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels





CBC2 layout



C4 layout, 250um pitch, 19 columns x 43 rows

30 interchip signals (15 in, 15 out), top and bottom gives continuity across chip boundaries

right-most column wire-bond (for wafer probe test)
- access to:
  - power
  - fast control
  - I2C
  - outputs

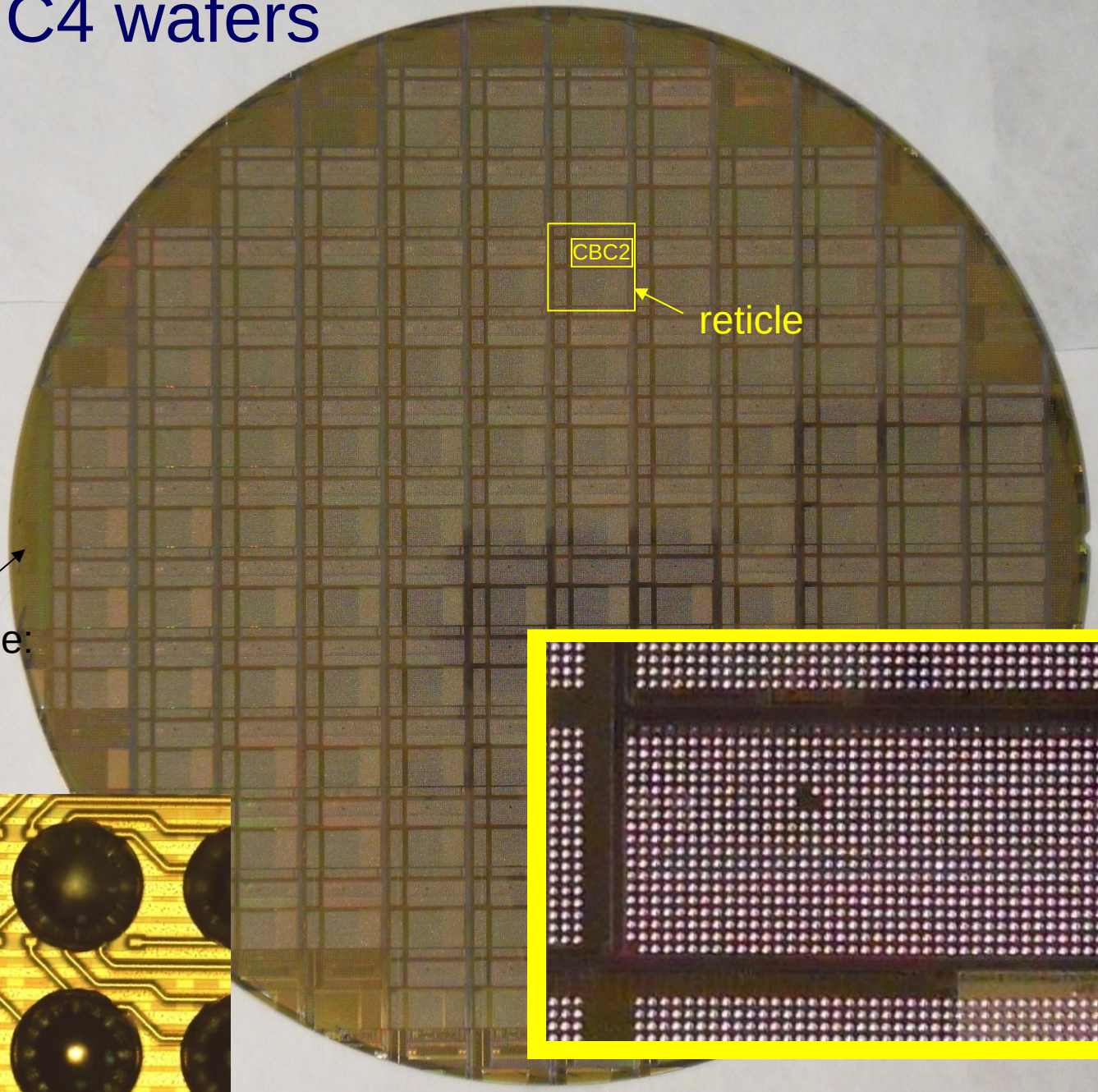
prototype powering features retained
- CERN bandgap, LDO for analog powering, same as prototype
- improved DC-DC switched capacitor circuit (CERN)
  - slower switching edges & rad-hard layout

chip submitted for fabrication July 2012

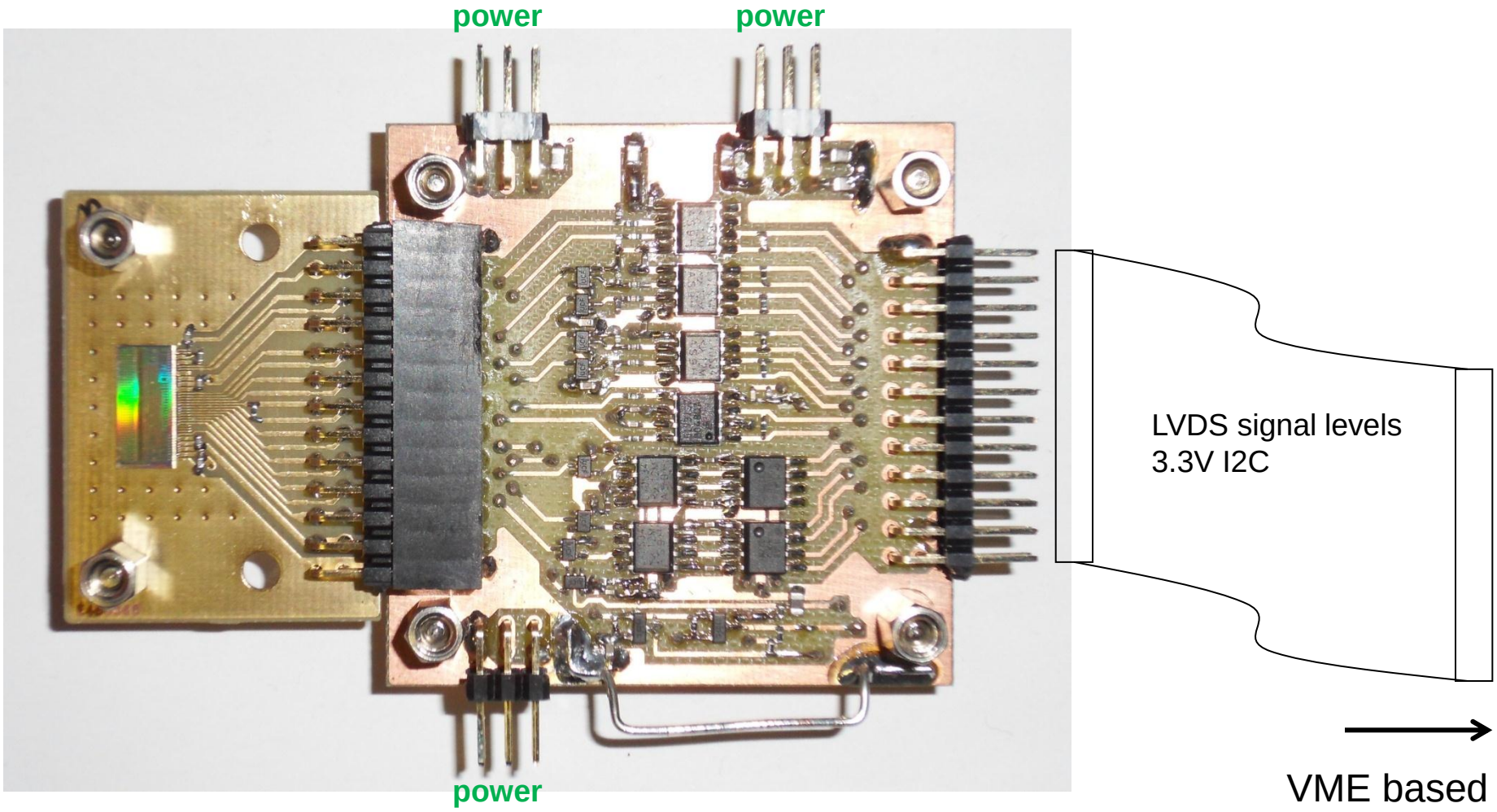
wafers back January 2013

Davide Braga,
Mark Prydderch,
Peter Murray
(RAL)

CBC2 C4 wafers



wirebond CBC2 test setup

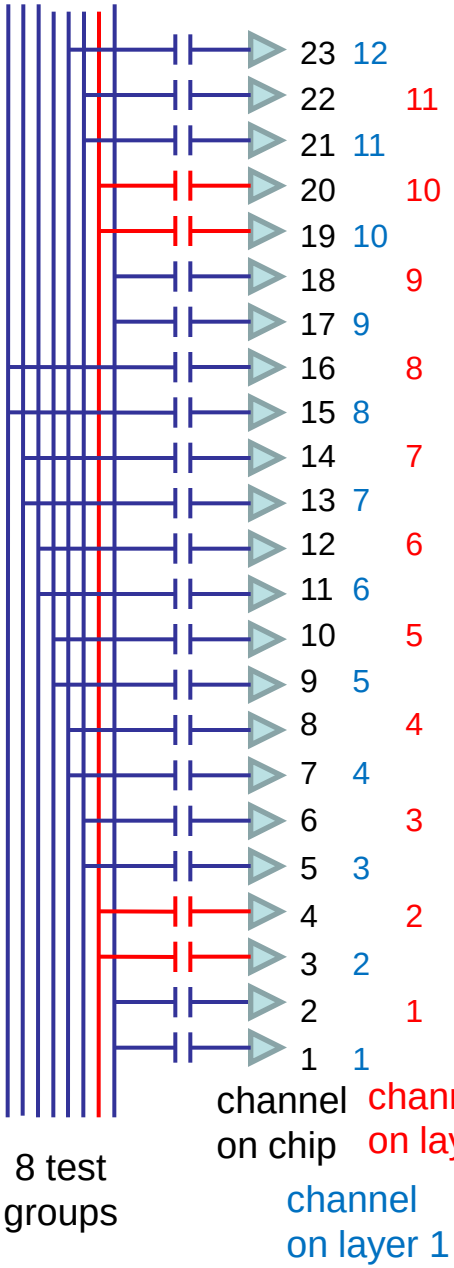


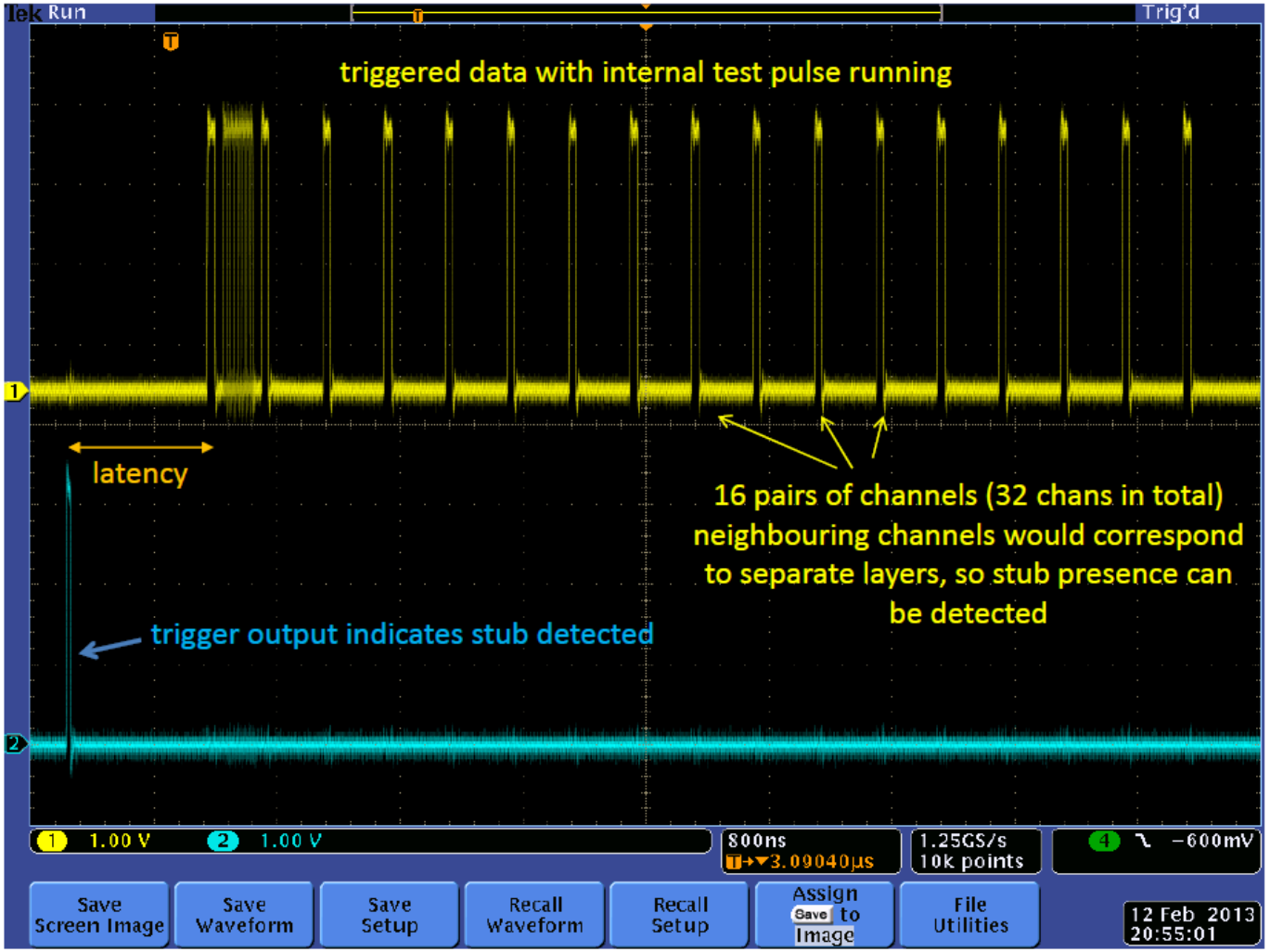
use wafer probe pads to wirebond single CBC2 die to carrier
(CBC2 chips from diced wire-bond (XFEL) wafer)

convenient setup for developing detailed wafer probe procedures

13

first result



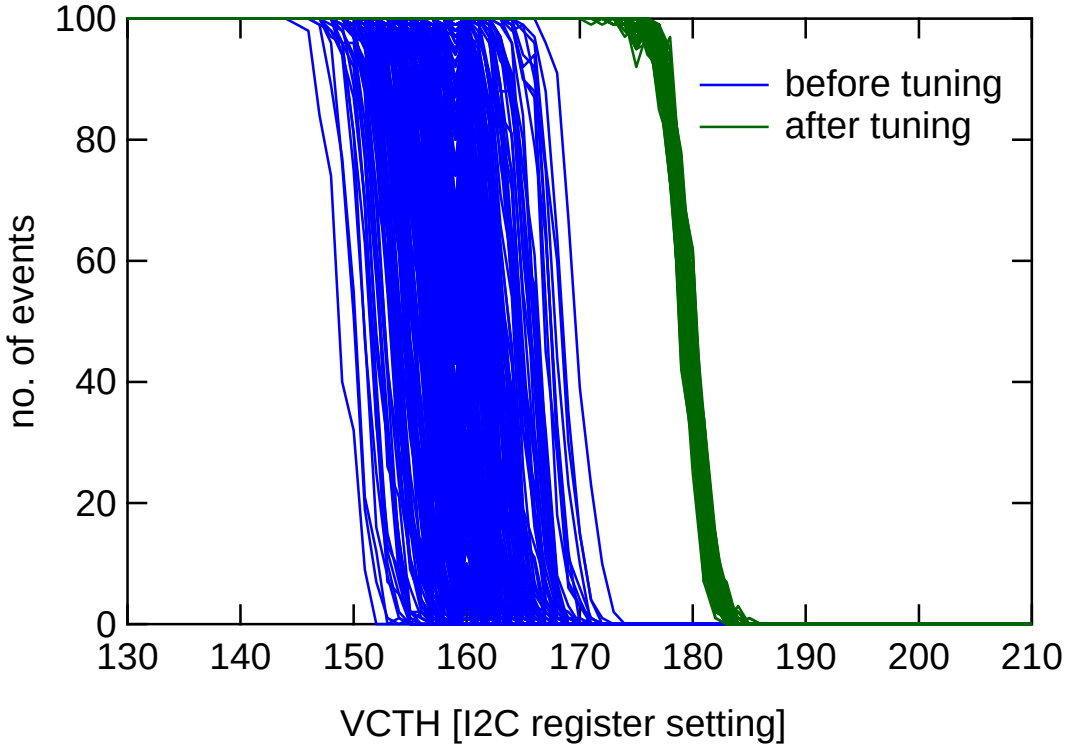


arrangement of 8 groups of test pulse connections allows to simulate signals from different layers and therefore exercise correlation logic

can also verify correlation window width using channel mask register and window offset

=> chip is working

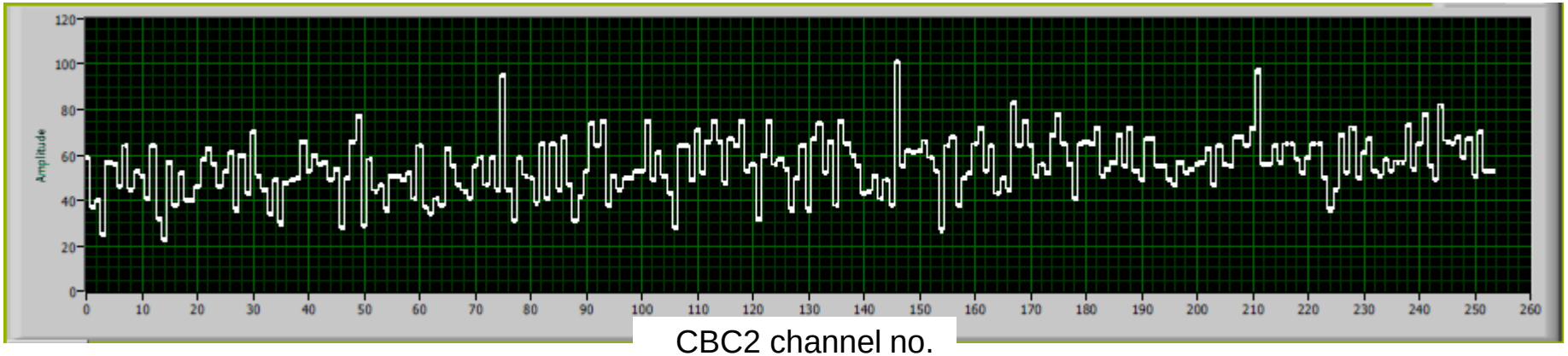
S-curves and tuning



254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to VCTH setting of 180

254 offset values after tuning



CBC2 qualitative observations

emphasis so far on verifying functionality - no detailed study

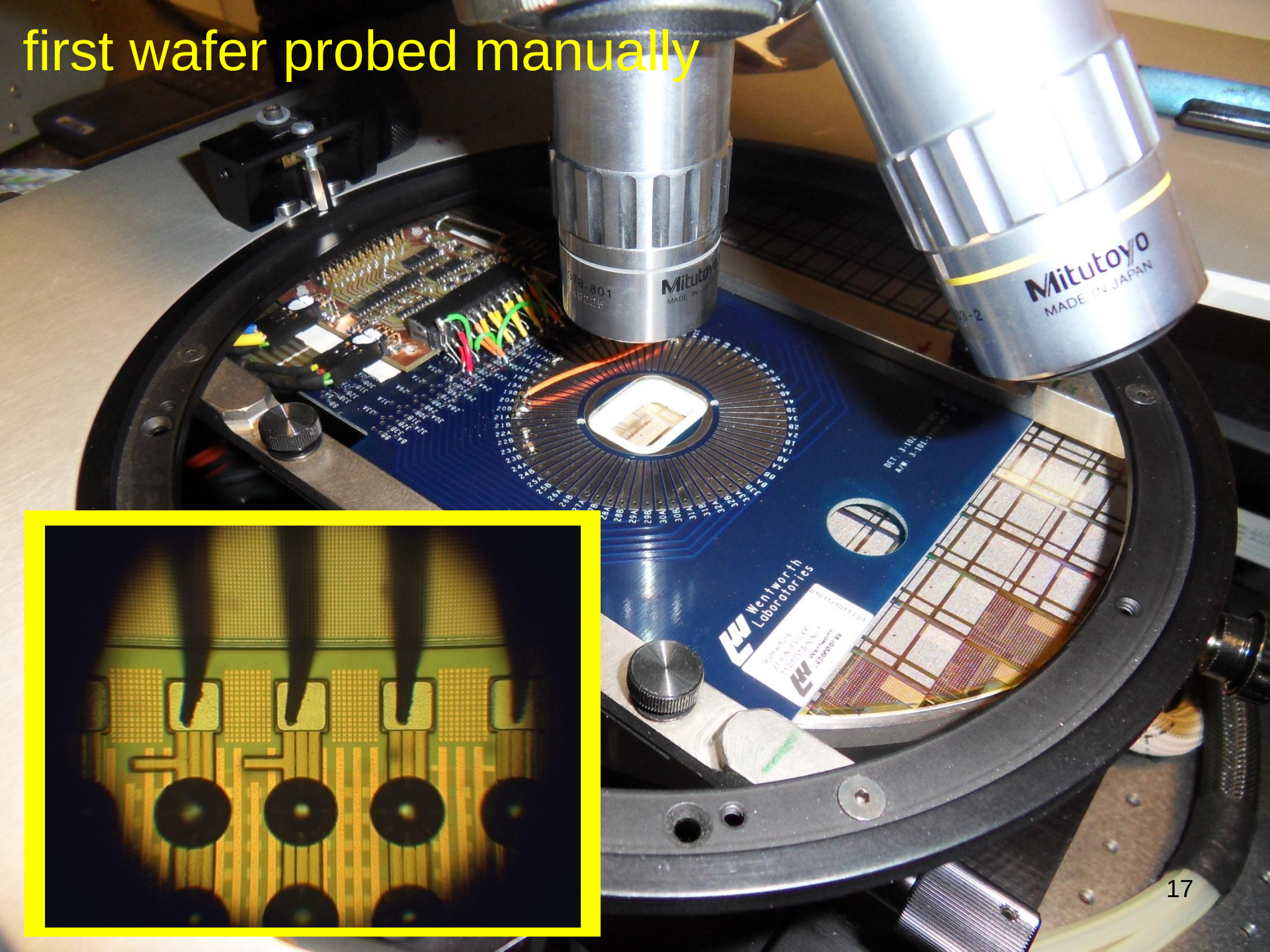
=> have spent most time preparing basic wafer probe test

what can be said so far?

no signs of instability => fixes have worked
power consumption seems “about right”
LDO functioning as expected
2.5 -> 1.2 DC-DC converter also functioning
correlation and window logic verified as far as possible

detailed studies may yet show undesirable features, but chip almost certainly working well enough to allow module development to progress

first wafer probed manually



wafer test procedure

chip clocked at 40MHz
I2C parameters downloaded

not an exhaustive test - but should be enough to differentiate bump-bond assembly problems from chip problems

power consumption recorded

power consumption dependence on I2C value for some bias currents swept

final yield for 1st wafer

112 reticles
108 good chips
4 bad chips

bad chips due solely to physical damage from probe card

bad chip

CBC2

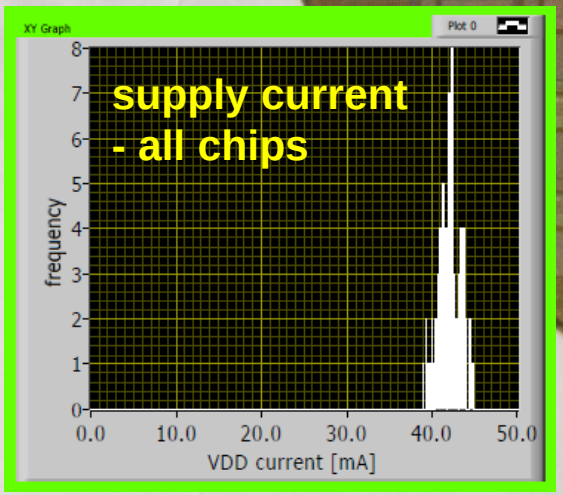
reticle

no defective channel found on any of 112 chips tested on this first wafer

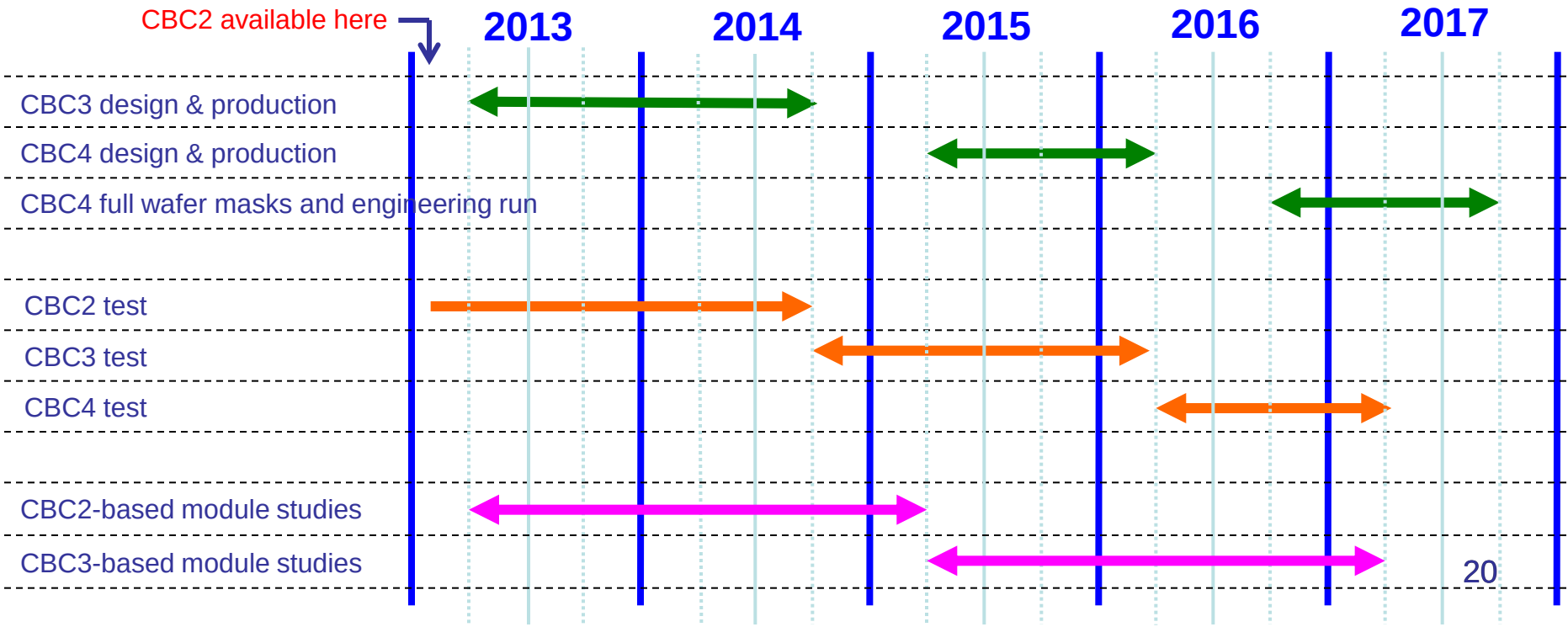
=> 100% yield

perhaps not too surprising if overall wafer yield high

CBC2 is relatively small area of reticle & significant fraction of CBC2 area not occupied by active circuitry



future plans



CBC2 (and modules based on CBC2) will dominate test activity over next ~ 2 years

next prototype, **CBC3**, should be very close to final chip – available towards end 2014

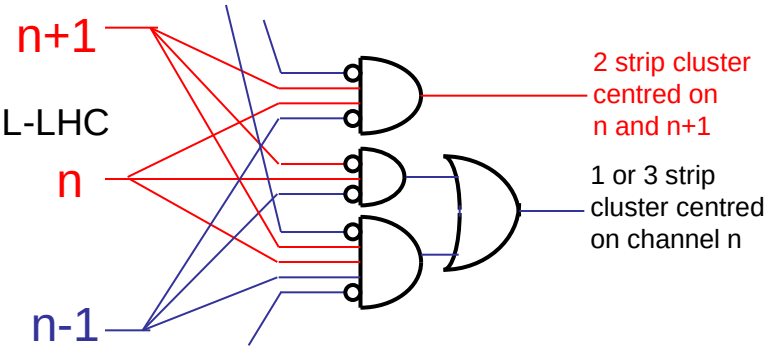
incorporate functionality to generate and transmit stub addresses

… new features

CBC4 pre-production iteration (2015/16) allows final bug fixes before full-wafer engineering run in 2017

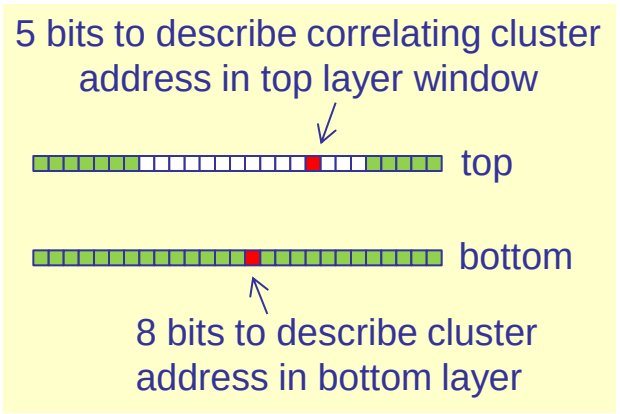
~ 5 years assumed for large scale production, module construction, integration, commissioning, …

CBC3 - the “final prototype”



next version of chip should incorporate all features required for HL-LHC

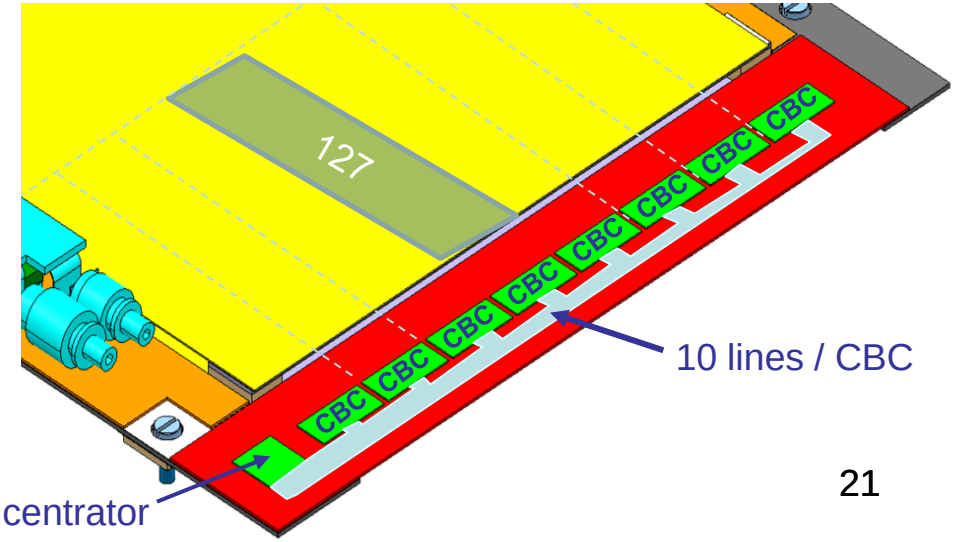
- **final choices for front end**
  - ½ strip cluster resolution
    - 2 strip cluster position assigned to mid-point
- **stub data definition**
  - 8 bits address (for ½ strip resolution) of cluster in bottom layer
  - 5 bit bend information
    - address of correlating cluster in top layer
- **stub data formatting & transmission to concentrator**
  - 13 bit / stub, up to 3 stubs/BX => 39 bits
  - +1 bit unsparsified L1 triggered readout data
  - => 40 bits / 25 nsec
    - e.g. 10 lines at 160 Mbps (per chip)
- **other useful features**
  - e.g. slow ADC to monitor bias levels
  - …



CBC data to concentrator

25 ns

S1	S1	S1	S1	S1	S1	S1	S1	B1	B1
B1	B1	B1	S2	S2	S2	S2	S2	S2	S2
S2	B2	B2	B2	B2	B2	S3	S3	S3	S3
S3	S3	S3	S3	B3	B3	B3	B3	B3	**R**



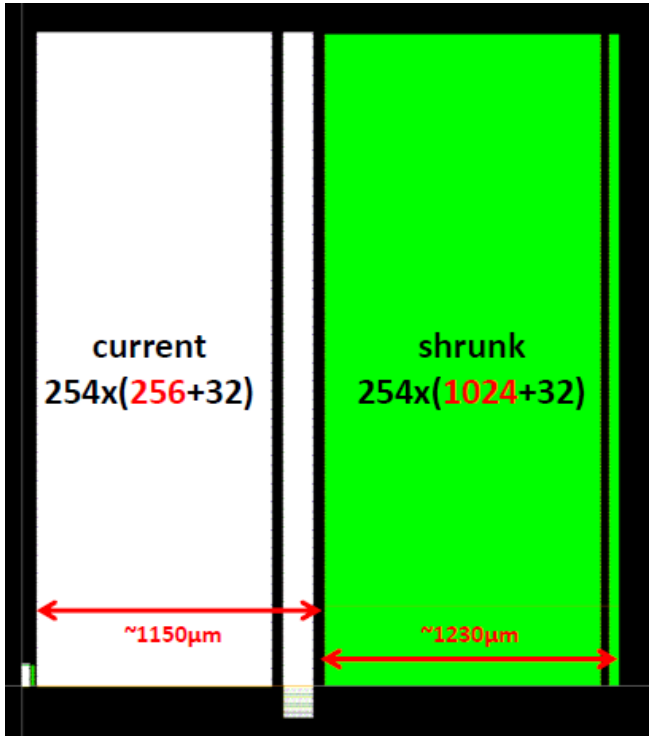
recent developments

- up to now have assumed max. L1 latency of 6.4 usec and L1 accept rate 100 kHz
  - constraints originate in ECAL readout electronics

- ECAL now considering FE board replacement – removing these constraints

- can we increase latency on CBC?
  - factor 4 increase seems feasible ~25 usec
  - denser pipeline layout should mean chip doesn't need to grow (much)
  - longer latency beneficial for L1 data processing

- can we increase trigger rate capability (500 kHz?, 1 MHz?)
  - wider implications for architecture
  - at ~ 500 kHz unsparsified readout data dominates available off-module bandwidth
    - no room left for stub data
  - at 1 MHz sparsification becomes unavoidable
    - where to do it? front end chip? concentrator?



D.Braga (RAL)

summary

- CBC2 early test results look promising
  - appears to be working well enough to allow progress with module development
  - subtleties of performance will become clear when chips are bump-bonded
    - dual CBC2 substrates (Georges Blanchot)

- substantial test effort
  - chip: performance vs. temperature, radiation, powering scheme, …
  - module: performance in lab and test beam
    - mini-module using dual CBC2, and full-size 8-chip substrates

- further CBC development plans matched to large scale tracker construction effort beginning ~ 2017
  - CBC3 should be final prototype
  - ongoing effort to finalise specs., functionality and interfaces
  - submission mid 2014

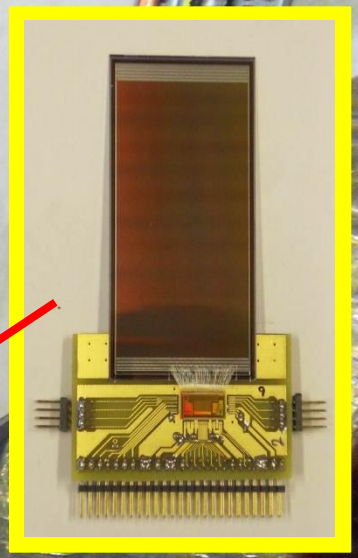
extra

CBC1 test beam in 2012: Oct. 8th - 22nd

CBC prototype + Infineon sensor (Vienna)
300 um thick, p-on-n
5cm long strips, 80 um pitch
close to dimensions proposed for 2S-Pt modules

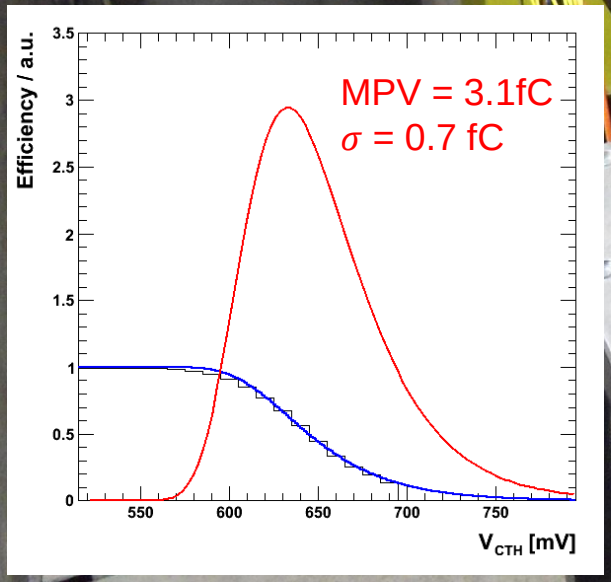
beam tracking plane using APV

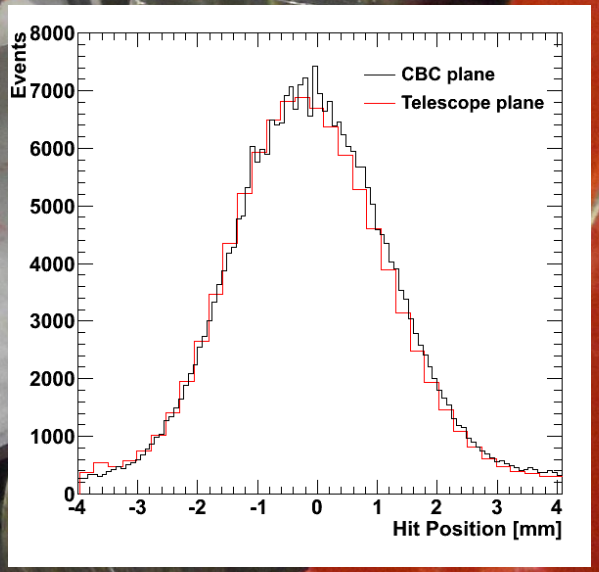
scintillator



CBC + Infineon sensor box

400 GeV protons





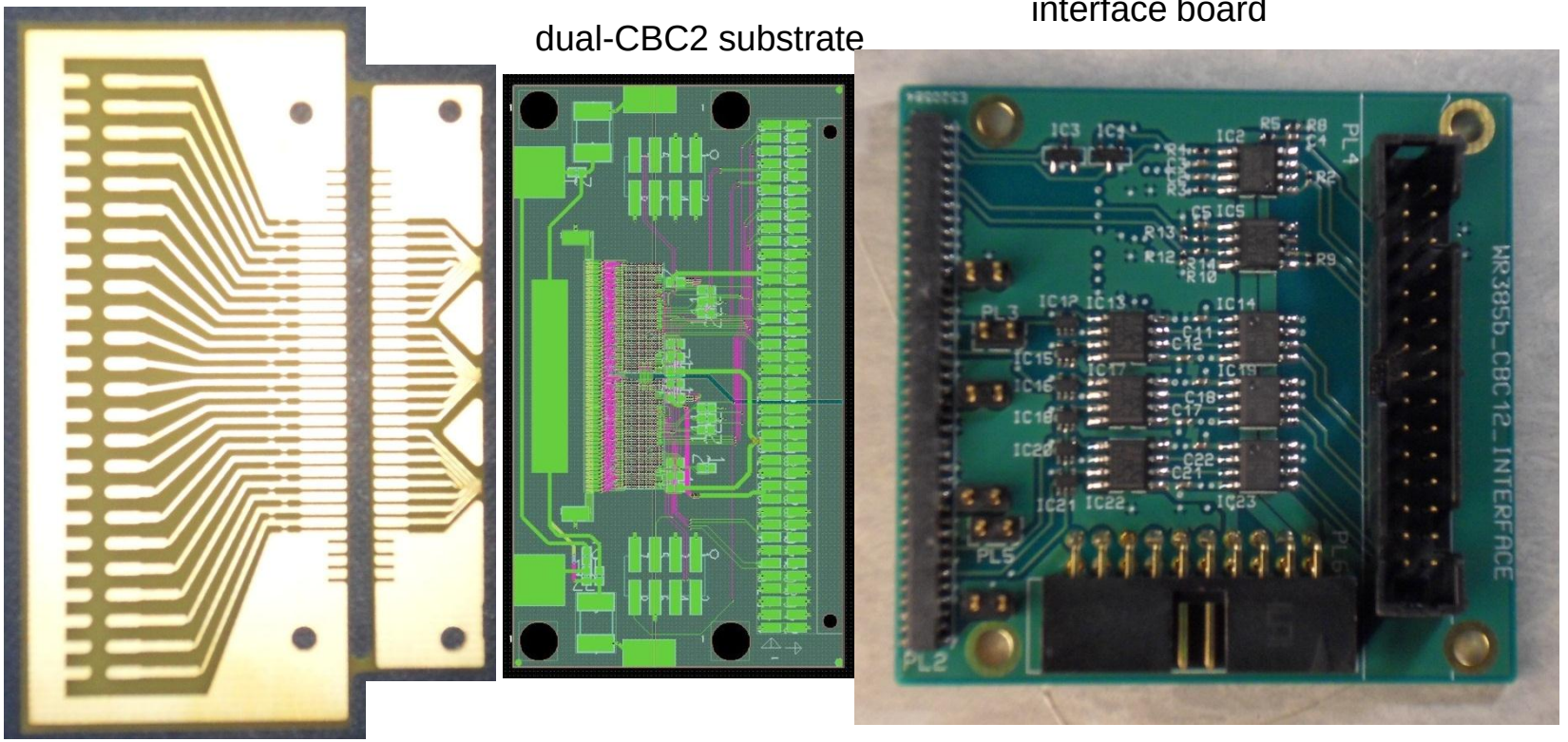
dual-CBC2 substrate test setup

charge inject

PA

dual-CBC2 substrate

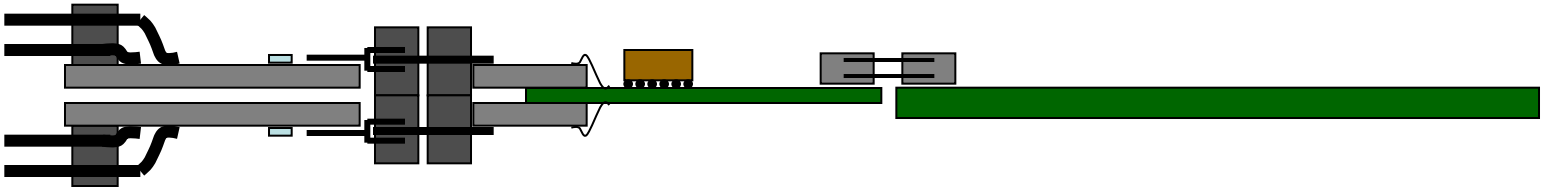
interface board



LVDS signal levels

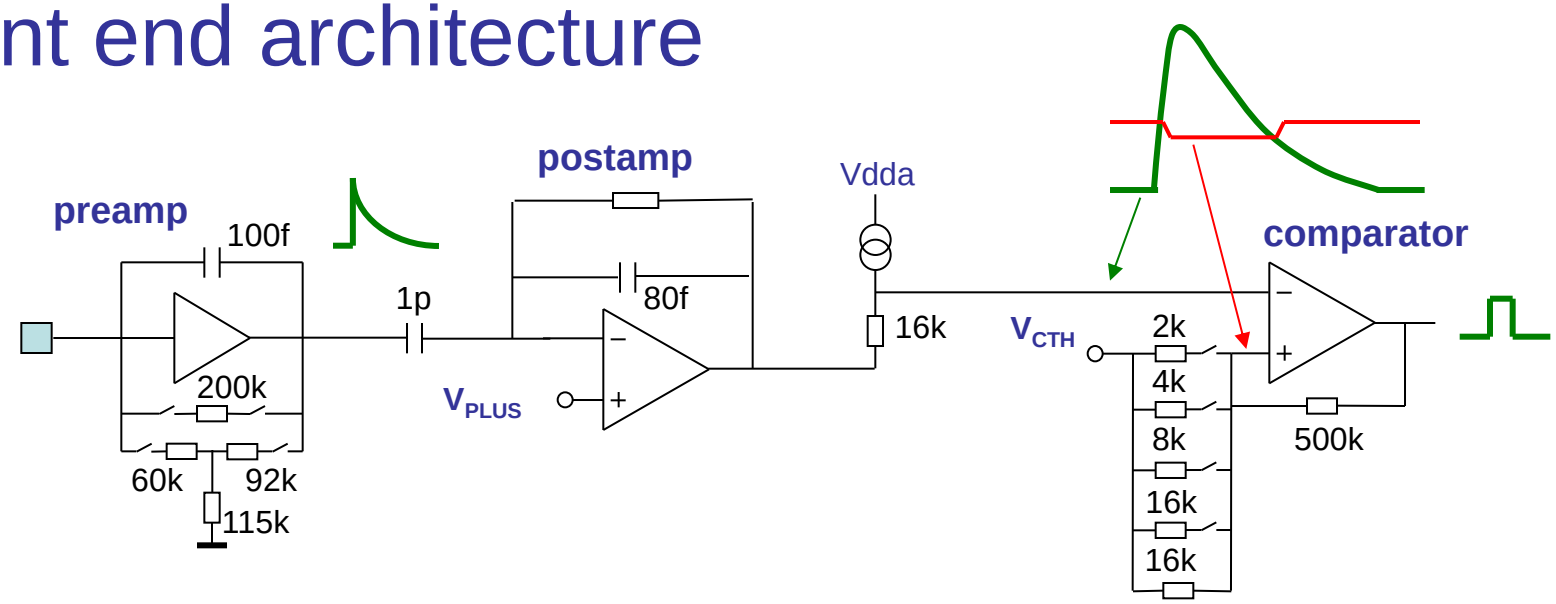
3.3V I2C

power



2xCBC substrate + PA (both sides) becomes device under test
pluggable charge inject board allows different external capacitance

front end architecture



preamp

resistor feedback absorbs I_{LEAK}
works with both sensor polarities
electrons: single 200k resistor
holes: T-network (equiv to 200k)
RfCf implements short 20ns time constant (no pile-up issues)

postamp

AC coupled removes DC shift from leakage current
provides gain: ~50 mV / fC at comparator input
individually programmable O/P DC level implements
channel threshold tuning

comparator

global threshold V_{CTH}
programmable hysteresis

simulated post-amp output pulse