CBC Power aspects & testing plans

Outline

- brief chip description & current status
- powering options and test features
- test setup status
- summary & plans

CBC introduction (1)

binary, unsparsified architecture, 130 nm CMOS

intended for short strip (few cm) outer tracker readout for Phase 2

amplifier

fast pulse shape (20ns peaking)

DC coupling to sensor (1uA leakage tolerance), compatible with both sensor polarities

noise < 1000e for C_{sensor} = 5 pF

comparator

threshold individually programmable & programmable hysteresis

timewalk < 16ns between 1.25 & 10 fC signals

256 cell pipeline

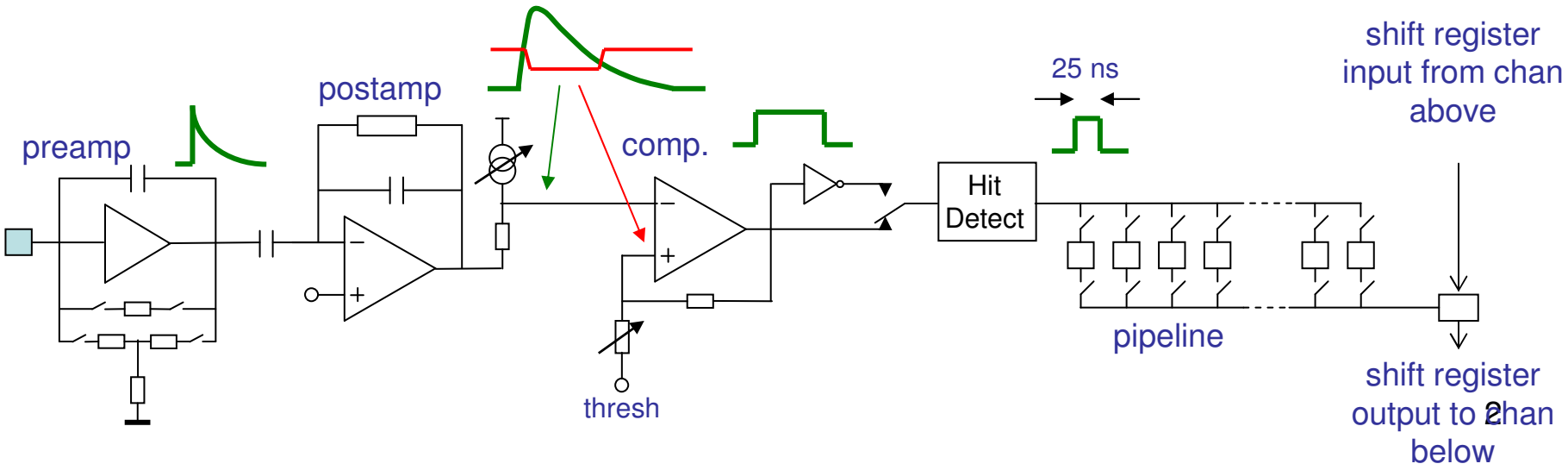
(up to 6.4us latency)

32 deep buffer for triggered data awaiting output

power

target power consumption 0.5 mW / channel (0.2 analog, 0.3 digital)

=> 128 chan chip consumes 20 mA analog, 30 mA digital



CBC introduction (2)

128 channels, 50um input pitch

SLVS inputs and output (fast signals)

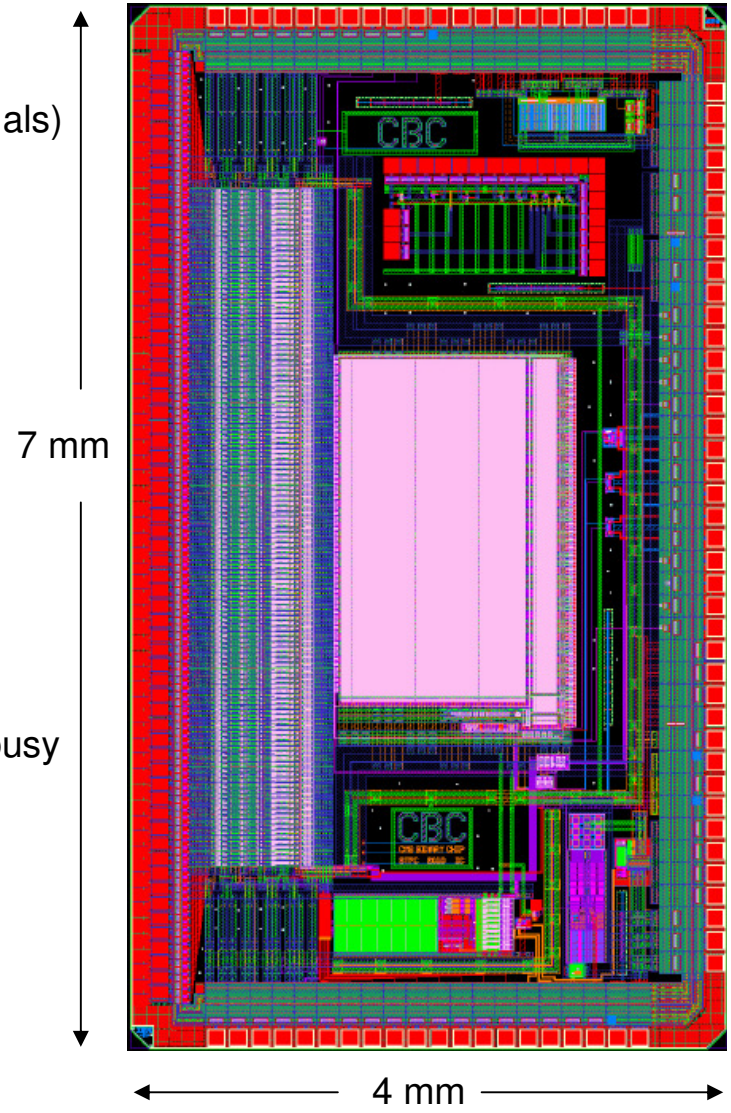
I2C slow control

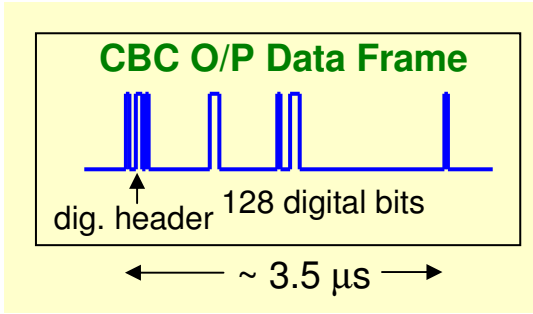
output frame like APV except
digital bits, not analog samples

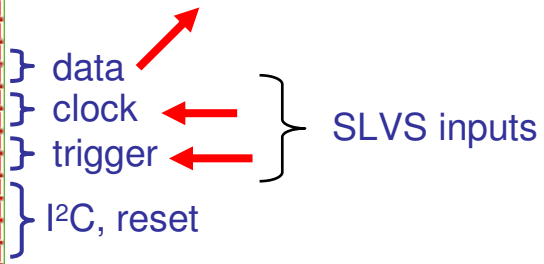
current production status

MPW data to IBM in July
=> we were expecting chips
back ~ October

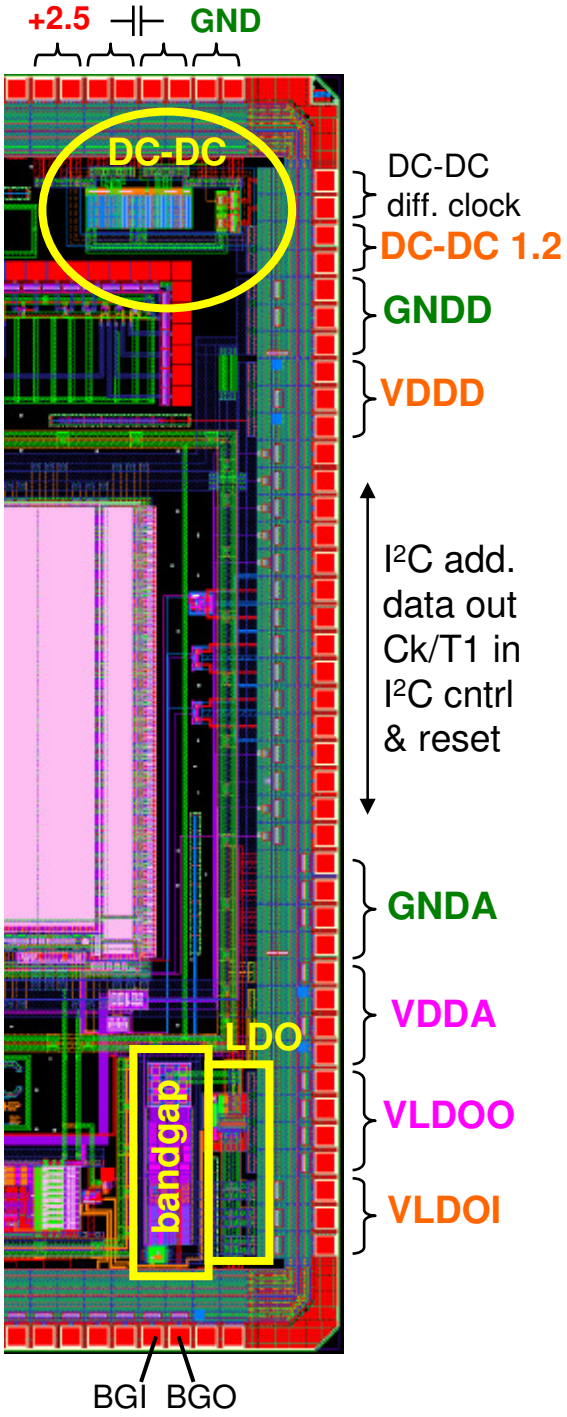
but production delayed, foundry busy
=> now expect wafers delivery
end November
=> chips in hand sometime
in December







CBC powering options



DC-DC switched cap. – Michal Bochenek et al, TWEPP 2010 (& previous talk)

converts 2.5 -> 1.2
can use 1.2 to provide CBC digital rail (**VDDD**)
and to feed LDO input (**VLDOI**)
needs 1 MHz differential clock

LDO linear regulator - PWG, Tracker Upgrade Workshop, Sep.'09

regulates 1.2V input to 1.1V output (**VLDOO**)
can use to power analog circuitry (**VDDA**)
(analog front end designed for 1.1V operation)
provides power supply rejection
uses **CERN bandgap circuit** (Paulo Moreira et al) for ref. voltage

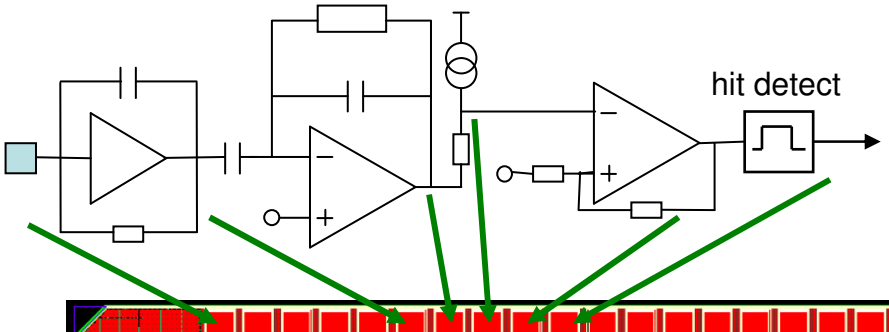
DC-DC block at top right of chip

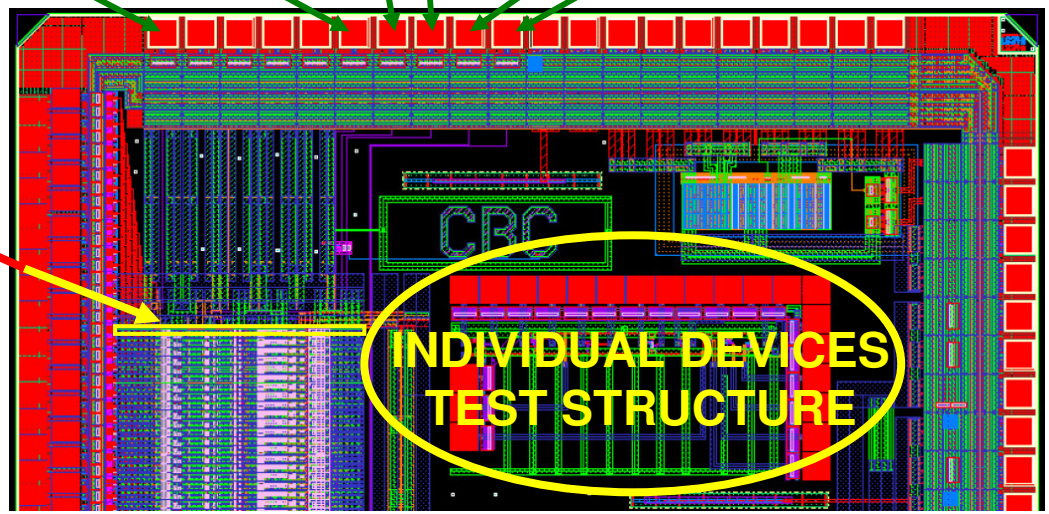
as far as possible from sensitive circuitry (analog front end, bandgap)
not difficult to achieve for this chip
~ plenty of space in this layout
ought to offer good chance of success

power options incorporated with low risk

all pads accessible => individual circuits can be used or bypassed,
to study behaviour with/without the different options
(will show 3 examples)

other test features



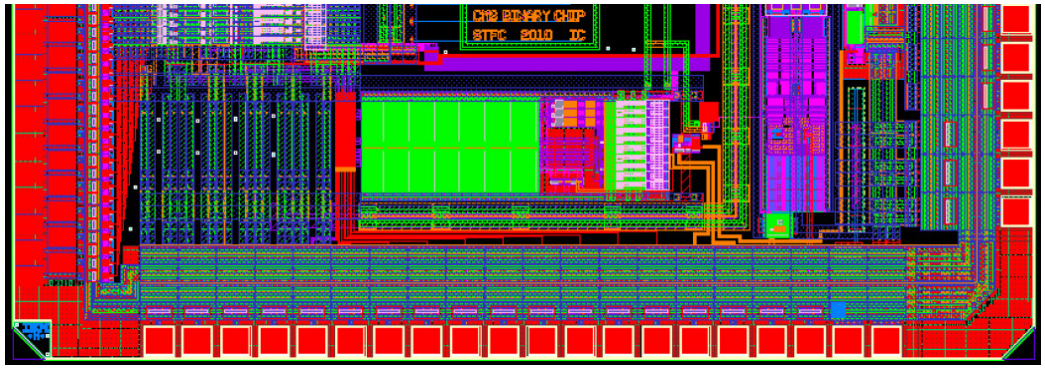


one complete dummy front end channel with buffered signals available along chain on top edge of chip

- may be useful to study powering issues (e.g. interference)

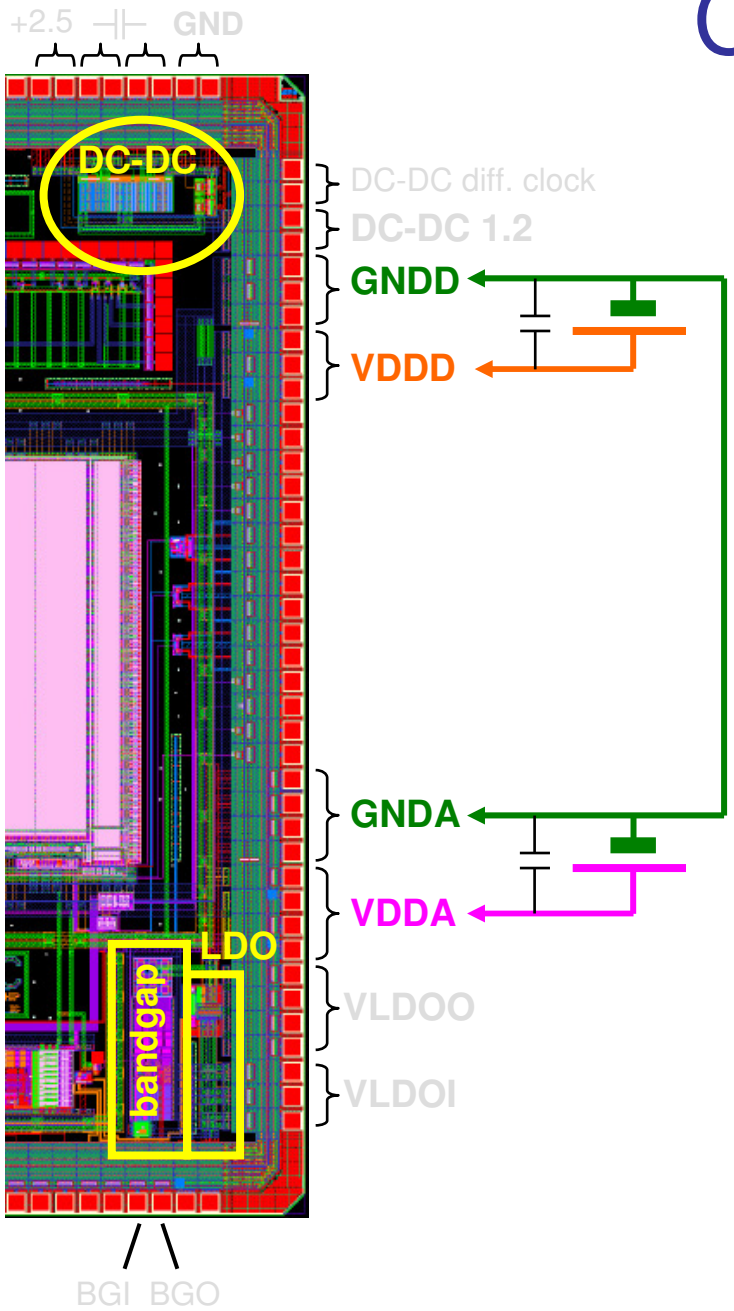
individual devices test structure

- different transistor geometries



access to all bias generator outputs on bottom edge, to allow to study BG performance, diagnose faults, or if necessary, overide

CBC powering options (1)



stage 1: direct powering

don't use any of the on-chip options

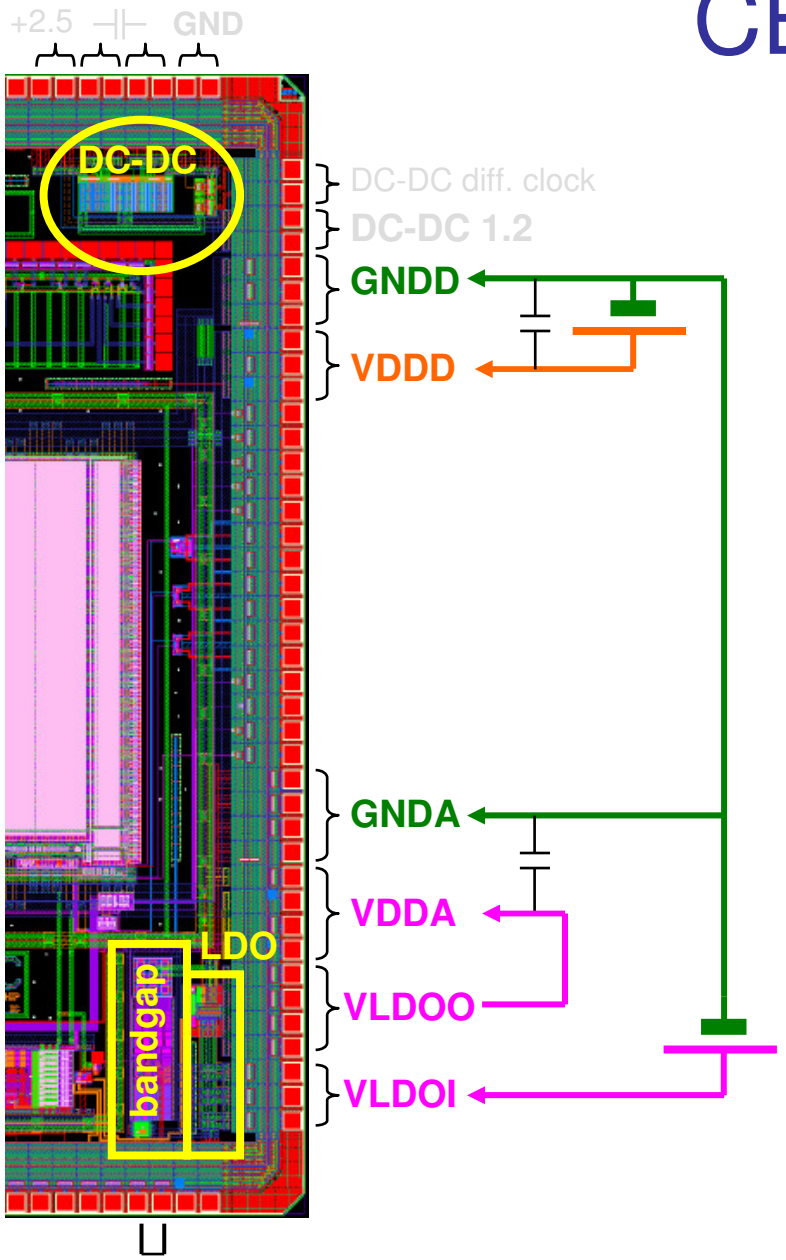
can set **VDDA** (analog) and **VDDD** (digital) independently

investigate digital power savings with lower voltage operation

can add sinusoidal ripple to **VDDA** and measure supply sensitivity

2 external capacitors

CBC powering options (2)



stage 2: analog power via LDO

can still set **VDDD** independently

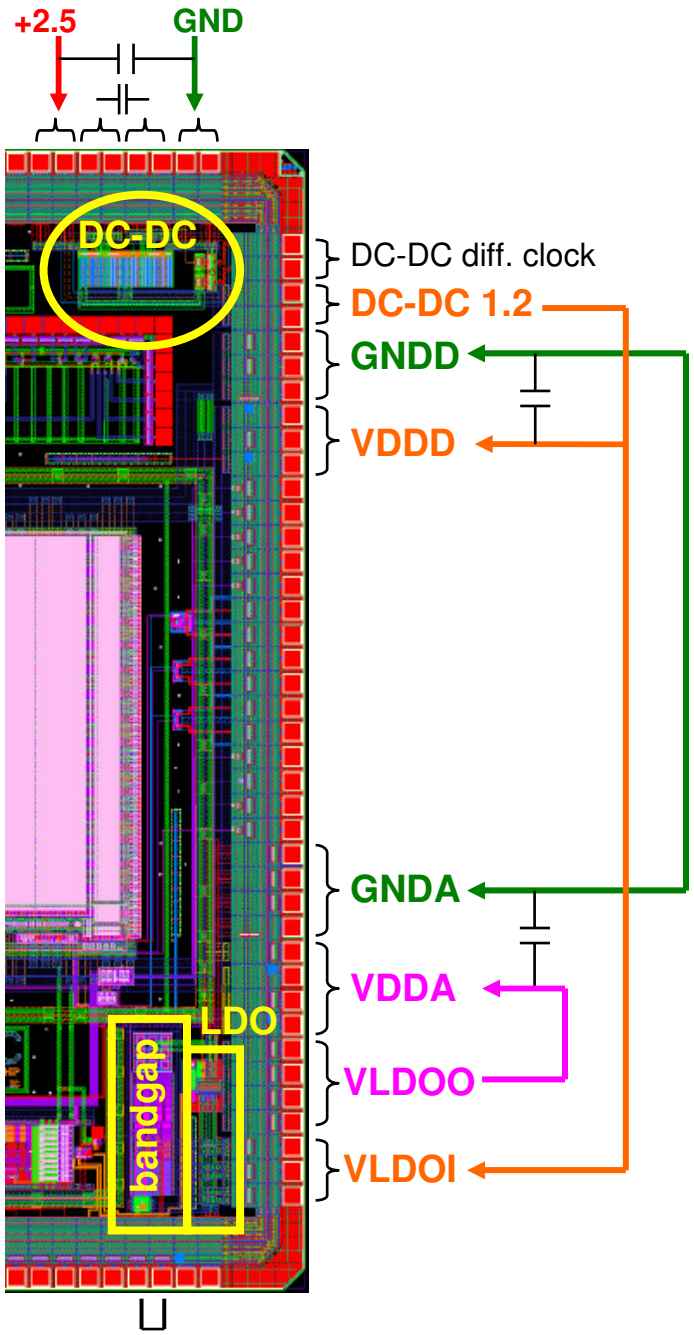
(or use to supply **VLDOI**)

can add sinusoidal ripple to **VLDOI** and measure supply rejection effect

can provide voltage reference to LDO from on-chip bandgap, or from external reference

2 external capacitors

CBC powering options (3)



stage 3: digital power via DCDC & analog power via LDO

one **+2.5V** supply

1 MHz diff. clock to DCDC circuit

DC-DC 1.2 feeds **VDDD** and **VLDOI**

4 external capacitors

how to study effects?

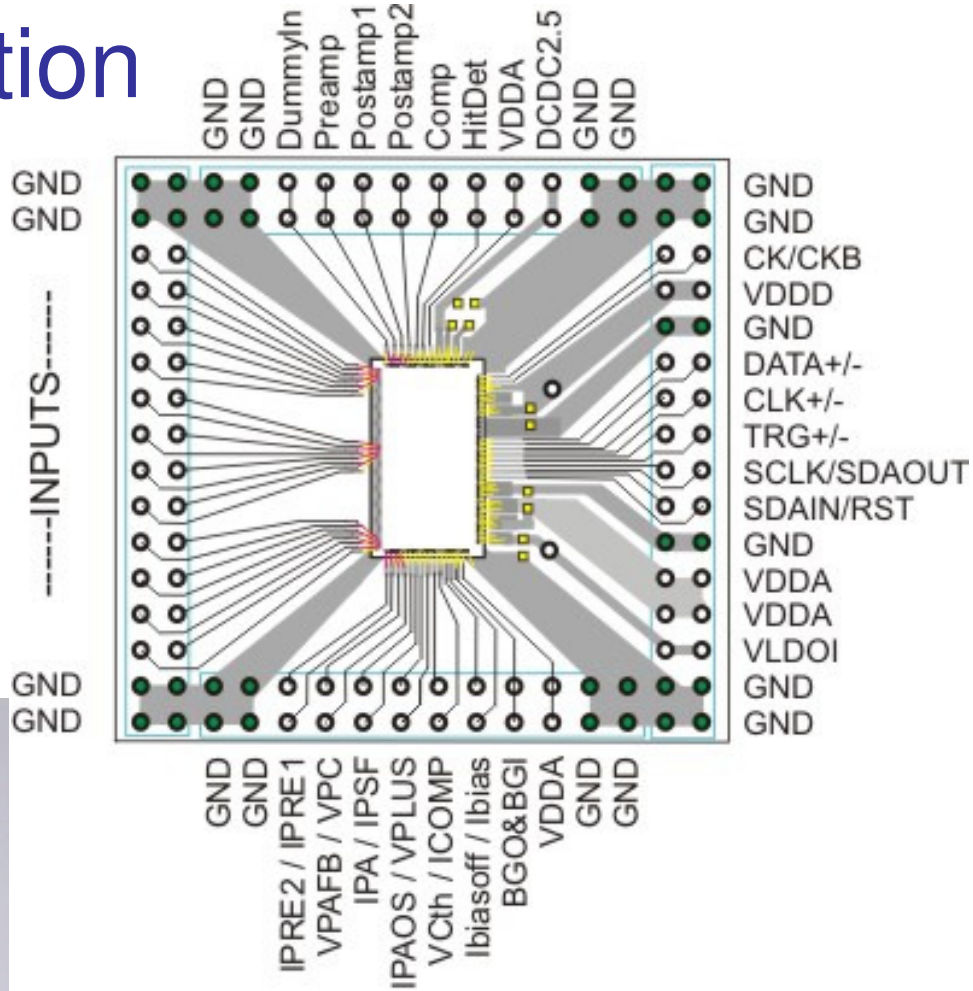
look for distortions in 'S' curves
can look at dummy channel

test setup in preparation

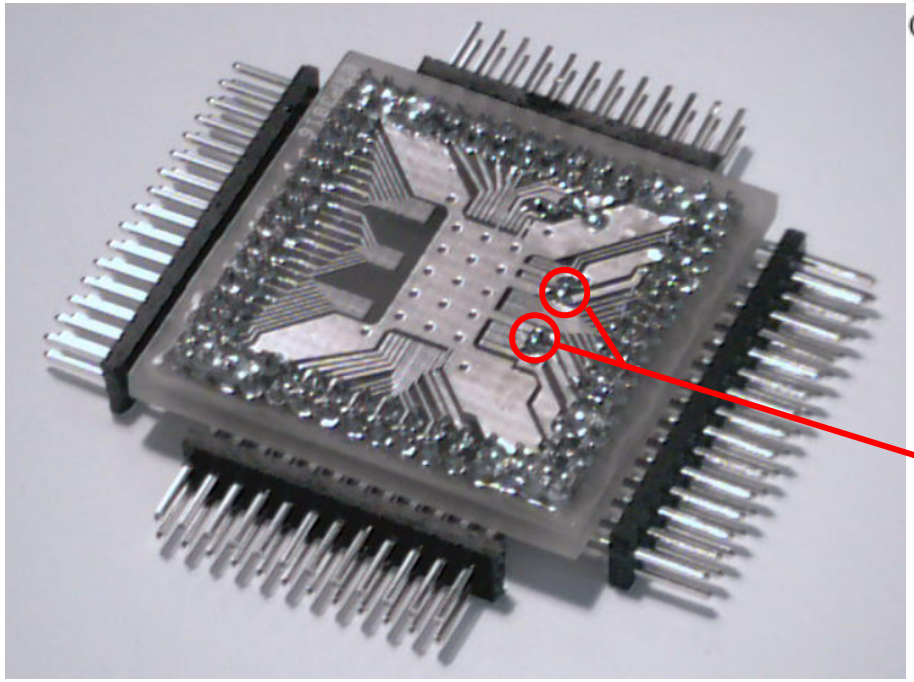
fineline board to take chip already produced

allows to access 24 inputs
8 top, 8 middle, 8 bottom

different bonding configurations on top
& bottom edges depending on particular test
dummy channel, bias generator outputs
or all channel test input signal access

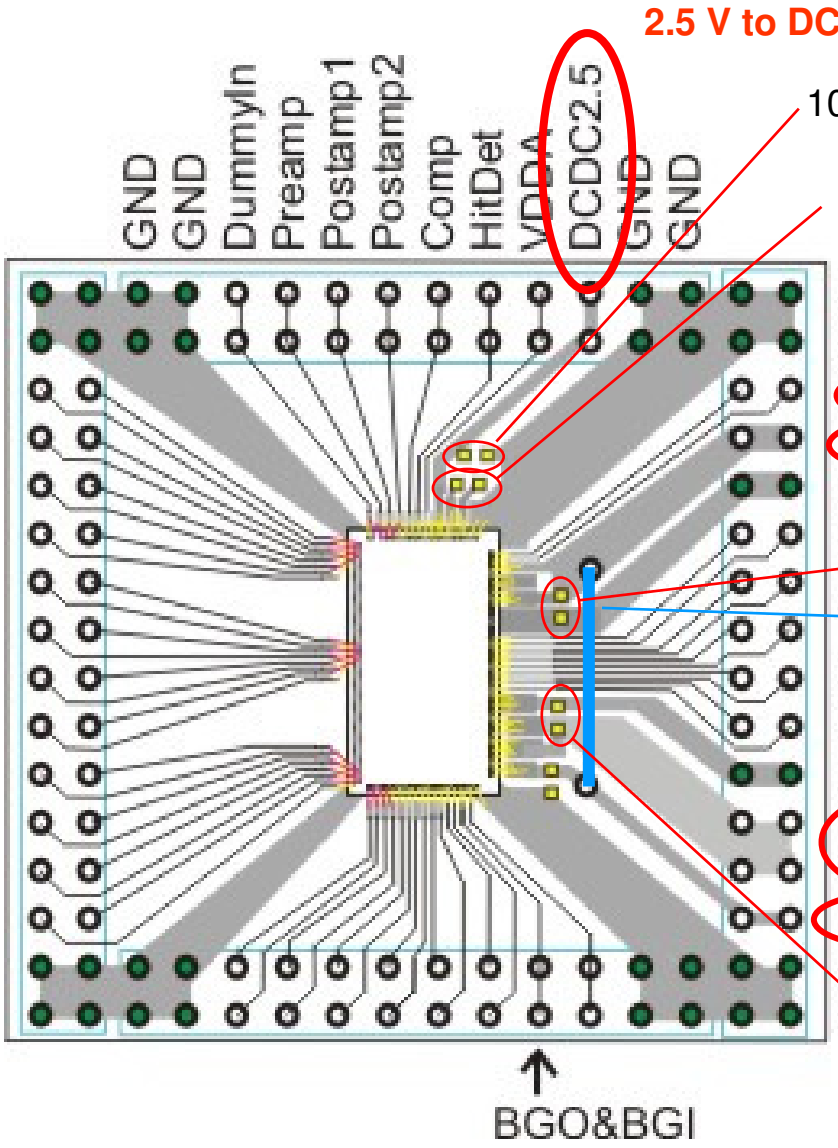


~ 2 x 2 cm^2



0201 capacitors

power provision



2.5 V to DC-DC

100 nF (0201) decoupling on 2.5 V rail

1 uF (0402) flying capacitor for DC-DC

1 MHz differential clock to DC-DC

DC-DC provides ~ 1.2V digital supply to CBC
(or don't bond DCDC and supply VDDD externally)

decoupled by 220 nF (0201)

wire link can also take DC-DC output to…

…LDO input

LDO output connected to **VDDA**
(or don't bond VLDOO and supply VDDA externally)

100 nF (0201) decoupling on LDO output

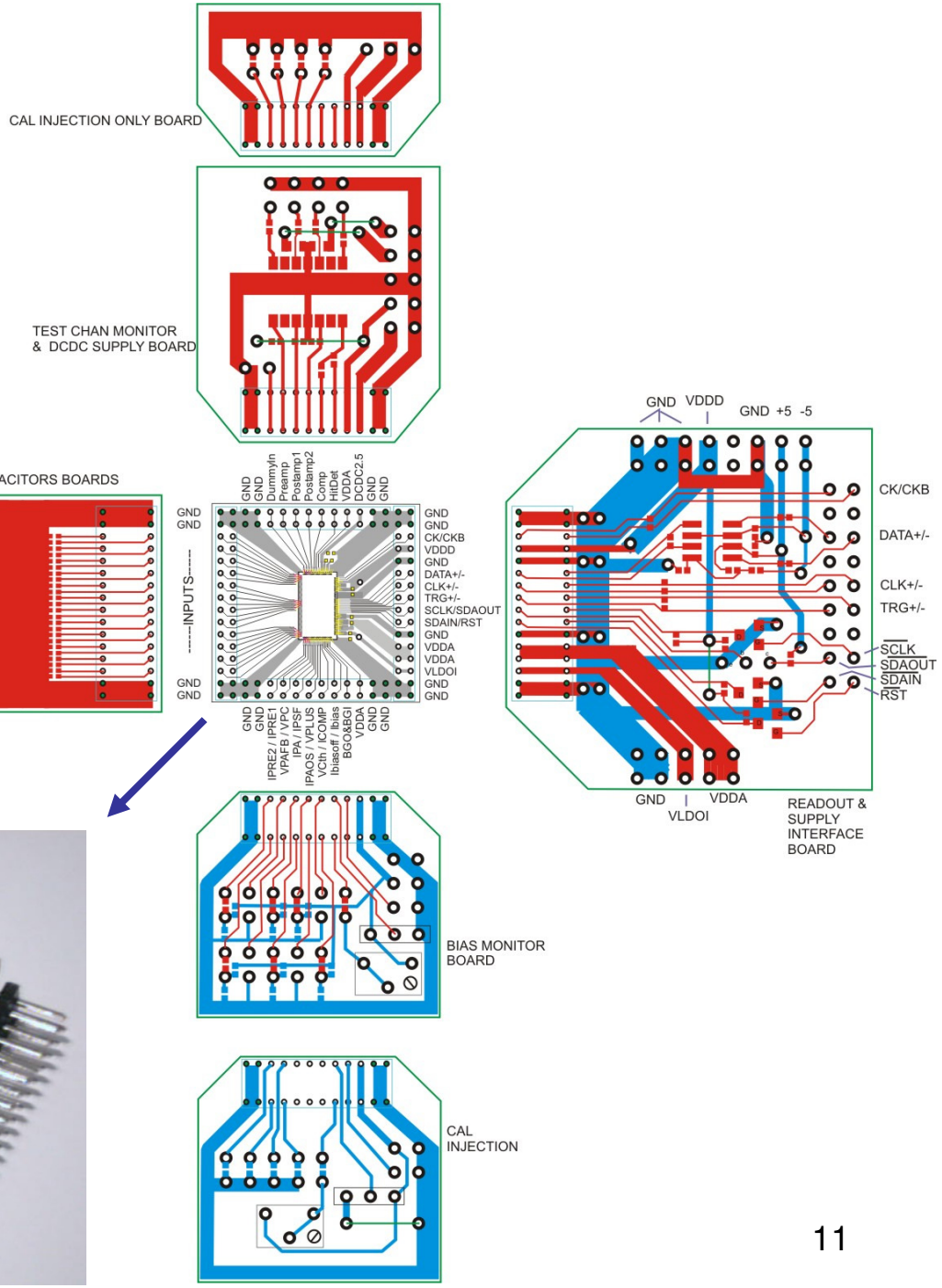
… bit complicated but bottom line is that all powering options can be studied by different chip bonding options and different external connections

test setup in preparation

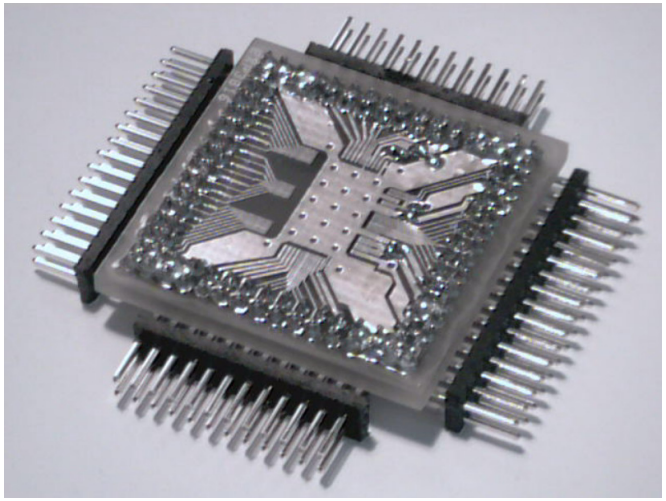
modular system surrounding fineline board

different types of peripheral boards to interface signals and access test features are in preparation

different bonding patterns on fineline board depending on what you want to test



~ 2 x 2 cm²



summary, plans and comments

summary

expect chips to be under test ~ end of year (~180 expected)
test setup hardware at advanced stage

plans

will want to characterise chip performance **without** powering options first
establish baseline performance
(hard to predict how long this will take – depends how well the chip works)
moving on to powering options study
following stage 1, stage 2, stage 3 procedure as described here
… not much point trying to be more specific than that at this stage

will concentrate initially on detailed functionality and performance at IC
Bristol looking at module and system test stand (David Cussans talk at last PWG)
see: *http://indico.cern.ch/getFile.py/access?contribId=3&resId=0&materialId=slides&confId=97972*

comments (on DC-DC powering issues)

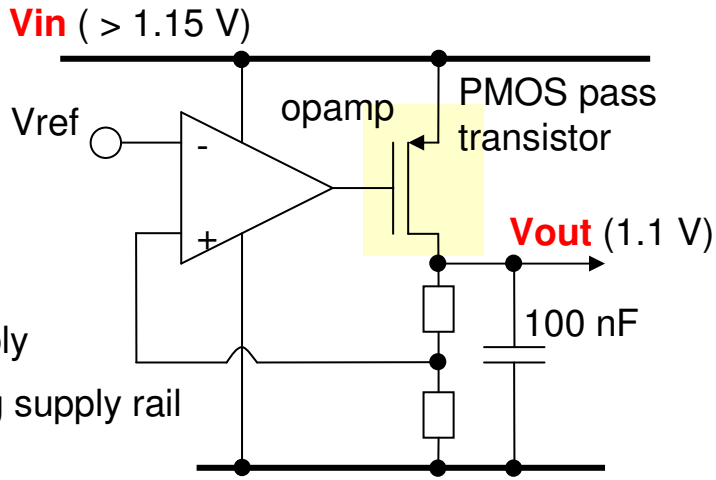
current CBC layout probably optimal for DC-DC inclusion
can keep it well away from sensitive areas
may not be the same for a future version (other FE chip layouts still under consideration)

one possible scenario - it works well on this chip, we adopt it as the baseline option, we make significant changes to a future chip, then find it doesn't work so well on that version…

CBC web page: *http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/*

EXTRA

LDO effect



benefit of filtering effect due to LDO – supply rejection > 30dB

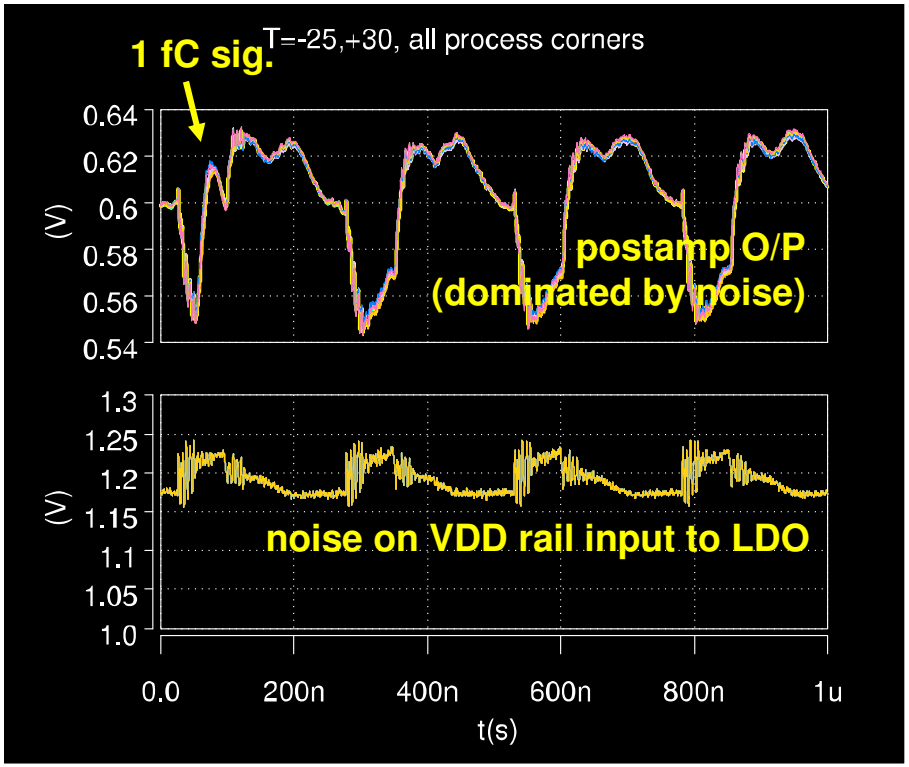
mainly due to output capacitor (passive filtering would also give significant improvement)
get additional advantage of stable, reference related, DC supply

simulated by adding artificial 80 mV pk-pk noise waveform to analog supply rail

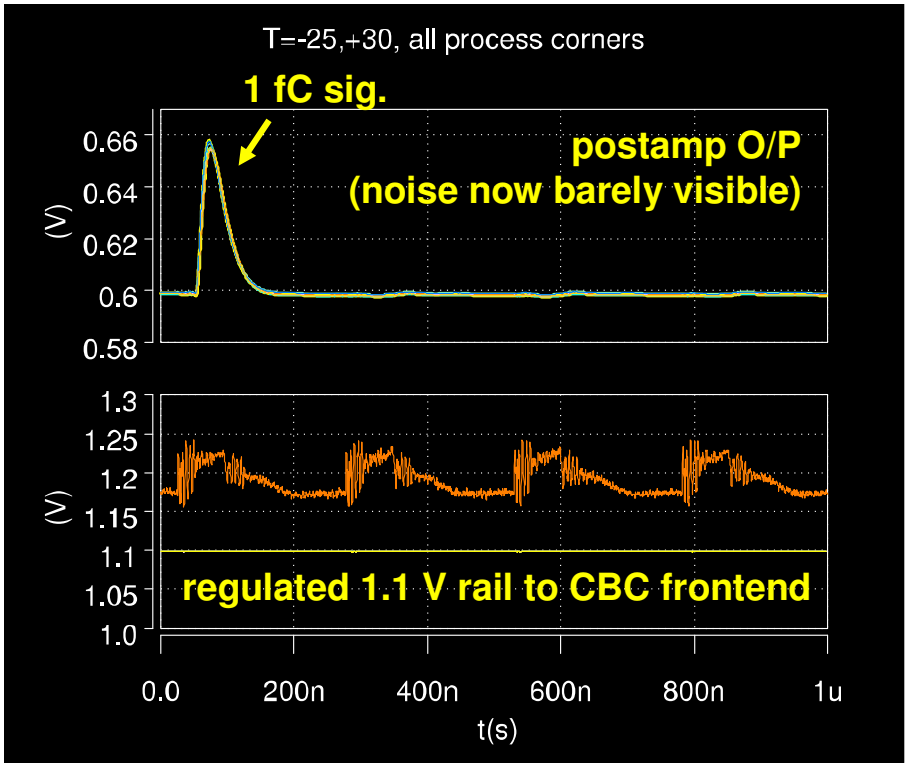
for more details see previous PWG talk

http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/LDO_PWG_Sep09.pdf

without LDO



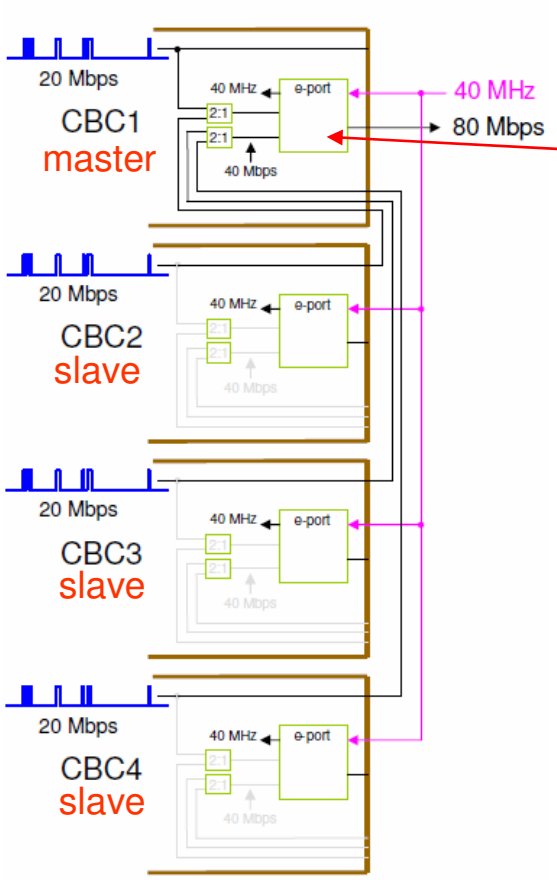
with LDO



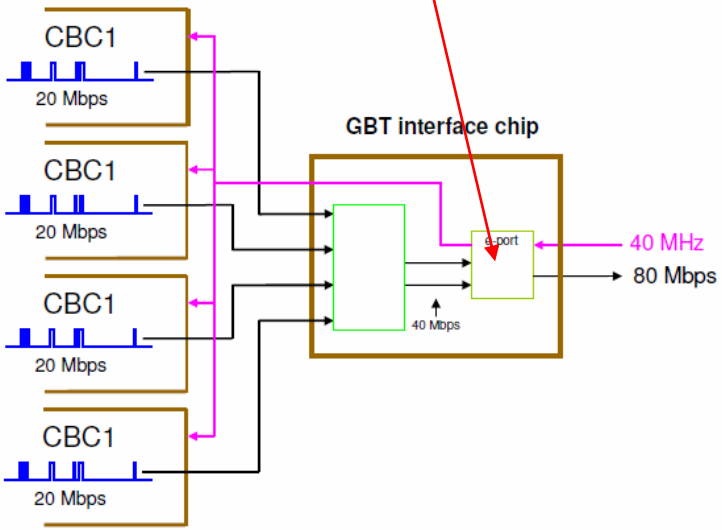
future chip developments (1)

CBC prototype designed to be complete working readout chip
but some system functionalities not yet present

system aspects have been discussed in TUPO meetings
e.g. how to combine data and interface to GBT
discussions will continue, but more than one viable option exists

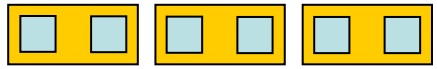


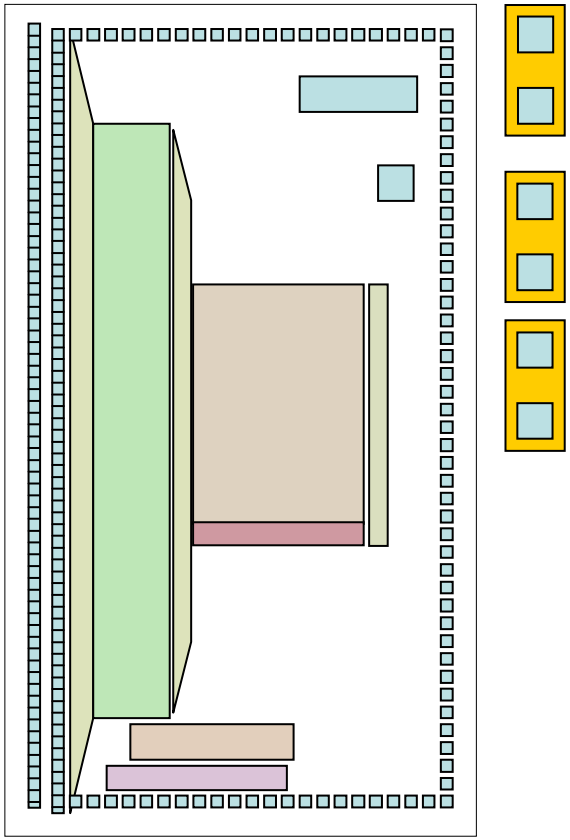
e.g. e-port (GBT interface circuit block)
either inside master CBC
or in separate chip

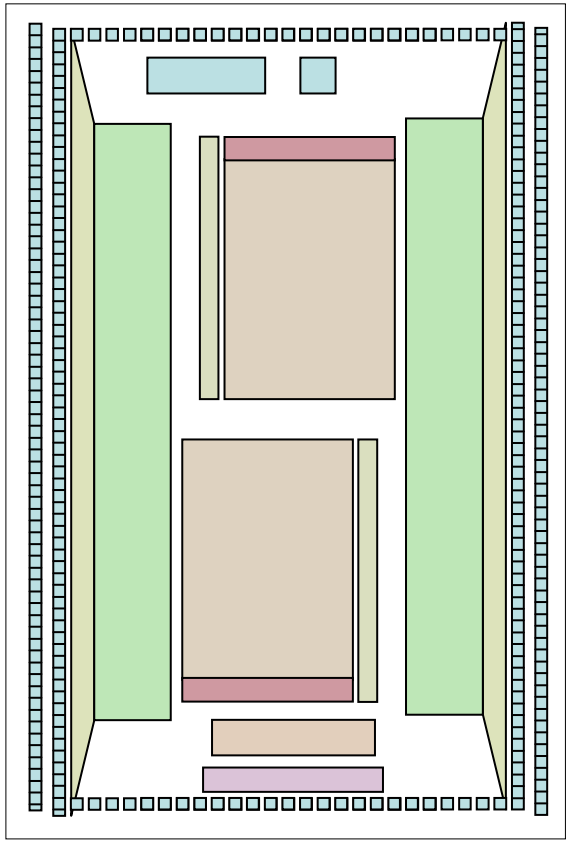


future chip developments (2)

0201 capacitors







128 -> 256 back-to-back

can share some functionality
- e.g. power, control
- but not much else

reduced area, cheaper

less pads available on 256 version

less flexible

overall power consumption
probably not much different

conclusions

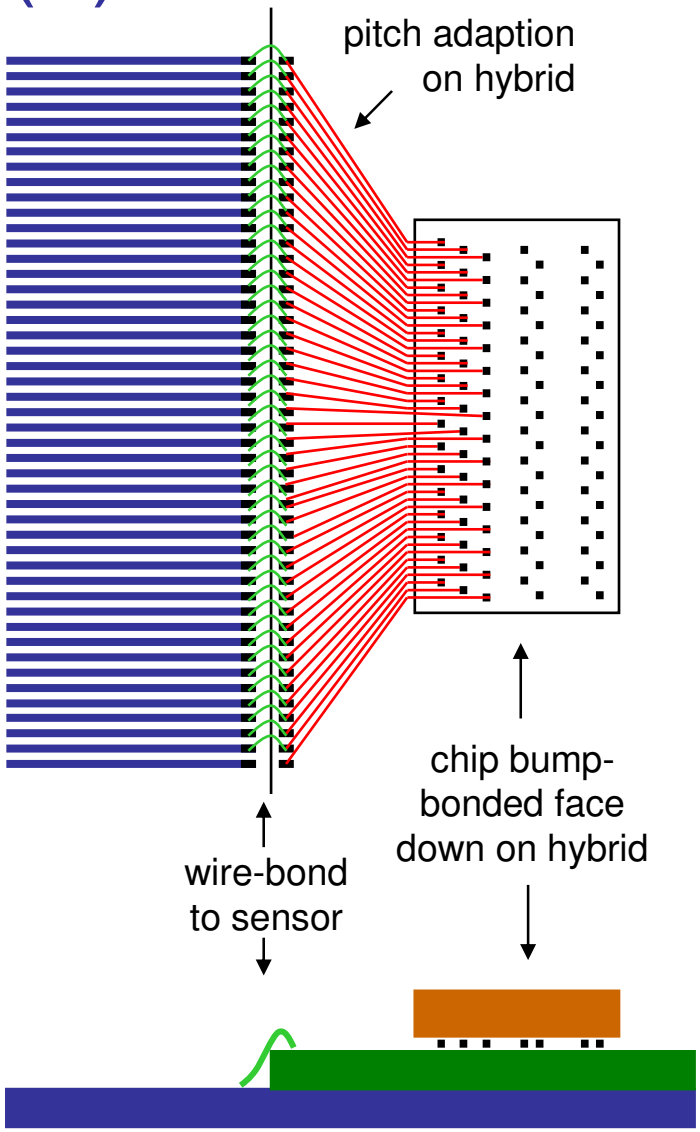
256 back-to-back probably not impossible
- but more detailed study may yet reveal difficulties
- e.g. hard to see where DC-DC conversion can fit without causing problems
  - (interference & room for external capacitors)

future chip developments (3)

bump-bonding?

removes ½ of the wire-bonds
pitch adaption on hybrid

significant changes to layout
hybrid & wire-bond to sensor still required
else where to put passives, route power, …



CBC power

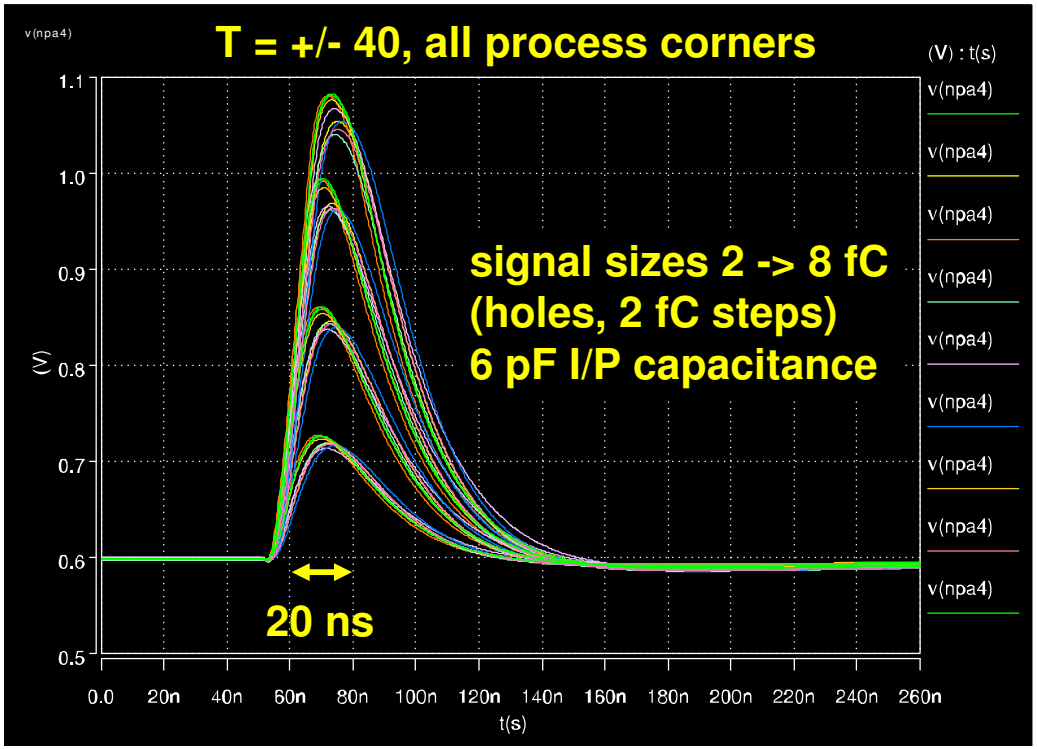
	power/FE chan.	
preamp/postamp		
20 nsec peaking time, short strips C_{SENSOR} ~ 5pF (~ 100 + (20 x C_{SENSOR}))	200 μW	~ 200 μW analogue
comparator	14 μW	
digital		
take 0.25μm APV25 (digital 400 μW) /10 for technology, x3 for SEU (pessimistic? CBC logic should be simpler)	120 μW	~ 300 μW digital
output		
LV differential ~ few mW / 128 chans.	30 μW	
contingency		
just guess nominal figure to bring overall power to 0.5 mW	150 μW	

0.5 mW / channel seems like an achievable target (c.f. 2.7 mW for APV25)

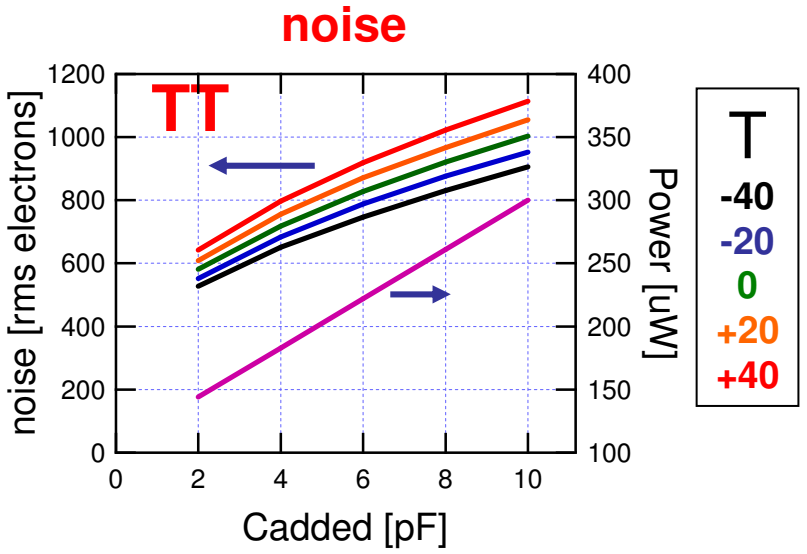
digital is biggest uncertainty, and maybe largest contributor
hope to improve estimate as design progresses
- can consider running at lower voltage (dig. power ~ V^2) => extra contingency
  - e.g. 1.2 -> 0.85 power consumption halved
- will keep power rails separate on chip to keep option open

using numbers above: 128 chan. chip needs ~ 20 mA analogue, ~30 mA digital

postamp output pulse shape & noise



~ 20 nsec peaking, ~ 50 mV / fC
robust to temperature (-40 -> +40) and process variations
electron signal gives opposite polarity



preamp input device power varied with Cadded (added input capacitance) to maintain constant pulse shape

(otherwise preamp risetime increases with Cadded and overall pulse shape affected)

for 1 uA leakage current add 440e in quadrature