CBC testing status

CMS Binary Chip

130nm CMOS chip for short strip readout at sLHC

chips under test since 14th February

early test results presented ACES workshop - March 10th

summary of testing status presented CMS Upgrade workshop ~ 2 weeks ago

will repeat those results again here

but add some more “work-in-progress” type measurements

Tracker week electronics meeting, May 2011.
Mark Raymond, Imperial College.

CBC introduction

key features

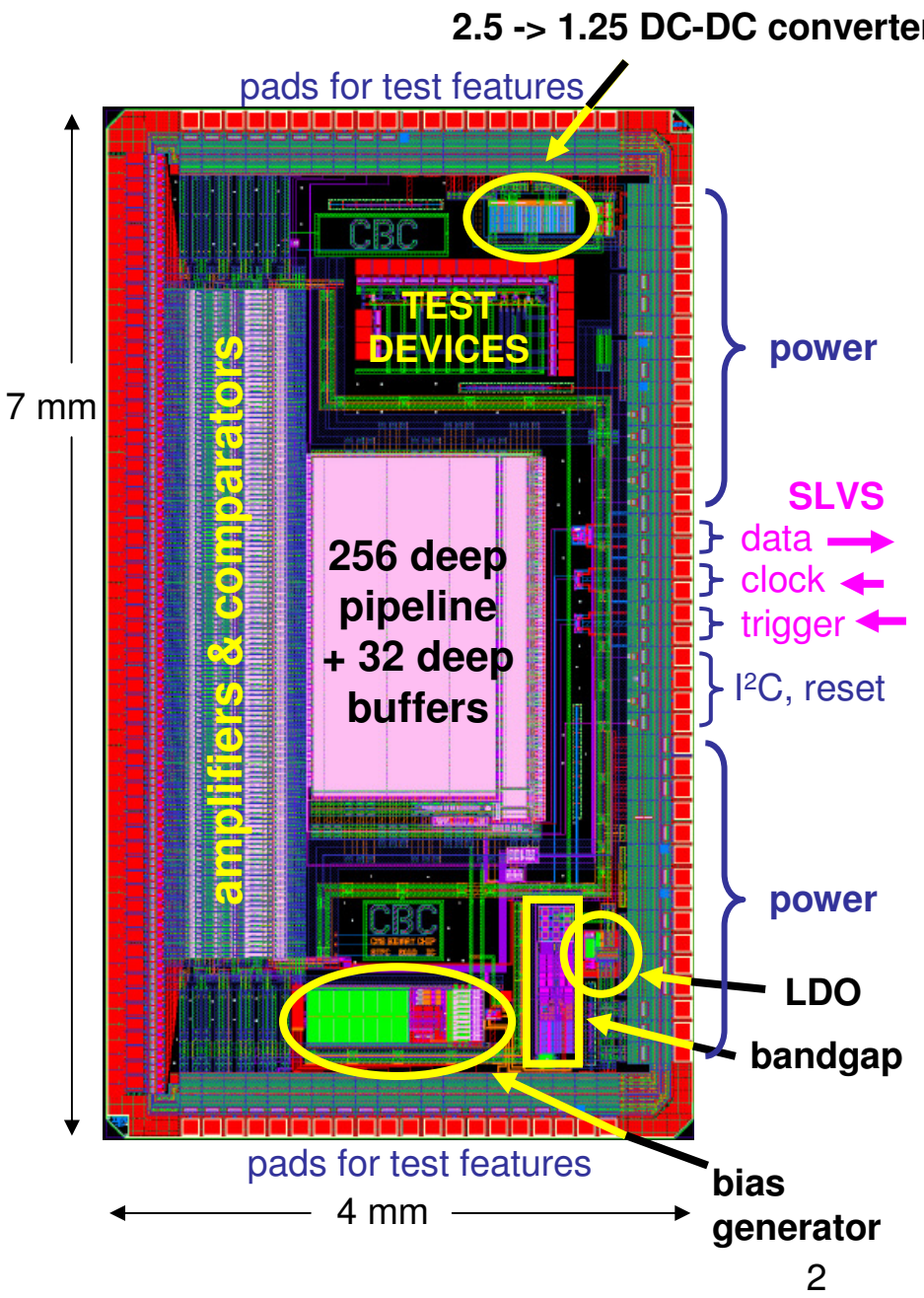
- designed for short strips, ~2.5–5cm, < ~ 10 pF
- full size prototype - 128 channels (50 μm pitch)
- not contributing to L1 trigger
  (could be adapted to 2-in-1 type triggering)
- binary un-sparsified readout
  chip & system simplicity, low power
- powering test features
  2.5 -> 1.2 DC-DC converter
  LDO regulator (1.2 -> 1.1) feeds analog FE

main functional blocks

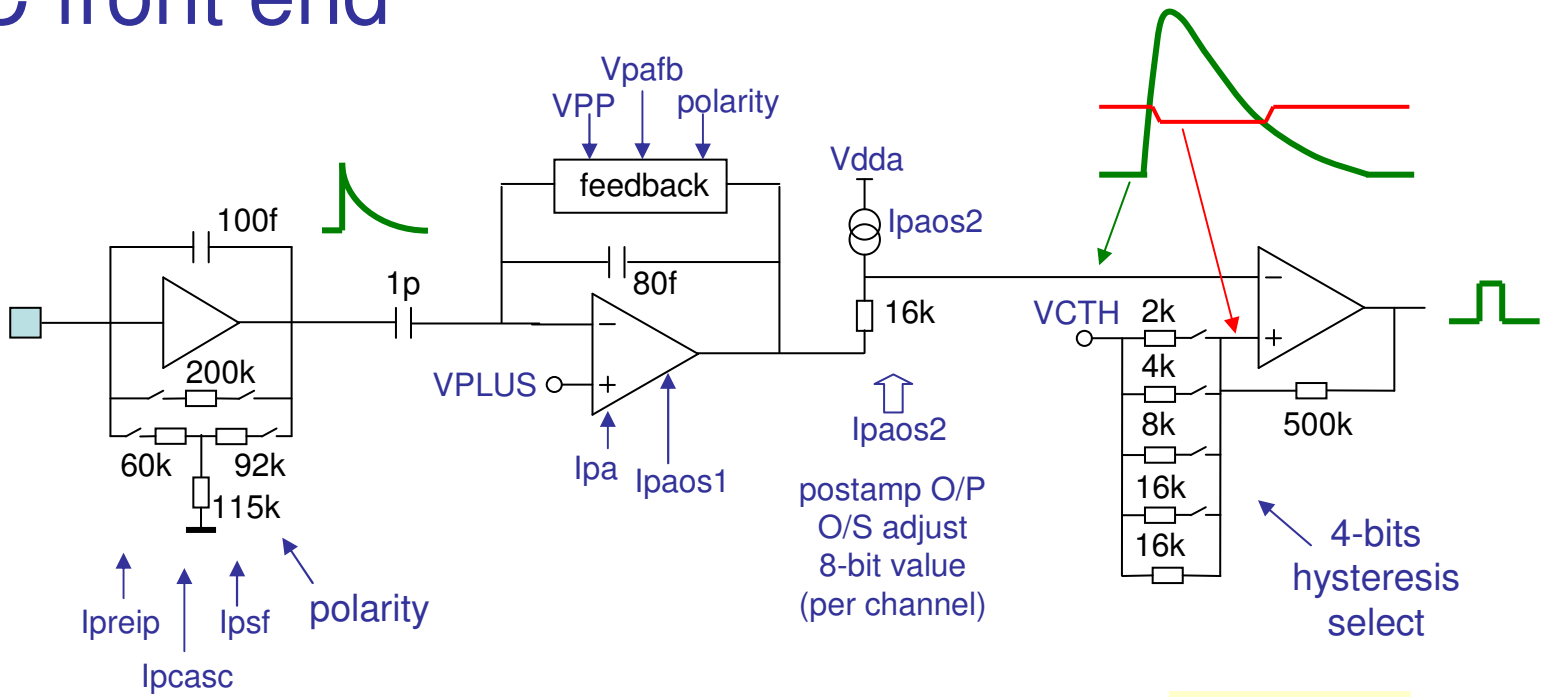
- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- output shift register and SLVS driver
- fast (SLVS) and slow (I2C) control interfaces

some target specs

- DC coupling to sensor – up to 1 uA leakage
- can be used for both sensor polarities
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
  < 0.5 mW/channel for C_{SENSOR} ~ 5 pF



CBC front end

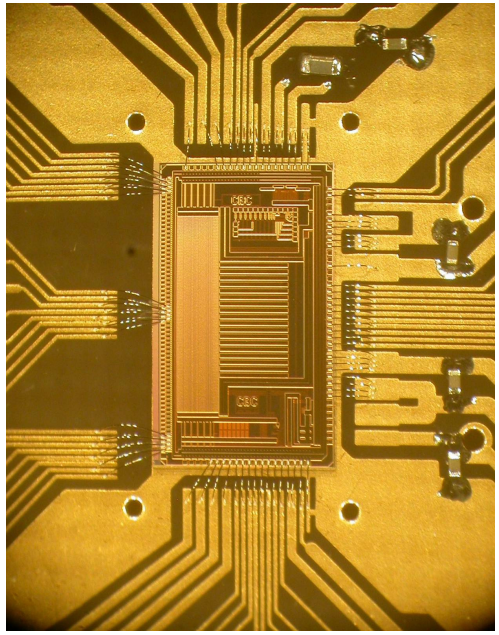


preamp
resistive feedback absorbs I_{leak}
T network for holes
Rf.Cf implements short diff. time constant
(good for no pile-up)

postamp
provides gain and int. time constant
~ 50 mV / fC
AC coupled removes I_{leak} DC shift
individually programmable O/P DC level
implements channel threshold tuning
8-bits, 0.8 mV / bit, 200 mV range

comparator
global threshold
(indiv. tuning at postamp O/P)
programmable hysteresis

test setup



dummy channel
interface board
fast & slow control
& data out interface
test
charge
injection
CBC test board
~ 22 x 22 mm²
bias generator
test board

basic functionality

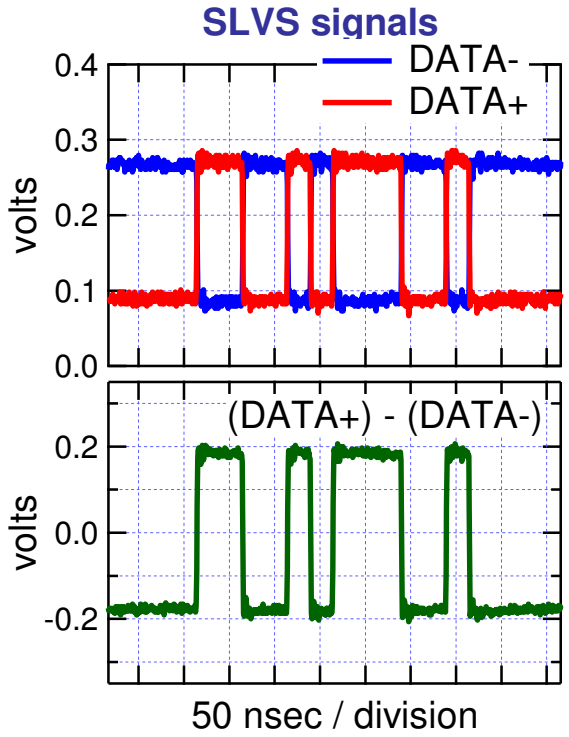
communication interfaces

fast: SLVS (Scalable Low Voltage Signalling)
SLVS circuits provided by CERN (S. Bonacini, K.Kloukinas)
used for 40 MHz clock I/P, L1 trig and data out

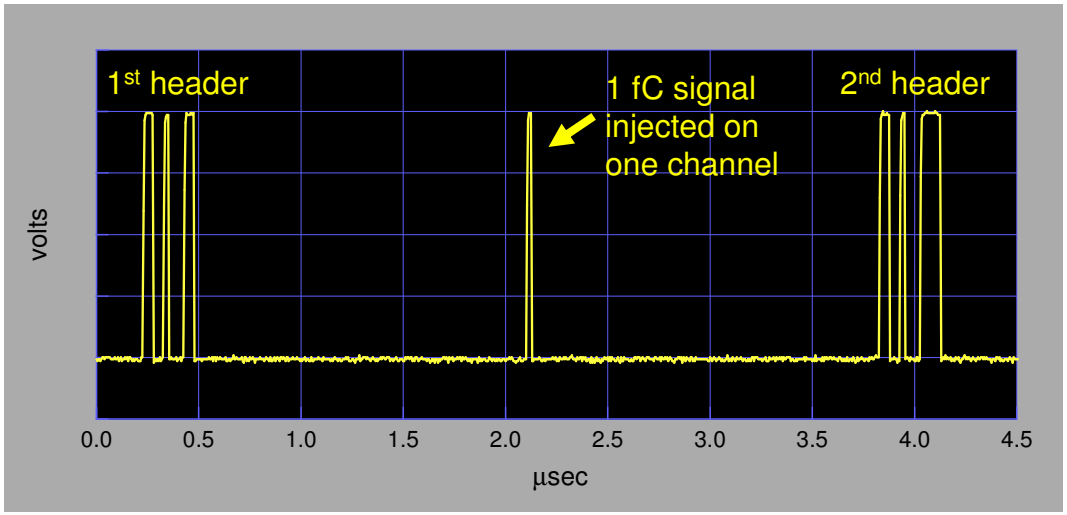
slow: I2C - used to programme
bias generator
operational modes, latency,..
128 comparator threshold trim values

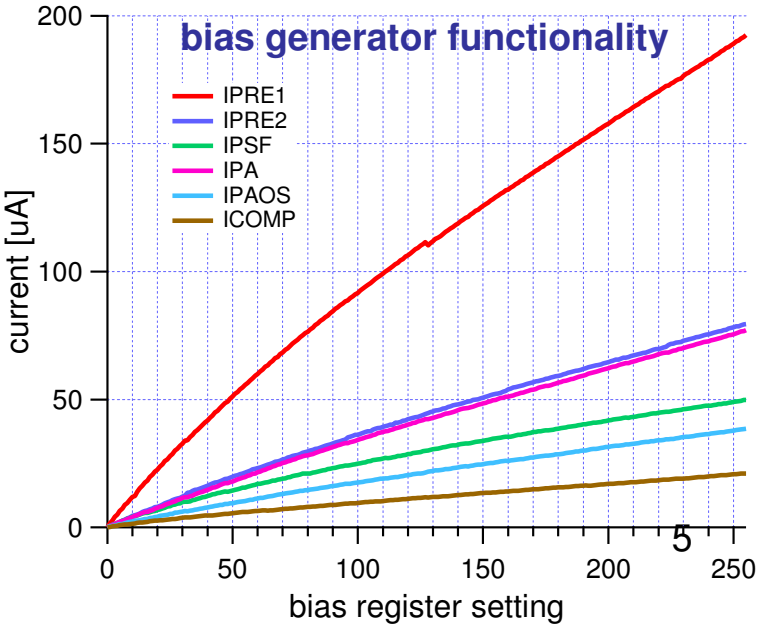
output data frame

following trigger get 12-bit header
2 start bits, 2 error bits (latency, fifo overflow), 8 bit pipe address
followed by 128 channel bits



e.g. 2 consecutive data frames (2 triggers)

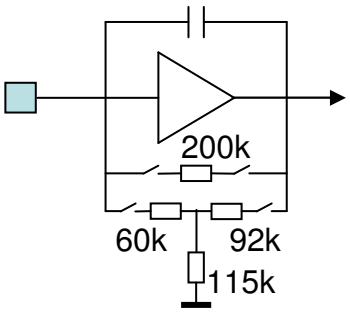




leakage current tolerance

Ileak absorbed by preamp
resistive feeback

=> DC shift at preamp O/P



electrons mode

single 200k resistor, leakage shifts output +ve

plenty of headroom

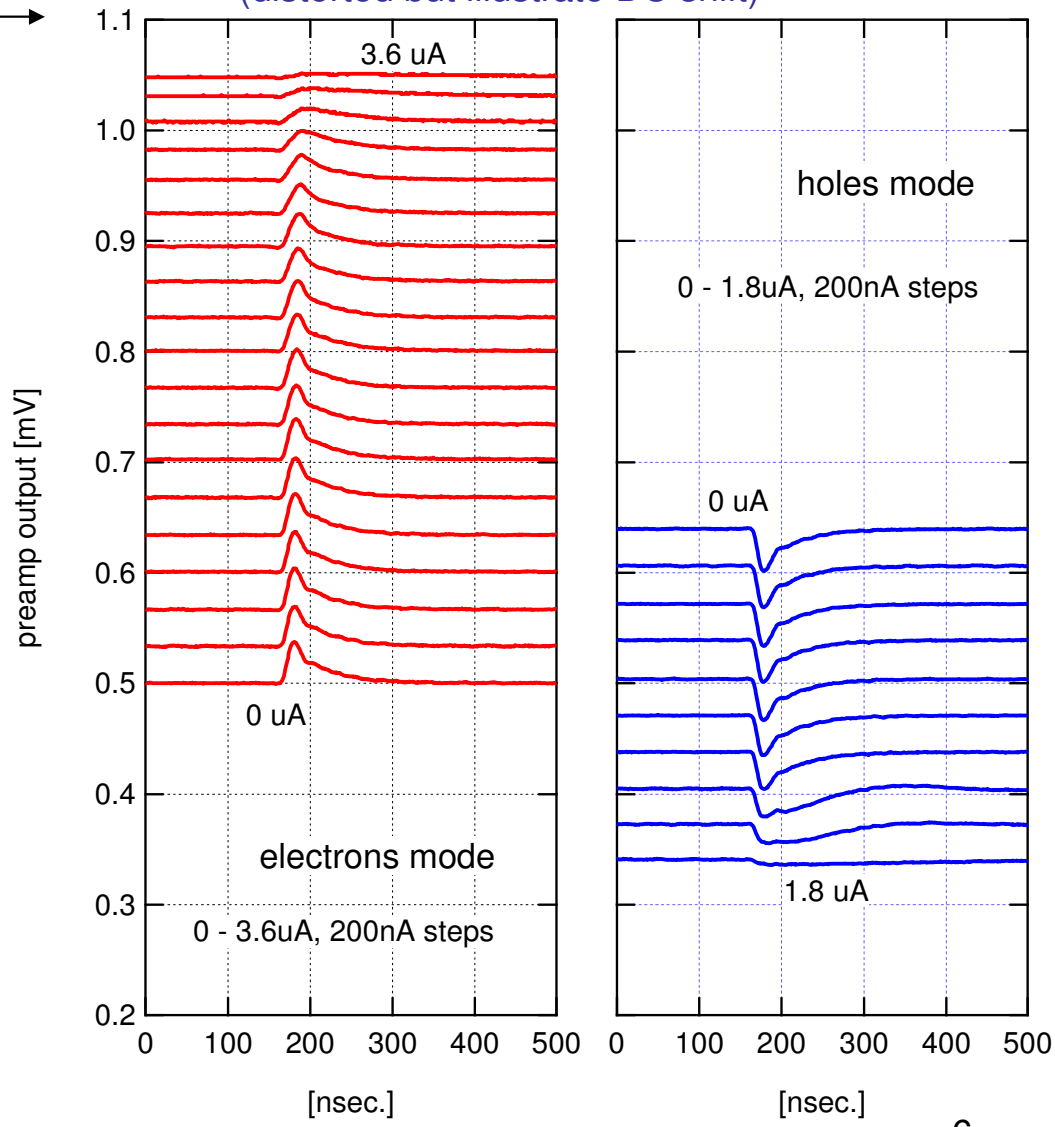
holes mode

T network produces +ve offset
leakage shifts output -ve

sufficient headroom for 1 uA

(note: waveforms include ~ 300 mV offset
due to source follower on test channel O/P)

waveforms measured on test channel
(distorted but illustrate DC shift)

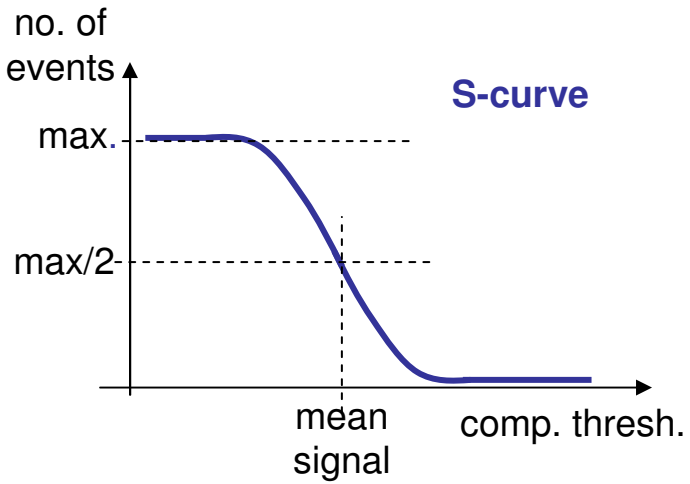


testing front end performance using comparator

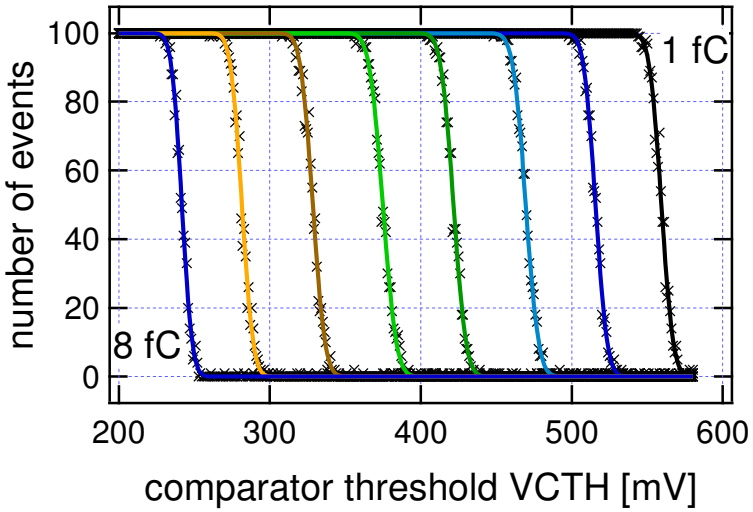
can learn a lot about front end performance by varying:
- comparator threshold
- magnitude of injected charge

can look at S-curves
- no. of events vs. threshold value
- fit with complementary error function (erfc)
  - gives mean signal (S-curve midpoint) and sigma

=> gain and noise



S-curves and gain

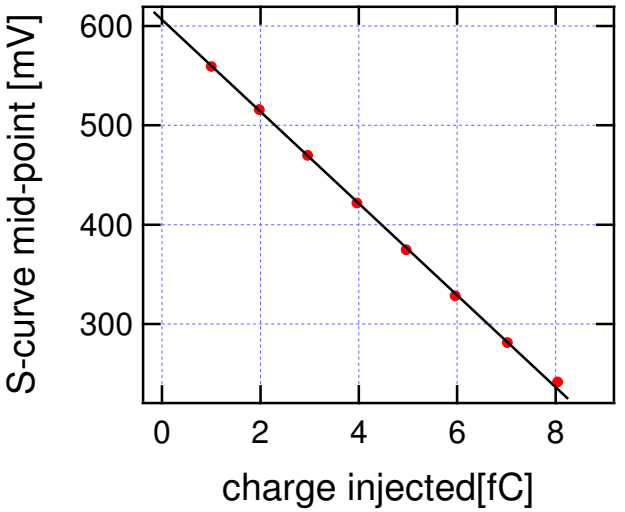


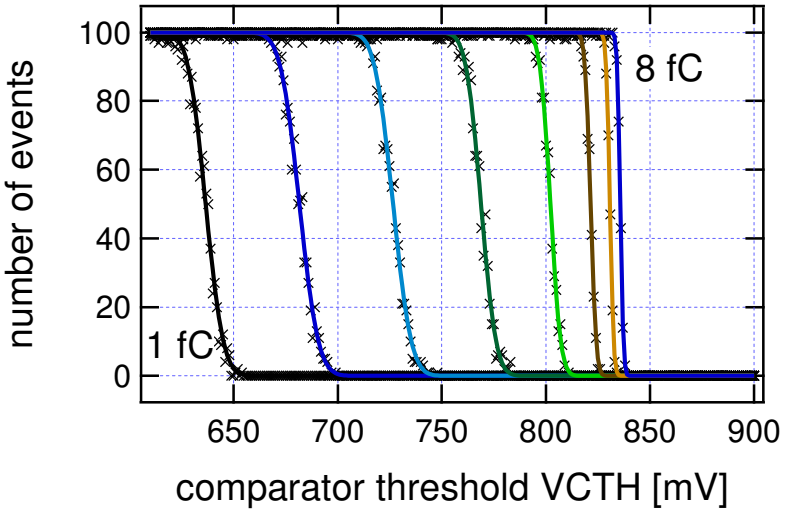
electrons mode

gain ~ 50 mV / fC

signals in range 1 - 8 fC

in 1 fC steps

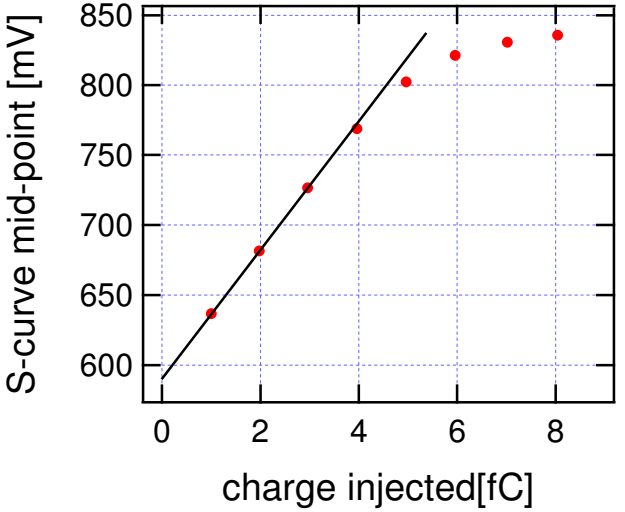




holes mode

gain ~ similar

dynamic range more limited - but still linear in region where normal comp. threshold will be set



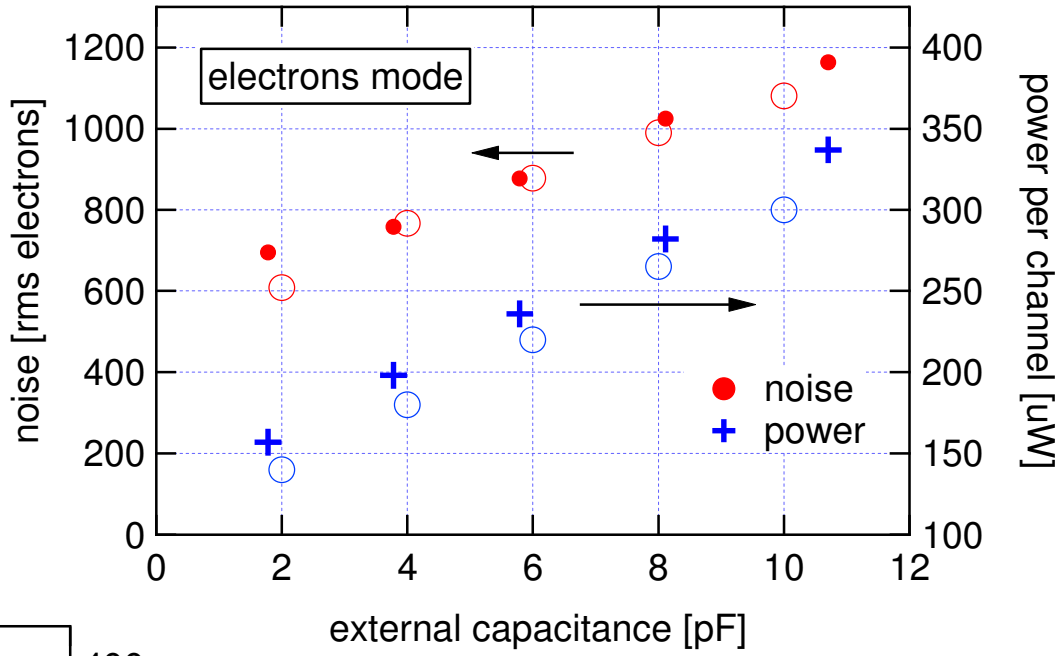
noise

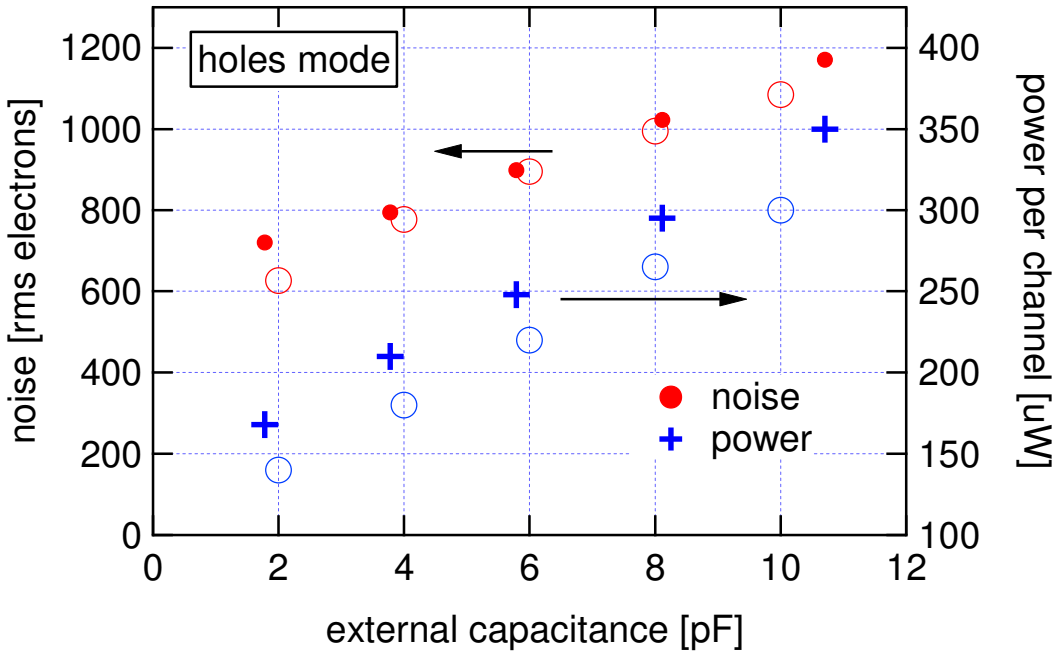
plots show dependence on external added capacitance in both operational polarities

current in input transistor adjusted to maintain pulse shape - so overall analogue power varies

results very close to simulation (open circles)

target spec. < 1000e for 5 pF sensor





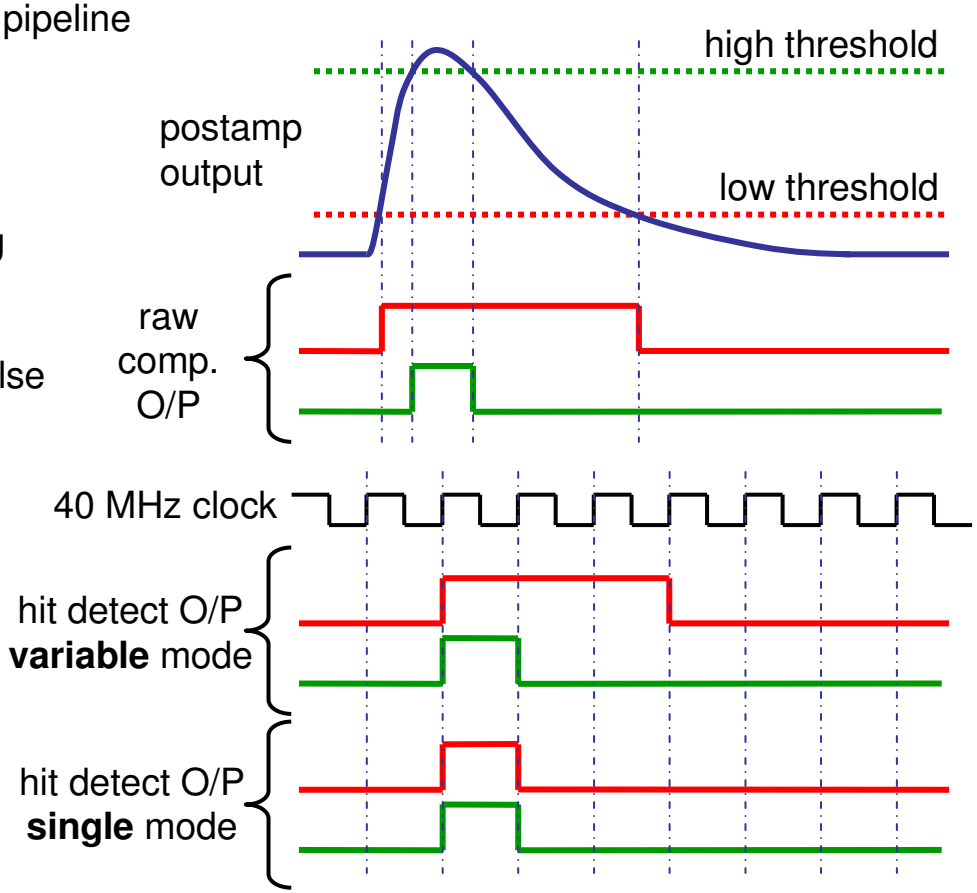
“hit detect” circuit

hit detect circuit sits between comparator output and pipeline

operates in 2 modes:

variable - raw comp. O/P sampled into pipeline
consecutive pipeline samples high as long as comp. O/P stays high

single - comp. O/P shortened to single 25ns pulse
only one sample in pipeline however long comp. O/P stays high



hit detect functionality

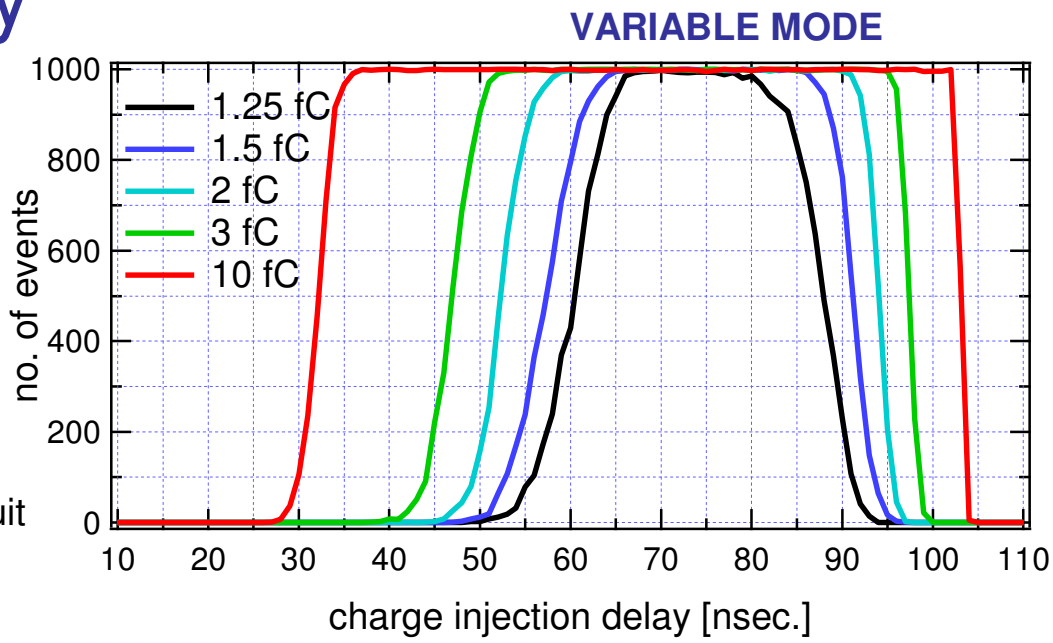
sweep signal charge injection time for
both modes of operation – fixed trigger time

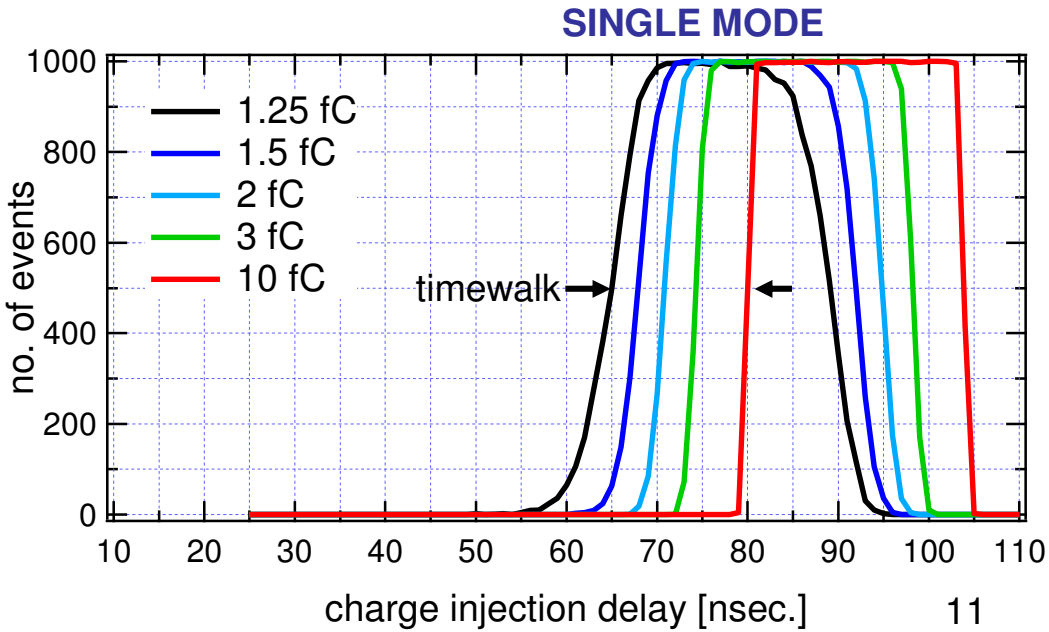
comparator threshold fixed at 1 fC

VARIABLE mode picture shows pulse width increasing as signal amplitude increases

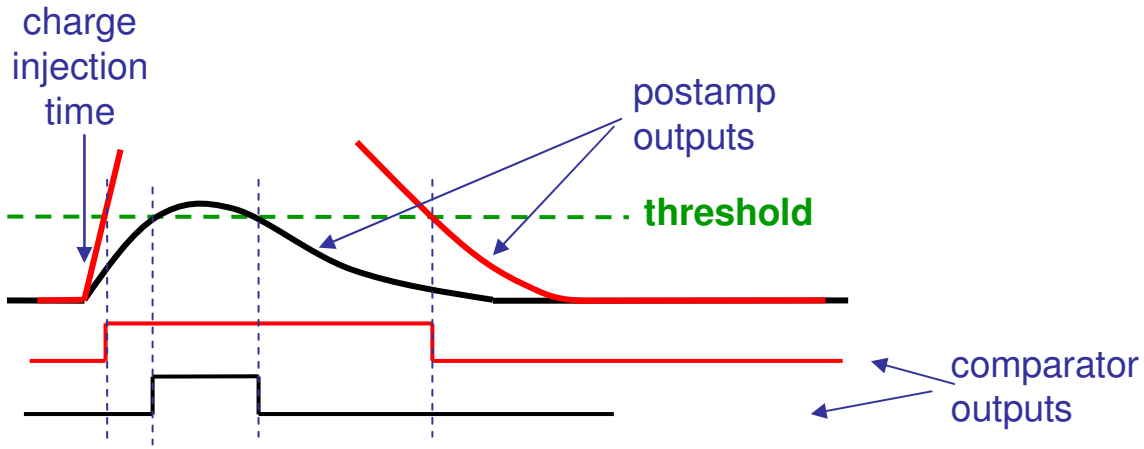
SINGLE mode picture shows *hit* detect circuit keeps pulse width at 25 ns

timewalk ~ 15 ns
(just within spec.)





explanation of charge injection pictures (1)



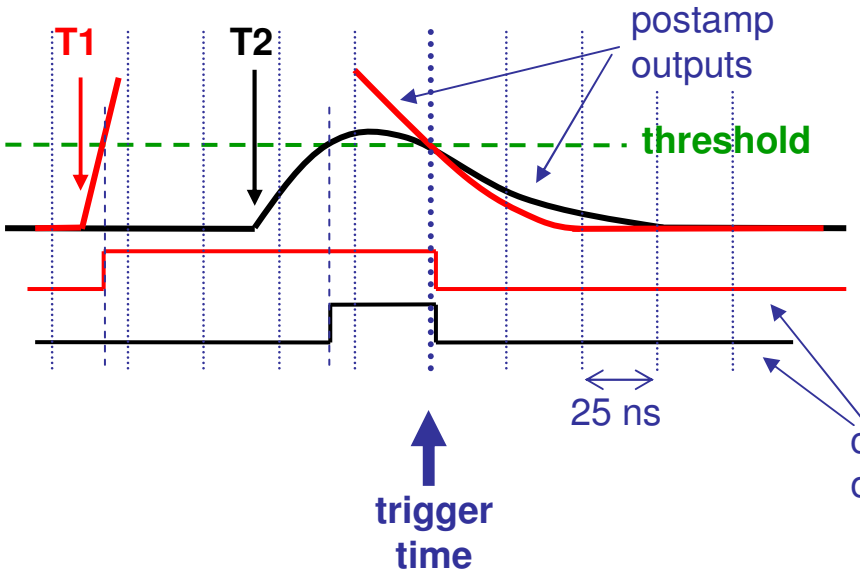
2 signals : big signal in red, small signal in black

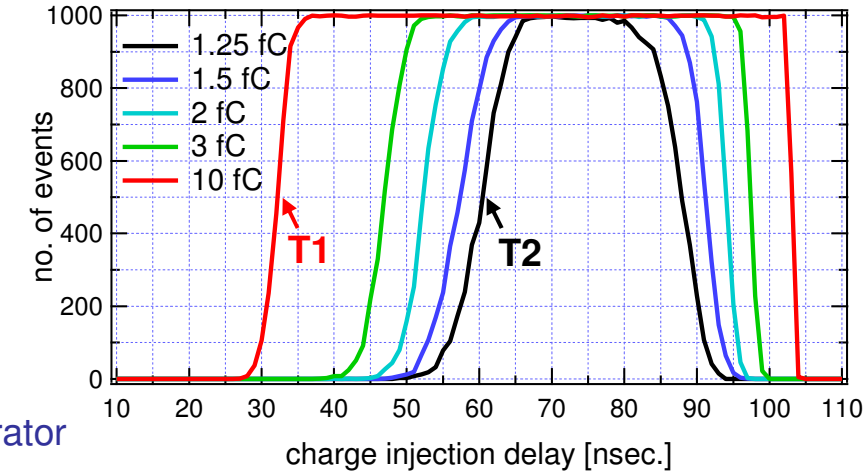
raw comparator output stays high as long as postamp O/P exceeds threshold

picture above shows both signals injected at same time

will now “walk through” scenario where charge injection time varied w.r.t. pipeline sampling clock

explanation of charge injection pictures (2)





inject 2 signals : big signal in red, small signal in black

always triggering same pipeline column (hit detect circuit in **variable** mode)

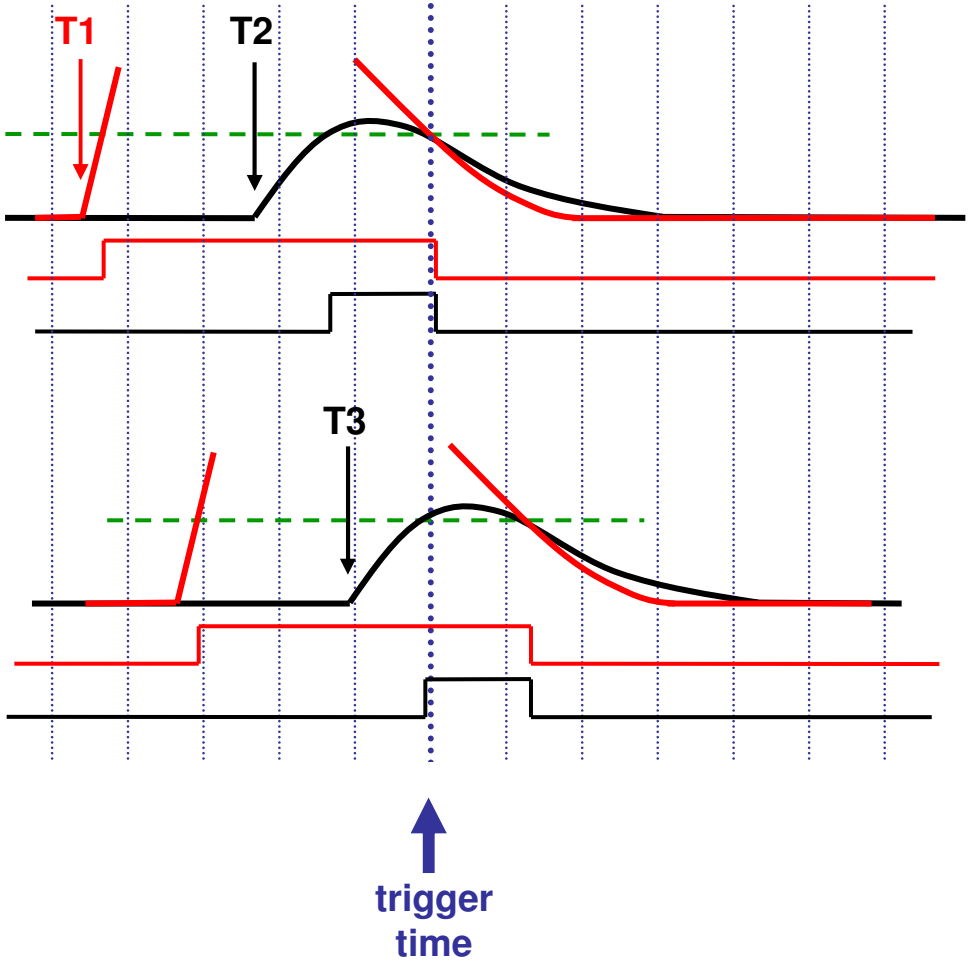
"**trigger time**" = clock edge which writes comp O/P into the triggered pipeline column

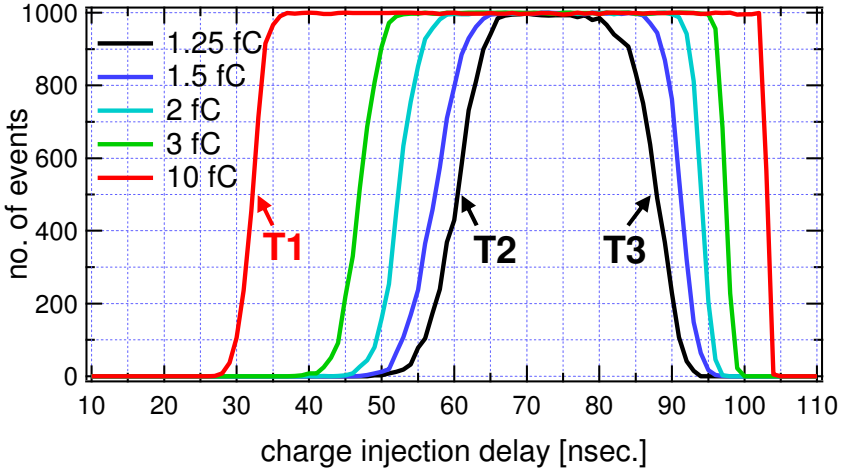
T1 : earliest time of **big signal** charge injection for comparator output to be registered at trigger time

T2 : earliest time of **small signal** charge injection for comparator output to be registered at trigger time

in terms of charge injection delay, **T1 < T2**

explanation of charge injection pictures (3)



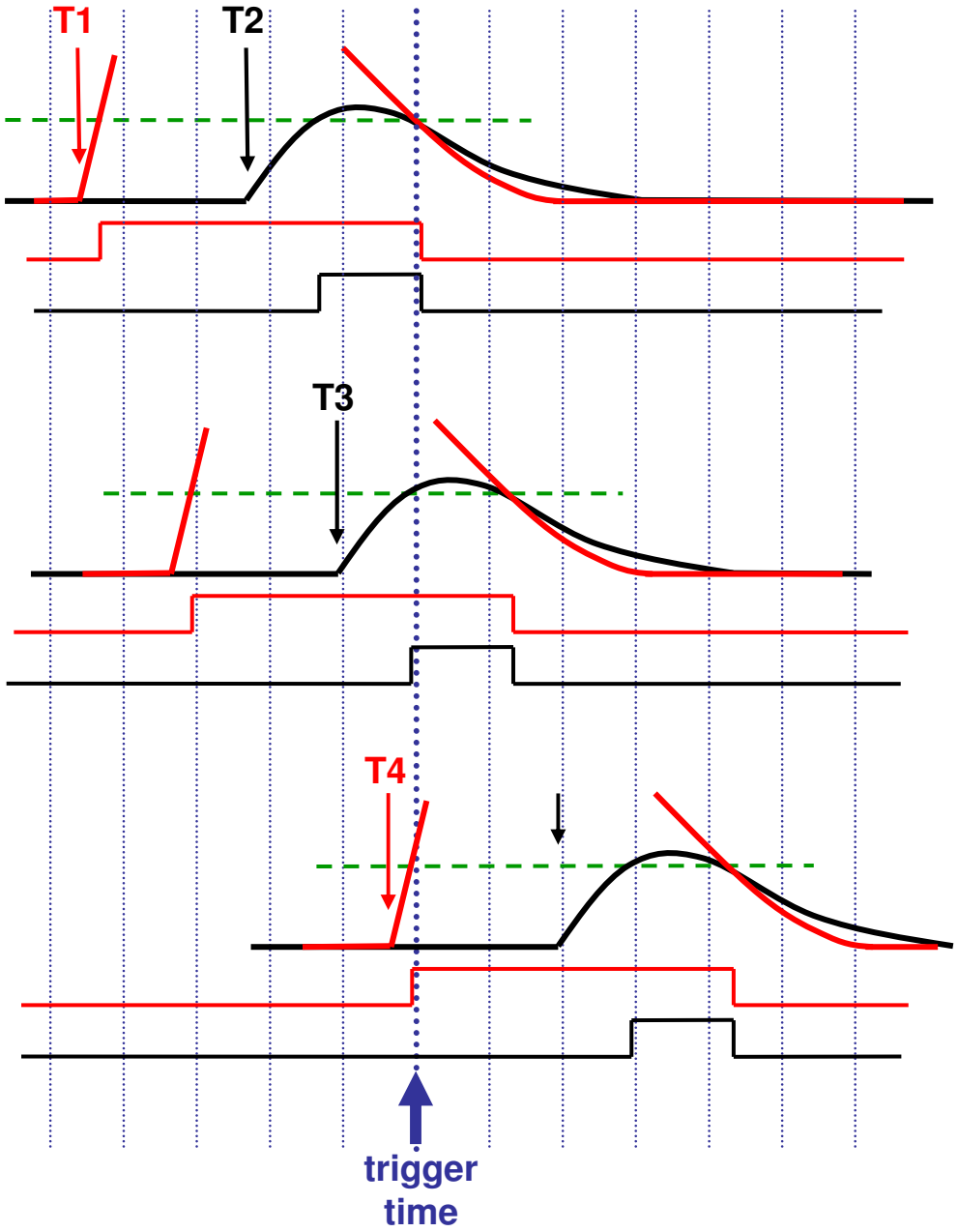


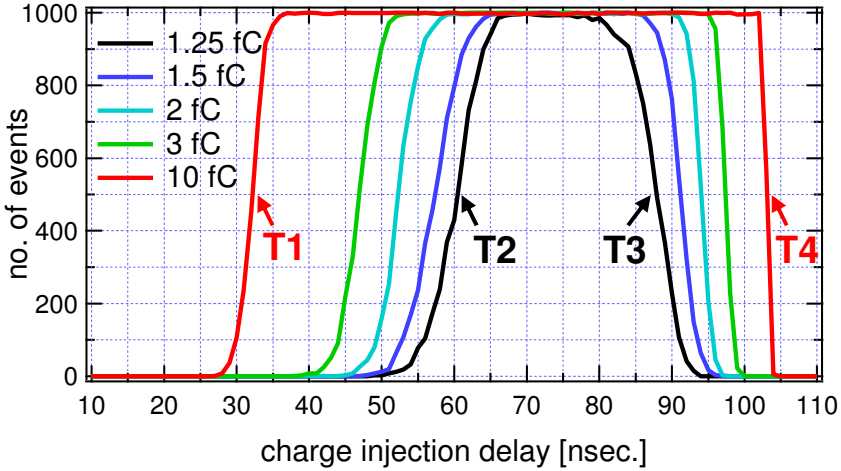
some time later…

T3 : **latest** time of **small signal** charge injection
for comparator output to be registered at trigger time

T1 < T2 < T3

explanation of charge injection pictures (4)



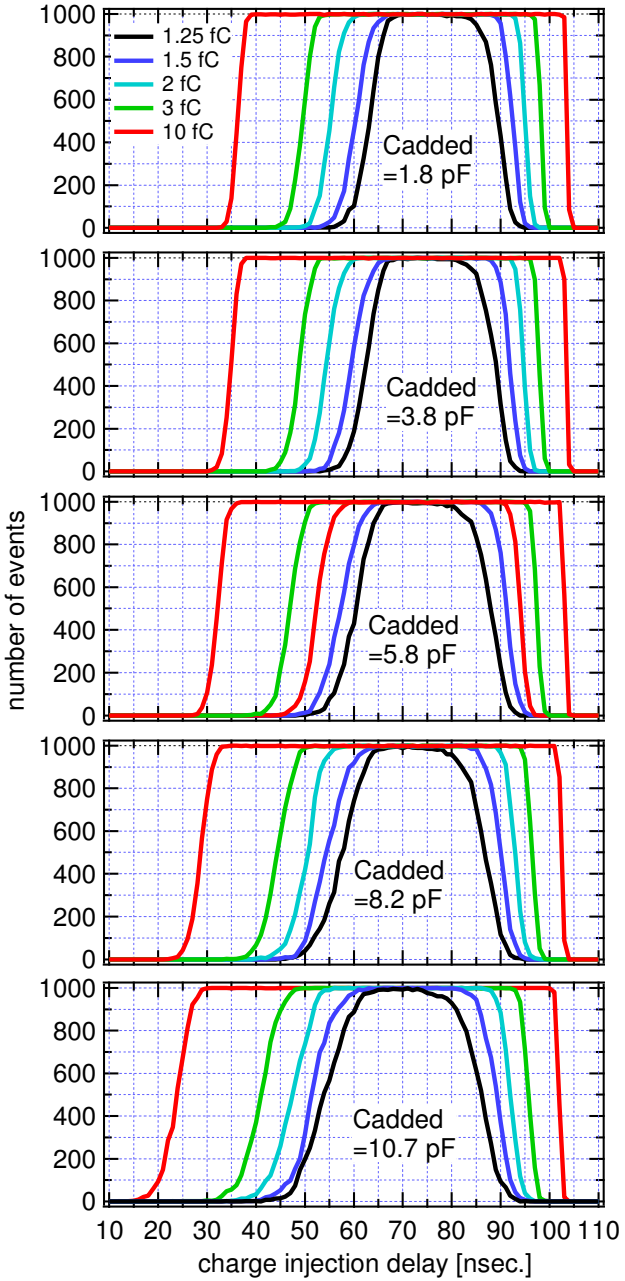


… later still

T4 : **latest** time of **big signal** charge injection
for comparator output to be registered at trigger time

T1 < T2 < T3 < T4

time-walk pictures vs. external capacitance

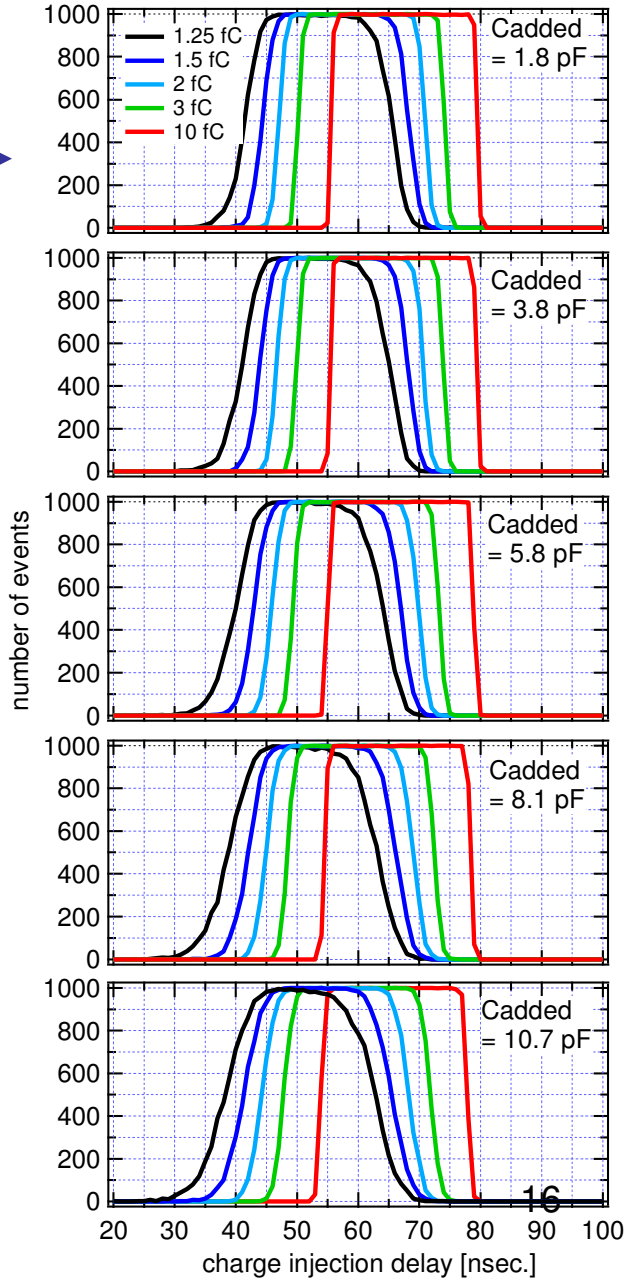


VARIABLE MODE

SINGLE MODE

increasing noise "rounds off" the edges

start to lose efficiency for 1.25 fC signals at larger capacitances



comparator threshold uniformity

all channels have same
comparator global threshold (VCTH)

individual channel tuning achieved by
introducing programmable offset on the
comparator input signal (postamp O/P)

128 registers, 8-bit precision

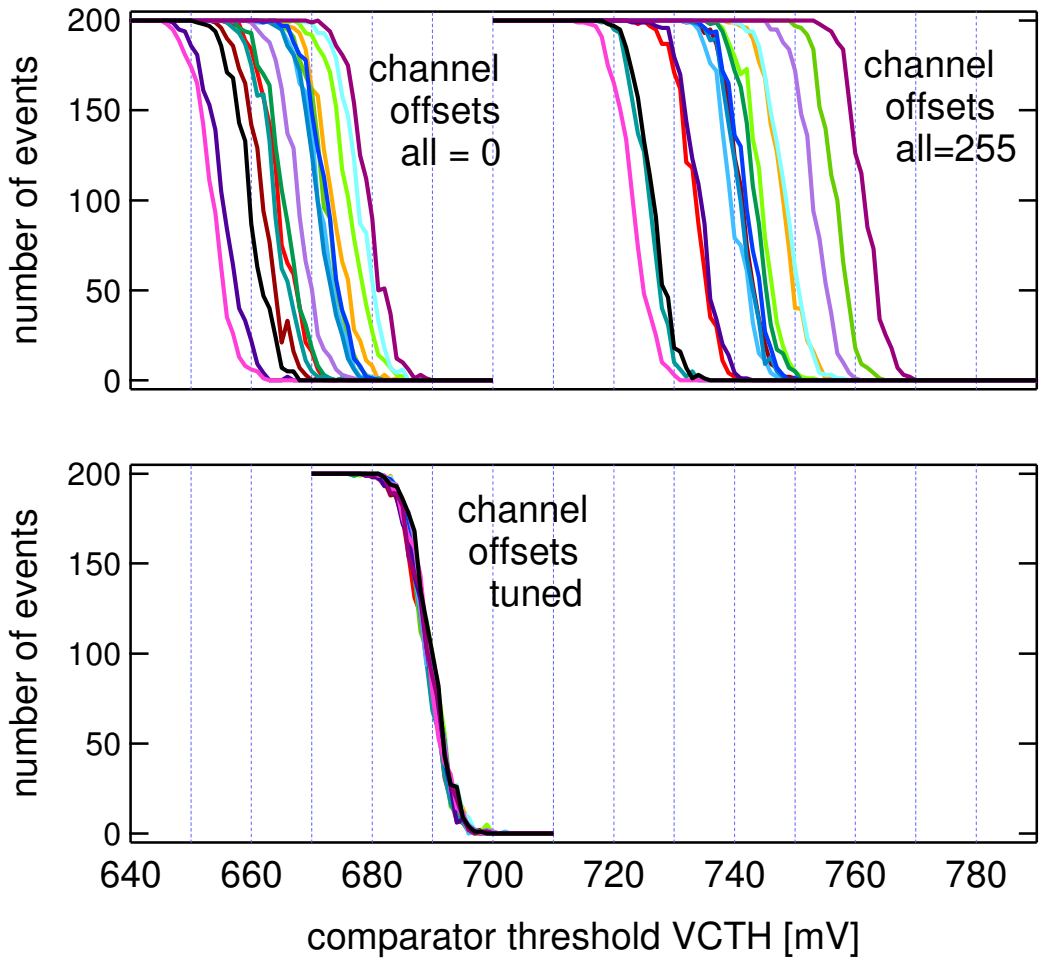
peak-to-peak threshold spread ~ 30 mV

< 1 fC before tuning

pictures demonstrate effectiveness of
tuning to achieve comp. threshold matching

~ mV precision achievable

threshold tuning - 16 channels



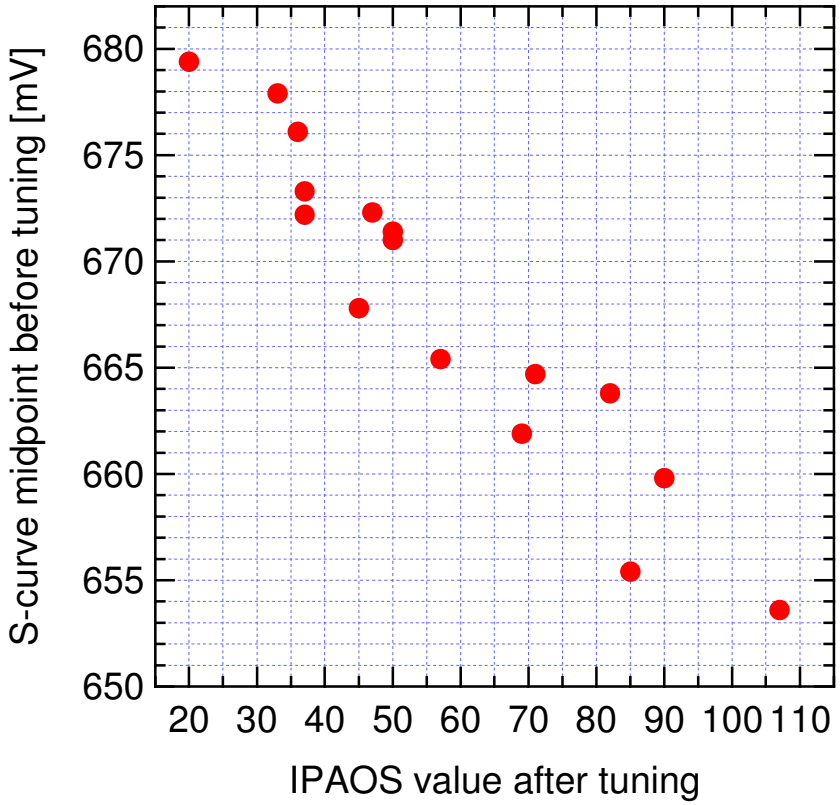
comparator threshold uniformity (2)

correlation between S-curve midpoints before tuning and offset register values after

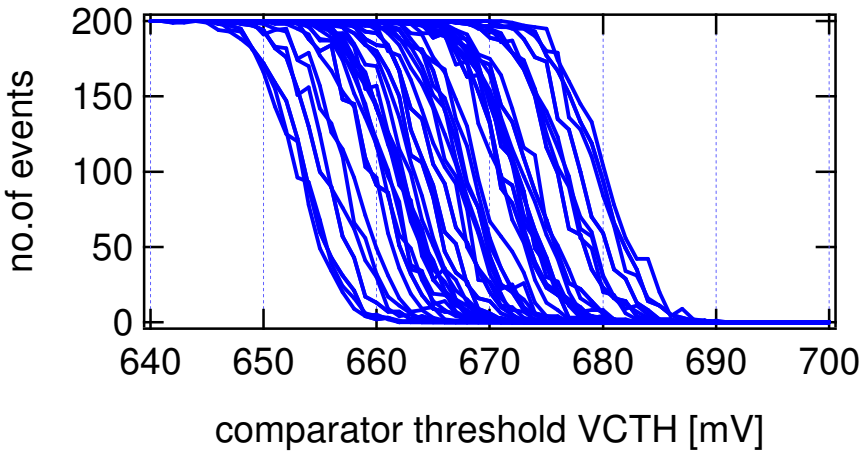
can maybe use to get first approximation to overall uniformity

but individual scans required to achieve final close matching

=> a lot of I2C activity



S-curves, 64 channels, all offsets = 0



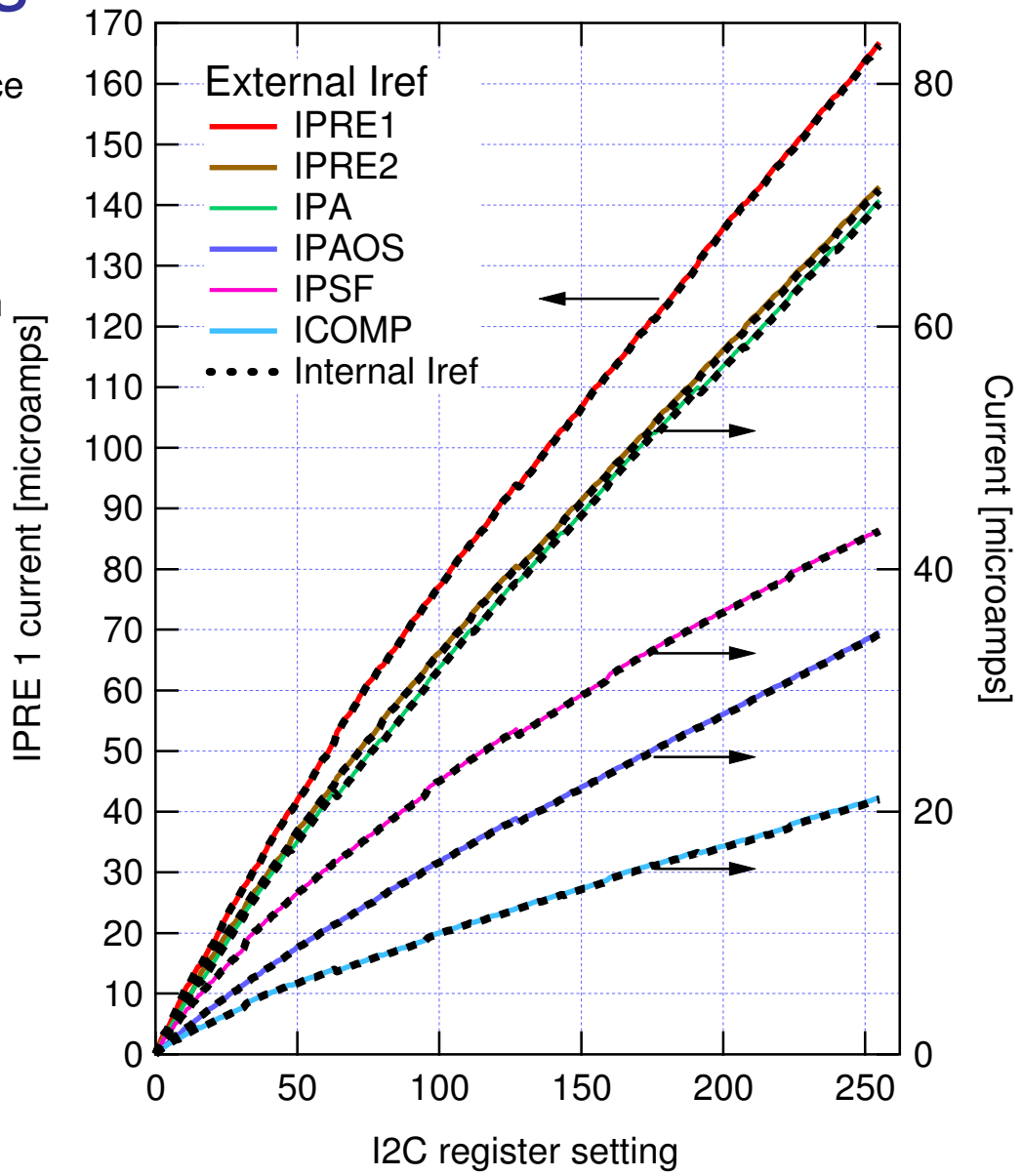
CBC biasing - currents

can choose to bias CBC using internal reference
    64 uA derived from bandgap

or provide external current (via resistor)

plot shows current biases measured using both methods
    external tuned to 64 uA

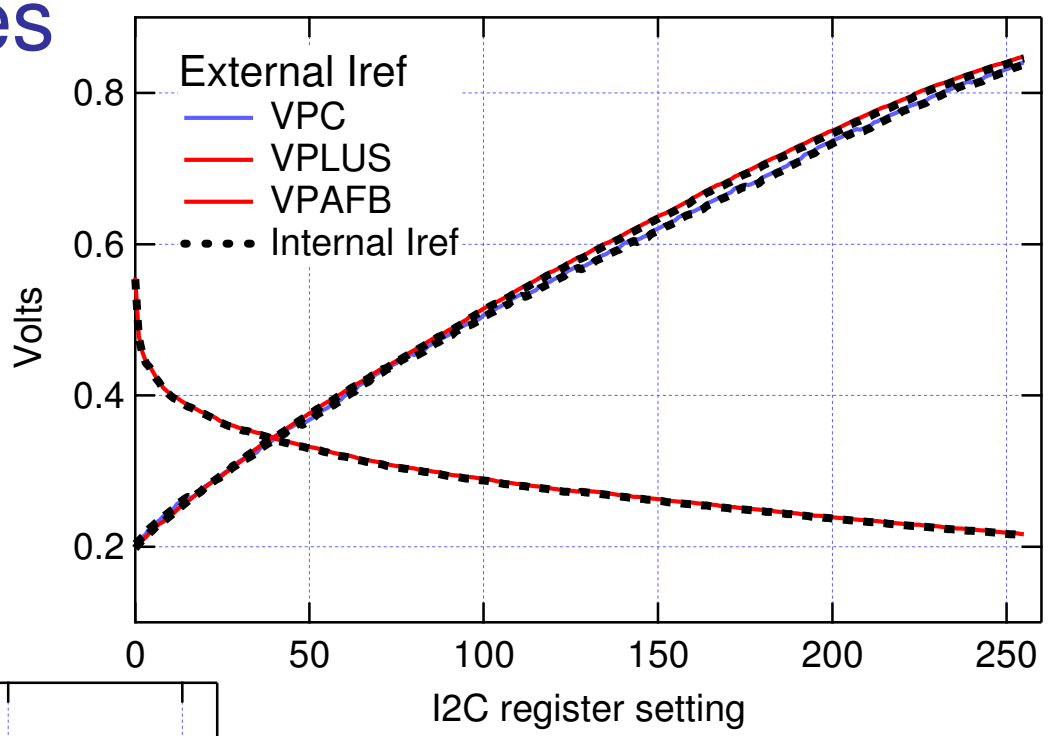
=> internal reference very close to 64uA
    (at least for this chip)



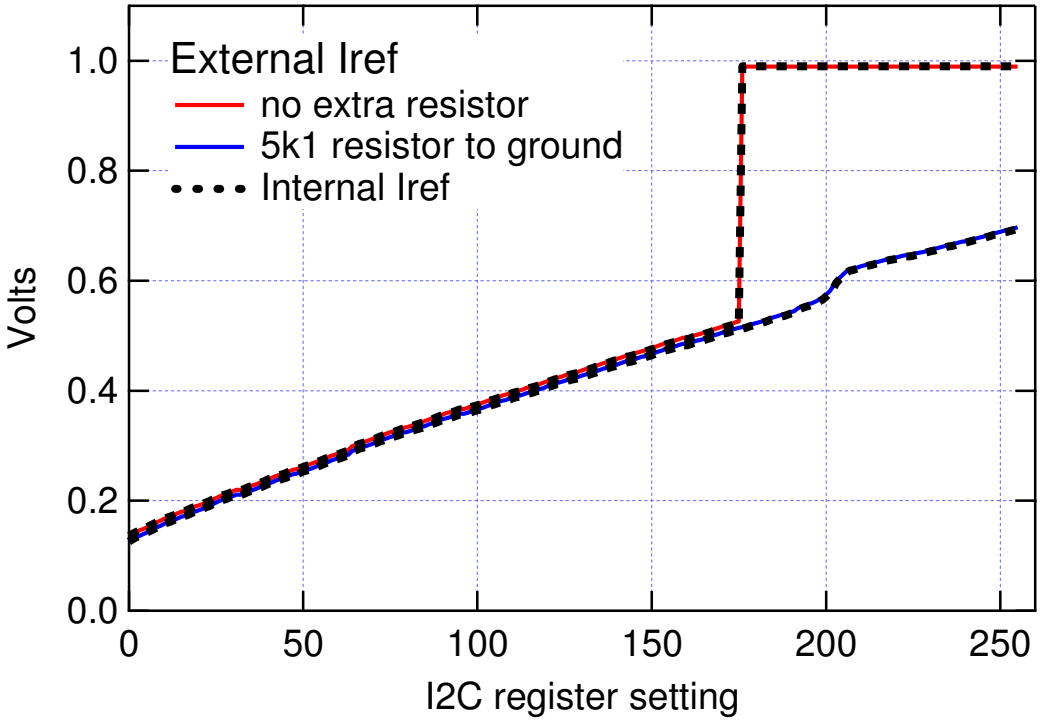
CBC biasing - voltages

VPC - preamp cascode voltage
VPLUS - postamp reference
VPAFB - postamp feedback bias

all work as expected



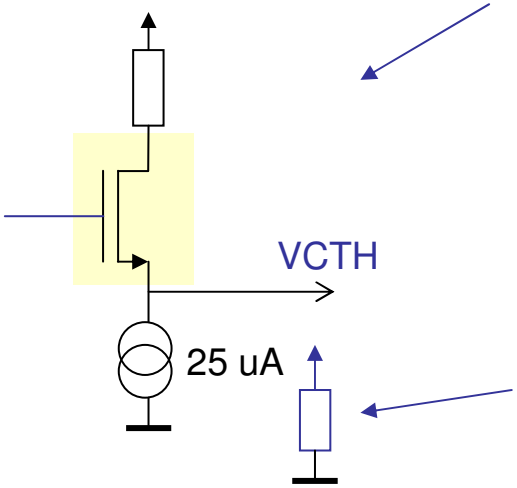
VCTH



VCTH - comparator global threshold

has a problem - next slide

VCTH problem



VCTH drive circuit can source current but sink capability fixed at 25 uA

if VCTH > Postamp output for all channels, then Nint positive for all channels

500k in parallel for all channels = ~4k

~ 0.5 V / 4k = 125 uA

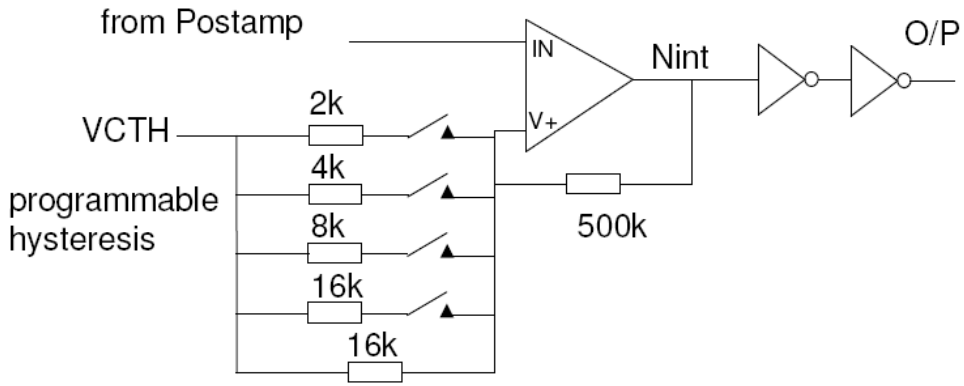
drive circuit can't sink this so VCTH gets pulled high

can fix with external resistor to ground (on VCTH pad) to provide extra current

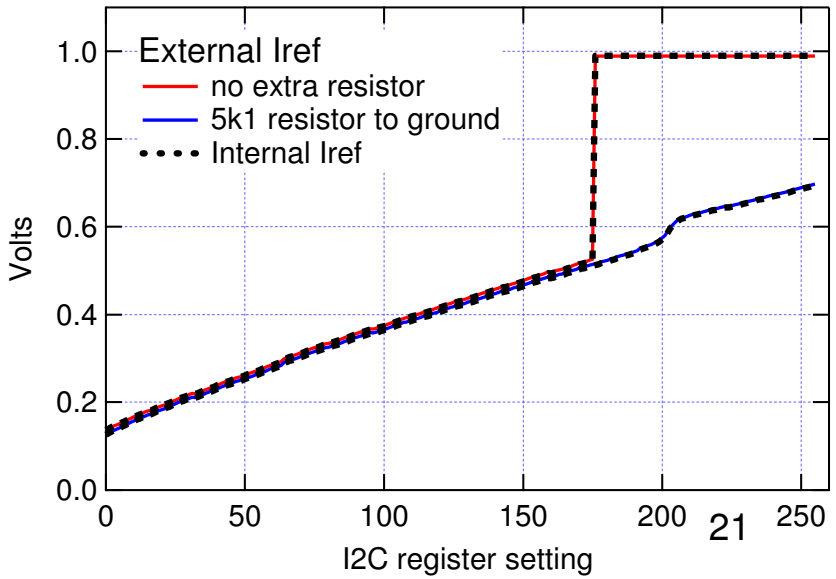
or drive VCTH with external DAC

(look for better fix for next CBC version)

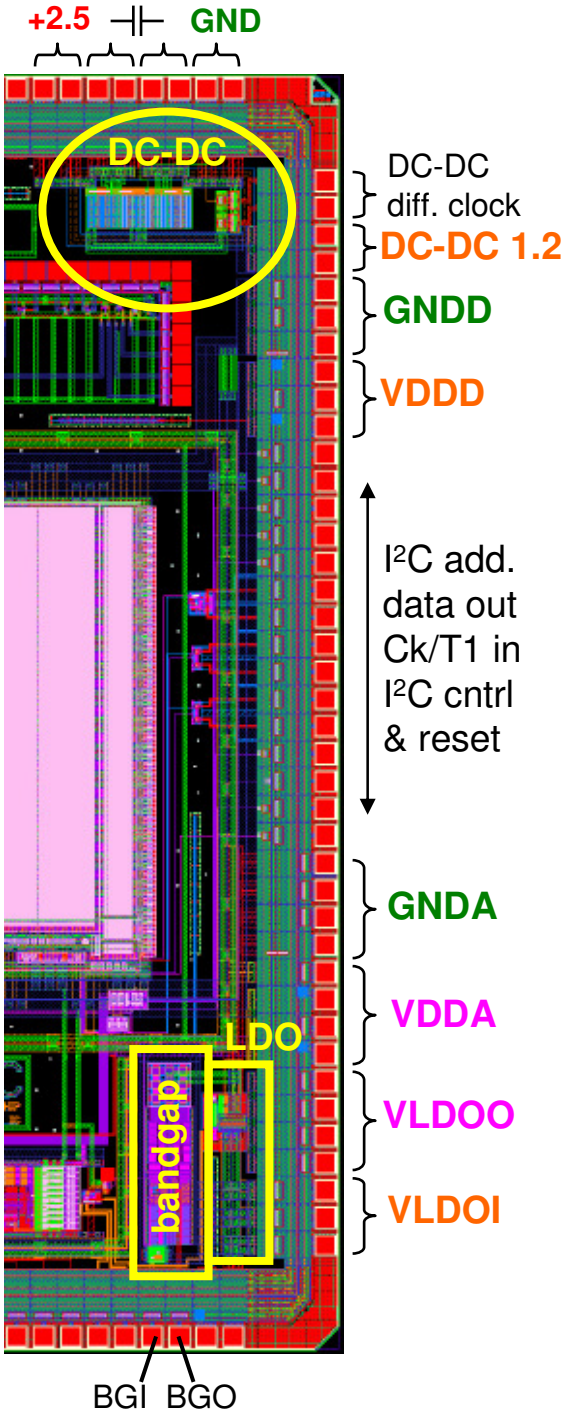
COMPARATOR CIRCUIT



VCTH vs I2C setting



power circuitry

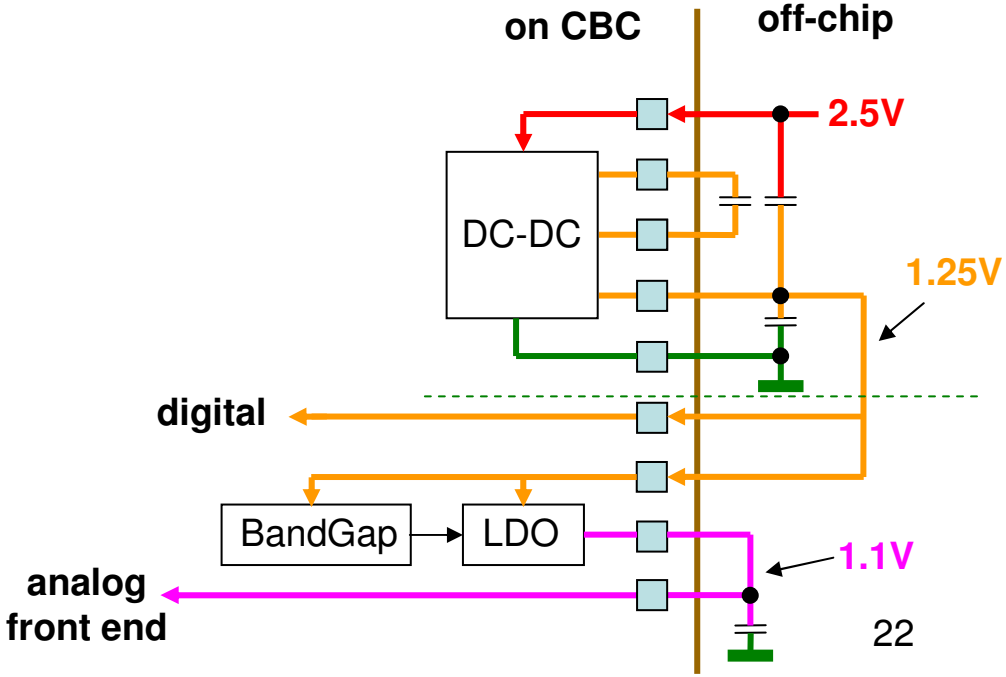


CBC incorporates on-chip circuitry to investigate powering options

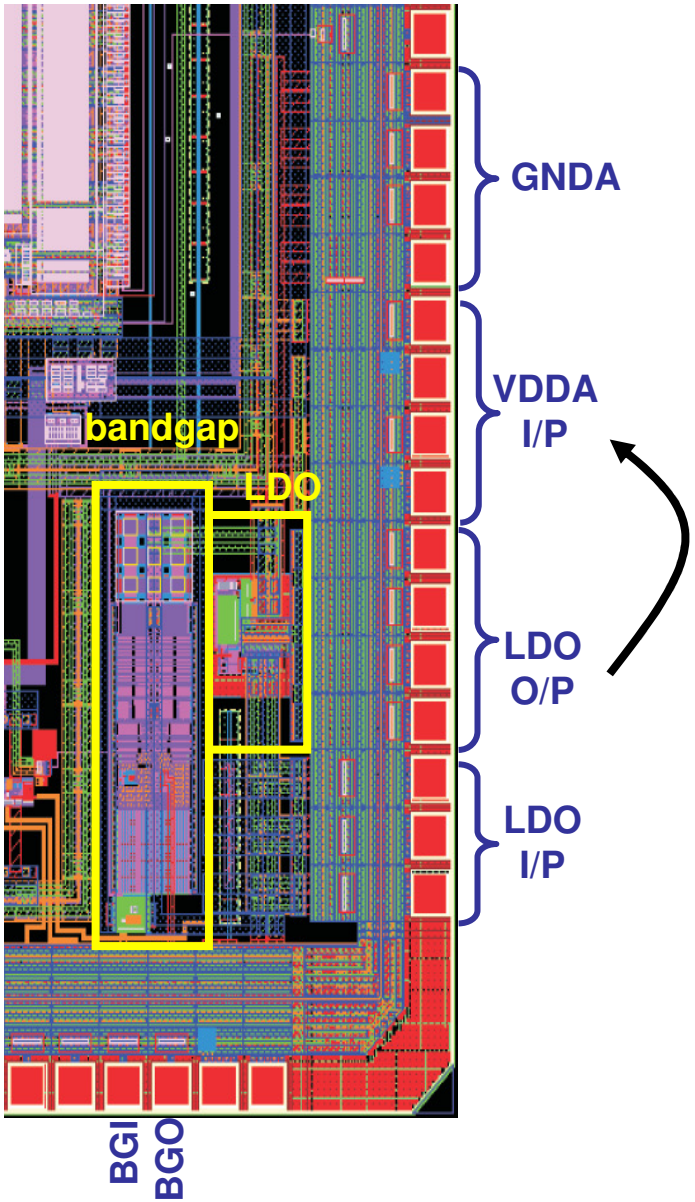
switched cap. DC-DC (CERN)
- converts 2.5 -> 1.25 in scenario where buck converter
- provides 2.5 V from 12 V rail

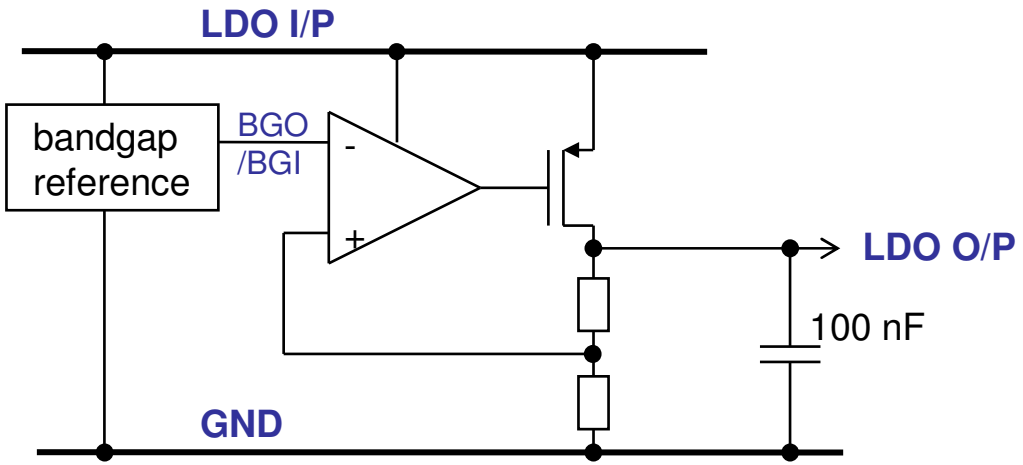
can use 1.25 to provide CBC digital supply

LDO regulator
- regulates 1.25 -> 1.1 for analogue front end
- uses CERN bandgap for voltage reference



LDO - intro





LDO included to provide clean, regulated rail to analog FE

~ 1.2 Vin, 1.1 Vout

uses CERN bandgap as Vref (0.6 V)

bandgap output (BGO) and input to LDO (BGI) taken to pads to allow to measure and/or over-ride

LDO design needs care to achieve stability
no stability issues found with CBC design

LDO - DC performance

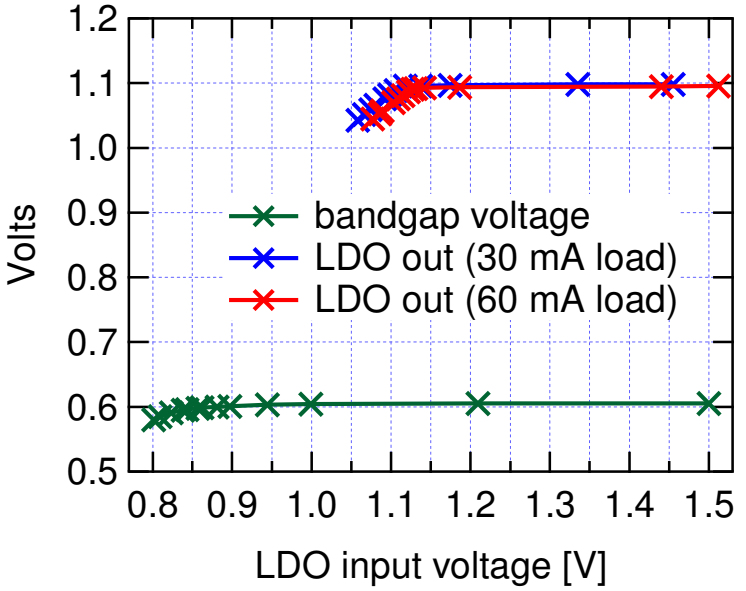
DC measurements show LDO performing well

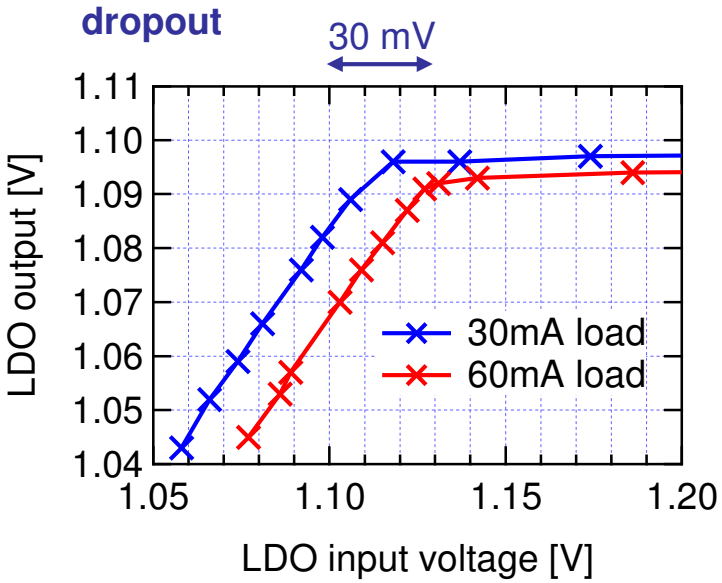
bandgap flat down to 0.9 V

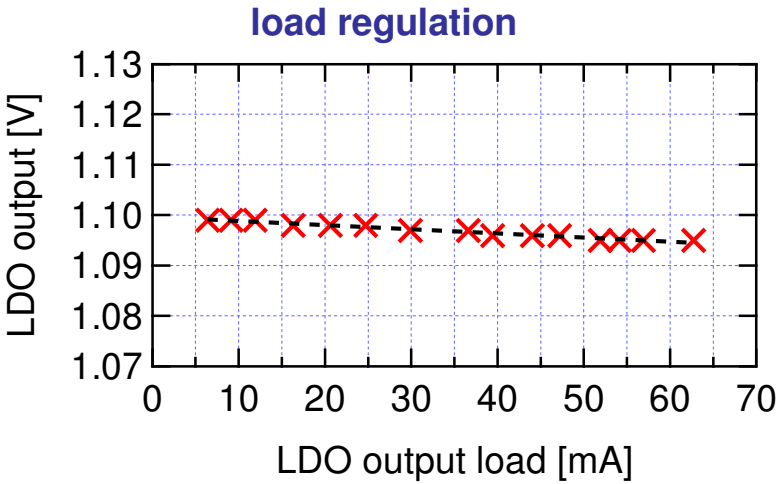
dropout only 30 mV for 60 mA load

load regulation

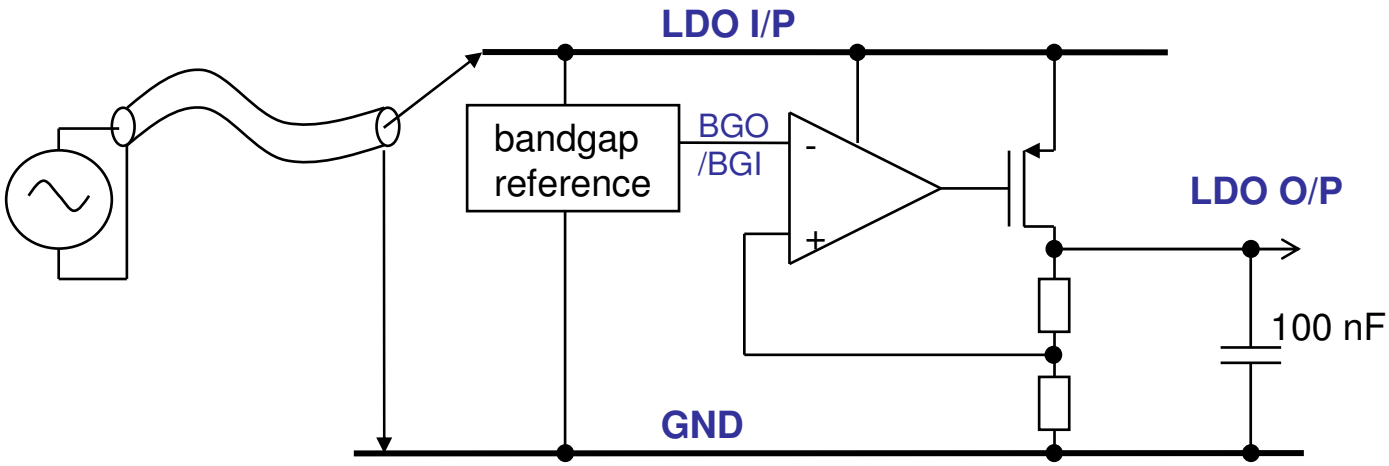
~ 5 mV change in Vout for 60 mA change in load







LDO - AC performance



measurement techniques still under development - work in progress

in principle simple

superimpose sinusoidal waveform on DC supply (LDO I/P)
measure what appears on LDO O/P

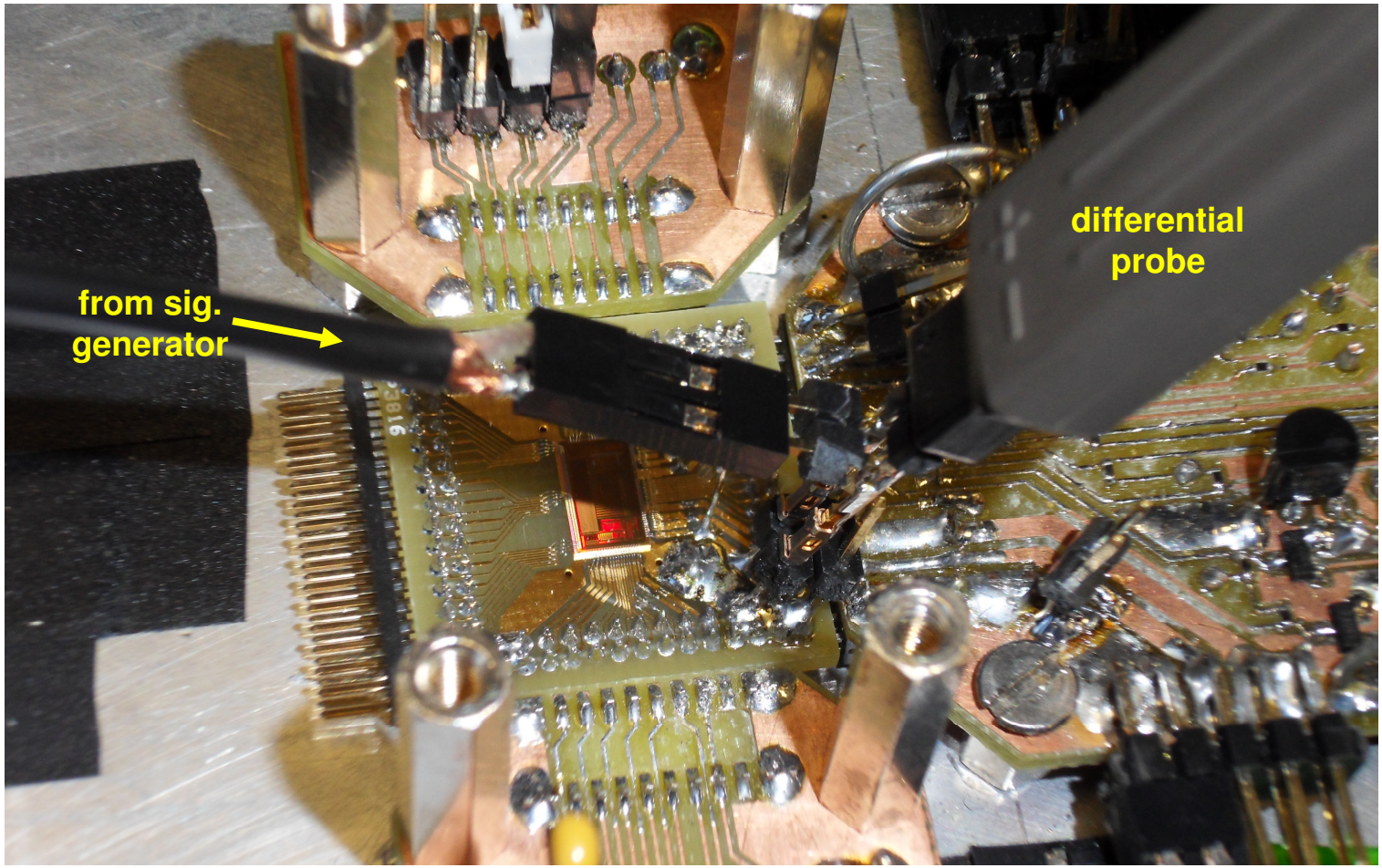
in practice

difficult to introduce and measure signals
“clean” measurement complicated by stray components (e.g. track parasitics)

design issue identified

bandgap output affected by noise on supply - passes it on to LDO
can fix with external capacitor on BGO/BGI - need better fix in future

measuring LDO - AC performance



probably need to improve technique to exclude parasitic effects as much as possible

maybe need a dedicated test setup?

LDO - AC performance

LDO O/P measured for 100 mV p-p sinewave ripple on 1.25 V DC LDO I/P

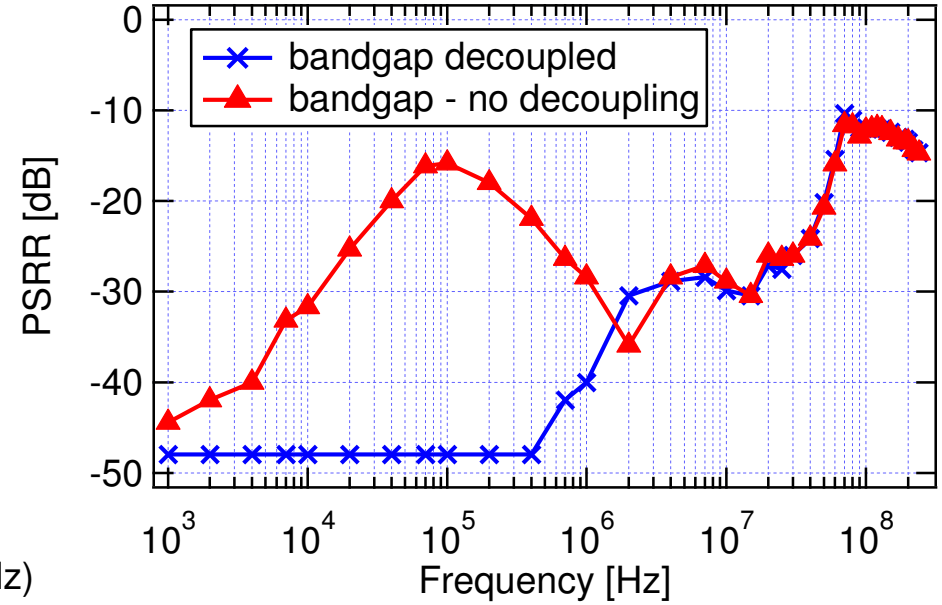
PSRR = 20.log[(LDO O/P)/(LDO I/P)]

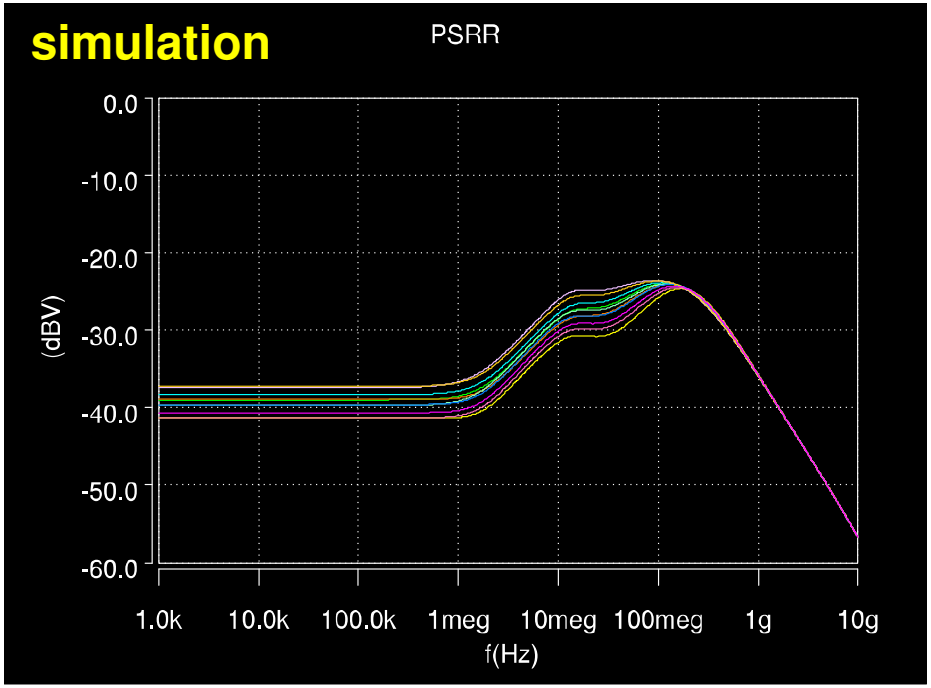
measurement has some agreement with simulation

with bandgap decoupled get v.good rejection at low frequencies (signals at limit of measurability)

discrepancies at highest frequencies (> ~ 20-30 MHz)

but quite good rejection up to ~ 10 MHz



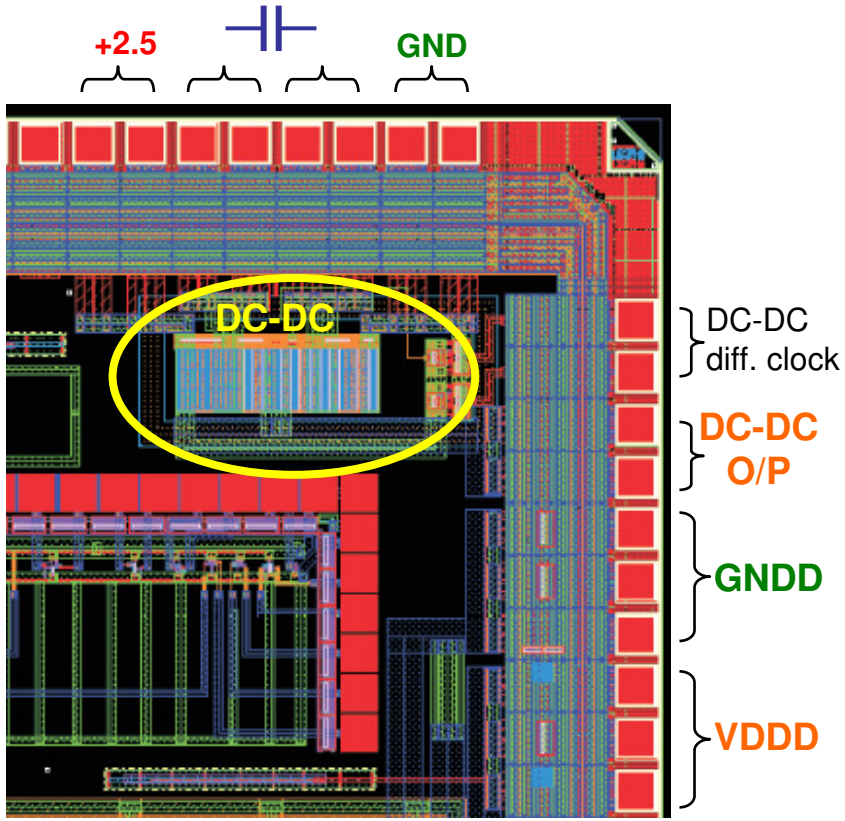


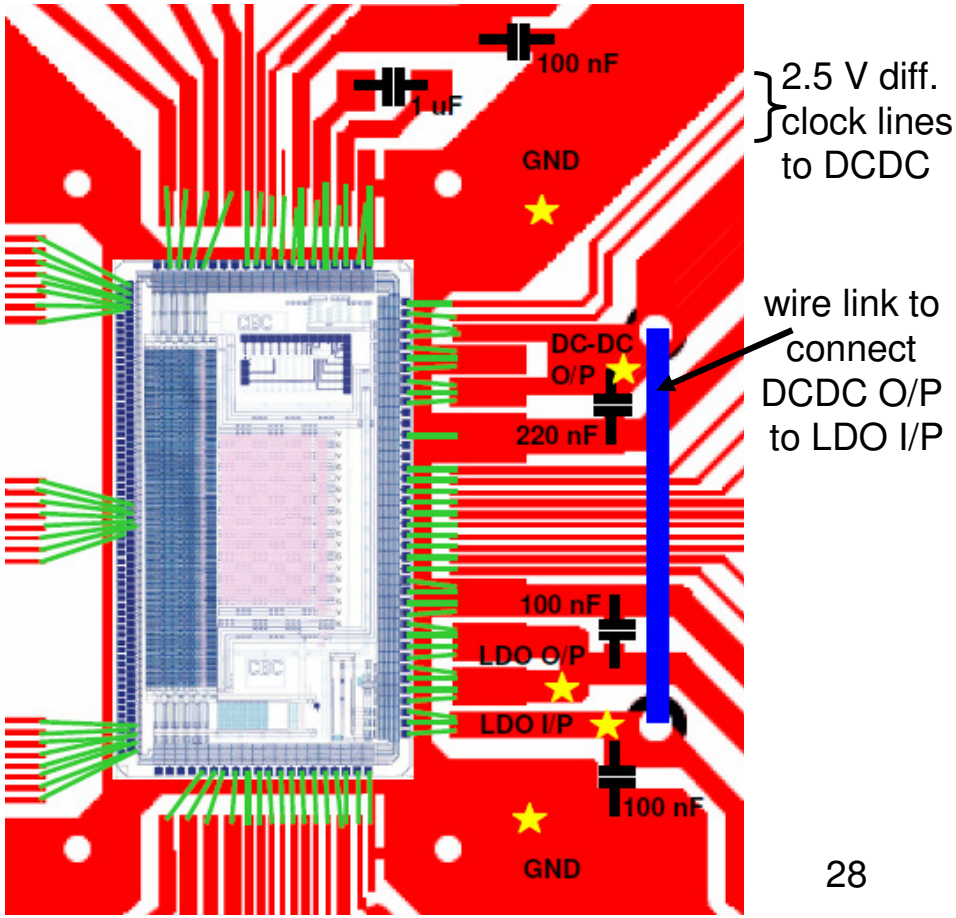
DC-DC circuit measurements

DCDC switched capacitor converts 2.5 -> ~ 1.2 using 1 MHz clock

measure voltages using differential probe between signal under study and nearest ground area

yellow stars show probe points on CBC test board





DC-DC circuit results

red/blue waveforms either end of wire link on CBC test board

should be the same voltage

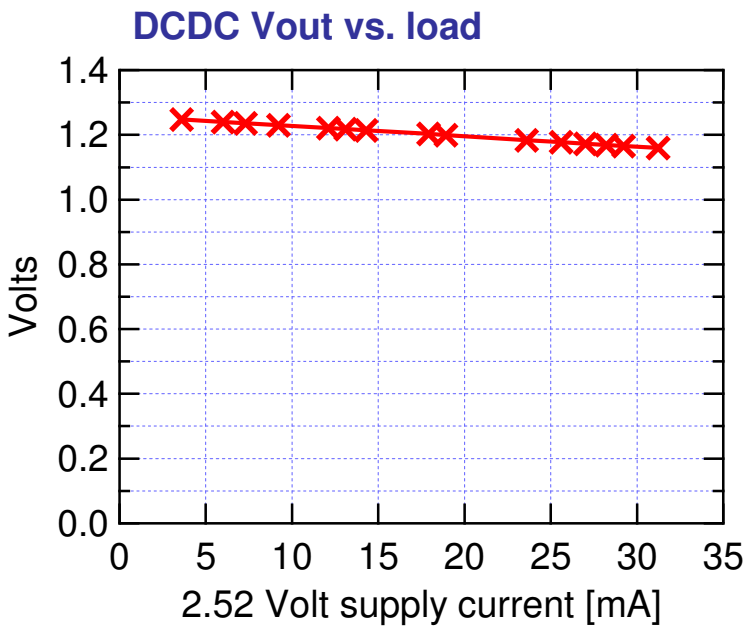
differences possibly due to

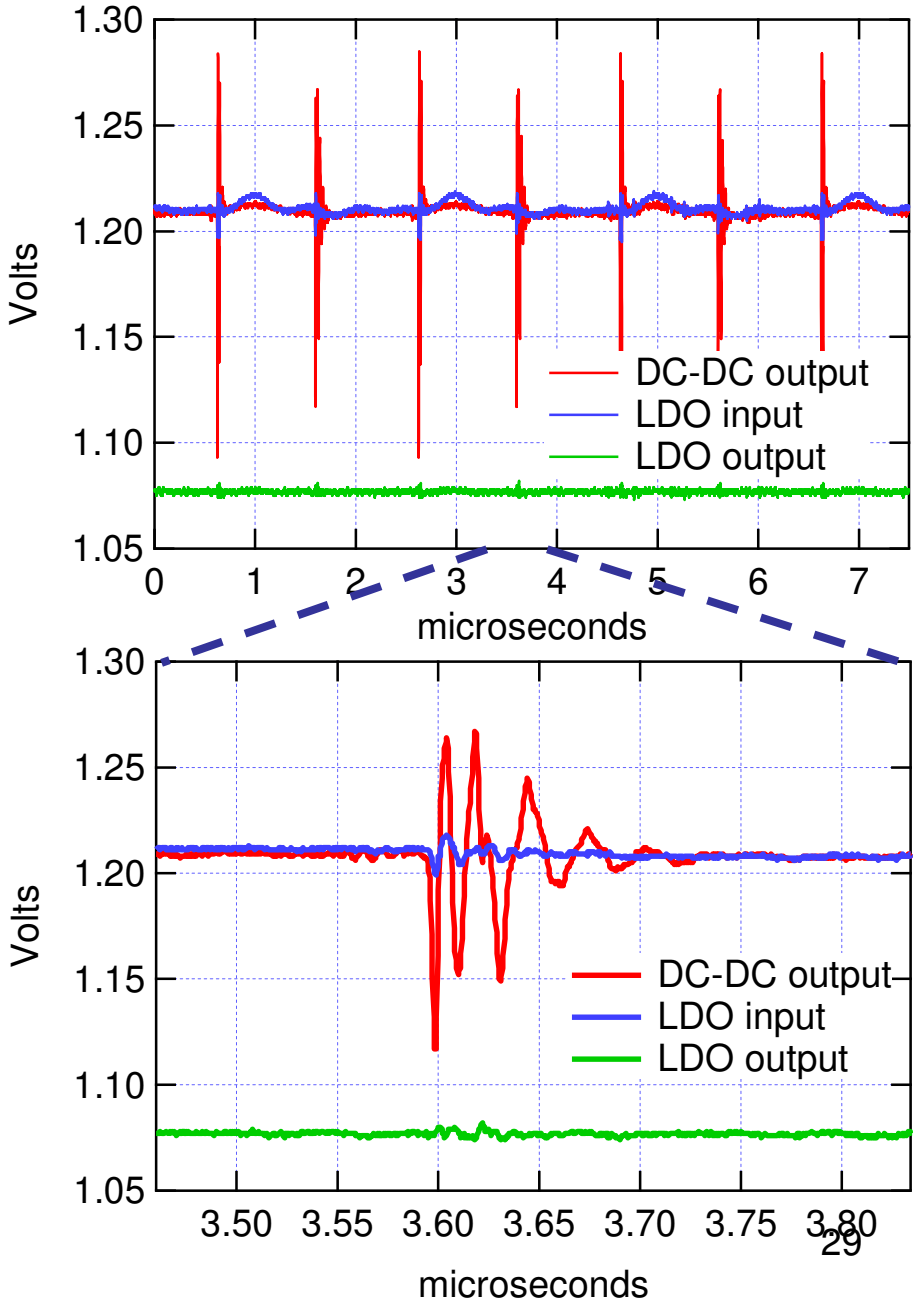
differences in local parasitic impedances?
probe pick-up?

efficiency measured for ~ nominal CBC load

2.52 V / 14.2 mA -> 1.2 V / 26.4 mA
=> ~ 90%

effect of DC-DC circuit on CBC channel noise under study





power consumption

analogue

depends on sensor capacitance

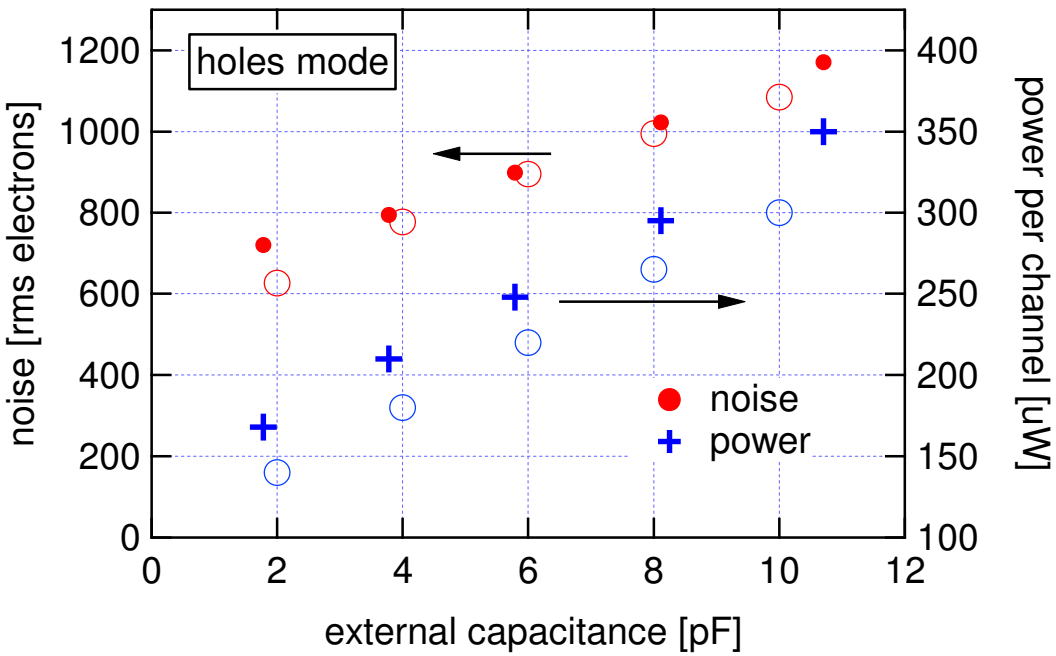
130 + (21 x C_{SENSOR}[pF]) uW

digital

I_{VDDD} = 2.8 – 4.5 mA for whole chip

(depending on SLVS bias setting)

< 50 μW / channel



no measurable dependence on L1 trigger rate

(0 – 100 kHz)

digital circuitry functions correctly down to V_{DDD} = 0.9V

total

180 + (21 x C_{SENSOR}[pF]) uW

e.g. < 300 uW for 5 pF sensor capacitance

(c.f. APV25 ~2.7 mW / chan. (but long strips))

digital power sufficiently low that possible savings from operating at lower voltages probably not worth the extra complication

testing programme status

blue = reasonably advanced
green = needs more work
red = not looked at yet

baseline performance (conventional (clean) powering scheme)

- **digital functionality**
  - fast (Ck/T1 - SLVS) & slow control (I2C) interfaces setup and operation
- **analogue functionality**
  - amplifier
    - pulse shape, noise, linearity, overload tolerance, ..
      - C_{IN} dependence, signal polarity dependence, across chip & chip-to-chip uniformity
    - leakage current tolerance
- **comparator**
  - timewalk, threshold tuning and uniformity, hysteresis

all above will depend on bias generator settings
=> large parameter space to cover

- **power consumption**

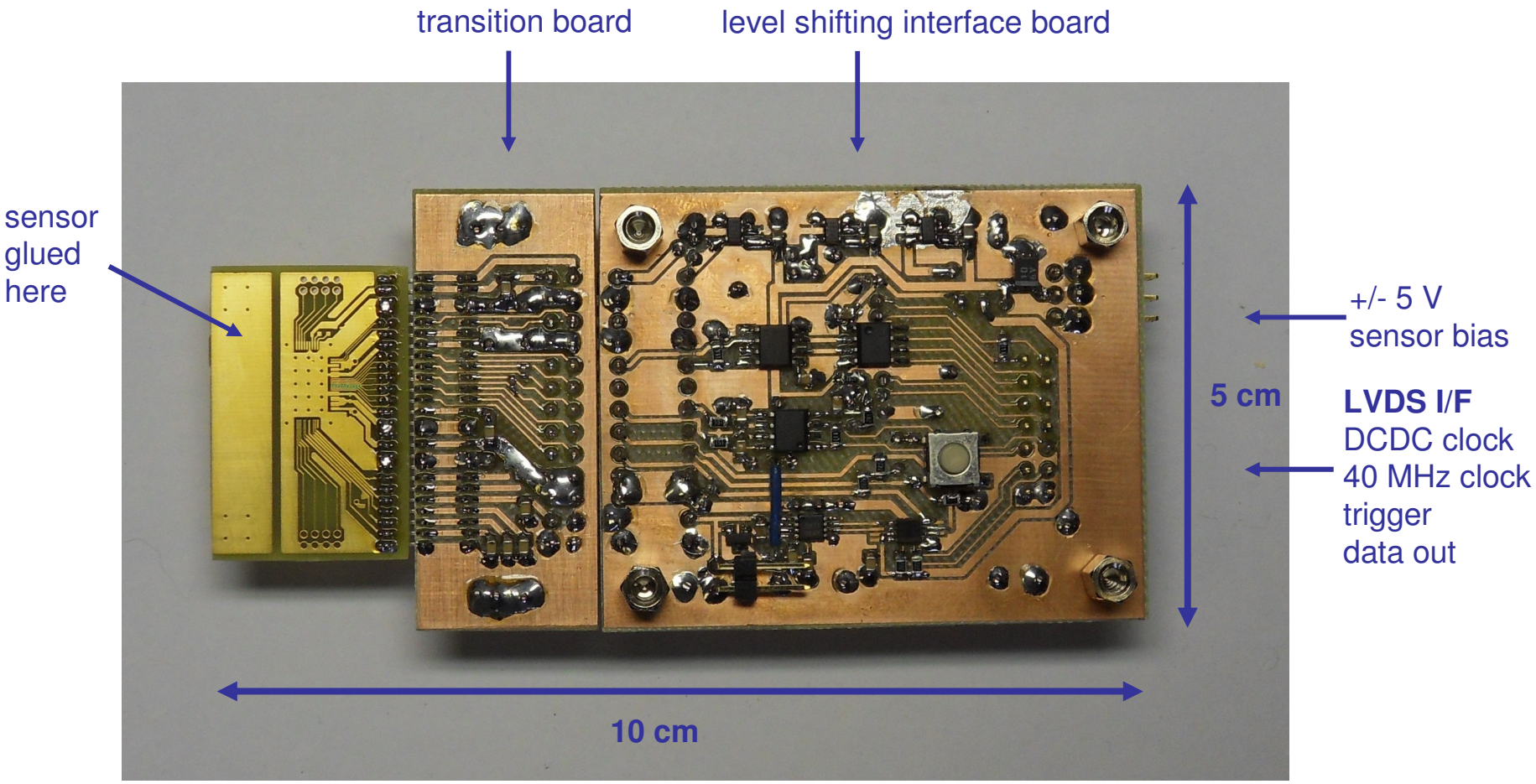
powering options studies

- supply sensitivity with/without various on-chip options

longer term

- temperature effects (~ all of above vs. T) ← no firm plans yet
- tests with sensors ← test setup in preparation (next slide)
- radiation: ionizing & SEU sensitivity ← no firm plans yet
- test beam ← hope to put simple setup in beam later in the year

single CBC + sensor test board



transition board and interface board could be connected by twisted pair flat cable

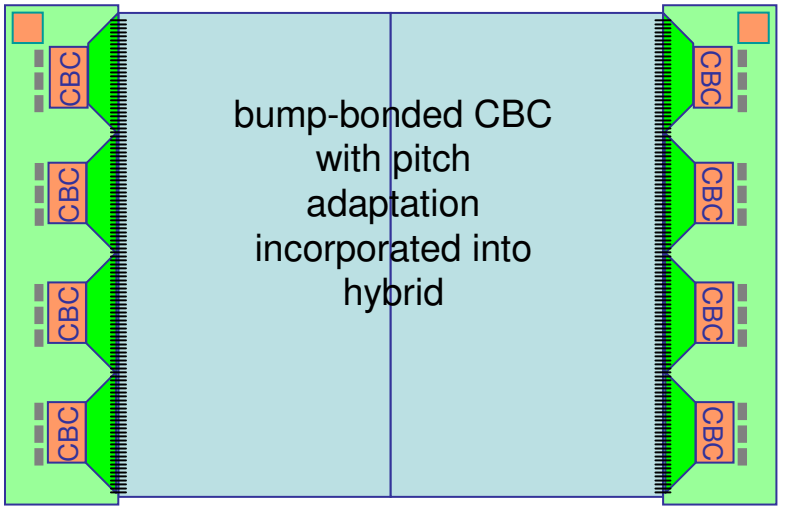
nothing tested yet

future directions

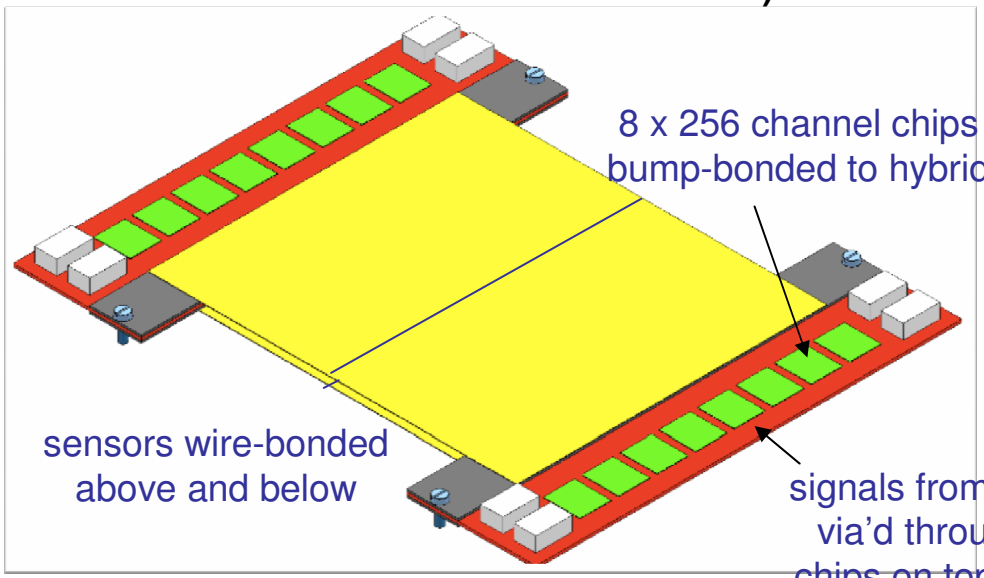
currently looking at:

1) bump-bonded version

allows to integrate pitch adaption to sensor on hybrid
hybrid has to be “hi-tech” substrate
fine pitch bonding (C4 ~ 250 μm) and tracking
chip layout should proceed in parallel with substrate design
things to learn about hybrid technology and impact on chip
plenty of scope for collaboration here



2) 256 channel version with 2-in-1 triggering capability



existing CBC L1 triggered short strip chip can be adapted to provide 2-in-1 type trigger data for CMS outer tracker

need

cluster width discrimination
offset and correlation
trigger formation and transmission

summary

130 nm CBC prototype working quite well

already providing valuable information

performance achievable and power budget required

no show-stopping problems

mainly biasing issues - relatively simple workarounds

will not stop us learning all we need to from this prototype

long testing programme ahead, including

powering options - further studies

temperature effects

tests with sensors

radiation: ionizing & SEU sensitivity

test beam

CBC documentation:

http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/