CMS Binary Chip User Guide 1.0

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1. Introduction

The CBC is to be used within the tracker of the CMS experiment on the SLHC. The SLHC will accelerate two beams of charged particles in opposite directions around a circular particle accelerator based at CERN in Geneva. The particles are concentrated into bunches and the paths of these bunches cross at intervals around the ring. The CMS experiment is based at one such point and the tracker forms the inner region of the experiment – its purpose is to track charged particles produced in the bunch collisions. The inner region of the tracker comprises pixellated silicon detectors whilst the outer region comprises silicon strip detectors.

The CBC chip reads out the charge generated by ionising events within the silicon strips of the CMS detector. It converts these events into a "hit" or "no hit" binary value for each of the channels. These ionising events are synchronised with the bunch crossing event interval of 25ns and without knowing which events are suitable for readout the chip must store the data from each event up to a maximum of 256 bunch crossing intervals (6.4μs for a 25ns clock). This time is known as the trigger latency, and is the time it takes the external system to decide which of the events are worth reading out.

When the CBC receives a trigger signal the event stored one trigger latency previously is read out into a data buffer where it is stored until it can be read out from the chip. The data buffer is required because data is read out serially from the chip at no faster than the clock rate or a programmable sub-division thereof. For a clock rate of 40MHz, reading 128 channels, a time stamp, plus a few other bits requires 3.5μs. At the same time the CBC must continue to take data every bunch crossing.

The average trigger rate is 100kHz (10μs). However, due to the random nature of the trigger, the data buffer must be deep enough to cope with several triggers arriving faster than 100kHz. Provided the data from one event is read out quicker than 10μs then the data buffer only rarely fill up and events be lost.

Since there will be several thousand CBCs operating within the small volume of the tracker, the power consumption must be minimised as far as possible. During operation of the SLHC the environment will be highly radiated with charged particles requiring the electronics to be designed using radiation tolerant techniques, both for total dose and for Single Event Transients (SETs). The chip is fabricated in 130 nm CMOS.

2. Specifications

2.1 Front End

- 128 channels + 2 dummy channels. Pad pitch: 50μm.
- 1 dummy channel outputs available for test.
- 128 channels + 2 dummy channels. Pad pitch: 50μm.
- Reads both electrons and holes (selectable)
- Charge collection time: less than 10ns.
- Amplifier peaking time: less than 20ns.
- Amplifier noise: less than 1000 electrons up to 5pF detector capacitance and leakage current of 1μA.
- Detector leakage current noise: less than 500 electrons up to 1μA leakage
- Time walk: (difference in timing in the output of the comparator at 0.5 VDD for 1.25fC and 10fC signals and a comparator threshold of 1fC) ≤ 16ns (from the ABCD3T specification).
- 8 bit trim of for comparator threshold matching.
- Overload recovery: response to normal signal <2.5 μs after a heavy ionising particle (HIP) of 4pC.

2.2 Pipeline, Buffering and Logic

- Pipeline depth (latency) from 1 to 256 clock cycles (6.4μs at 40MHz).
- Latency and FIFO overflow error checking.
- Capable of buffering 32 triggers awaiting readout.
- Critical control blocks designed with SEU tolerance.

2.3 Control

- Slow control via an I^2C interface used to configure the chip.
- Fast control via the trigger input. Two functions: Trigger & Reset101.

2.4 Input/Output

- Fast Input: SLVS (Scalable Low Voltage Signalling)
- Fast Output: SLVS
- Slow control: I^2C pads.

2.5 Power

- Analogue supply (VDDA) 1.1 to 1.2V.
- An on-chip DC-DC converter can be used to generate 1.2V from 2.5V.
- An on-chip LDO regulator can be used to supply VDDA at 1.1V
- DC-DC and LDO selectable using bond-pad configuration.
- Digital supply (VDDD) up to 1.2V.
- Power consumption 0.5mW / channel for a sensor capacitance of 5pF. This breaks down to 200μW for the front end and 300μW for the digital functionality. Total is 64mW for the full chip.
- Power supply rejection as good as possible for a single ended input stage.

3. Functional Description

3.1 Summary

The CMS Binary Chip (CBC) is the front end readout ASIC for silicon strips in the CMS tracker for SLHC. The original LHC readout chip (APV25-S1) had an analogue non-sparsified readout architecture. For SLHC, a binary non-sparsified readout has been chosen as the target architecture for the CBC.

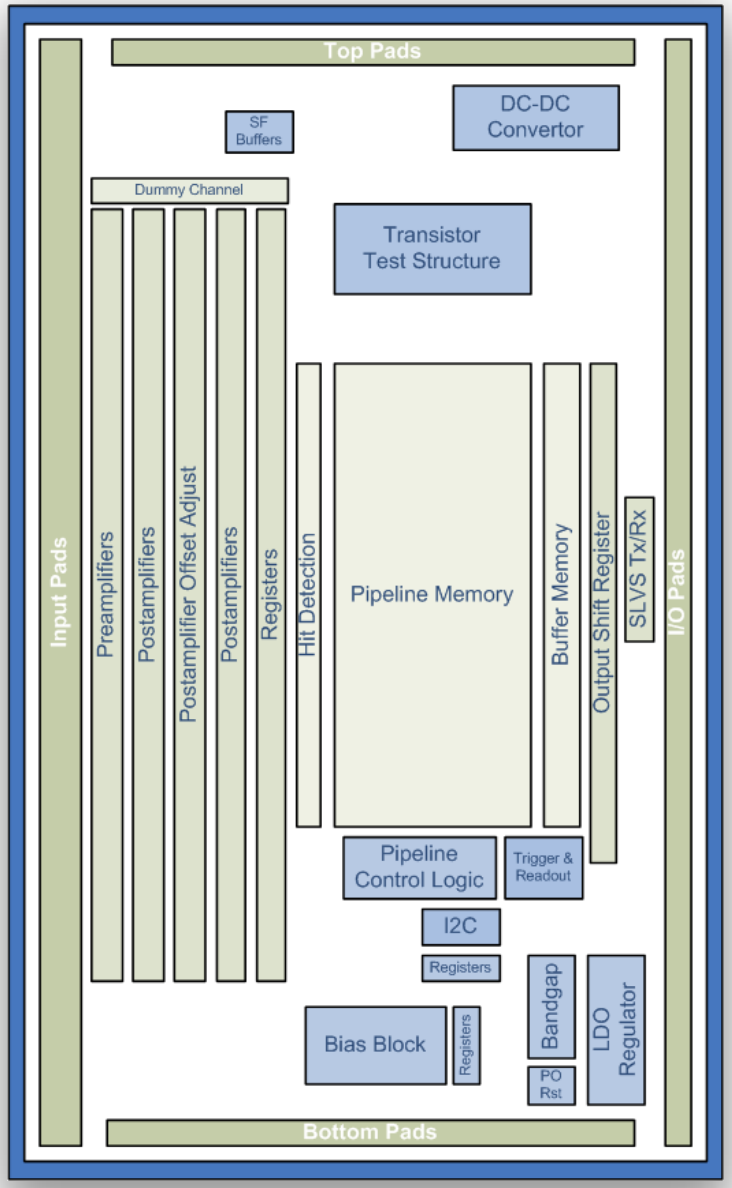

Figure 1. CBC block diagram

Non sparsified data simplifies the readout architecture and has the added benefit that it can be emulated off-detector making it easy to spot chips which become out of synchronisation with the rest of the system. A binary architecture has been chosen to reduce the amount of data that needs to be processed.

The design has been partitioned to perform the requirements as shown in figure 1. The front end consists of 128 channels of charge preamplifers followed by gain amplifiers. Comparators detect any signals over threshold and pulse detection logic generates "hit" signals. The binary output from each channel is then continuously written into a 256 deep pipeline RAM.

The *Pipeline Control Logic* (PCL) sequences the writing of data from the *Hit Detection* circuit into the *Pipeline Memory*. The PCL controls the transfer of data from the *Pipeline Memory* into the *Buffer Memory* when an external trigger signal is received.

Data is held in the *Buffer Memory* until such a time that it can be read out. This will depend on how many previous triggered data are also held in the buffer. When the data is read out, it is serialised together with the column address from which it originally came and some information bits. This function is controlled by the *Trigger & Readout logic* and data read out through the *Output Shift Register* and *SLVS* output.

A Programmable *Bias Block* is used to supply bias voltages and currents for the front end analogue electronics. A programmable *Postamplifier Offset Adjust* allows 8-bit control for comparator offset matching. A further *Register* configures the operation of the chip. These are all programmed via an *I2C* interface.

A band gap provides a reference voltage for the bias circuit, and this is initialised by a power-on-reset circuit.

A *Low Drop Out* voltage regulator (LDO) can be used to supply the analogue front end and bias generator with 1.1V from the 1.2V supply. This increases power supply rejection, especially if the DC-DC Converter is used to supply the 1.2V from 2.5V.

Also included on the chip are some source followers (which buffer the dummy channel outputs onto pads for testing), and some test transistors for characterisation.

3.2 Front End

The CBC front end is shown in figure 2. The input is bonded to one strip of the detector. Charge generated by an ionising event in the strip is read out by a *preamplifier* and integrated onto a feedback capacitor. The feedback capacitor is discharged by a resistive feedback network which is selectable to optimise the circuit for both electrons and holes.

The resulting voltage pulse from the preamplifier is further amplified by a capacitive gain *postamp*. A large value feedback resistance stabilises the amplifier. This feedback network is also selectable depending on the polarity of the input charge. To compensate for any mismatch in amplifier and comparator thresholds the *postamp*

has a programmable offset controlled using a differential current Ipaos. These currents are programmed using an 8 bit register in each channel

The comparator detects signals over a defined threshold and will produce a digital "1" pulse during this period. A polarity select circuit is used to keep the polarity the same no matter whether electrons or holes are being read out. A 4 bit programmable level of hysteresis is also available.

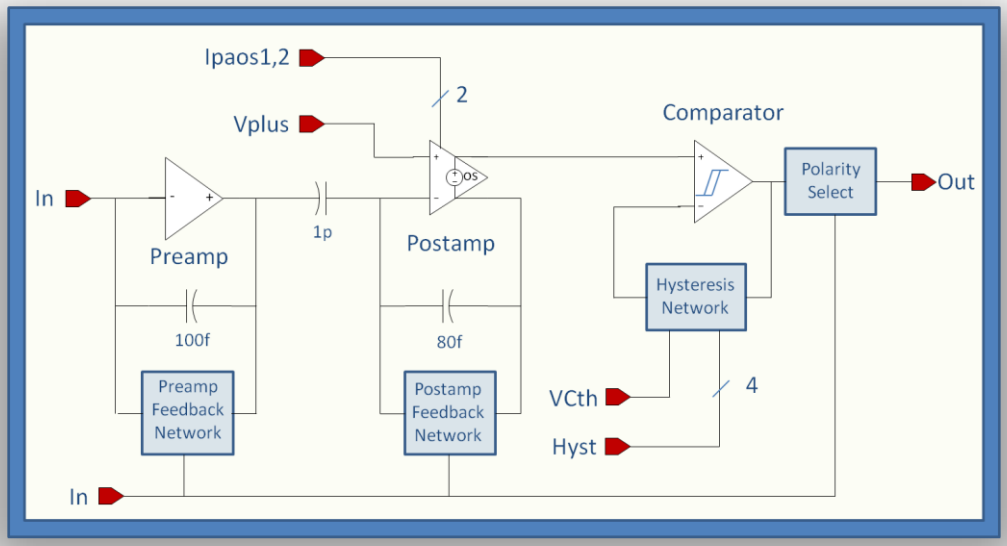

Figure 2. CBC Front End

3.3 Preamplifier

The *preamplifier* (figure 3) consists of a single ended cascode amplifier, a source follower at the output, and a feedback capacitor and resistor network.

The open loop voltage gain (A_V) must be sufficiently high such that most of the charge generated by an ionising event is removed from the detector. The detector capacitance (5p) and any parasitic capacitance at the input, must be small compared to $A_V.C_f$ so that most of the charge is integrated onto the feedback capacitor C_f. In addition, the feedback capacitor connects to the input of the source follower and therefore helps in compensating the amplifier.

The integrated charge is discharged through the feedback network. If electrons are being read out the switches "*e*" will be closed and a single resistor of 200k forms the feedback resistance. If holes are being read out then switches "*h*" will be closed and a t-network forms the resistive feedback.

The resistance of the feedback network must be sufficiently large such that the time constant R_fC_f is not so small compared to the rise time of the signal such that signal is lost. However, the feedback resistor must not be so large that any offset due to detector leakage current reduces the dynamic range of the amplifier.

The resulting voltage pulse is driven to the gain amplifier with the low output impedance of the source follower which also provides a voltage step which ensures the cascode transistor remains in saturation. The cascode bias *Vc* must be supplied.

The single ended nature of the amplifier does make it susceptible to noise on the power and ground lines.

The design makes use of the triple well process allowing the NFET substrates to be biased independently from ground..

The nominal current used by the preamplifier is 90+10+25 = 125uA.

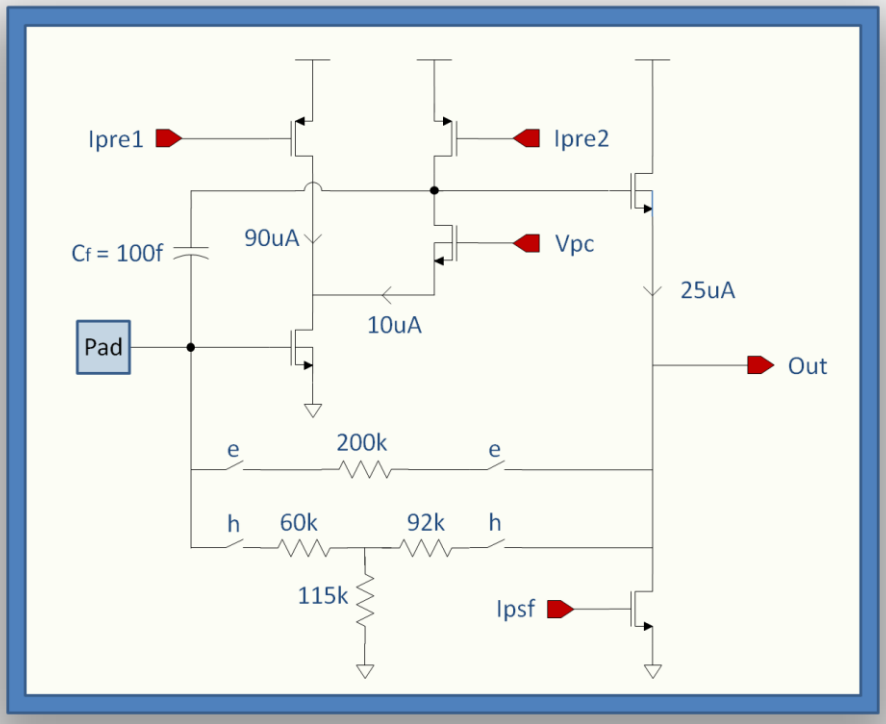

Figure 3. Preamplifier Schematic

3.4 Postamp

The *postamp* (figure 4) is comprised of a differential amplifier – an input capacitor *Cin* and feedback capacitor *Cf* provide the voltage gain. DC stability is provided by a feedback network, selectable depending on the polarity of the signal. Two diode connected PFETs are used in the first stage of the amplifier to limit the differential swing to speed recovery time for very large (HIP) signals. A capacitor *Cc* compensates the amplifier, providing stability.

A resistor in the output branch allows the offsetting of the postamp output voltage. This is done by adjusting the differential currents *Ipaos1* and *Ipaos2*. These are set by loading an 8 bit control register in the channel.

The nominal current in the postamplifier is 20+ 12.7 = 32.7uA

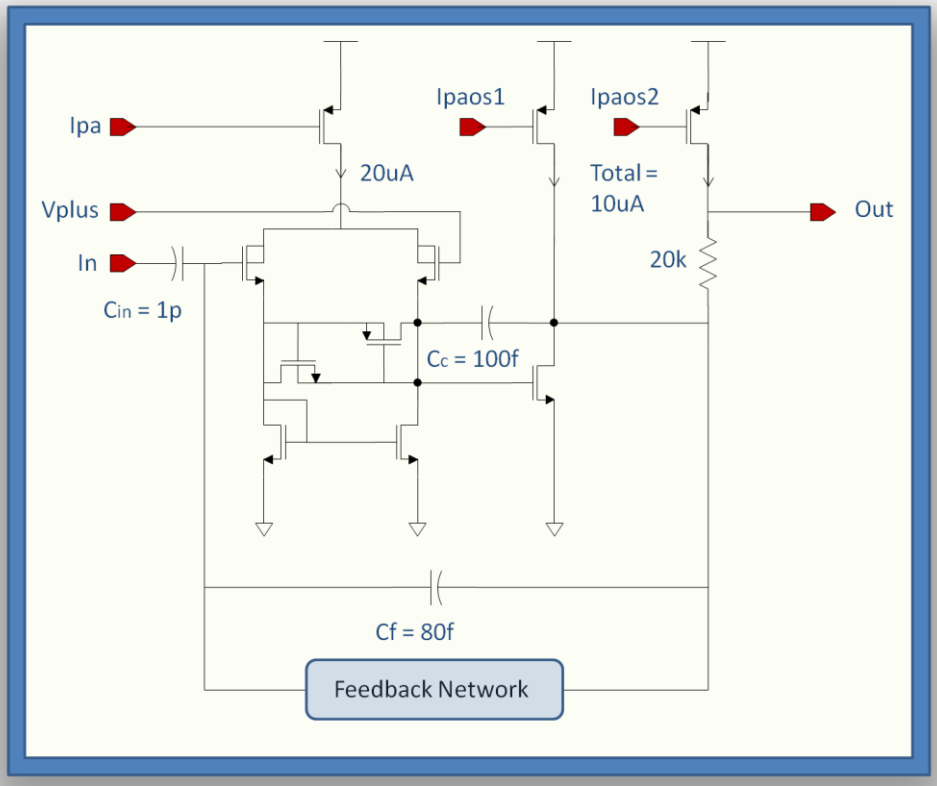

Figure 4. Postamplifier Schematic

The feedback network in both case of polarity comprises a long PFET biased with a small current. However the connections are slightly different for electrons and holes.

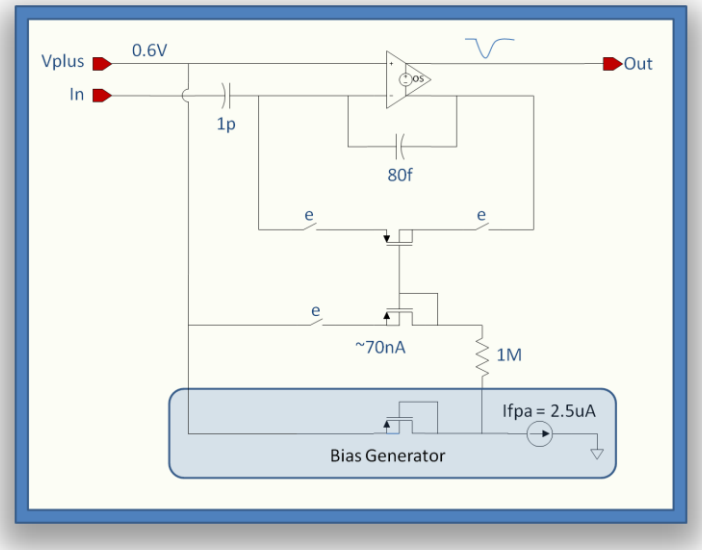

Figure 5. Postamp "electrons" configuration

Figure 5 shows the conguration for electrons. The 3 switches "*e*" connect a current mirror in the configuration shown. Since the output signals are negative going, the sources of the current mirror transistors must be connected to the higher potential (Vplus). A further circuit in the bias generator (common to all channels) can be used to adjust the current in the feedback circuit.

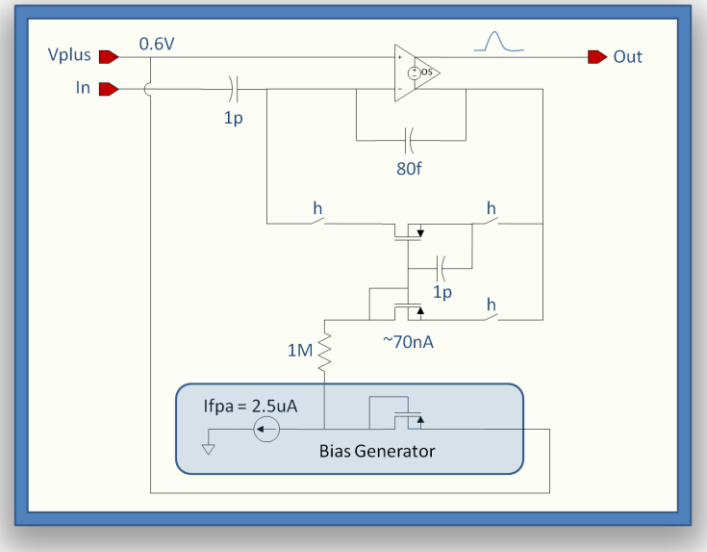

Figure 6. Postamp "holes" configuration

Figure 6 shows the configuration for reading out holes. In this case the output signal is positive going so the sources of the current mirror transistors must connect to the output. A 1pF capacitor is used to ensure that the gates of the transistors in the current mirror follow the output to maintain linearity.

3.5 Comparator

The *comparator* comprises a simple 2-stage differential architecture as shown in figure 7 followed by some logic. The differential stage is powered from the analogue domain, and the logic from the digital domain. The polarity of the output is selectable depending on whether electrons or holes are being read out – the output from the comparator should always be positive for a signal.

The comparator will have a different response time depending on the size of the input signal. This time walk is mostly dependent on the rise time of the input signal and the gain of the comparator The time walk should be less than 16ns between a 1.25fC and a 10fC signal when the comparator threshold is set at 1fC .

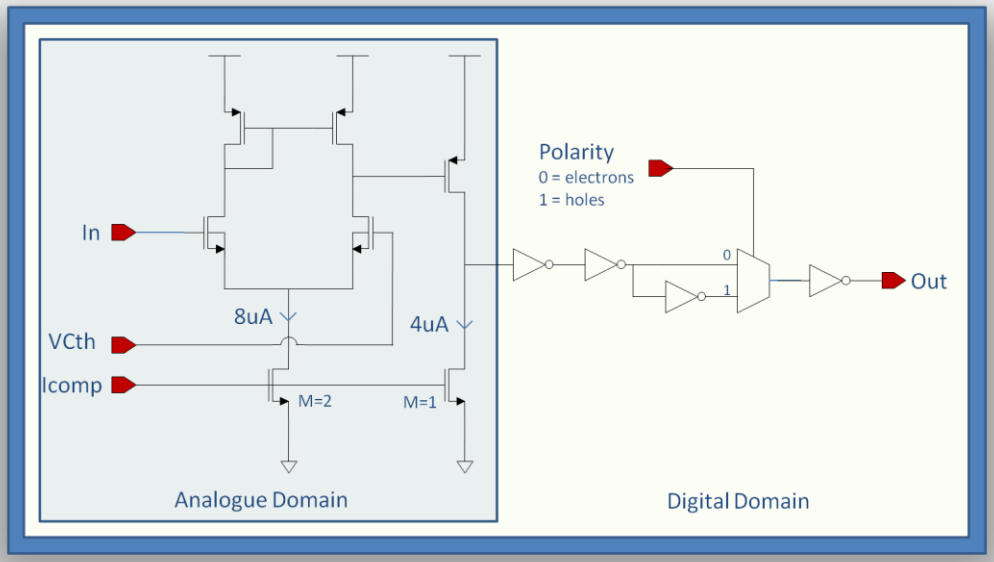

Figure 7. Comparator

The comparator also has programmable hysteresis. This is achieved using the circuit shown in figure 8. The potential divider formed by the feedback resistor and selectable input resistors modifies the comparator threshold depending on whether the output is at logic “0” or logic “1”. This amount of hysteresis is controlled globally by programming a 4 bit register. The default setting is for maximum hysteresis.

The nominal current in the comparator is 8+4=12uA.

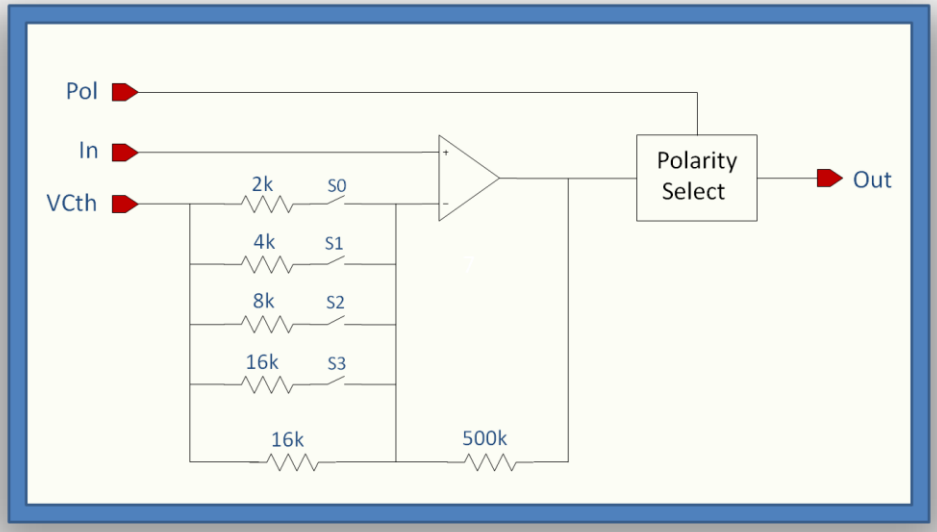

Figure 8. Comparator Hysteresis

3.6 Postamp Offset Adjust

The comparator threshold to each channel is set globally. In order to compensate for threshold mismatches in the comparator input transistors producing different input offsets from channel to channel it was decided to adjust the level of the input signal to the comparator rather than the comparator threshold voltage *VCth*. A programmable, differential current is used to bias the output branches of the postamp. The voltage at the output of postamp is offset by adjusting the current through the 20k resistor. Using the default setting for *Ipaos*, this gives a range of 0 to +200mV of offset (figure 8). The default offset is 100mV. The nominal current is 14uA.

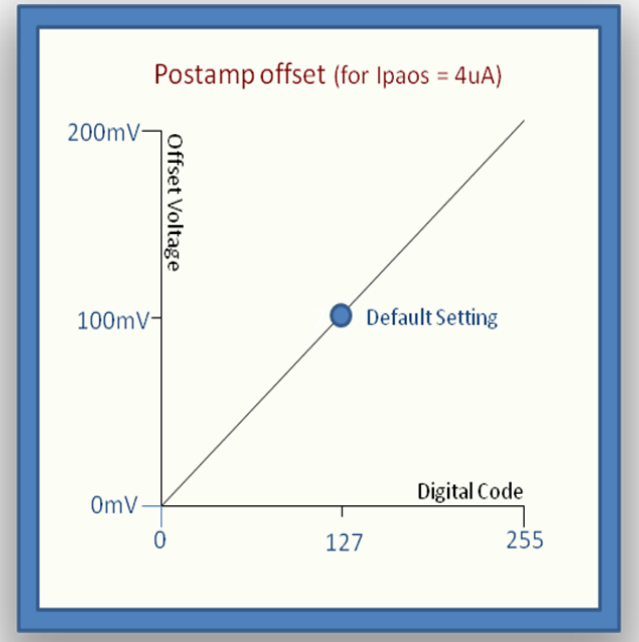

Figure 9. Offset Adjust Range

3.7 Hit Detection Logic

Some logic is required after the comparator to synchronise its output to the clock – the *Hit Detection Logic*. Two modes of operation can be selected. The first mode just passes a synchronised version of the comparator output through to the Pipeline RAM. The second mode detects the rising edge of the comparator and produces a pulse of one clock cycle's length no matter what the length of the comparator signal. In addition, the *Hit Detection* can be completely switched off using a control signal.

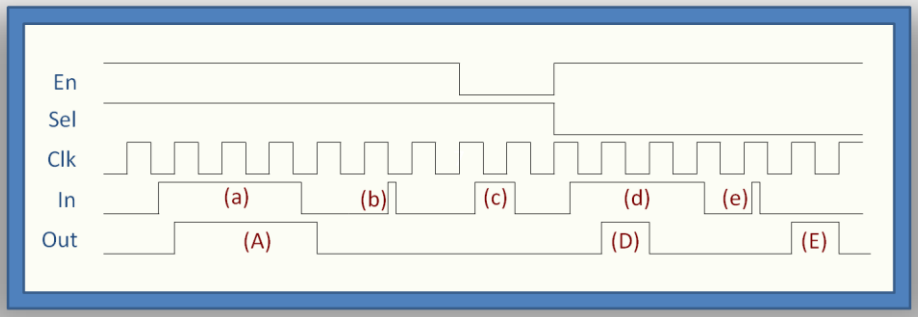

Figure 9. Comparator Hysteresis

Figure 9 shows the output from the *hit detection logic* for several cases of input. For case (a) and (b) the circuit is enabled (*EN=1*) and *SEL=1* which means a synchronised version of the input should pass through to the output. This is true of (a), however (b) was not high for enough time to be synchronised to the clock. In case (c) the circuit is disabled (*EN=0*) and nothing passes to the output. In cases (d) and (e), the circuit is enabled and *SEL=0*. This means that all comparator pulses are increased or decreased in length to be one clock cycle in length. The output from the Hit detection circuit feeds directly into the pipeline RAM.

3.8 Pipeline RAM

Figure 10 shows the data path of the CBC. The *Pipeline RAM* has a depth of 256 bits to give storage capacity of 256 clock cycles and is 128 bits wide to match the channel count. The RAM cells are of simple dual-port architecture and are not required to be immune to SEU events since loss of data can be tolerated. *Pipeline Control Logic* sequences writing and reading of data into the *Pipeline RAM*.

3.9 Data Buffer RAM

The *Data Buffer RAM* stores data from bunch crossings which have been triggered as useful. When this happens data is read from the *Pipeline RAM* and written into the buffer RAM. It has a depth of 32 bits to store 32 events awaiting readout and is 136 bits wide to match the channel count plus the pipeline address from which the data came. The RAM is of the same design as the pipeline RAM and essentially operates as a FIFO. Write and read pointers sequence data to and from the FIFO.

3.10 Data Serialiser

The data stored in the data buffer must be serialised before it can be output from the CBC. This is performed by a 140-to-1 shift register. The 140 bits include the channel data (128), the pipeline address (8), and 2 bit header plus 2 error bits.

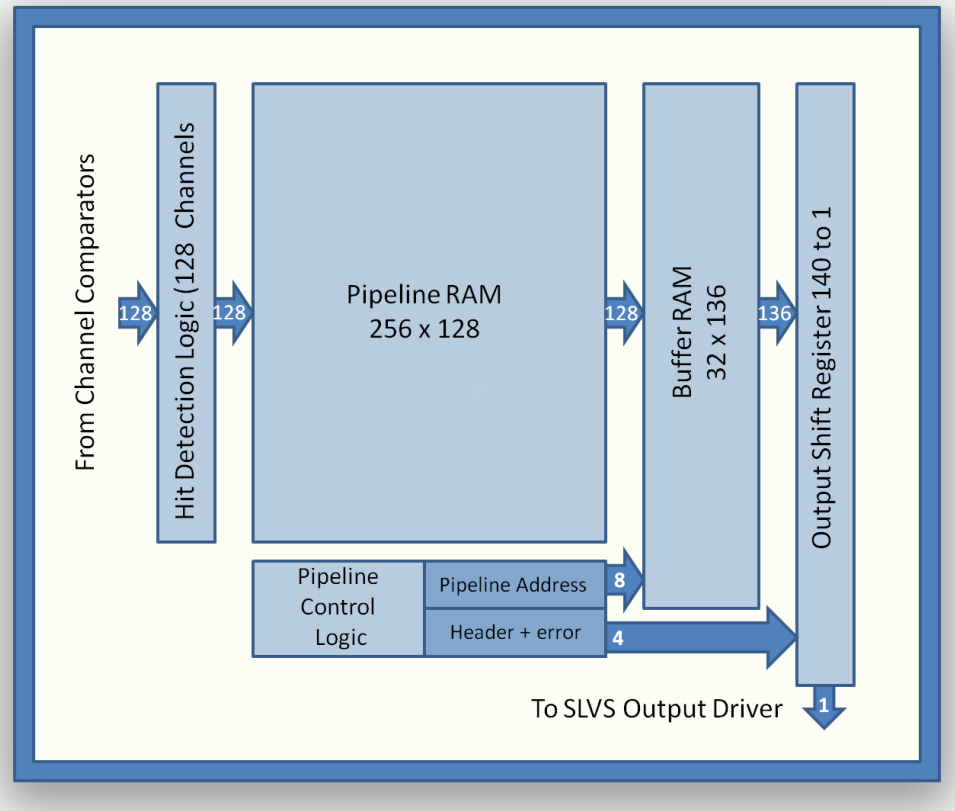

Figure 10. CBC Data Path

3.11 Pipeline Control Logic

Figure 11 shows a block diagram of the Pipeline *Control Logic*. The sequencing of data being written into the pipeline RAM is controlled by two pointers, the *write pointer*, and the *trigger pointer*. Both of these consist of counters and decoders.

When the CBC is first initialised, the *write counter* will start counting from 0. The *write decoder* will convert this count to a RAM position were the data from the front end will be written. The counter will continue counting to 255 before wrapping around to start again. Data previously written will now be overwritten.

The *trigger counter* will not start counting until a predefined latency behind the write counter. The *trigger decoder* will decode this count to point to the RAM position from where data will be read if an external trigger is received.

Pointer Start Logic is used to set the correct latency as determined by the *Latency Register*. The latency between trigger pointer and write pointer is constantly moni-

tored by a latency check circuit. If the measured latency does not match the programmed latency then an error bit is set.

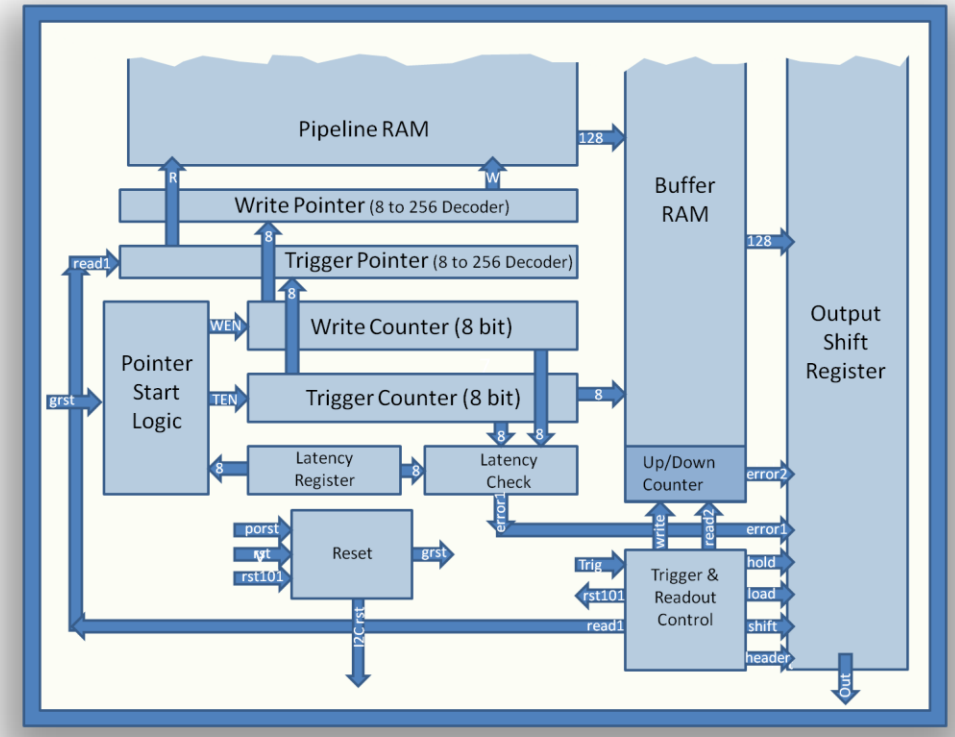

Figure 11. Pipeline Control Logic

The *Reset* circuit takes the chip input reset, the power-on-reset and the trigger decoded reset (*rst101*) and routes them to the relevant blocks. The power-on-reset and chip input rst (rst) are used to reset the I2C and I2C registers. Both of these resets are used to reset the rest of the logic, but an additional reset (*rst101*) is also used. When a *rst101*is sent it will synchronise all chips to the same clock cycle.

The *Trigger and Readout Control* block has three functions. The first function is to decode signals on the trigger input. This is explained in the next section.

Secondly it controls the transfer of data from pipeline to buffer. If a trigger signal is received then a read signal (*read1*) and a buffer write signal (*write*) are generated. These transfer the data and also the address of the pipeline into the buffer.

Thirdly, it controls transfer of data from the *Buffer RAM* to the *Output Shift Register*. It monitors whether there is any data in the *Buffer RAM*. If there is none, then it holds the shift register from loading or shifting. Once data becomes available it generates the signals for transferring the data from the *Buffer RAM* to the *Output Shift Register* (read2, load). The data is then shifted out of the register (*shift*).

A couple of error flags are used to indicate problems with the operation of the circuit. The first is set by the *Latency Check* circuit. This monitors the difference between the *Write Counter* and *Trigger Counter* and compares it to the *Latency Register*. If there is a difference, the latency error flag is set. The second error comes from the *up-down counter*. This holds the number of items stored in the *Buffer RAM* and if this reaches 32 then a FIFO full flag is set. Both of these error flags are read out in the header of each data packet.

3.12 Trigger Decoder

The *Trigger Decoder* monitors the trigger input for two encoded commands. The first command is called *RESET101* and the second command is *TRIG*. Figure xxx shows how these are encoded onto the trigger input. A RESET101 consists of two pulses each a clock cycle in length separated by one clock cycle (a). A TRIG consists of a single pulse one clock cycle long (c,d). Consecutive TRIGs will only be recognised if there is a gap of 2 clock cycles between them. The delay between the TRIG input and the TRIG output is 2 clock cycles. The circuit will then recognize the trigger a clock cycle after this.

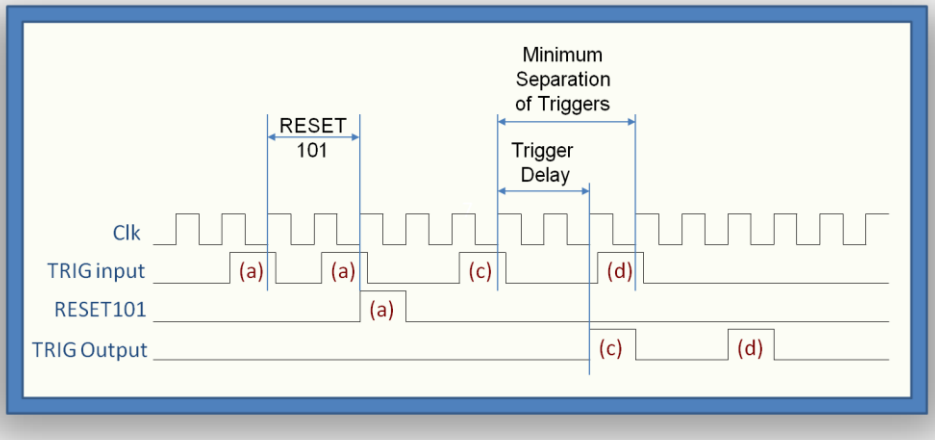

Figure 12. Trigger Decoder

3.13 Slow Control

The *Slow Control* is the interface between the external system and the control registers which set up how the CBC will operate. It is implemented in I^2C slave architecture.

Figure 13 shows a typical I^2C configuration, with one master controlling several slaves. In addition to sending and receiving data (SDA), the master also generates the clock (SCL). I^2C output drivers are open-drain, requiring pull-up resistors. The maximum value of resistor that can be used is determined by the clock frequency and total capacitance on the I^2C bus. In addition it must be remembered that for small values of resistor, the open-drain outputs will not be able to pull the signals all the way down to 0V.

Since all devices share a common bus, only one may use it at a time.

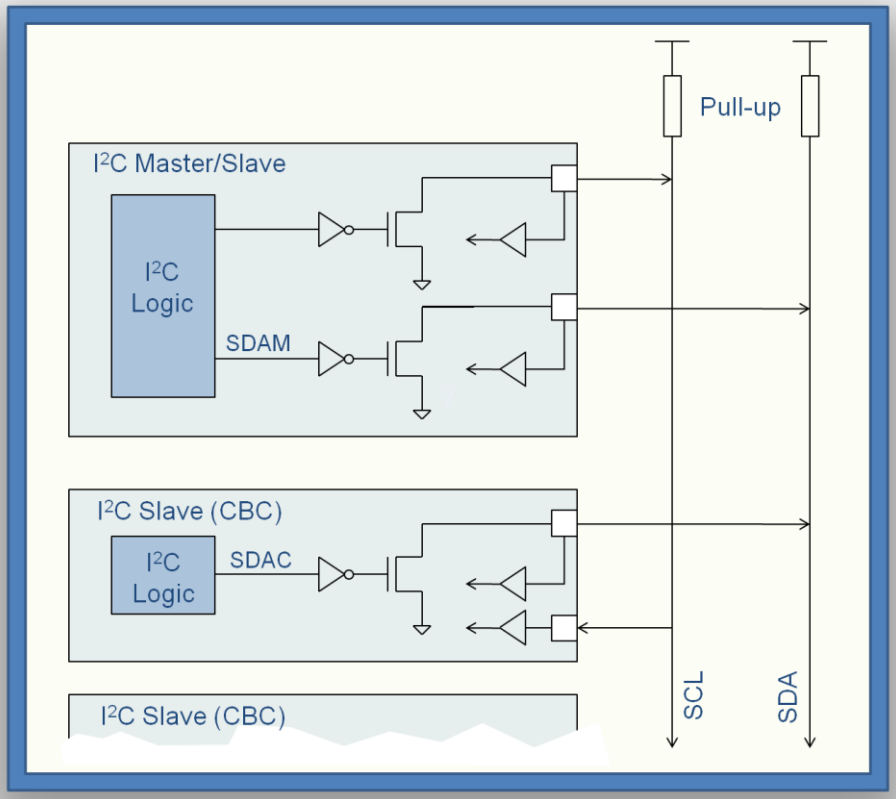

Figure 13. I2C Master/Slave Configuration

The CBC chip has 5 address inputs, which compose the 5 LSBs of the address. I^2C chip addresses must consist of 7 bits, so the remaining CBC address bits have been internally wired to "10". Therefore, when sending an I^2C command to an individual chip, the 2 most significant bits of the chip address must be set as "10". For example, to address a chip with the 5 address inputs set to "00000", the I^2C command must have a chip address of "1000000".

Figure 14 shows the signals for an I2C "write" transaction. When the I2C is inactive, both the clock and data buses are high. A transaction must start with an I2C write condition. This occurs when the data line (SDA) goes low when the clock (SCL) is high. This is initiated by the master on SDAM (using fig 13 signal names). During this time the slave is inactive (SDAC). All data must then change only when the clock is low.

The master sends the address of the slave it wants to communicate with, which in this case is 1000001, followed by a "0" which indicates it wants to write information to the slave. It then releases SDA by taking SDAM high and the slave acknowledges receipt of the address by taking SDAC (and hence SDA) low.

The master then sends the address of the register it wants to write to (in this case 00000001), and the slave acknowledges. The last piece of information is the data that is to be written into the register (00001110). The slave acknowledges, and the master sends the I2C stop condition (SDA goes high when clock is high).

Every register on any chip can be written to in this way by supplying the relevant chip and register address. The chip address "1111111" is reserved for addressing all chips connected to the same bus at the same time.

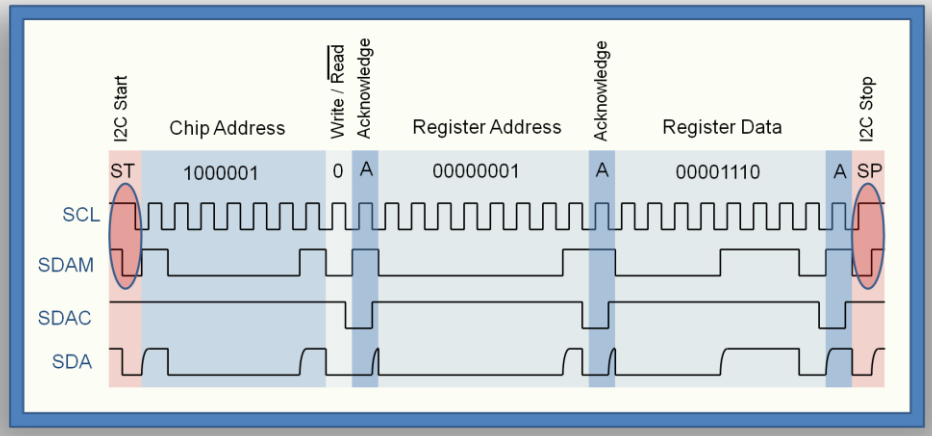

Figure 14. I2C Write Transaction

Figure 15 shows the format for read from a register as well as writing to it. As the write operation has already been described this section will deal with the read transaction.

To begin a read transaction, the register on the chip you want to read from has to be addressed. This is done by firstly sending a start condition and addressing the chip with the write/read bit set to 0 (write mode). Then the register that is to be read is addressed and a stop condition is sent. This has set up the internal I^2C interface to address the relevant register.

Secondly, beginning with a start condition, the chip has to be addressed for a second time, but in this case, the write/read bit is set to 1 to indicate a read transaction. The register data is then loaded onto an internal bus, the master releases the SDA bus and the slave, detecting a read condition, outputs the register data over the SDA bus. The slave releases the bus, and the master acknowledges.

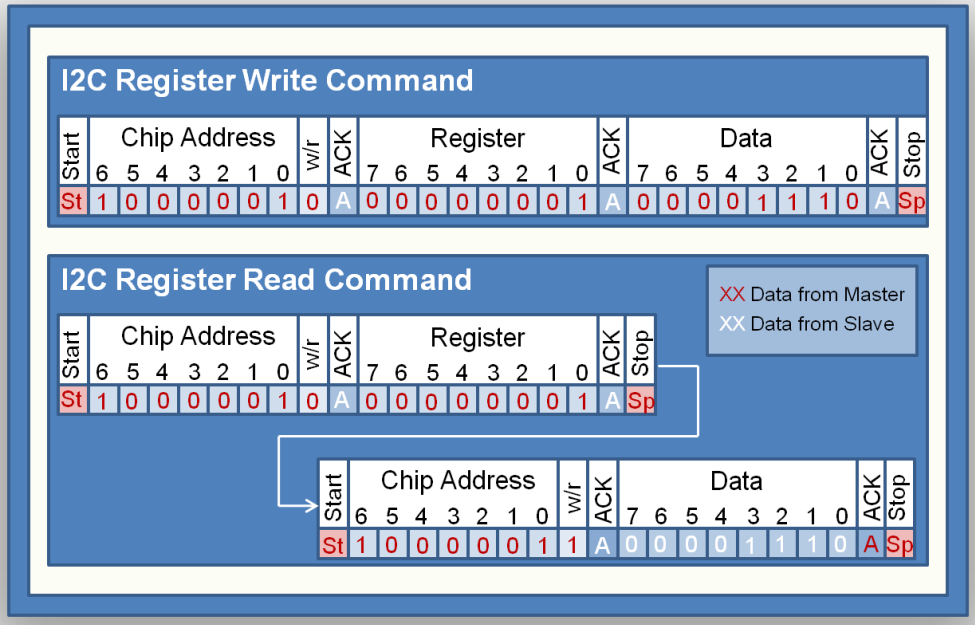

Figure 15. I2C Write/Read Transaction

All control register are written to and read from using the I2C interface. The next sections list all available control registers.

3.14 Control Registers

The control registers define how the CBS will operate. On start-up all registers will reset to default values. Tables 1,2,3 list chip control registers. Table 4 lists the channel offset registers and table 5 lists the control registers in the Bias Generator.

Table 1: Front End Control (I2C Register Address 00000000)

Bit	Function	Default
7	Not Used	0
6	Comparator Polarity (0=holes, 1=electrons)	0
5	Comparator Hysteresis Bit 3	1
4	Comparator Hysteresis Bit 2	1
3	Comparator Hysteresis Bit 1	1
2	Comparator Hysteresis Bit 0	1
1	Postamp Polarity (0=holes, 1=electrons)	0
0	Preamp Polarity (0=holes, 1=electrons)	0

Table 1shows front end control bits. The polarity of the signal is set by bits 0,1 & 6. For electron polarity these are set to 1, for holes these are set to 0. The comparator hysteresis is set using bits 2-5. Maximum hysteresis occurs when all four bits are set to 1.

The defaults settings for the front end control register are for holes polarity and for maximum hysteresis. The register address is 00000000.

Table 2: Trigger Latency (I2C Register Address 00000001)

Bit	Function	Default
7	Trigger Latency Bit 7	1
6	Trigger Latency Bit 6	1
5	Trigger Latency Bit 5	0
4	Trigger Latency Bit 4	0
3	Trigger Latency Bit 3	1
2	Trigger Latency Bit 2	0
1	Trigger Latency Bit 1	0
0	Trigger Latency Bit 0	0

Table 2 shows the the trigger latency register. This defines the pipeline separation in clock cycles between the write and trigger pointers. The default value on power up is 200 clocks. The register address is 00000001

Table 3: Hit Detect & SLVS (I2C Register Address 00000010)

Bit	Function	Default
7	Not used	0
6	Hit Detect Mode (0=single, 1=variable)	0
5	Hit Detect Enable (0=OFF, 1=ON)	1
4	SLVS Off (0=ON, 1=OFF	0
3	SLVS Current Bit3	1
2	SLVS Current Bit2	0
1	SLVS Current Bit 1	0
0	SLVS Current Bit 0	0

Table 3 Shows the Hit Detect and SLVS control register. The hit detect modes are controlled by bits 5 and 6. Bit 6 controls the mode of operation – whether it outputs a pulse of a single clock cycle or a pulse of variable length. The default is 0 which is for a single pulse. Bit enable/disables the hit detect logic. The default value is 1 which is ON.

Bit 4 is the disable for the SLVS receiver circuit. The default is 0, which is ON. Bits 0-3 control the current to the SLVS transmitter. The bits are active low which means the minimum current (0mA) is set by "1111". The default value is for a current of 2mA and the maximum setting "0000" gives a current of about 2.5mA. The address of this register is 00000010

Table 4. Channel Offset Registers

Channel	I2C Address	Default
0	10000000	10000000
1	10000001	10000000
5	10000010	10000000
etc	etc	10000000
125	11111101	10000000
126	11111110	10000000
127	11111111	10000000
Dummy	11111111	10000000

Table 4 shows the channel offset registers. The values written into these registers control the amount of offset on the output of the postamplifiers. Values of 00000000 give 0V offset . The maximum offset is given by a setting of 11111111. The default setting is for a mid-range offset. The register addresses are 10000000 to 11111111.

With default bias settings, the offset range is 0-200mV with the default set to 100mV. However this range can be programmed by changing the Ipaos bias setting (see Bias Generator).

3.16 Bias Generator

The *bias generator* provides all of the bias currents and voltages necessary for operation of the front end analogue circuitry. Each current and voltage is set by loading a control register as listed in table 5. The digital output from these registers is then converted into the relevant bias by a multichannel DAC.

Table 5. Bias Generator Registers

Name	Function	Nominal	Range	I2C Address
Ipre1	Preamp Input Branch Bias Current	90uA	0-255uA	00000011
Ipre2	Preamp Cascode Branch Bias Current	10uA	0-51uA	00000100
Ipsf	Preamp Source Follower Bias Current	25uA	0-51uA	00000101
Ipa	Postamp Bias Current	20uA	0-51uA	00000110
Ipaos	Postamp Offset Adjust Bias Current	4uA	0-12.7uA	00000111
Ifpa	Postamp Feedback Bias Current	2.5uA	0-25.5uA	00001000
Icomp	Comparator Bias Current	2uA	0-12.7uA	00001001
Vpc	Preamp Cascode Bias Voltage	0.4V	0.2-0.8V	00001010
Vplus	Postamp Bias Voltage	0.6V	0.2-0.8V	00001011
VCth	Comparator Threshold Voltage	0.6V	0.2-0.8V	00001100

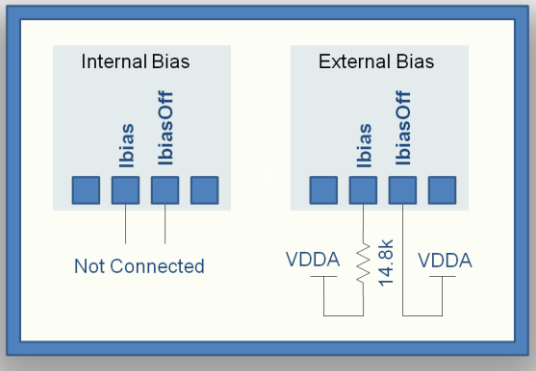

Figure 16. Bias pad configs.

The bias generator is requires a master reference current. This can be supplied in two ways. Firstly an internal current reference can be used to set the current. Secondly an external resistor connected to VDD can be used. The resistance must be such to supply 64uA so should be of the order of 14.8k.

Figure 16 shows the pad configuration for both modes of operation.

3.15 LDO Voltage Regulator

An LDO Voltage Regulator is included on chip as an independent block. All connections to the rest of the ASIC must be applied externally. The Input to the LDO should be 1.2V and can be the same supply as to the digital circuitry (VDDD). The output from the LDO can be connected to VDDA to supply the analogue circuitry. External capacitance must be added to the output to avoid oscillation.

3.16 SLVS I/O

The fast control and chip output use SLVS I/O (Scalable Low Voltage Signalling). The transmitter has programmable current with default setting of 2mA. With 100Ω termination at the receiving end this gives a differential voltage of 200mV centred on about 1.25V (figure 17).

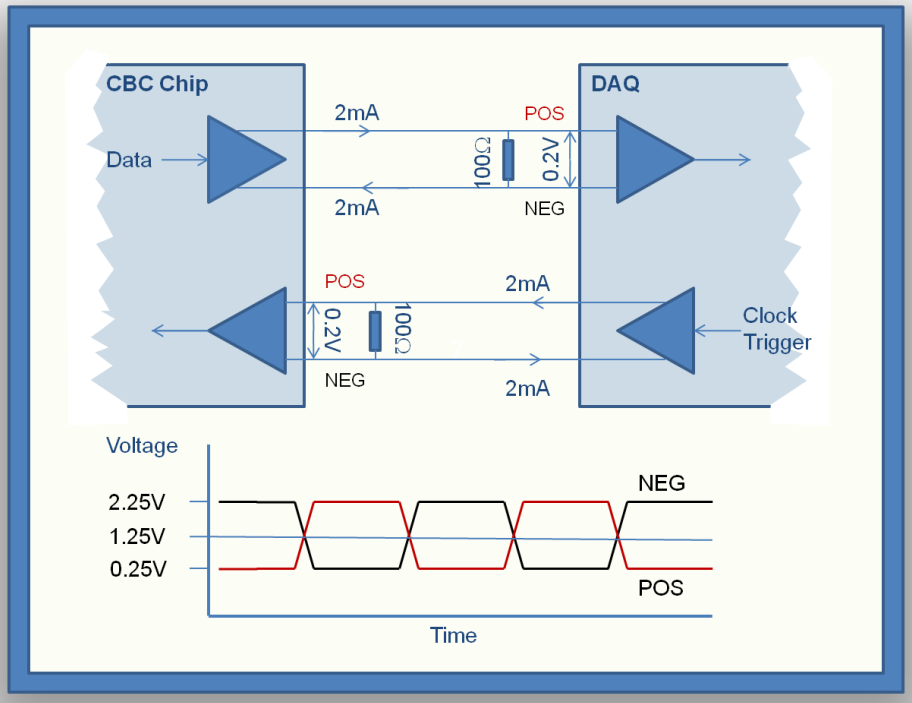

Figure 17. SLVS Data Format.

3.17 DC-DC Converter

A *DC-DC converter* has been placed as a completely independent block on the ASIC. This block can be used to generate The1.25V supply from a 2.5V supply. There are no connections to the rest of the ASIC on the chip. All connections will have to be made externally.

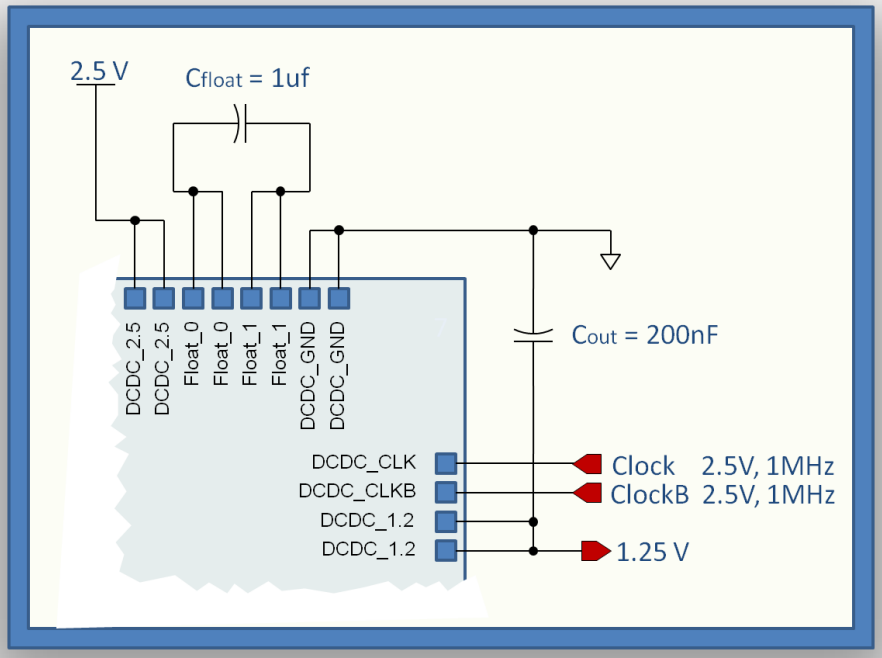

Figure 18. Connections for DC-DC Converter.

The *DC-DC Converter* should be connected as shown in figure 17. A 1uF capacitor (Cfloat) is connected between pads *Float_0* and *Float_1*. A 200nF capacitor (Cout) is connected between the output (1.25V) and ground. The circuit is clocked using the *Clock* input, a 2.5V signal running at 1MHz. Since the clock signal may cause interference to the front end of the chip by charge injection through stray capacitance, a dummy clock signal (*ClockB*) is provided for balance.

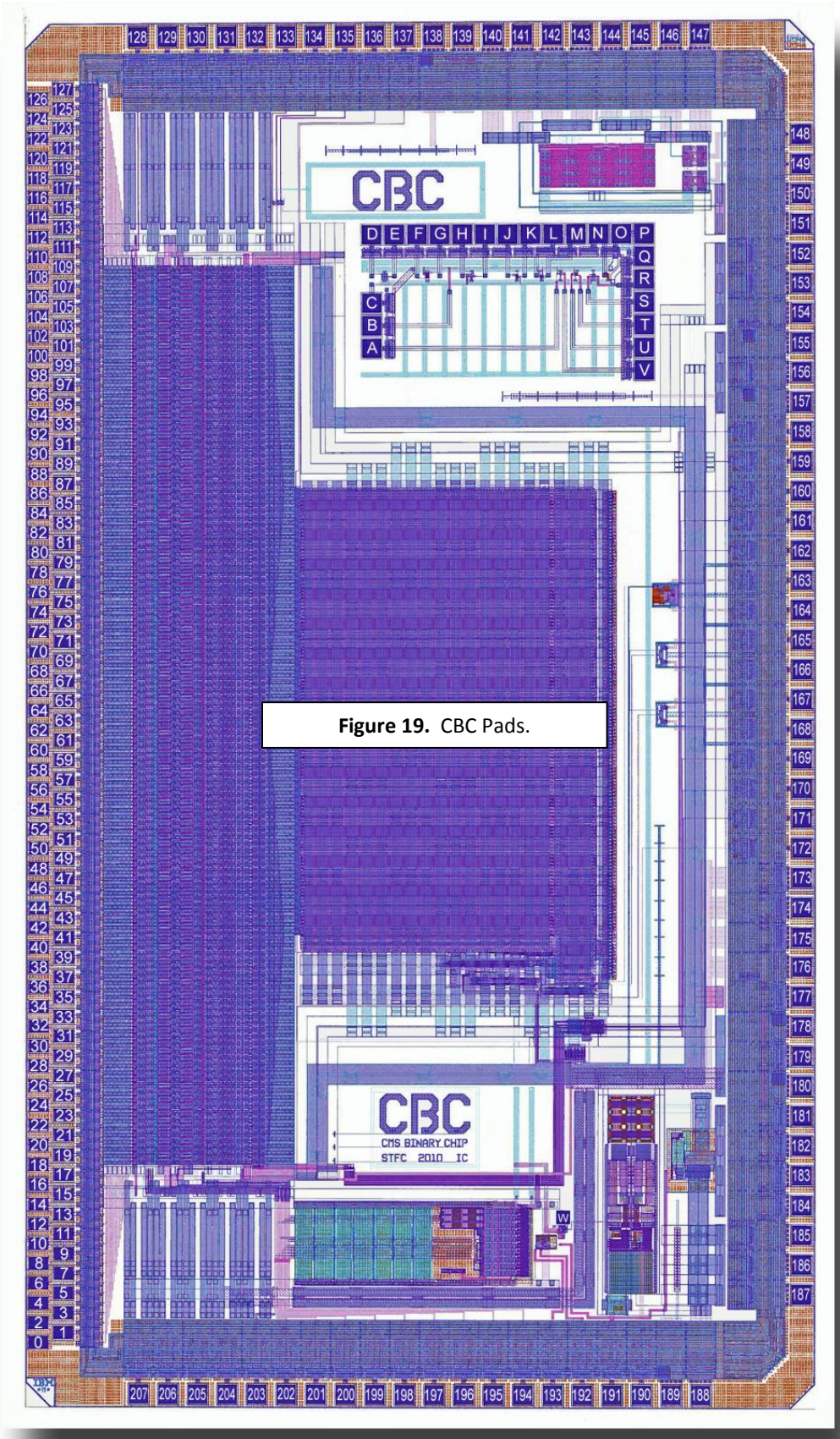

Figure 19. CBC Pads.

4. CBC Input/Output Pads

Figure 18 shows the position of the pads on the CBC chip. The following tables list the functions of each pad.

Table6: Top Pads

Pad	Name	Type	Function
128	DummyIn	Analogue	Dummy Channel Preamp Input
129	Cal4	Analogue	Calibrate Capacitor No. 4 Input
130	Cal5	Analogue	Calibrate Capacitor No. 5 Input
131	Cal6	Analogue	Calibrate Capacitor No. 6 Input
132	Cal7	Analogue	Calibrate Capacitor No. 7 Input
133	PreAmp	Analogue	Dummy Channel Preamp Output
134	PostAmp1	Analogue	Dummy Channel Postamp Output 1
135	PostAmp2	Analogue	Dummy Channel Postamp Output 2
136	Comp	Digital	Dummy Channel Comparator Output
137	HitDet	Digital	Dummy Channel Hit Detect Output
138	VDDA1	Supply	1.1V – 1.2V Analogue Supply
139	GNDA	Supply	Analogue Ground
140	DCDC2_5	Supply	2.5 V DC-DC Converter Supply
141	DCDC2_5	Supply	2.5 V DC-DC Converter Supply
142	Float_0	Analogue	DC-DC Converter External Capacitor 0
143	Float_0	Analogue	DC-DC Converter External Capacitor 0
144	Float_1	Analogue	DC-DC Converter External Capacitor 1
145	Float_1	Analogue	DC-DC Converter External Capacitor 1
146	DCDC_GND	Supply	DC-DC Converter Ground
147	DCDC_GND	Supply	DC-DC Converter Ground

Table 7: Bottom Pads

Pad	Name	Type	Function
188	GNDA	Supply	1.1V – 1.2V Analogue Supply
189	VDDA1	Supply	Analogue Ground
190	BGO	Bias Output	Band Gap Output
191	BGI	Bias Input	Bias to Current Reference (Short to BGO)
192	IbiasOff	Digital	0V for internal bias or 1.2V for external
193	Ibias	Bias Input	External Current Bias if IbiasOff=1.2V
194	VCth	Bias Output	Comparator Threshold Bias Monitor Point
195	ICOMP	Bias Output	Comparator Bias
196	IPAOS	Bias Output	Postamp Offset Adjust Monitor Point
197	VPLUS	Bias Output	Postamp Output Level Monitor Point
198	IPA	Bias Output	Postamp Bias Monitor Monitor Point
199	IPSF	Bias Output	Preamp Source Follower Monitor Point
200	IFPA	Bias Output	Postamp Feedback Monitor Point
201	VPC	Bias Output	Preamp Cascode Voltage Monitor Point
202	IPRE2	Bias Output	Preamp Cascode Branch Monitor Point
203	IPRE1	Bias Output	Preamp Input Branch Monitor Point
204	Cal3	Analogue	Calibrate Capacitor No. 3 Input
205	Cal2	Analogue	Calibrate Capacitor No. 2 Input
206	Cal1	Analogue	Calibrate Capacitor No. 1 Input
207	Cal0	Analogue	Calibrate Capacitor No. 0 Input

Table 8: Backend Pads

Pad	Name	Type	Function
148	DCDC_CLK	2.5V Digital	DC-DC Converter Clock Input
149	DCDC_CLKB	2.5V Digital	DC-DC Converter ClockB Input (Dummy)
150	DCDC1_2	Supply	DC-DC Converter Output (1.2V)
151	DCDC1_2	Supply	DC-DC Converter Output (1.2V)
152	GNDD	Supply	Digital Ground
153	GNDD	Supply	Digital Ground
154	GNDD	Supply	Digital Ground
155	VDDD	Supply	1.2V Digital Supply
156	VDDD	Supply	1.2V Digital Supply
157	VDDD	Supply	1.2V Digital Supply
158	ADD4	1.2V Digital	Chip Address 4
159	ADD3	1.2V Digital	Chip Address 3
160	ADD2	1.2V Digital	Chip Address 2
161	ADD1	1.2V Digital	Chip Address 1
162	ADD0	1.2V Digital	Chip Address 0
163	DATA+	SLVS Digital	Positive Data Output
164	DATA-	SLVS Digital	Negative Data Output
165	CLK+	SLVS Digital	Positive Clock Input
166	CLK-	SLVS Digital	Negative Clock Input
167	TRG+	SLVS Digital	Positive Trigger Input
168	TRG-	SLVS Digital	Negative Trigger Input
169	SCLK	1.2V Digital	I2C Clock Input
170	SDAOUT	Open Drain	I2C Data Output
171	SDAIN	1.2V Digital	I2C Data Input
172	RST	1.2V Digital	Chip Reset
173	GNDA	Supply	Analogue Ground
174	GNDA	Supply	Analogue Ground
175	GNDA	Supply	Analogue Ground
176	GNDA	Supply	Analogue Ground
177	VDDA2	Supply	1.1V – 1.2V Analogue Supply (Comparator)

178	VDDA1	Supply	1.1V – 1.2V Analogue Supply
179	VDDA1	Supply	1.1V – 1.2V Analogue Supply
180	VDDA1	Supply	1.1V – 1.2V Analogue Supply
181	VLDOO	Supply	1.1V LDO Output
182	VLDOO	Supply	1.1V LDO Output
183	VLDOO	Supply	1.1V LDO Output
184	VLDOO	Supply	1.1V LDO Output
185	VLDOI	Supply	1.2V LDO Input
186	VLDOI	Supply	1.2V LDO Input
187	VLDOI	Supply	1.2V LDO Input

Table 9: Frontend Pads

Pad	Name	Type	Function
0	IN0	Analogue	Input 0
1	IN1	Analogue	Input 1
2	IN2	Analogue	Input 2
.	.	.	.
.	.	.	.
125	IN125	Analague	Input 125
126	IN126	Analogue	Input 126
127	IN127	Analogue	Input 127

5. CBC Test Transistors

There is a block of test transistors and one test resistor on the CBC chip. The pads are labelled A to V. Table 10 lists the transistor/resistor sizes and their terminal connections.

Table 10

	Type	Size	Gate	Drain	Source	Bulk
1	N	400/0.36	D	E	Q	C
2	P	400/0.36	G	F	O	B
3	N	25/0.25	I	H	Q	C
4	N	25/0.5	J	K	Q	C
5	P	25/0.25	M	L	O	B
6	P	1/5	V	A	O	B
7	N	10/1	S	R	Q	C
8	P	10/1	U	T	O	B
	RES	200k	-	N	Q	-

6. Data Output Format

The data from the CBC is purely digital and will be output at the clock frequency (40MHz). The data will consist of a digital header (2 logic 1 bits), 2 error bits, the pipeline address (8 bits), and the data from all 128 channels (figure 7). The full data stream is therefore 140 bits in length.

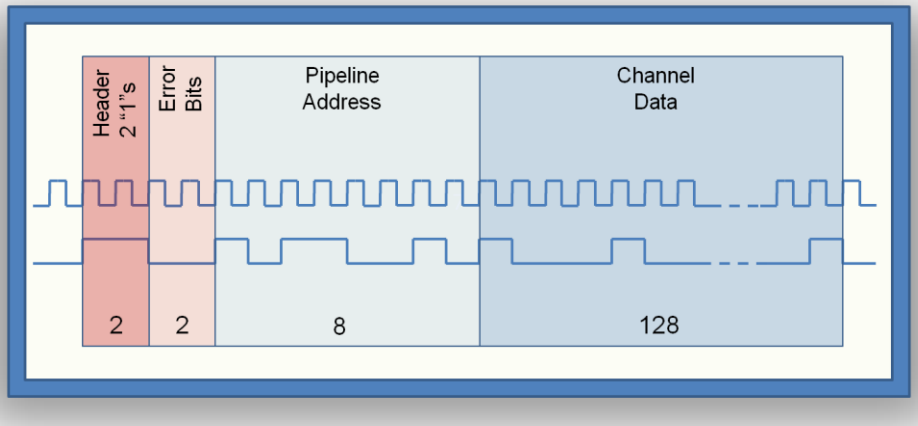

Figure 20. Data Format

The timing between the first trigger being received and the first data packet is shown in figure 20. There is a 7 clock cycle delay between the external trigger signal and the data being output.

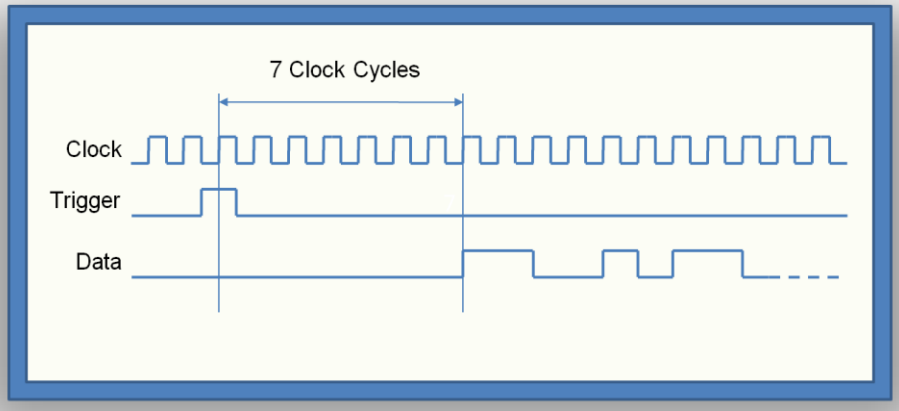

Figure 21. Data Timing

When multiple triggers occur there is a 4 clock cycle gap between consecutive data packets (figure 21).

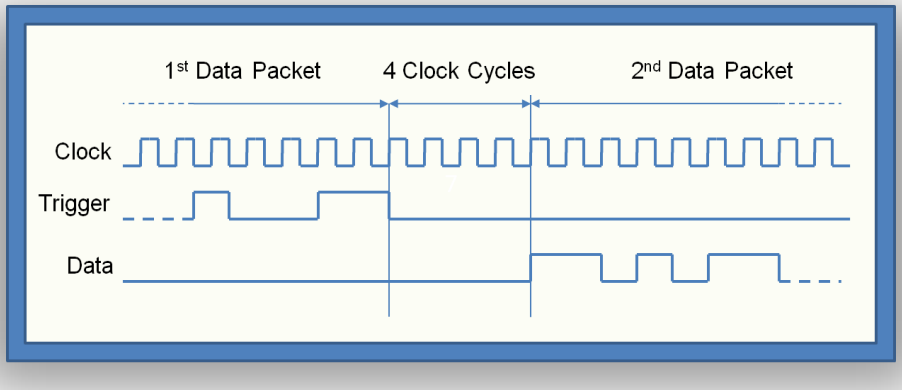

Figure 22. Consecutive Data Timing

6. Test Pulse Circuit

There are 8 on-chip capacitors which can be used to inject charge into the front end of the CBC chip. These capacitor connect to the chip inputs Cal0, Cal1, Cal2, Cal3, Cal4, Cal5, Cal6, and Cal7. Each capacitor is connected to 16 channels. The connection order is::

Cal0: 0,8,16,24.32.....etc
Cal1: 1,9,17,25,33.....
Cal2: 2,10,18,26,34.....
Cal3: 3,11,19,27,35.....
Cal4: 4,12,20,28,36.....
Cal5: 5,13,21,29,37.....
Cal6: 6,14,22,30,38.....
Cal7: 7,15,23,31,39.....

The capacitance is about 15fF.

For your notes: