CBC preliminary specifications

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These specifications relate to a binary, non-sparsified architecture. They should be considered as a target, and will change as the chip design evolves, in response to feedback from the CMS tracker community, and as we gain a better understanding of what is realistically achievable. The chip will be fabricated in 130 nm CMOS.

Change log	
March 2009	Preliminary version

Sensor-related specifications

Signal polarity

Negative – consistent with n-in-p type sensor elements. Signal and leakage currents flow out of amplifier

Coupling to amplifier

AC or DC.

DC leakage magnitude

The amplifier must tolerate a leakage current of up to 1 μA. Note that this will correspond to ~ 0.5 mW dissipated per sensor element – approximately the same as the target amplifier power consumption / channel - see below.

Strip pitch

For multiple chip readout the sensor strip pitch should not be less than 60 microns.

Amplifier noise

Less than 1000e for C_{SENSOR} up to 5 pF

Front end amplifier and comparator

Gain

The target gain referred to the comparator input will be 50 mV / fC

Amplifier noise

Less than 1000e for C_{SENSOR} up to 5 pF

Leakage current noise

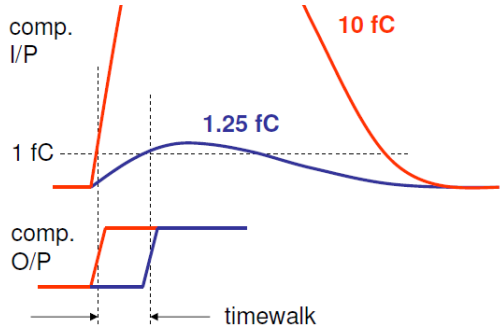
The pulse shaping should be chosen such that the corresponding noise contribution will be less than 500e for a leakage current up to 1 μA.

Pulse shaping

The amplifier rise-time should be ~ 20 ns and its performance, together with the following comparator and the sensor charge collection time, should be consistent with the time-walk specification below.

Time-walk

$\leq$ 16 ns. Time-walk defined as the maximum time difference between the comparator digital output signals (at 0.5 VDDD) corresponding to 1.25 fC and 10 fC, for a comparator threshold of 1 fC (see figure). This specification is based on the Atlas ABCD3T [Atlas ABCD3T ref].



Comparator threshold trim

There will be a global comparator threshold to all channels with an individual channel 4-bit trim DAC. The LSB will be 5 mV (equivalent to 625 electrons) allowing an overall adjustment range of 80 mV.

Overload recovery

An individual channel should respond to normal size signals < 2.5 µs following a hip-type signal of up to 4 pC.

Pipeline, buffering and logic

Pipeline

Pipeline depth (latency) should be programmable up to 256 clock cycles (6.4 µsec at 40 MHz).

Buffering

The chips should be able to buffer data from up to 32 triggers awaiting readout

SEU immunity

Critical parts of the chip, where upsets would cause the chip operation to “crash” or its operational state to be changed (e.g. bias generator registers), must be designed for SEU immunity.

External electrical interfaces

Fast (CK/T1)

Electrical spec. to be defined

Slow control

Electrical spec and protocol to be defined

Power

Power supplies

1.2 V analogue (VDDA). Up to 1.2 V digital (VDDD). VDDA and VDDD to be kept separate on chip to allow the digital parts to be run at lower voltage to save power.

Power consumption

Target power consumption is 0.5 mW / channel (64 mW per 128 channel chip) for a sensor capacitance of 5 pF. This breaks down into 200 μW for the front end (amplifier + comparator) with 300 μW for the digital functionality.

Power supply rejection

Care will be taken to achieve as good a performance as possible here, but note that a single ended input stage is required to achieve the target power consumption. Some rejection at all frequencies would be desirable, but it is possible that this can only be achieved by externally filtering the analogue supply voltage with passive (RC) components.

Miscellaneous

Bonding technology

It is assumed that the first prototype chip will be designed for wire-bonding.

References

Atlas ABCD3T ref: ABCD3T Chip Specification Version V1.2, July 24, 2000.