CMS Binary Chip specifications

CBC – 130 nm readout chip for short strips in CMS SLHC outer tracker

OUTLINE

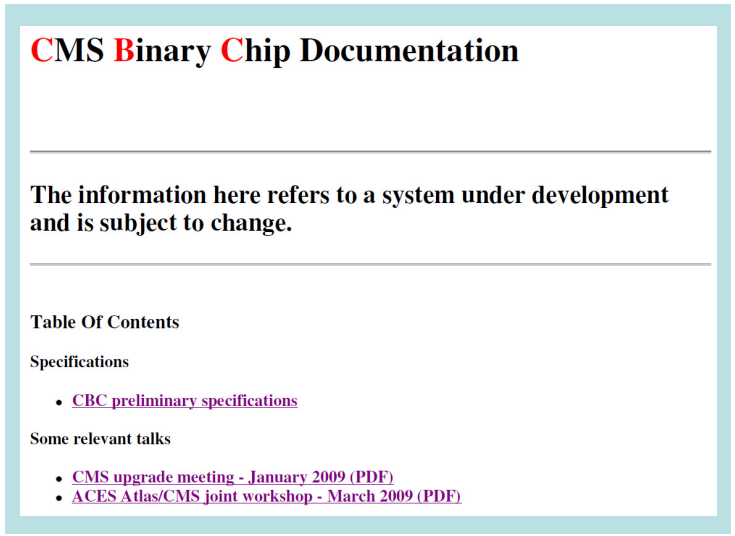
intro
specifications
- sensor related
- front end – amplifier & comparator
- digital – pipeline & interfaces
- noise & power

summary

design has begun – but still open to change

CBC related documentation (including preliminary specification doc.) can be found at:

http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation



Mark Raymond, Imperial College
tracker upgrade meeting – 24th April, 2009

introduction

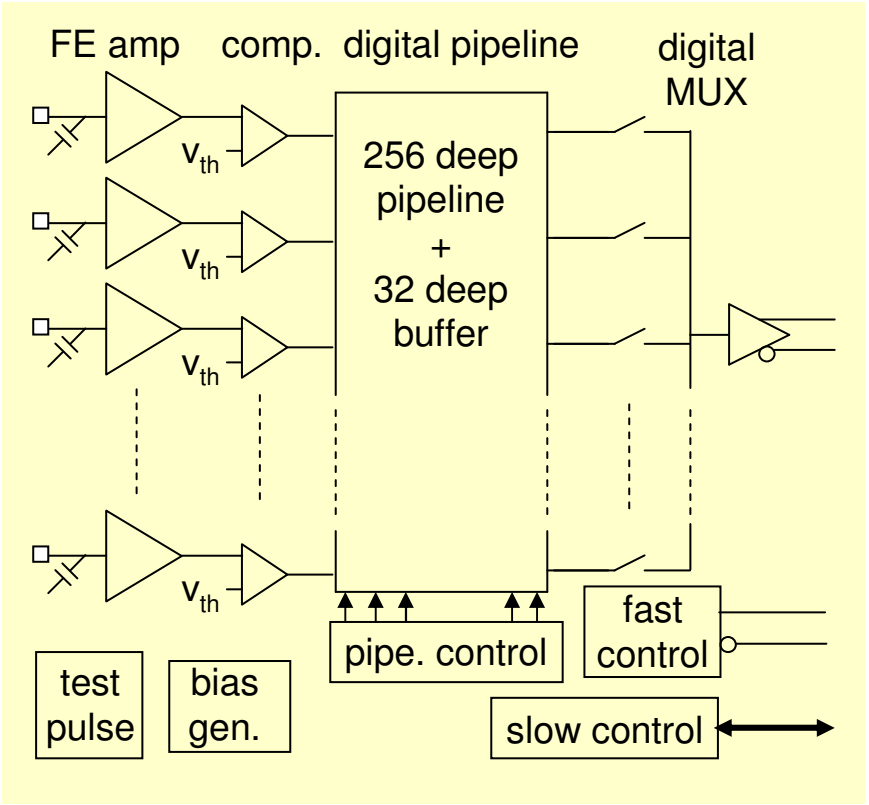
plan to submit prototype 130nm chip on timescale ~ 1yr

binary unsparsified architecture chosen

see previous talks* for reasons
(e.g. TWEPP'08, Jan'09 Tracker Upgrade, ACES'09 (March))

main functional blocks
- fast front end amplifier
- comparator with threshold trim
- pipeline
- buffer for triggered events
- output mux and driver
- fast and slow control interfaces
- programmable bias
- test pulse

CBC



sensor related specs (1)

Signal polarity

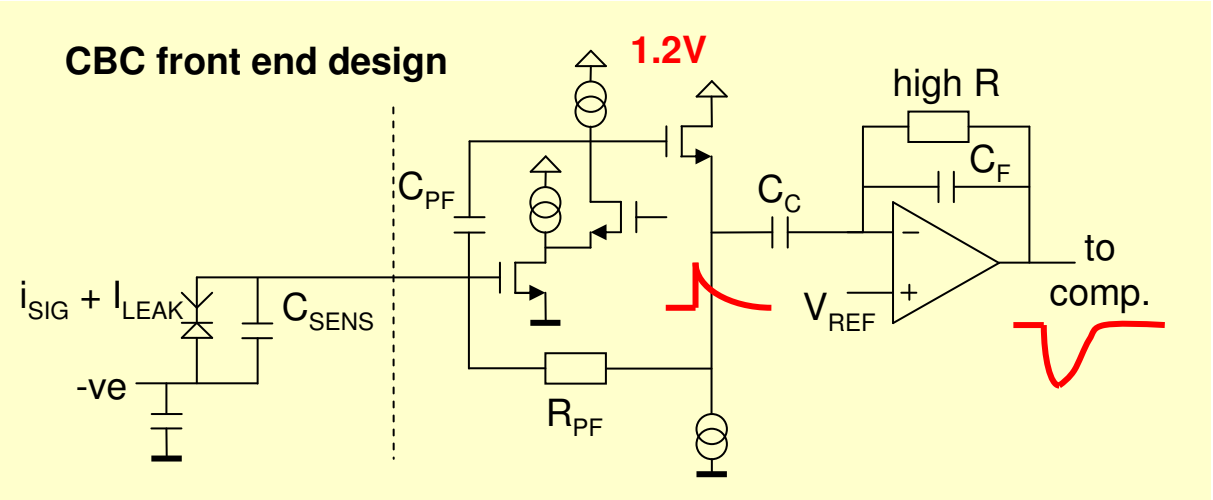
negative – consistent with n-in-p type sensor elements.
signal and leakage currents flow out of amplifier
may still be possible to accommodate both polarities with one design?
highly desirable – not necessary to commit to sensor polarity
(if not then alternative front end required (=> different chip))

Coupling to amplifier

DC assumed (if works for DC then will work for AC as well)

DC leakage magnitude

the amplifier must tolerate a leakage current of up to 1 μA.
note: this corresponds to ~ 0.5 mW dissipated per sensor element
(approximately the same as the target amplifier power consumption / channel)



sensor related specs (2)

Charge collection time

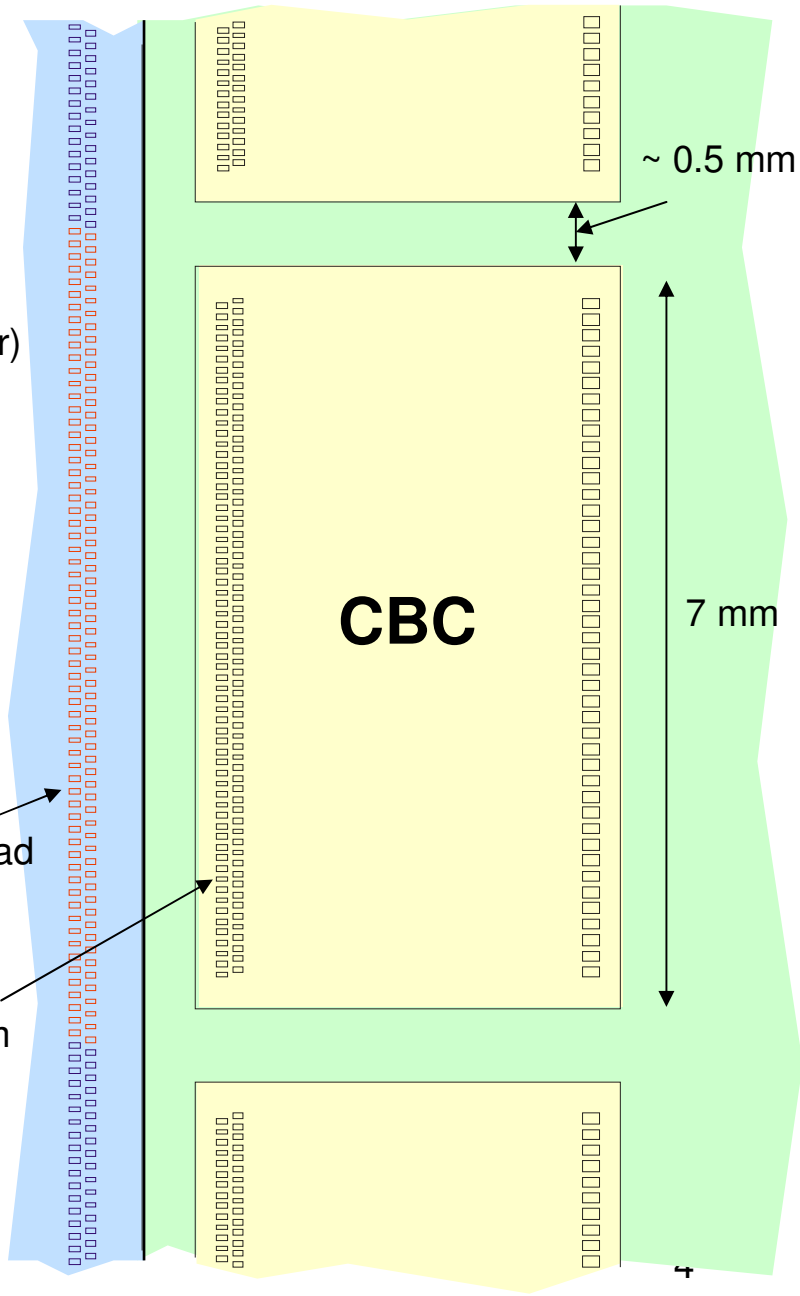
< 10 ns
determines effective pulse shape at amplifier output
has implications for time-walk at comparator O/P (see later)
value originates from Atlas spec.*

Strip pitch

for multiple chip readout the sensor strip pitch should not be less than ~ 60 microns

allows slightly relaxed pad pitch on CBC (c.f. APV) and reasonable gap between chips

(assumes 128 channel chip)



*ABCD3T Chip Specification Version V1.2, July 24, 2000

Front end amplifier and comparator (1)

Pulse shaping

need fast pulse for binary front end – hit must be registered in correct bunch crossing

again use Atlas binary FE spec. for guidelines

20 ns peaking time for pulse at comparator I/P

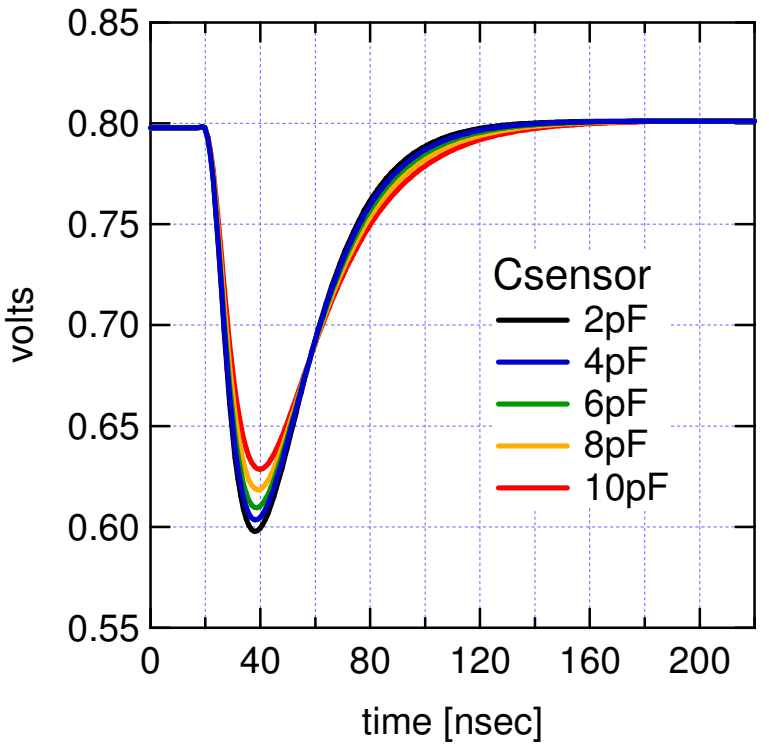
simulations show achievable in 130 nm design for range of sensor capacitances if allow to vary preamp power

e.g. ~ 200 μW for mid-range value C_{SENSOR} = 5 pF

more or less for higher or lower capacitances

(for 2 pF (10 pF): FE amp power ~170 (260) μW)

pulse shapes for 4 fC input charge (~ 45 mV / fC)



preamp risetime ∝ C_{SENSOR}/g_m (∝ C_{SENSOR}/I_{DS})

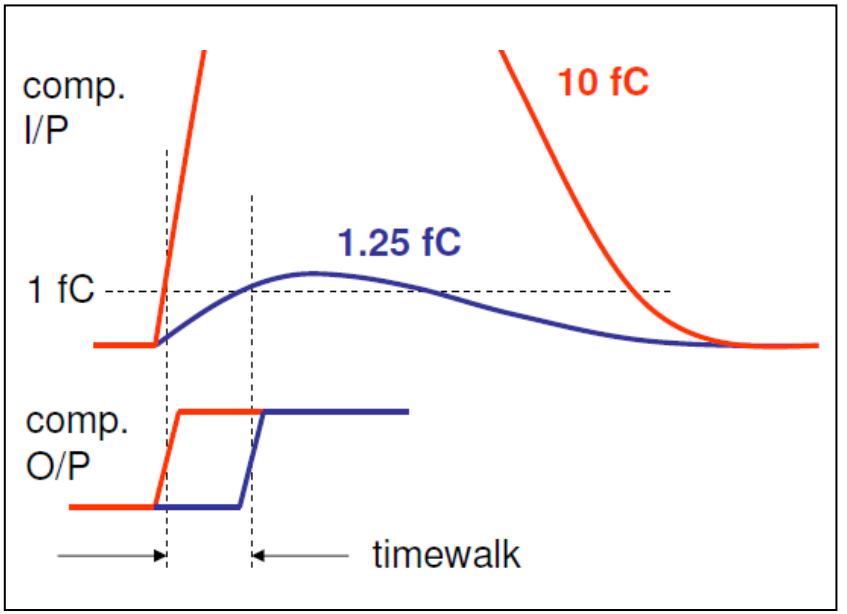
=> power scales linearly with C_{SENSOR} if want to keep risetime constant

Front end amplifier and comparator (2)

time-walk

dependence of comparator fire time on signal size must be less than 1 BX
once again taking Atlas spec.

≤ 16 ns time difference between comparator output edges for input signals of 1.25 fC and 10 fC, for a threshold setting of 1 fC



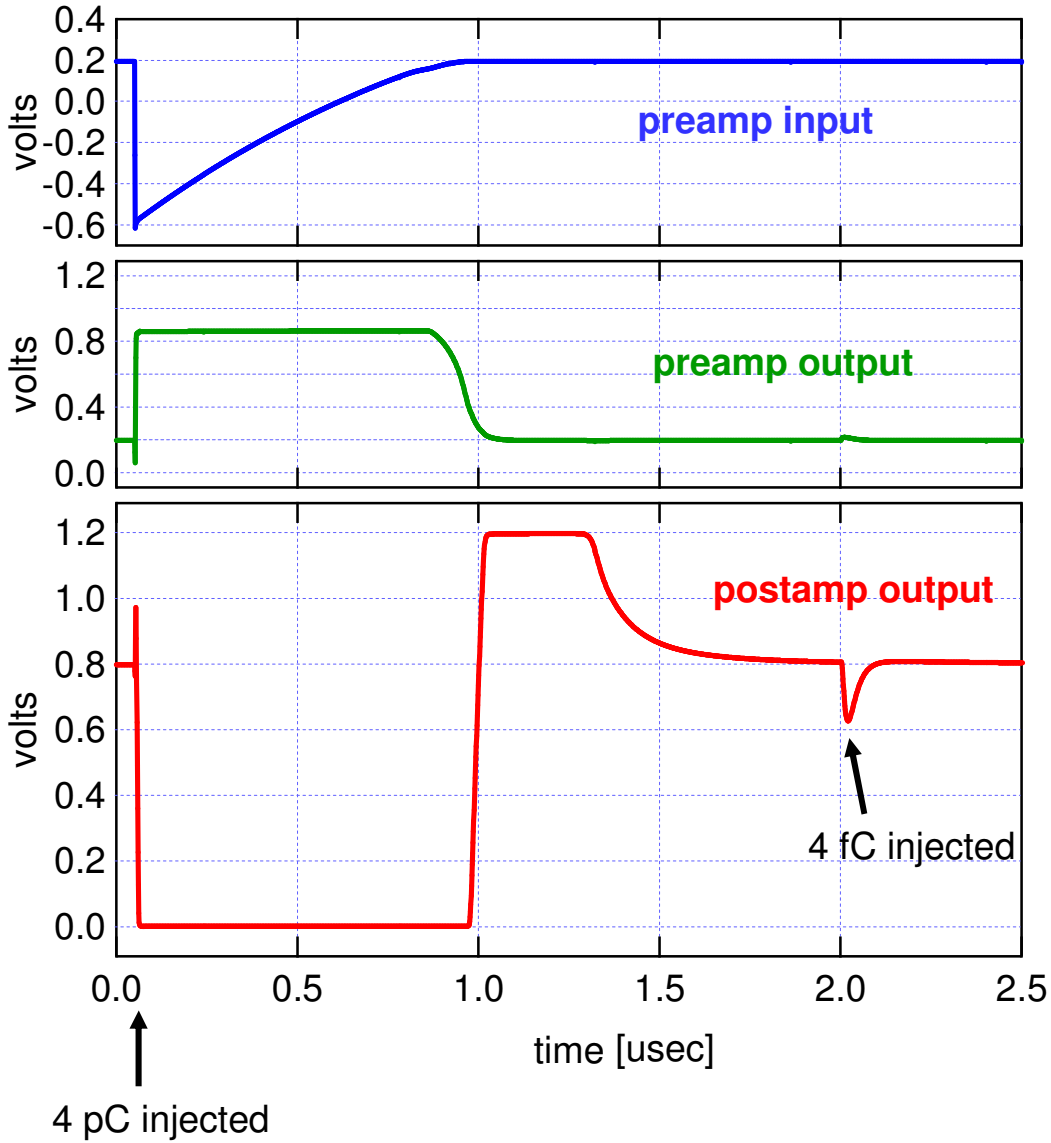
probably a good starting point

should keep under review if other threshold settings are considered (spec. defined for 300 μm sensors)

need pipeline interface logic

some **hit pulse detection** logic needed to ensure only one hit in pipeline (comp. O/P stays above threshold for more than one BX)

overload recovery



overload behaviour well-controlled in present design

(beneficial effect of low value preamp feedback resistor used to accommodate leakage current)

front end recovers from 4 pC signal and sensitive to normal signals within 2.5 μs

=> make this the spec.

An individual channel should respond to normal size signals < 2.5 μs following a hip-type signal of up to 4 pC

NOISE

hard to define a simple specification

noise/power/C_{SENSOR} are interrelated

amplifier noise

below 1000e for C_{SENSOR} ~ 5 pF
seems achievable

leakage current noise ~ $\sqrt{I_{LEAK}}$

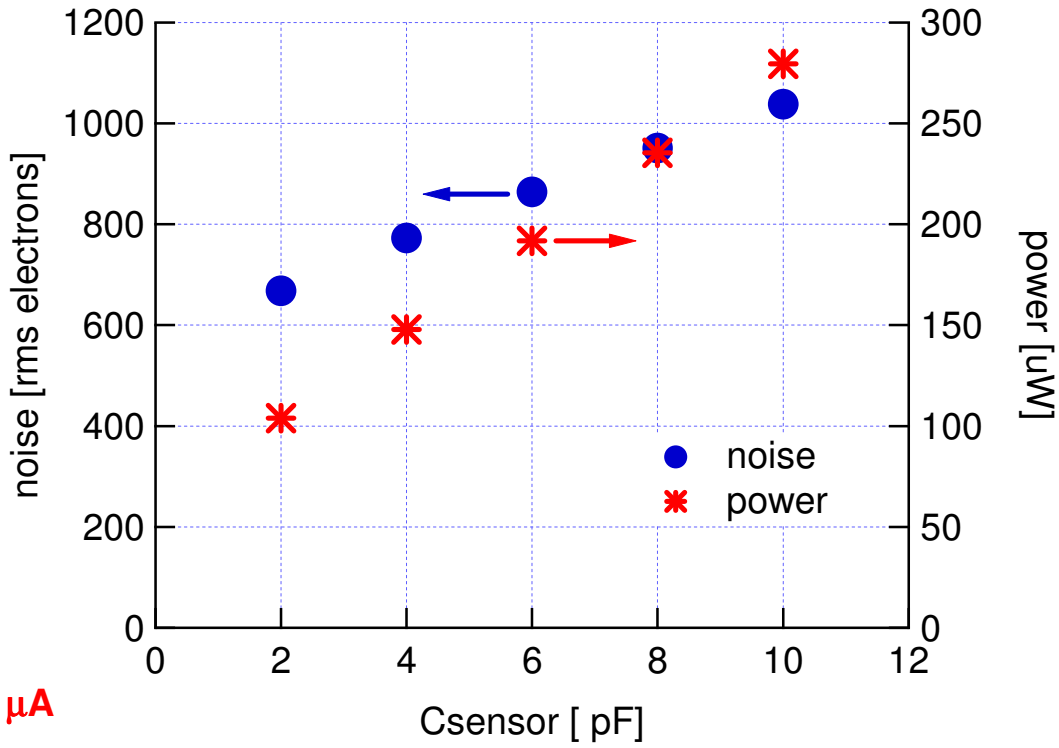
for 20 nsec pulse shape get 440e
for I_{LEAK} = 1μA

(adds in quadrature to amplifier noise)

target noise specification

< 1000e for C_{SENSOR} = 5 pF and I_{LEAK} = 1 μA

simulated amplifier noise & power vs C_{SENSOR} for 20 nsec peaking time pulse shape



final S/N will depend on sensor thickness and strip length

Digital

Pipeline

pipeline depth (latency) should be programmable up to 256 clock cycles (6.4 μsec at 40 MHz).

Buffering

chips should be able to buffer data from up to 32 triggers awaiting readout

SEU immunity

critical parts of the chip, where upsets would cause the chip operation to “crash” or its operational state to be changed (e.g. bias generator registers), must be designed for SEU immunity.

External electrical interfaces

Fast (CK/T1) and Data Out

electrical spec to be decided – some flavour of Low Voltage Differential

SLVS? (Scalable Low Voltage Signalling)

LCDS? (Low Current Differential Signalling)

(power consumption ~ few mW – so negligible per channel in both cases)

Slow control

I^2C

Power

Power supplies

1.2 V analogue (VDDA)
up to 1.2 V digital (VDDD).
VDDA and VDDD to be kept separate on chip to allow VDDD < VDDA

Power consumption

target power consumption 0.5 mW / channel (64 mW per 128 channel chip) for C_{SENSOR} ~ 5 pF
- 200 μW for the front end (amplifier + comparator) (confident)
- 300 μW allowed for digital (more speculative)

Power supply rejection

will take care to achieve as good a performance as possible here
but single ended input stage required to achieve target power consumption
some rejection at all frequencies desirable
may be necessary to use external passive filtering

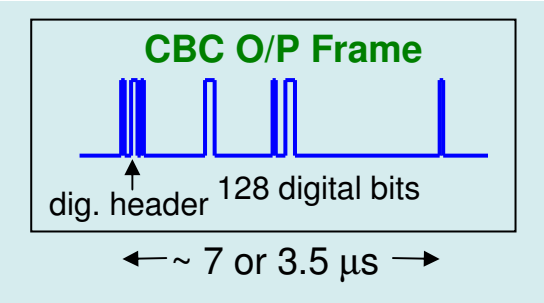
Miscellaneous

Comparator threshold adjust

global value + 4-bit trim per channel (80 mV range, 5 mV lsb – cf ~50 mV / fC)

Output format

"similar to APV" – digital header followed by 128 bits
20/40 Mbps selectable
frame appears promptly on triggering
=> no wait for APSP cycling => no tick marks

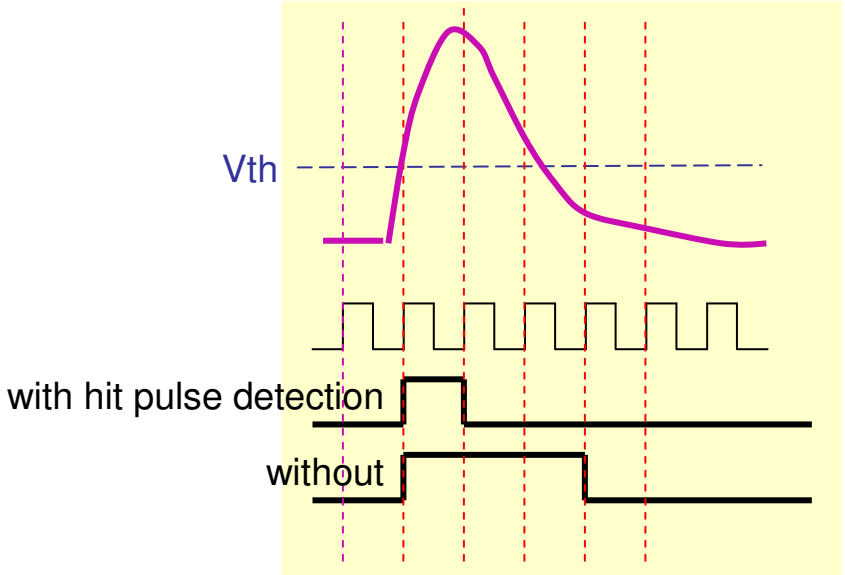


Test pulse

an "APV-like" system is planned
(variable phase, variable amplitude)

Hit pulse detection disable

allows length of time pulse shape over comparator threshold to be measured (in clock cycles)
can vary test pulse amplitude, time of injection and comparator threshold
allows diagnosis of pulse shape



Bonding technology

It is assumed that the first prototype chip will be designed for wire-bonding.

CBC specifications summary

sensor related

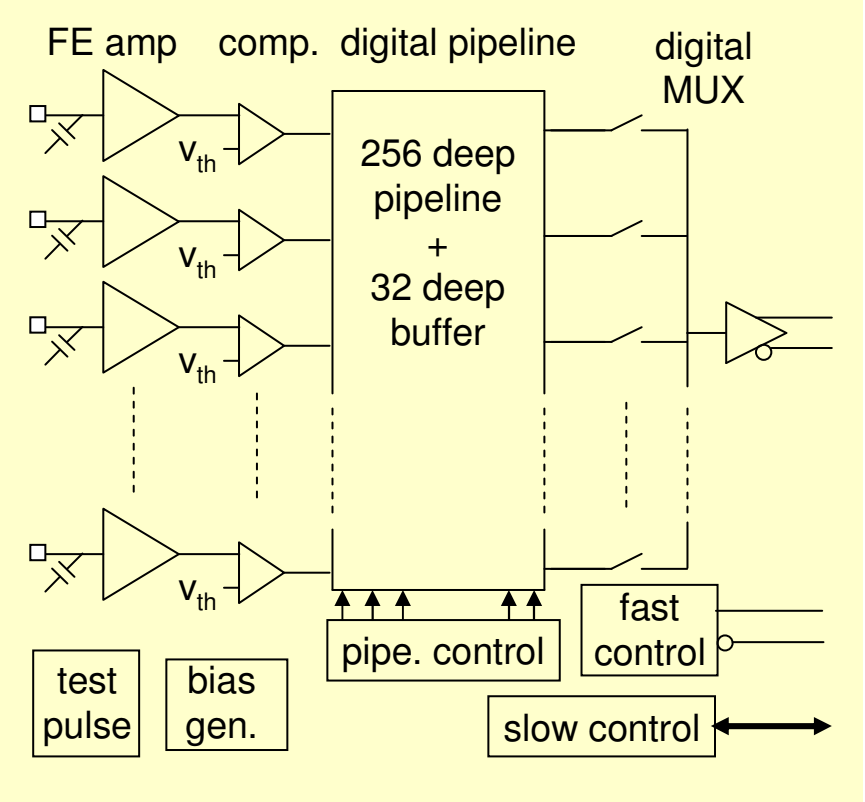
signal polarity: -ve
coupling: DC (or AC)
DC leakage: < 1μA
charge collection: < 10 ns
strip pitch: > 60 μm

front end and comparator

pulse shape: 20 nsec peaking time
time-walk: < 16 nsec
overload recovery: < 2.5 usec
noise: < 1000e for 5 pF and 1 μA

digital

latency: up to 256
event buffering: up to 32
attention to SEU tolerance



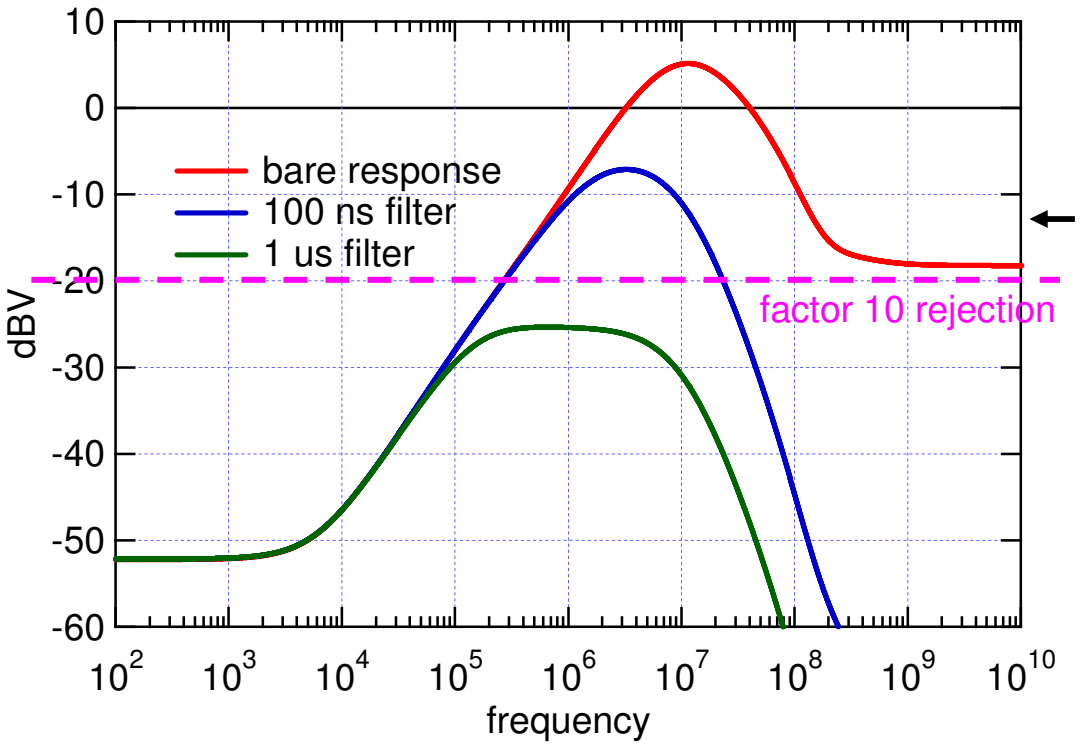
power

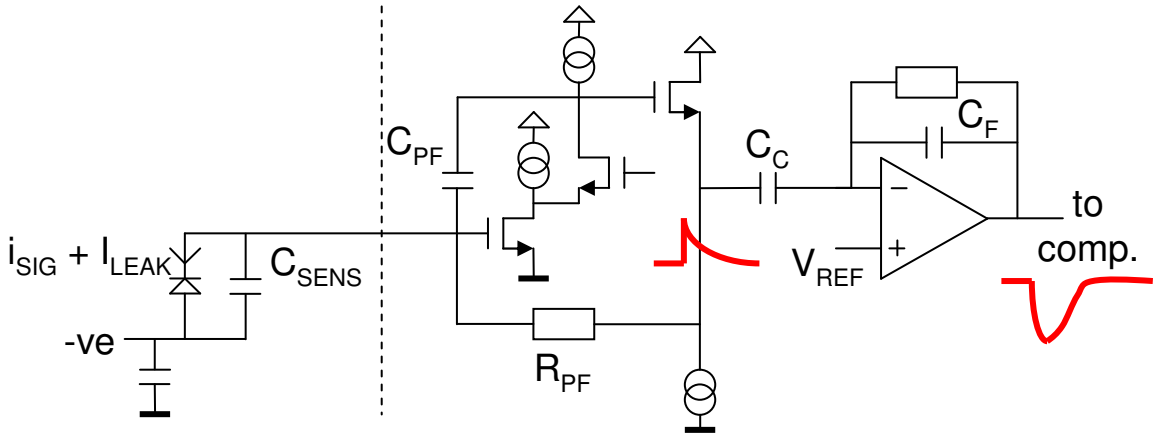
supplies: 1.2 Volts analog, up to 1.2 Volts digital
consumption: <0.5 mW/channel for C_{SENSOR} 5 pF
rejection: as good as possible

feedback welcome

EXTRA

power supply rejection





baseline choice for CMS tracker powering is parallel powering (DC-DC) so PSR will be an issue

power supply rejection at postamp output to sinusoidal waveform on positive supply rail

bare response shows good rejection at low frequency, peaking at ~10 MHz

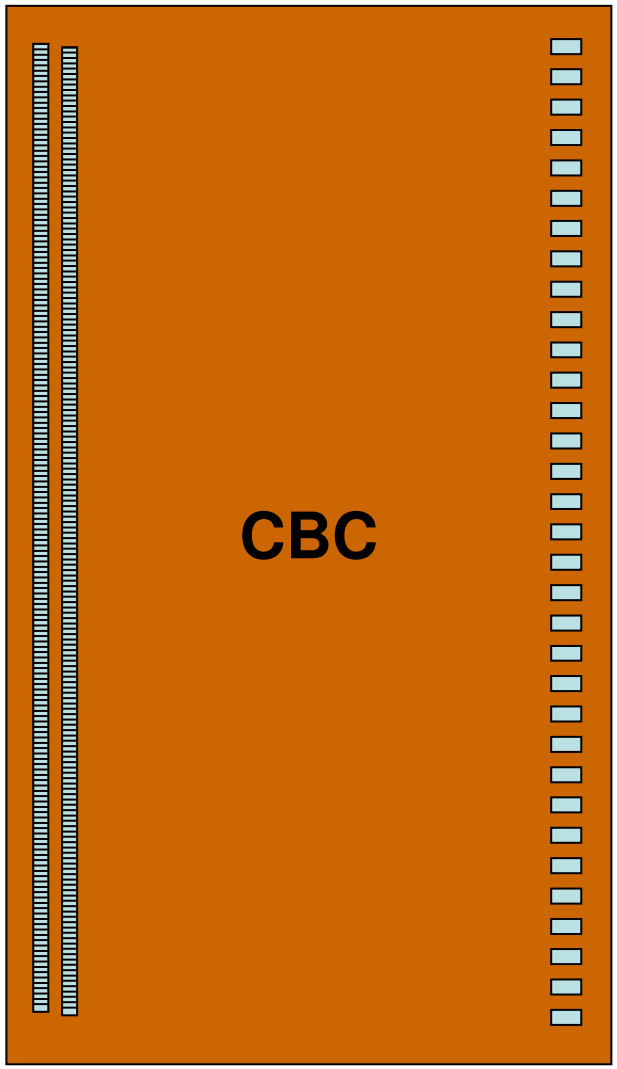
AC preamp/postamp coupling together with opamp postamp gives good low f behaviour

peaking at ~10 MHz (gain) due to coupling through bias circuits

can improve with realistic filtering, but would prefer some rejection at all frequencies to start with

needs further study

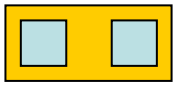
chip vs. passive size



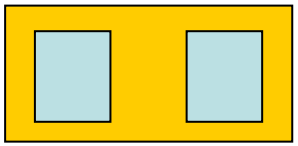
few mm

7 mm

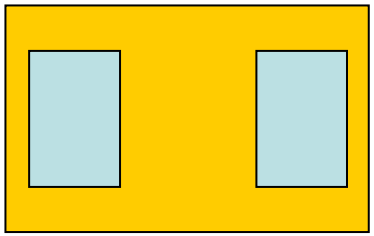
approximately to scale



0201 - up to 100 nF



0402 - up to 220 nF



0603 - up to 10 uF

passives take space
don't want too many per chip

decoupling necessary – don't ignore

DC-DC on-chip will add more passives

substrate coupled noise

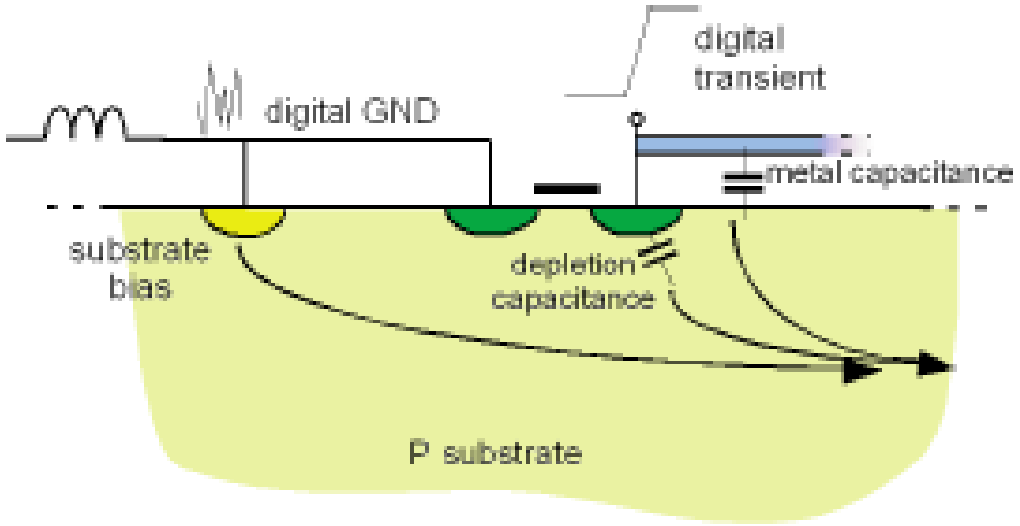


Fig. 1 Scheme of the potential sources of substrate noise.

http://pmos.upc.es/blues/publications/SignalIntegrity/chipps02.pdf

advantages of unsparsified binary readout

much simpler chip - will be lowest power architecture (no ADC)

- analog FE + comparator followed by simple digital pipeline and off-chip mux
  - faster development time – can be available sooner
  - analog chip would have to be sparsified – data volume dictates this
    - data volume known - no trigger-to-trigger variations – occupancy independent
- synchronous system - all FE chips doing same thing at same time – can be externally emulated
  - => easy to spot upset chips (pipe address wrong)
- no need to timestamp on front end
- relatively simple to implement cluster width trigger before pipeline
  - (not necessarily simple to get it off-chip)
- easier to scale design to even finer feature processes
  - (analog pipelines using gate capacitance probably only just possible in 0.13)
- off-detector functionality (FED) easier
- should be easy to keep dynamic power variations small or negligible
- detector module construction conventional => lowest cost
- ….

disadvantages

- no pulse shape information – relatively complicated to extract (comparator threshold scan)
- binary must be a bit worse for position resolution
- common mode immunity – need on-chip CM subtract (short strips will help – less pickup)
- ….