CBC – status and plans

OUTLINE

proposed CBC architecture summary
Atlas strips readout comparison
FE performance summary
FE solution for p-in-n sensors – new
proposed CBC specifications
current plans

Mark Raymond – Imperial College

progress in last ~ year

have converged on **binary un-sparsified** architecture for outer tracker short strip readout at SLHC

strip lengths 2.5 / 5 cm have been proposed

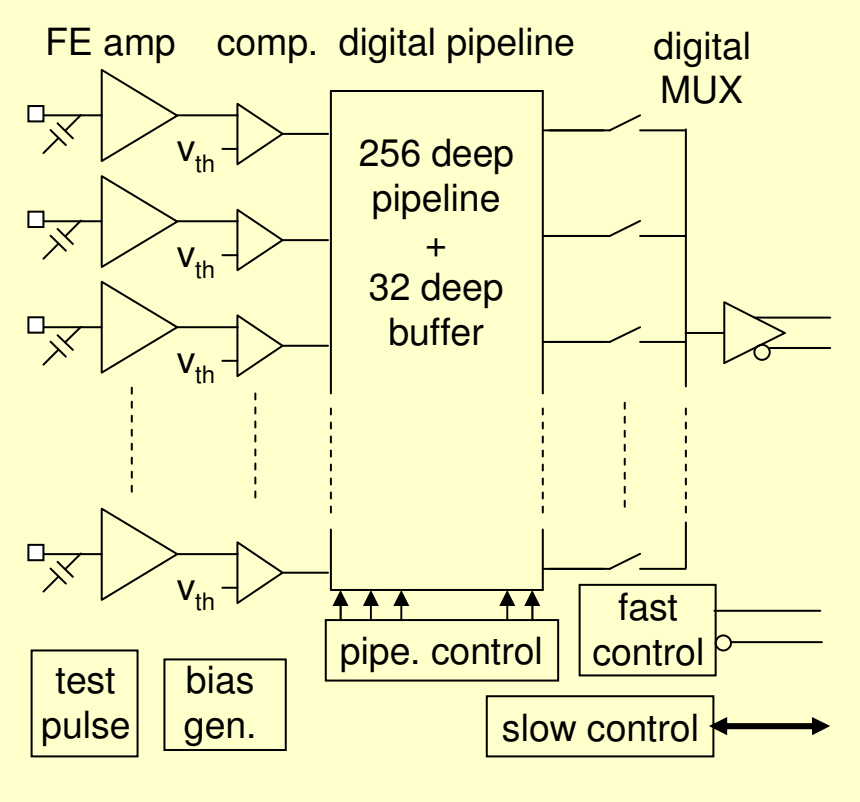
"digital APV" concept no longer under consideration*

some advantages:

- no ADC power
- simpler on-chip logic
- should offer lowest possible FE power
- compatible with cluster width approach to track triggering layers

retaining no zero suppression

- simpler overall system
- occupancy independent data volume

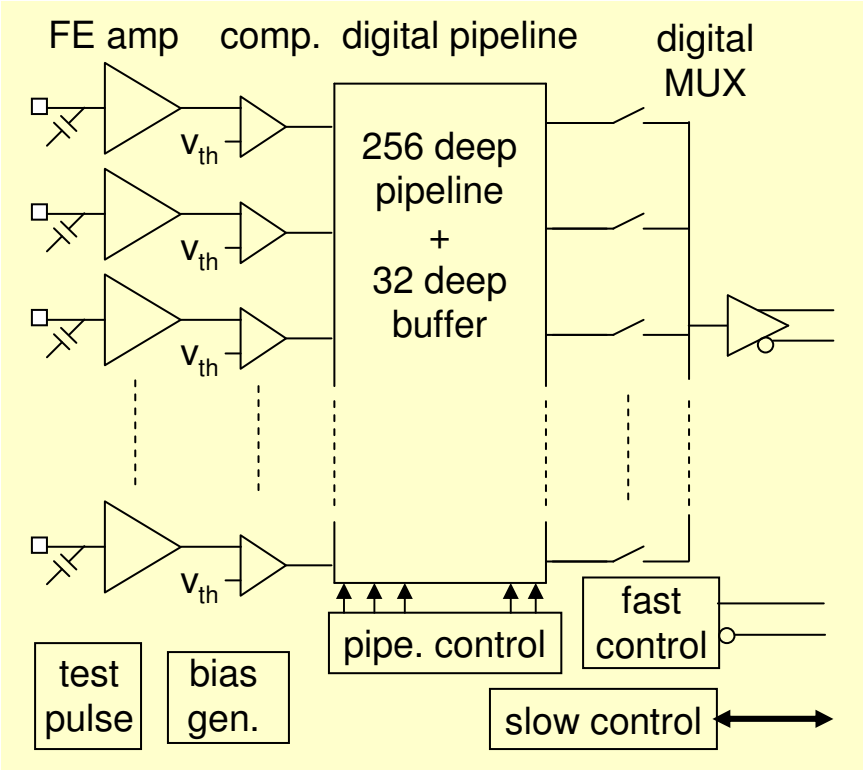


CBC – CMS Binary Chip

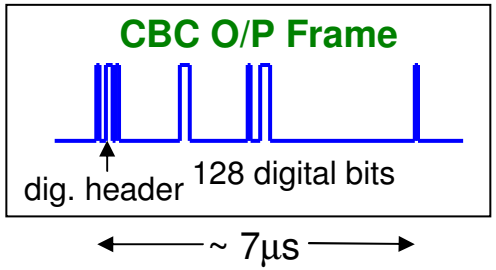
design of CBC functional blocks now underway in 130 nm

*see previous talks for details
(e.g. May'08 CMS Upgrade, TWEPP'08, Jan'09 Tracker Upgrade, ACES'09 (March))

CBC functional blocks



- fast front end amplifier – 20 nsec peaking
- comparator with individual threshold trim
- pipeline (256 deep)
- buffer for triggered events (32 deep)
- output mux and driver
- fast and slow control interfaces
- programmable bias
- test pulse (DLL based)



is pipeline type architecture right choice to deal with level 1 latency?

- unlimited buffer depth prior to level 1 (all hits are stored)
  important for high channel occupancy
- relatively simple synchronous architecture
- address of pipe location triggered can be output in digital header (like APV)
  strong check on data integrity (acts like a timestamp)
- continuously circulating pipe-control pointers give const. power consumption, independent of trigger rate
  (works well in APV – should try and maintain this feature in CBC)

comparision with Atlas

Atlas outer SLHC tracker

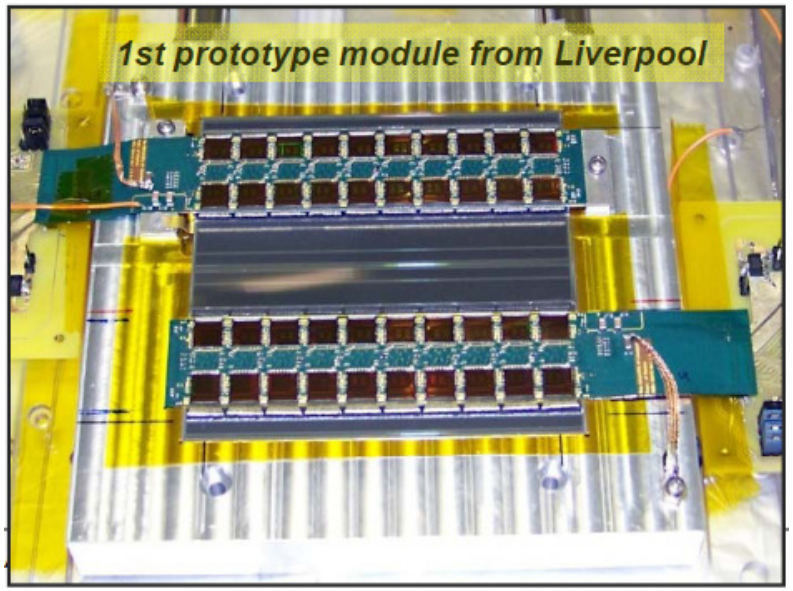
3 layers short strips (~ **2.5/5 cm** x 80 um) at r ~ 40 – 60 cm
2 layers longer strips (~ **10 cm** x 80 um) at r ~ 75, 95 cm
predicted occupancies ~ 1 – 2.6 %

readout electronics ~ evolution of same sparsified binary pipeline chip architecture as LHC

ABCD (in current detector)
-> ABCN (0.25um) (currently used for SLHC protyping) – 3.6 mW/ch
-> ABCN (130nm) (2010-11?) – predicted 0.5 – 0.7 mW/ch

prototype modules already in development
(based on ABCN25)

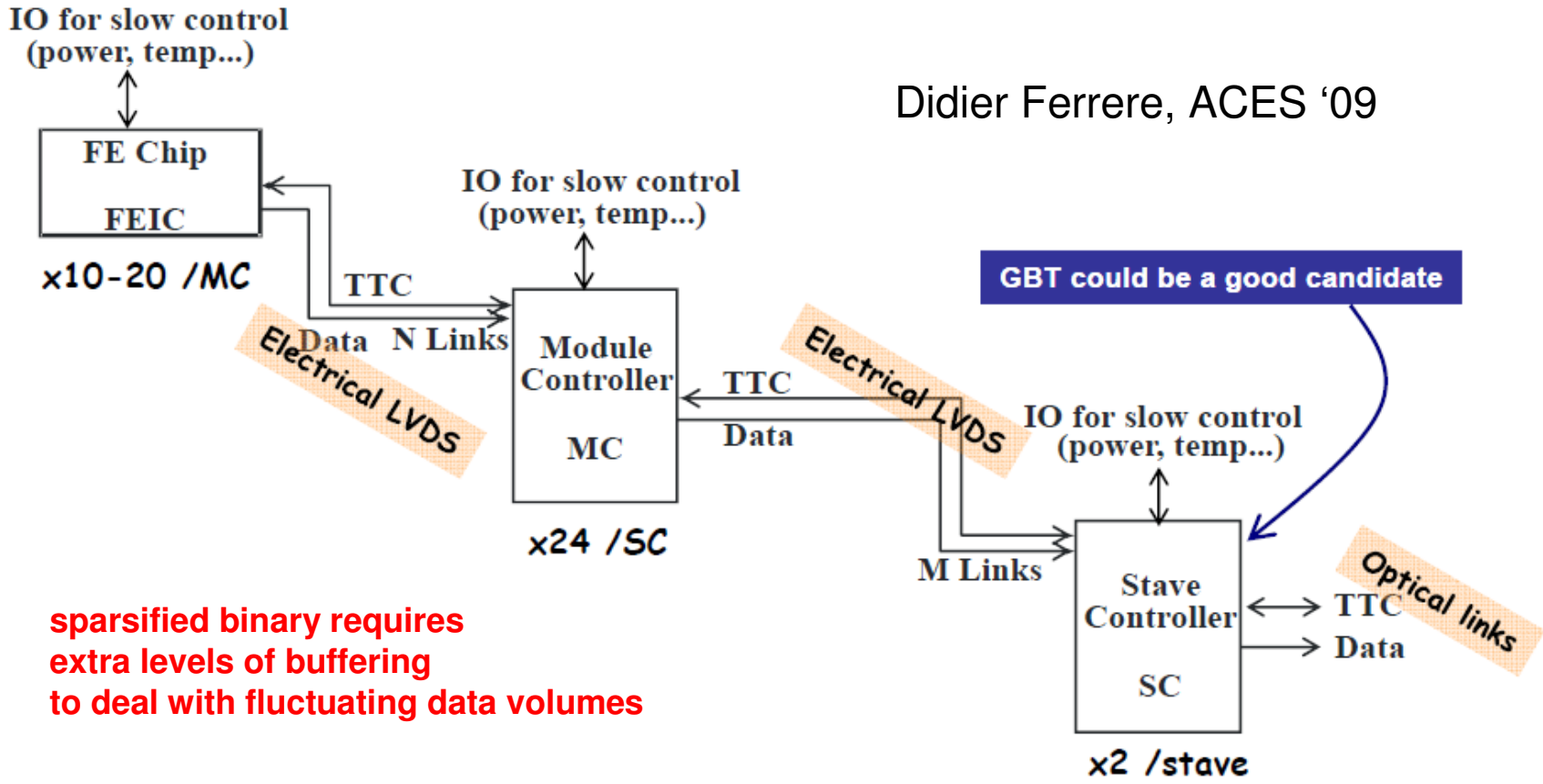
DC-DC or serial powering choice still open



details and pictures taken from:

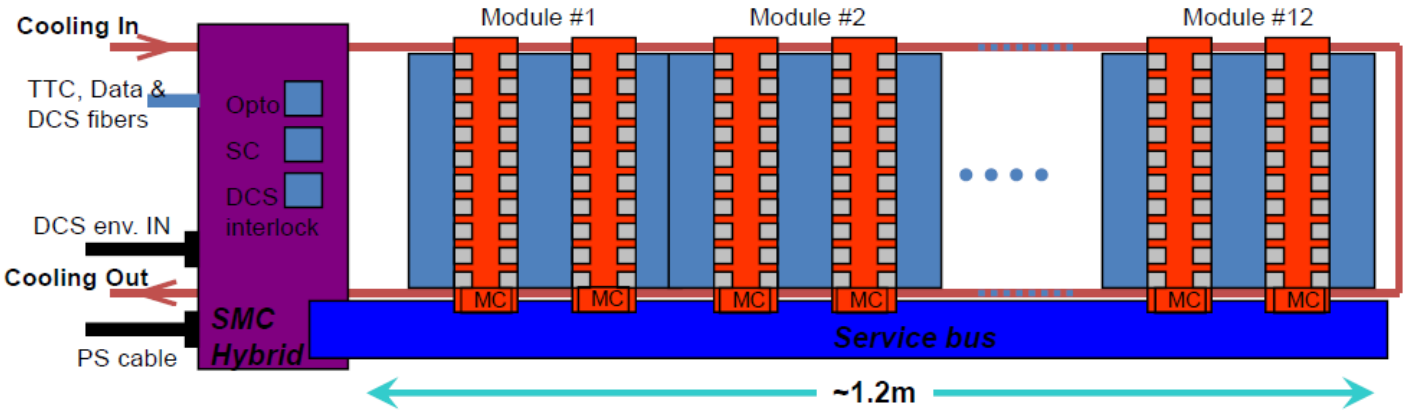
ACES '09 – Front end design for the Atlas microstrip detector at SLHC – Francis Anghinolfi
http://indico.cern.ch/getFile.py/access?contribId=25&sessionId=11&resId=1&materialId=slides&confId=47853
ACES '09 – Atlas Strips – Didier Ferrere
http://indico.cern.ch/getFile.py/access?contribId=4&sessionId=3&resId=1&materialId=slides&confId=47853

Atlas Readout Architecture



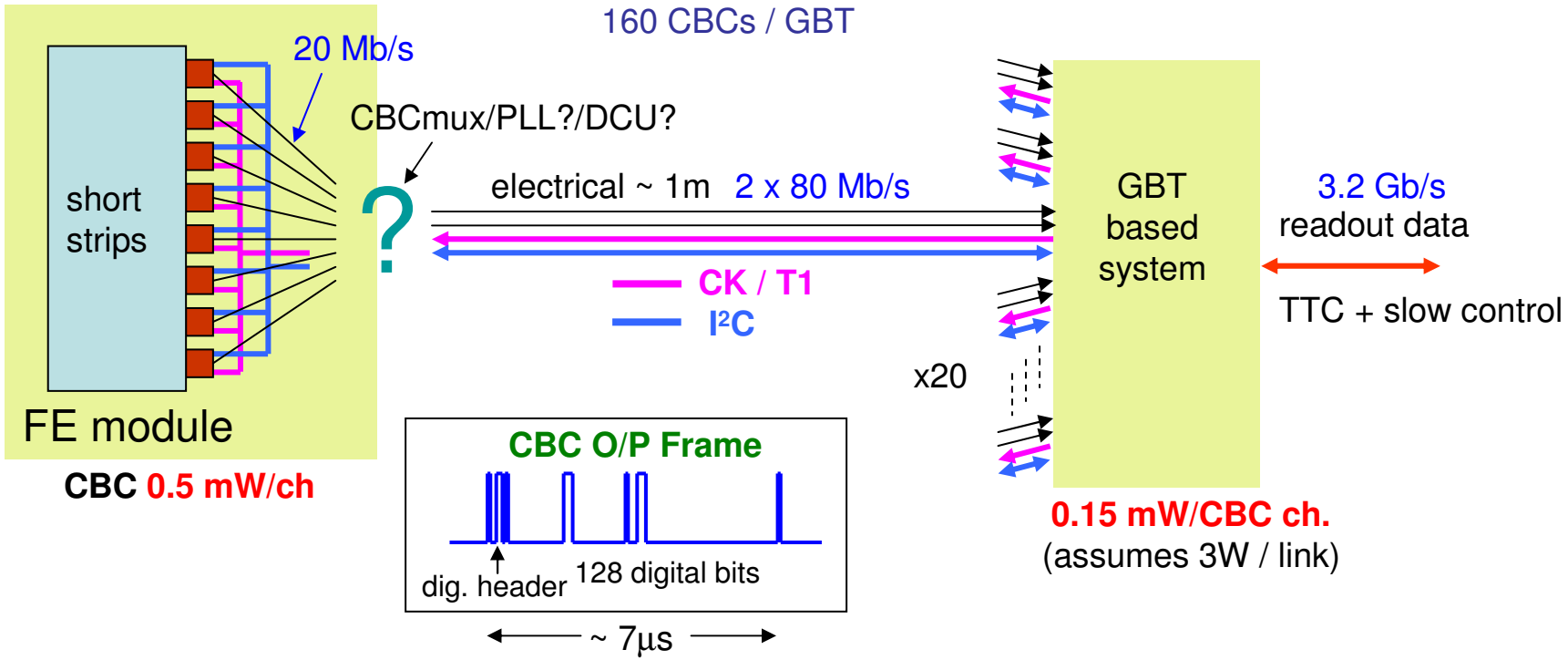
Didier Ferrere, ACES '09

sparsified binary requires
extra levels of buffering
to deal with fluctuating data volumes



Francis Anghinolfi,
ACES '09

possible CMS strips readout architecture



one potential system architecture

CBC provides unsparsified data at 20 Mbps (128 bits + 12 bits header)

combine 4 chips onto one 80 Mbps GBT electrical lane

=> 2 lanes for 8 chip module

=> 160 CBCs / GBT

is this the simplest/best solution? (I think so)

relative power contribution of off-detector transmission ~ 20%, but can be located remotely

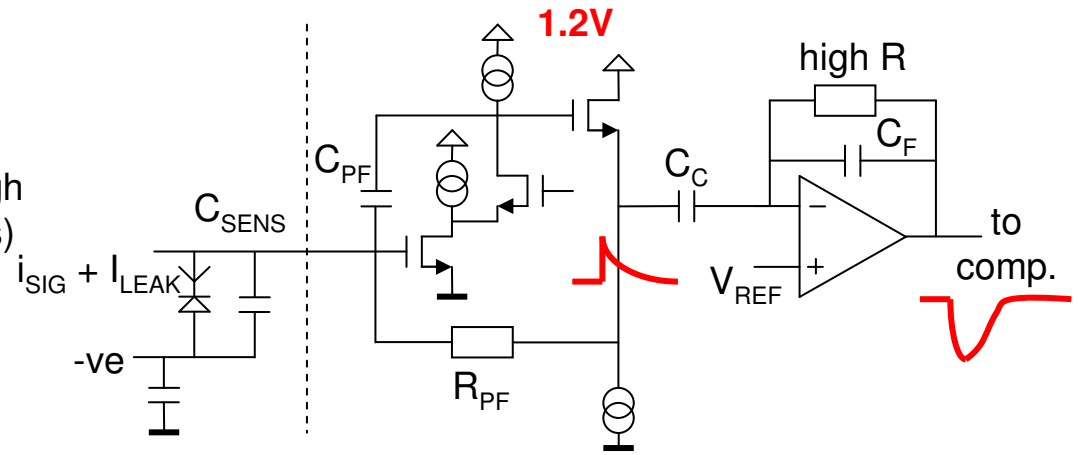
is this realisable with current GBT system? (I'm not sure)

130nm front end amplifier

Preamp

NMOS I/P device

no noise penalty - 1/f corner low enough
(simulation & published measurements)



DC coupling to sensors possible

low Rpf (200k) absorbs DC leakage
(1 µA -> 200 mV)
200k noise contribution only ~ 220e
Rpf//Cpf = 200k//100fF = 20 ns decay time constant of preamp (no pile-up)

Postamp

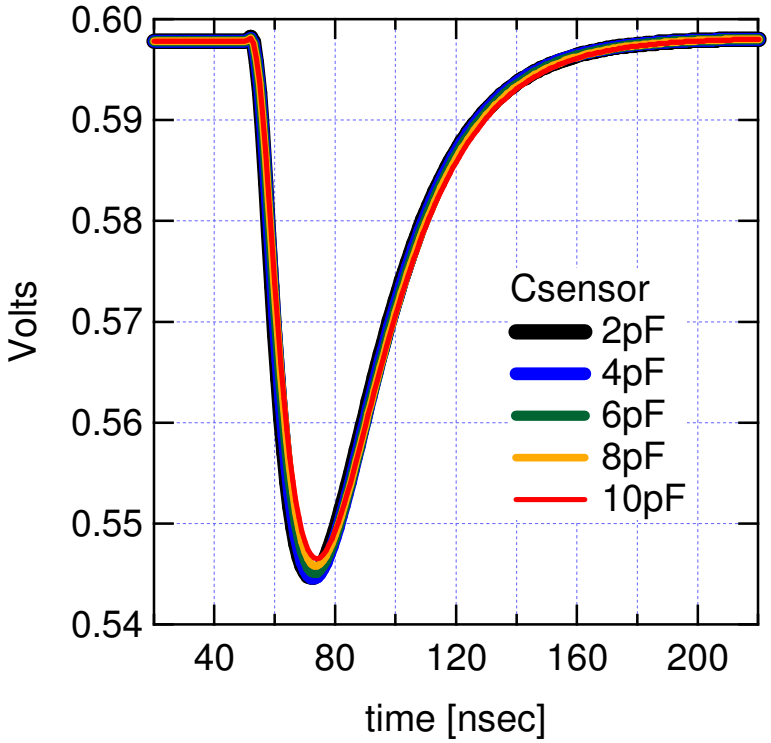
provides gain & risetime provides integrating time constant
AC coupled to preamp
blocks DC shift due to leakage (DC coupled sensors)

will show some simulated performance pictures

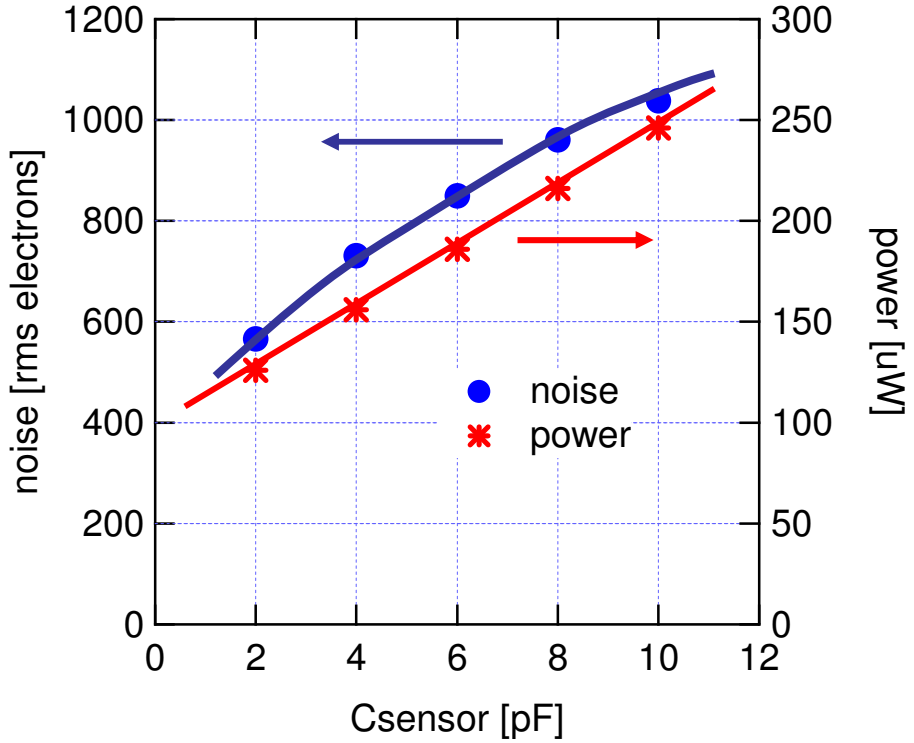
note: FE design up to now concentrated on readout for n – on – p type readout

pulse shape and noise

pulse shapes for 1 fC input charge (~ 50 mV / fC)



FE power and noise dependence on C_{SENSOR}

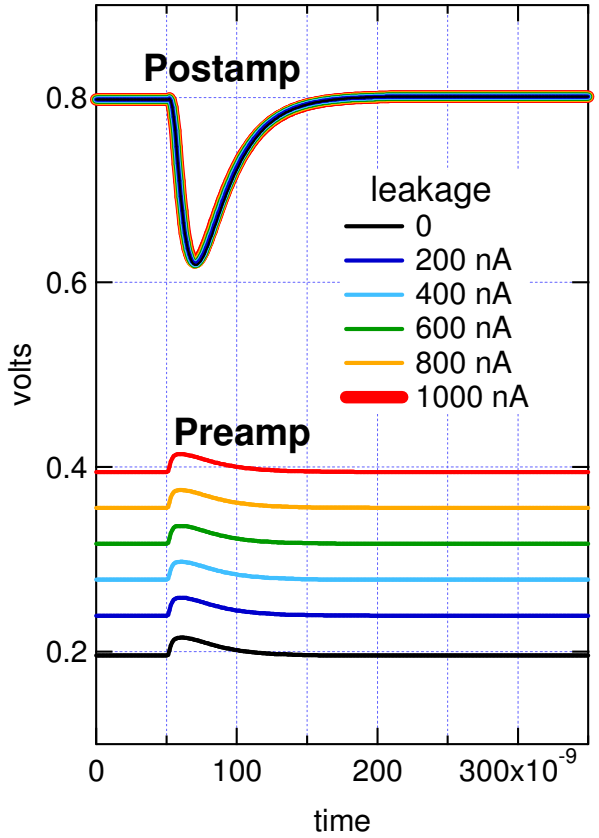


pulse shape tuned to keep peaking time ~ constant as C_{SENSOR} varies by increasing current in input FET (I_{DS})

amplifier optimised for mid-range C_{SENSOR} (**not** efficient for sub ~ pF sensor)

noise < ~900e for power ~ 200 μW for C_{SENSOR} ~ 6 pF

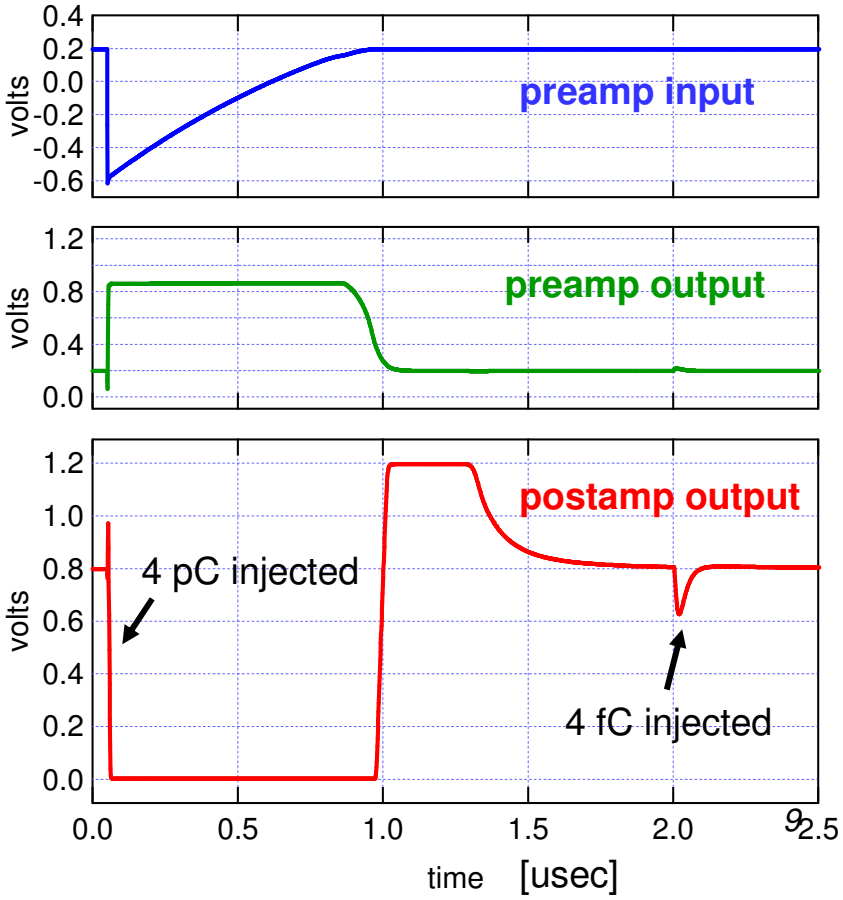
leakage current, overload performance



preamp output shows DC shift across preamp feedback, R_{PF}
postamp output unaffected (AC coupled)

1 µA leakage contributes ~ 440e noise

e.g. $\sqrt{\mathbf{900^2}\text{ (total amplifier for } C_{SENSOR} \sim 6\text{ pF)} + \mathbf{440^2}\text{ (leakage)}}$
= ~**1000**e total



overload behaviour well-controlled →
low R_{PF} beneficial
front end recovers from 4 pC signal and
sensitive to normal signals within 2.5 µs
=> no “APV-like” hips effect

opposite polarity sensors - new

for p-on-n type readout leakage current (& signals) flow the other way

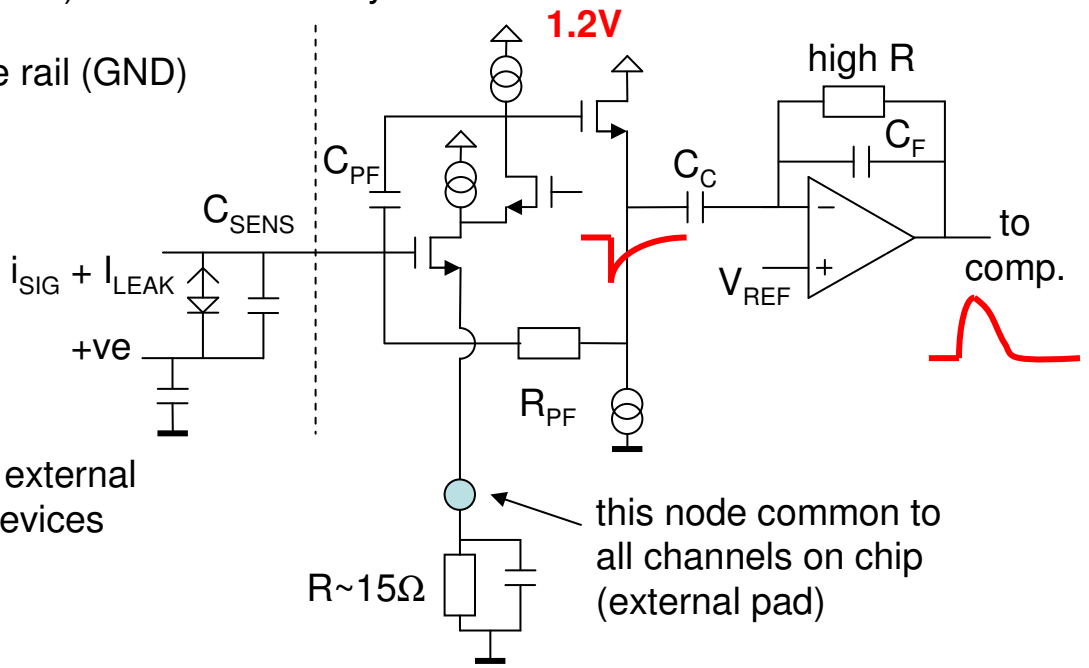
=> preamp output quickly saturates on the –ve rail (GND)

how to get around? in 130 nm CMOS can lift the bulk of NMOS FETs away from GND using triple-well device

=> can create headroom for negative going signals at preamp output

raise the input device source/bulk using small external resistor ~ 15 ohms, common to all 128 input devices

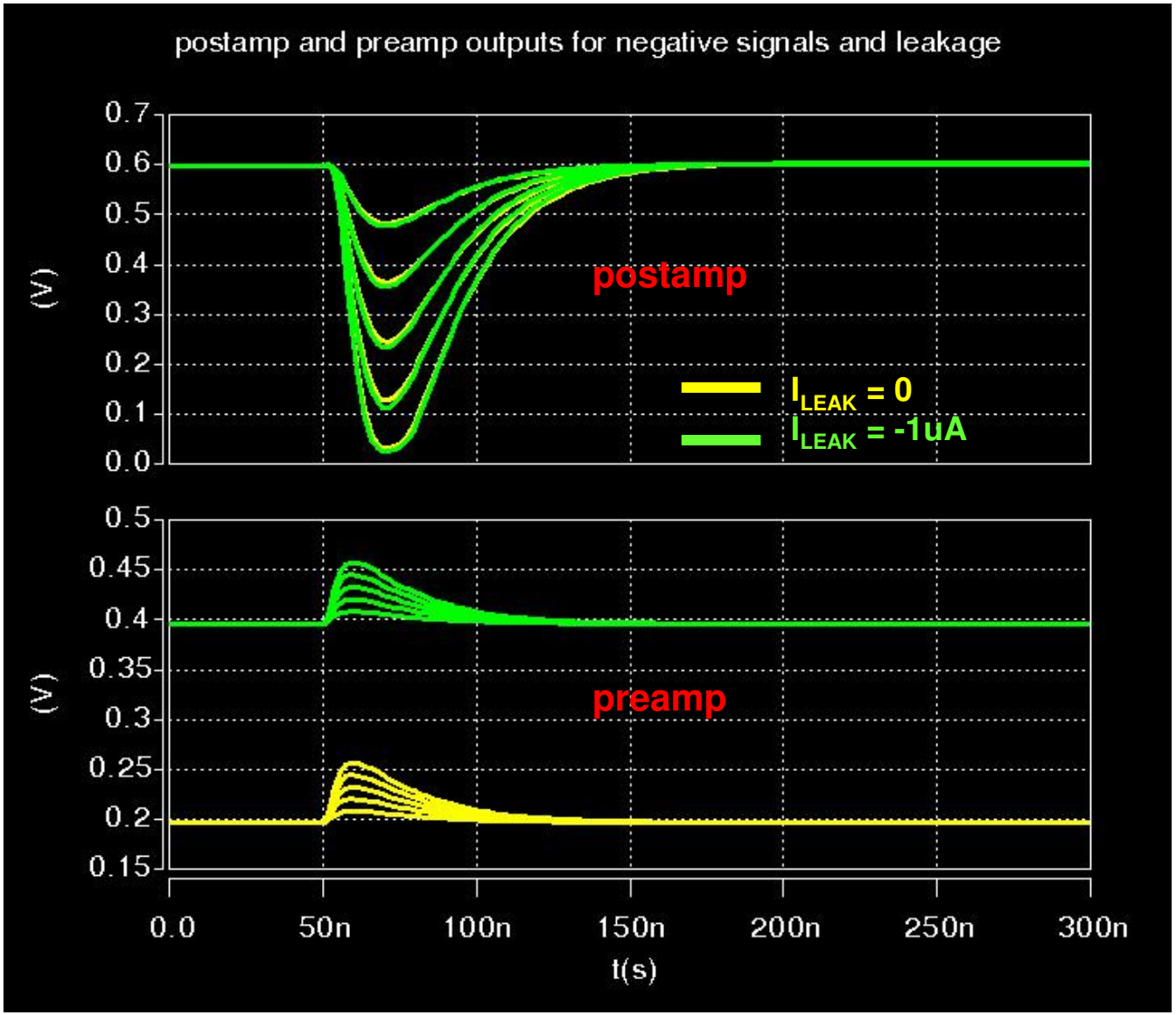
=> 15 x 128 x 100 uA = ~200 mV



penalty is maintaining separate connection to input source/bulk for both signal polarities

(+ external components (R & C) for p-side readout)

n-on-p polarity



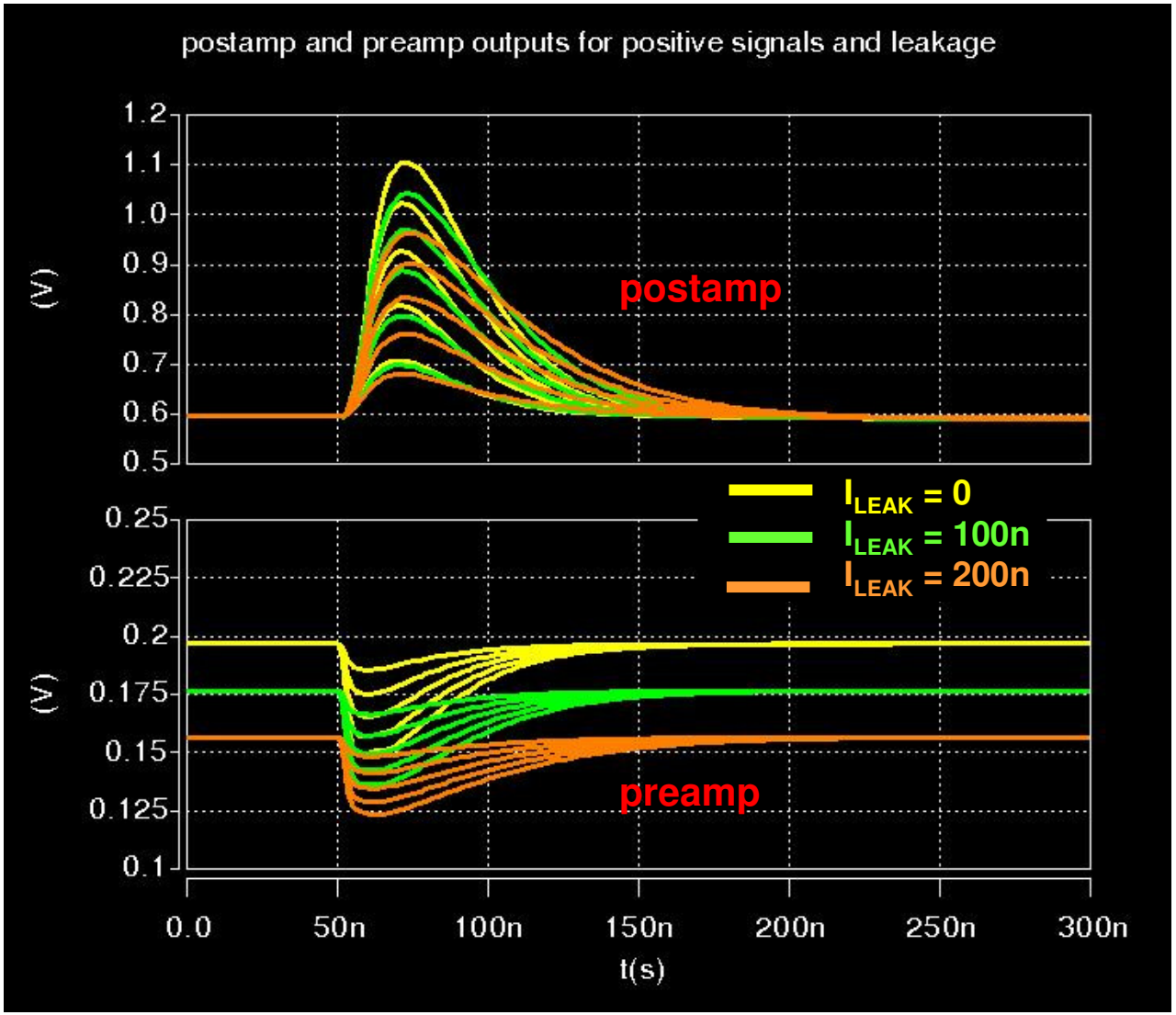
reminder of what happens for n-on-p

signals shown are 2 fC to 10 fC (2 fC steps)

preamp output shifts +ve with leakage
(1uA x 200k = 200 mV)

postamp output unnaffected

opposite: p-on-n polarity



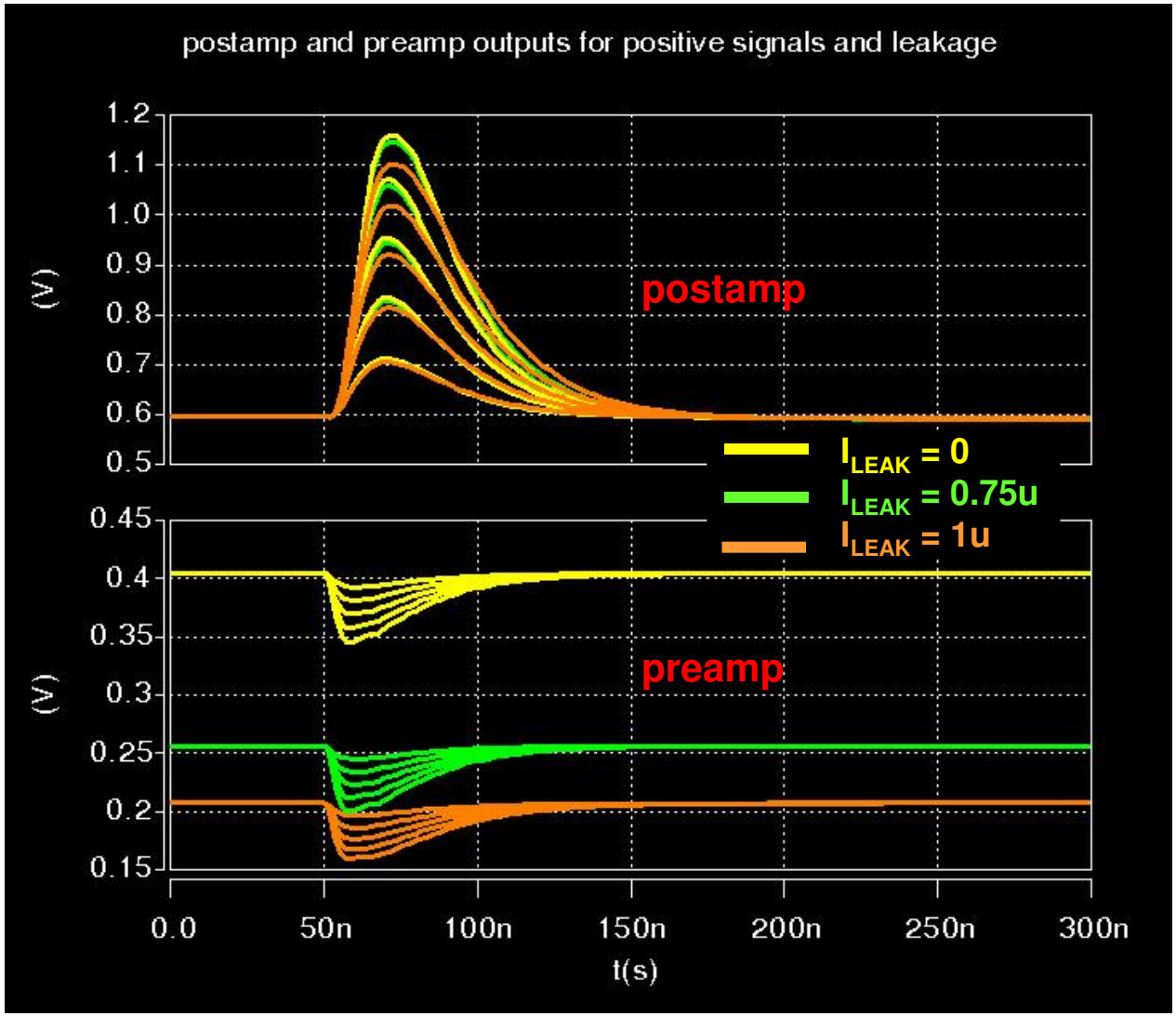
without input device source resistor

still enough headroom to cope with signals in absence of leakage

with modest leakage (~ 100nA) preamp output start to saturate

worth noting: don't need extra source resistor for AC coupled sensors

opposite p-on-n polarity



with input device source resistor

can now tolerate leakage up to ~ 0.75 uA

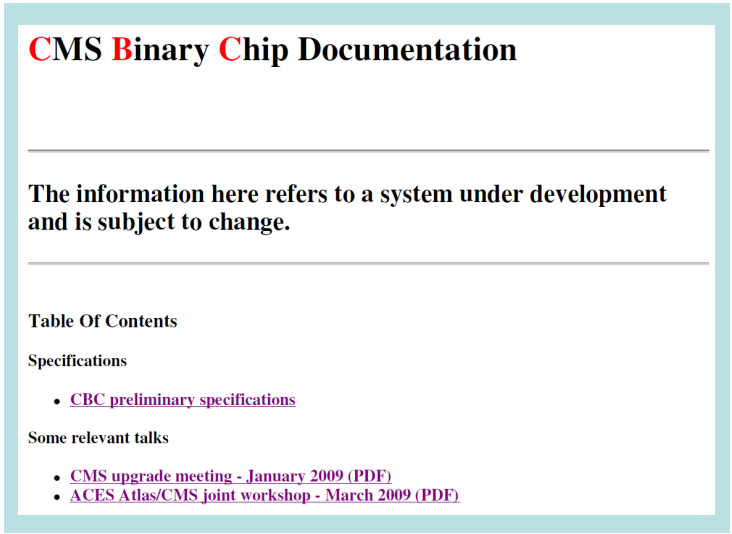
not quite as good as n-on-p but not bad

CBC specifications

http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation

abridged version of a previous talk*

organize specifications into
- sensor related
- front-end – amplifier and comparator
- digital – pipeline and interfaces
- noise and power



CMS Binary Chip Documentation

The information here refers to a system under development and is subject to change.

Table Of Contents

Specifications

- CBC preliminary specifications

Some relevant talks

- CMS upgrade meeting - January 2009 (PDF)
- ACES Atlas/CMS joint workshop - March 2009 (PDF)

*Tracker Upgrade Meeting, April '09
http://indico.cern.ch/getFile.py/access?contribId=12&sessionId=2&resId=0&materialId=slides&confId=47298

sensor related

signal polarity

negative (n in p type sensor elements)

signal and leakage currents flow out of amplifier

positive can also be accomodated with extra external R

(performance specifications for positive signals tbc)

coupling to amplifier

DC assumed (=> AC also possible)

DC leakage

up to 1 uA for negative signals (bit less for +ve (TBC))

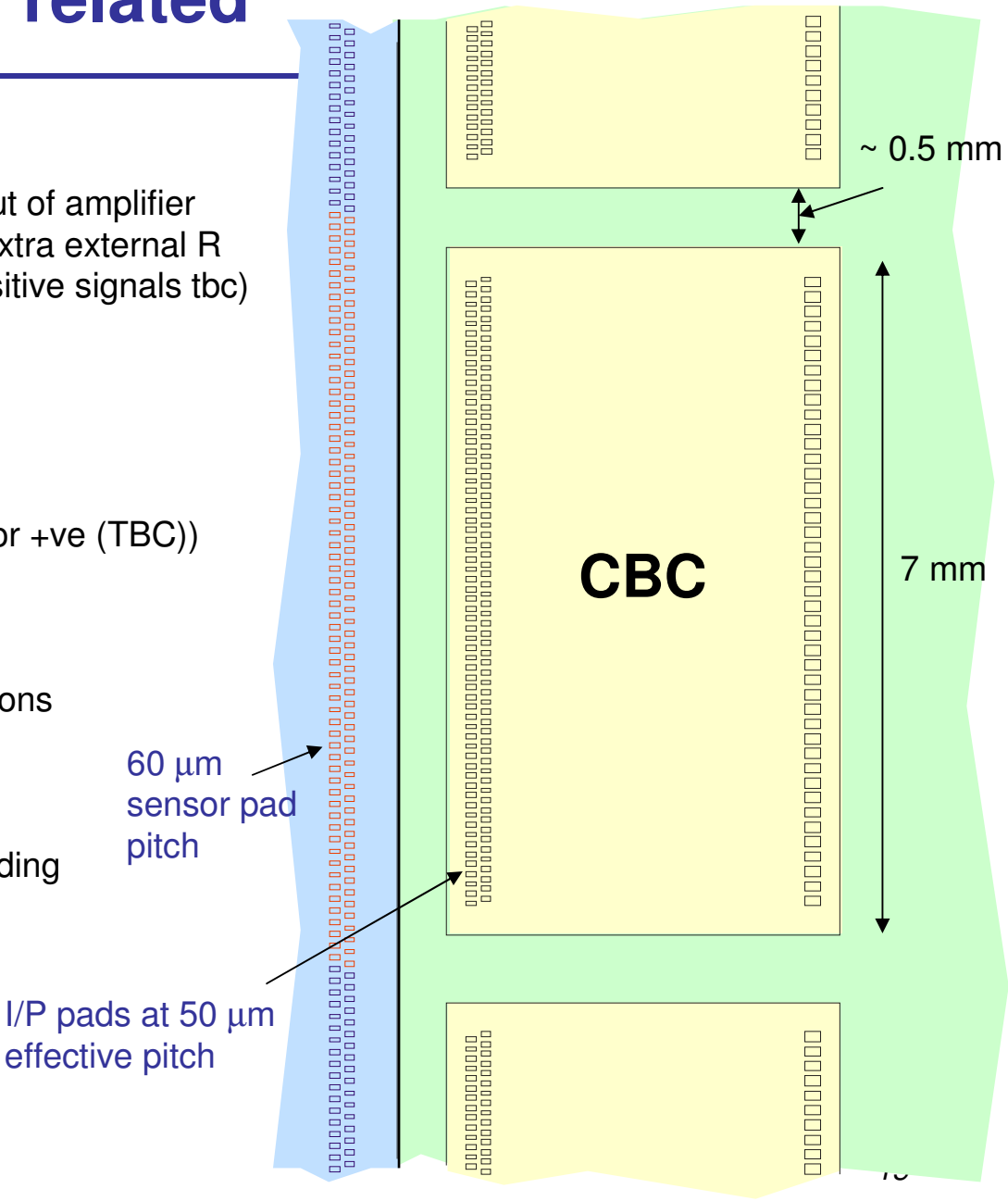
charge collection time

< 10 nsec

(long charge collection time has implications for timewalk performance)

strip pitch > ~ 60 um

assumes 128 channel chip and wire-bonding



front end amplifier & comparator

pulse shaping

20 ns peaking time for pulse at comparator I/P

time-walk*

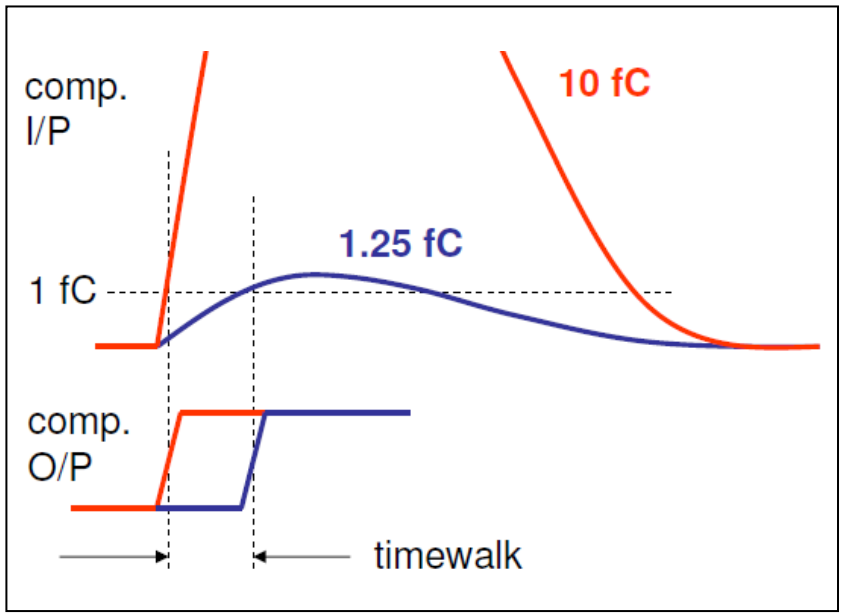
≤ 16 ns time difference between comparator output edges for input signals of 1.25 fC and 10 fC, for a threshold setting of 1 fC

overload recovery

individual channel should respond to normal size signals < **2.5 usec** following a hip-type signal of up to 4 pC

noise target

< **1000e** for C_{SENSOR} = 5 pF and I_{LEAK} = 1 uA
(final S/N will depend on sensor thickness and strip length)



** timewalk (and other) specifications drawn from:*
ABCD3T Chip Specification Version V1.2, July 24, 2000

digital – pipeline and interfaces

pipeline depth

256 – programmable – up to 6.4 usec @ 40 MHz

buffering

chips should be able to buffer data from up to 32 triggers awaiting readout

SEU immunity

critical parts, where upsets would cause chip operation to “crash” or operational state to be corrupted (e.g. bias generator registers), must be designed for SEU immunity

electrical interfaces

fast – low voltage differential

slow – I^2C

power

Power supplies

1.2 V analogue (VDDA)
up to 1.2 V digital (VDDD).
VDDA and VDDD to be kept separate on chip to allow VDDD < VDDA

Power consumption

target power consumption 0.5 mW / channel (64 mW per 128 channel chip) for C_{SENSOR} ~ 5 pF
200 μW for the front end (amplifier + comparator) (confident)
300 μW allowed for digital (more speculative)

Power supply rejection

see talk this afternoon

current plan: risks and advantages

current plan

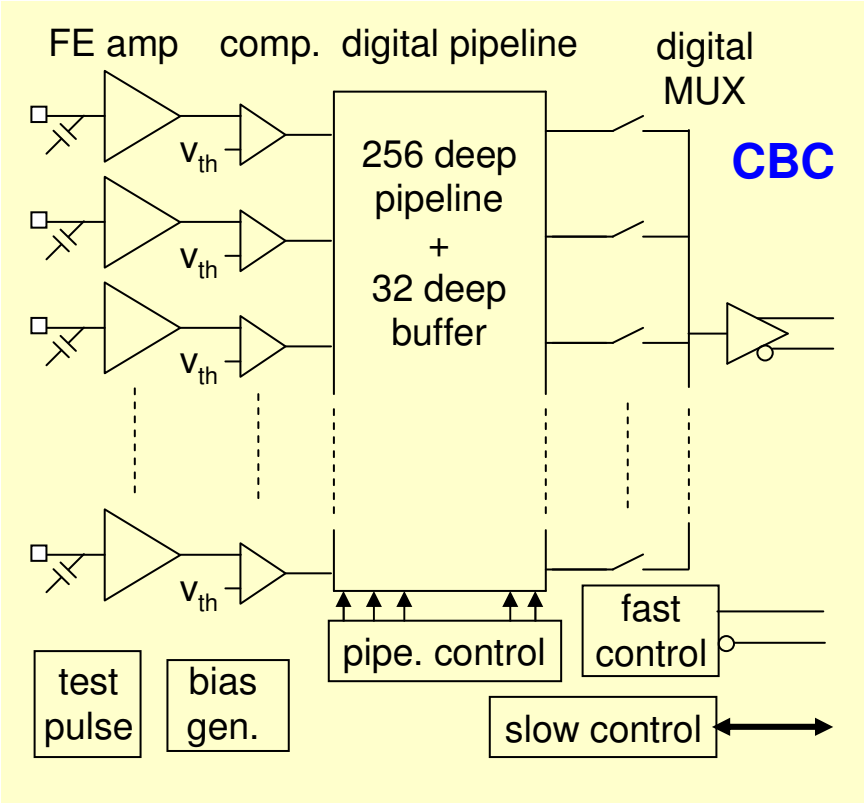
submit complete chip prototype
Preliminary Design Review at RAL – 21st April
lead engineer Lawrence Jones
hope to submit early 2010

risks (of complete chip prototype)

always present, but remember APV6 (1.2 um)
-> APV25 (0.25um) in one iteration
CBC much less complex than "digital APV"

advantages of complete chip prototype (if it is usable)

- will learn a lot sooner rather than later
  radiation, SEU, PSR, ... apart from "normal" functionality characterization
- provides collaborators with something to use to evaluate sensors and develop modules
- time is always shorter than you think
  should aim to go eventually into production with a mature, **thoroughly evaluated**, design



but CBC is a prototype

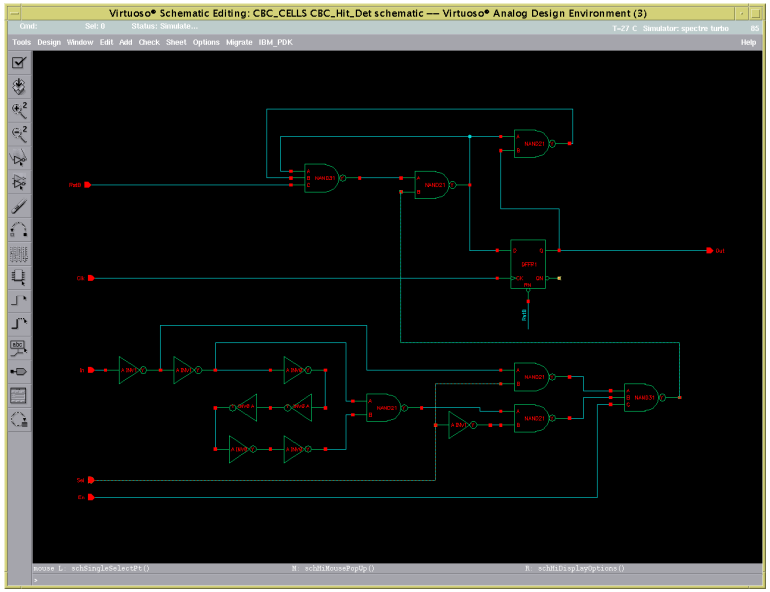
=> need plenty of diagnostics
e.g. extra analogue only channels
bias gen. (slow control) override
test structures
….

Simulation of the Hit Detect Logic

– synchronises the comparator output to the clock

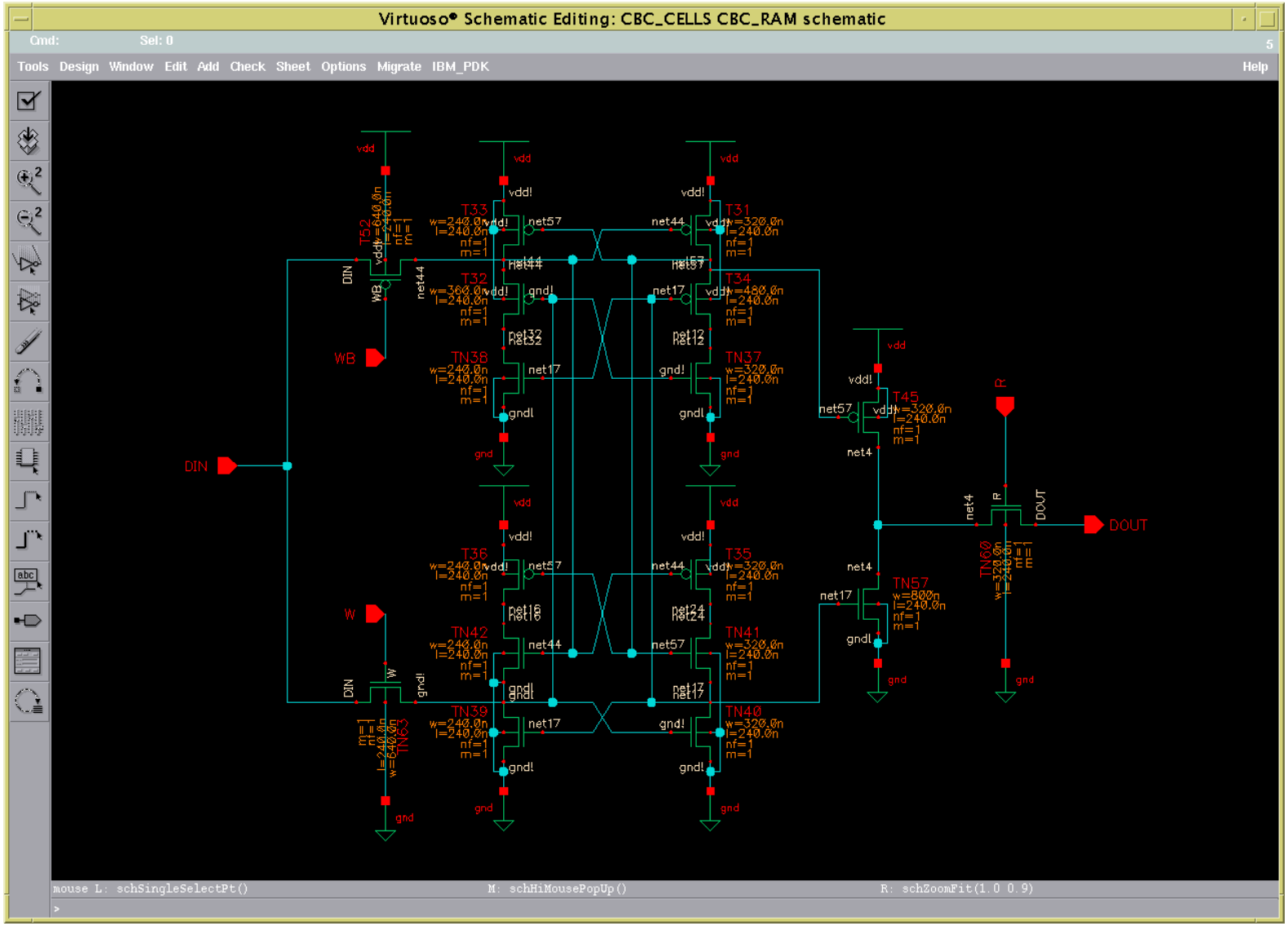
slides from Lawrence

Case 1 - large time over threshold.
Sel = 0, Out goes high for 1 clock cycle no matter how long In is high.
Sel = 1, Out goes high for as many clock cycles as the input is high.



Case 2 - short time over threshold.
Sel = 0 or 1, Out goes high for 1 clock.

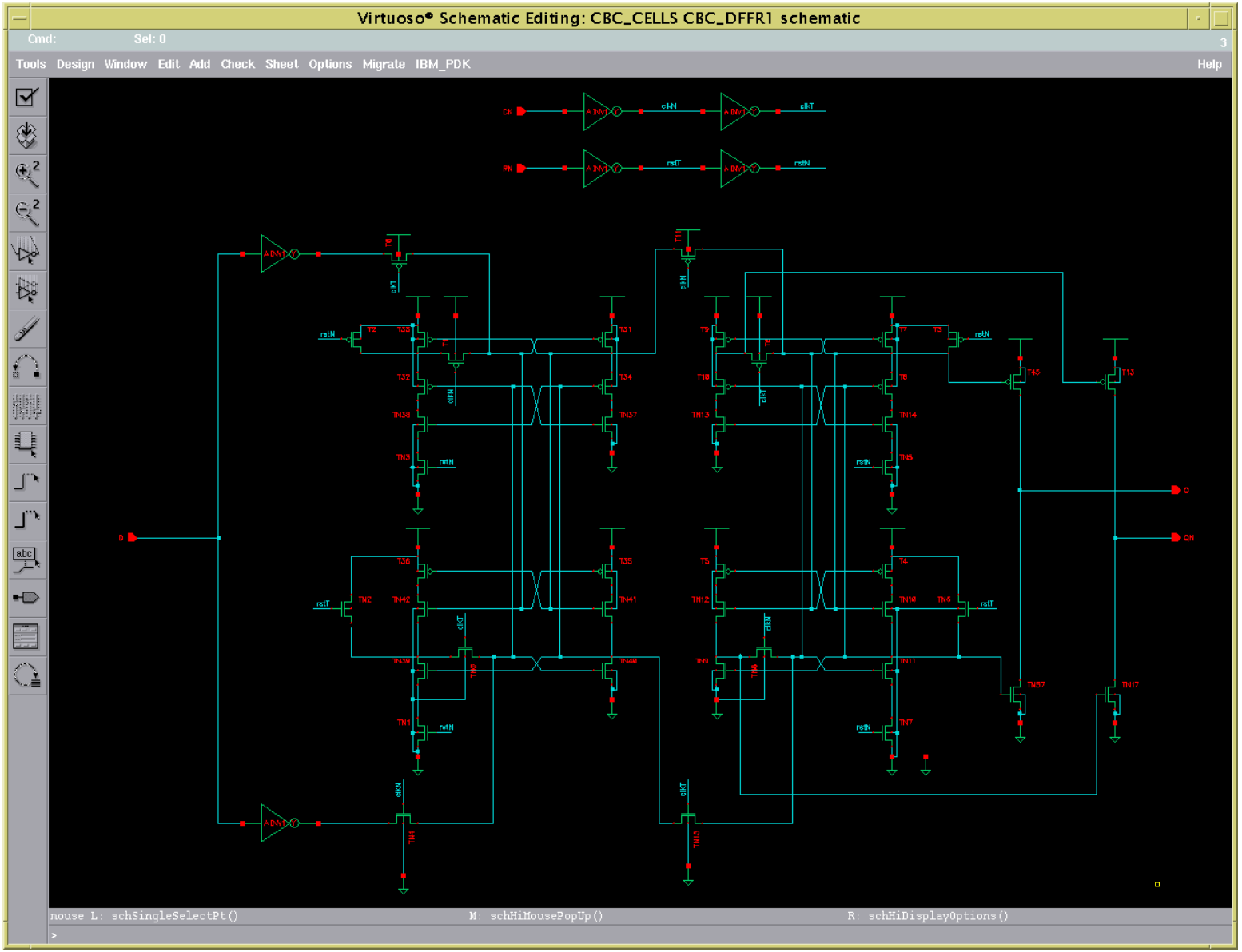
Self Correcting RAM – corrects for SET upset in the storage element, but still vulnerable on the data input and output.



slides from Lawrence

Self Correcting Flip Flop – corrects for SET upset in the storage elements, but still vulnerable on the data input, output, and clock buffers.

One storage element forms the basis of a RAM cell.



CBC specifications summary

sensor related

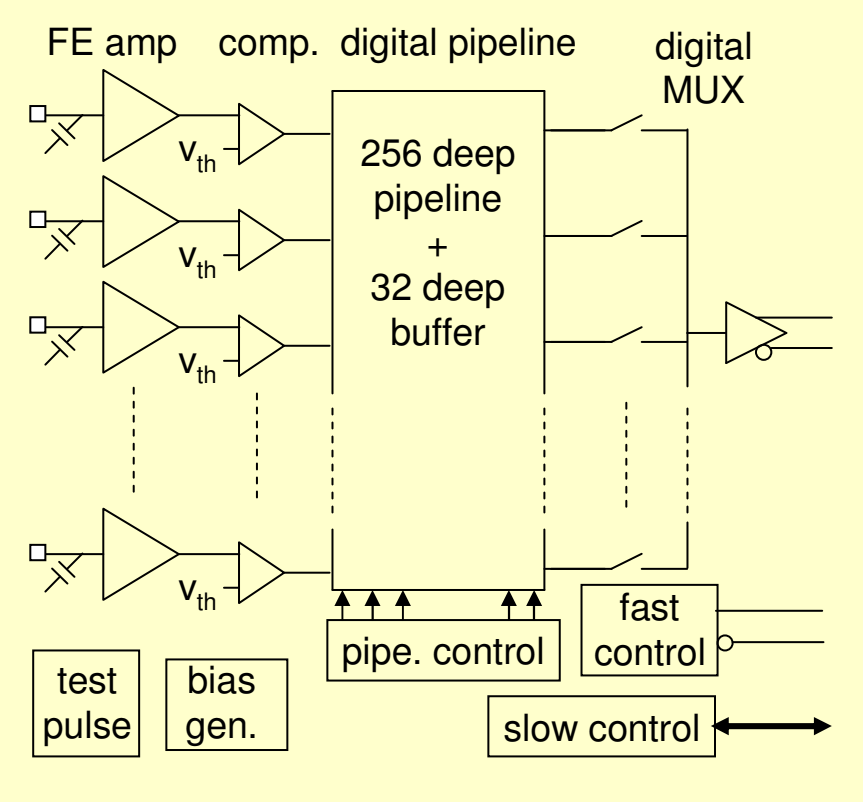
signal polarity: -ve (n-side readout)
+ve now preferred
coupling: DC (or AC)
DC leakage: < 1μA
charge collection: < 10 ns
strip pitch: > 60 μm

front end and comparator

pulse shape: 20 nsec peaking time
time-walk: < 16 nsec
overload recovery: < 2.5 usec
noise: < 1000e for 5 pF and 1 μA

digital

latency: up to 256
event buffering: up to 32
attention to SEU tolerance



power

supplies: 1.2 Volts analog, up to 1.2 Volts digital
consumption: <0.5 mW/channel for C_{SENSOR} 5 pF
rejection: as good as possible (expect to be powered by DC-DC converters)

EXTRA

CBC estimated power consumption

	power/FE chan.	
preamp/postamp		
20 nsec peaking time, short strips C_{SENSOR} ~ 5pF (~ 100 + (15 x C_{SENSOR}))	180 µW	~ 200 µW analogue
comparator		
estimate (preliminary simulations)	20 µW	
digital		
take 0.25µm APV25 (digital 400 µW) /10 for technology, x3 for SEU (pessimistic? CBC logic should be simpler)	120 µW	~ 300 µW digital
output		
LV differential ~ few mW / 128 chans.	30 µW	
contingency		
just guess nominal figure to bring overall power to 0.5 mW	150 µW	

0.5 mW / channel seems like an achievable target (c.f. 2.7 mW for APV25)

digital is biggest uncertainty, and maybe largest contributor
hope to improve estimate as design progresses
- can consider running at lower voltage (dig. power ~ V^2) => extra contingency
  - e.g. 1.2 -> 0.85 power consumption halved
- will keep power rails separate on chip to keep option open

using numbers above: 128 chan. chip needs ~ 20 mA analogue, ~30 mA digital

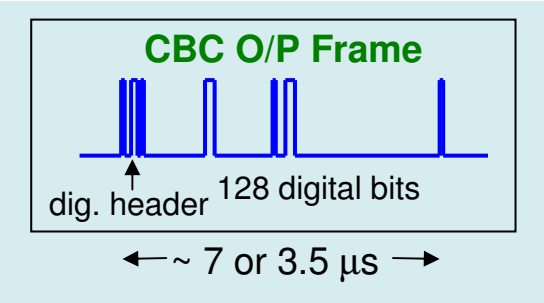
Miscellaneous

Comparator threshold adjust

global value + 4-bit trim per channel (80 mV range, 5 mV lsb – cf ~50 mV / fC)

Output format

"similar to APV" – digital header followed by 128 bits
20/40 Mbps selectable
frame appears promptly on triggering
=> no wait for APSP cycling => no tick marks

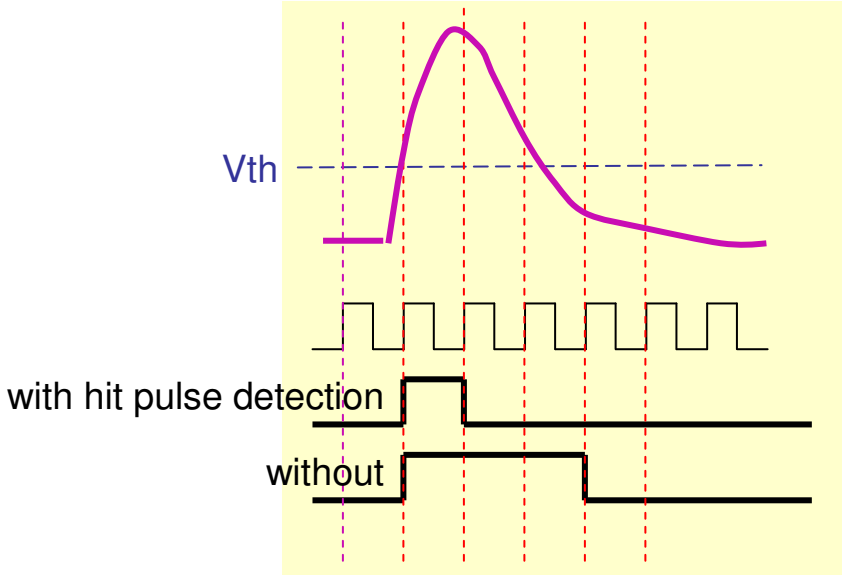


Test pulse

an "APV-like" system is planned
(variable phase, variable amplitude)

Hit pulse detection disable

allows length of time pulse shape over comparator threshold to be measured (in clock cycles)
can vary test pulse amplitude, time of injection and comparator threshold
allows diagnosis of pulse shape



Bonding technology

It is assumed that the first prototype chip will be designed for wire-bonding.

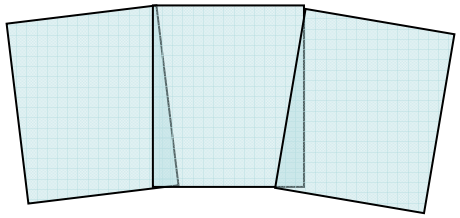
Progress in modelling modules for outer Tracker*

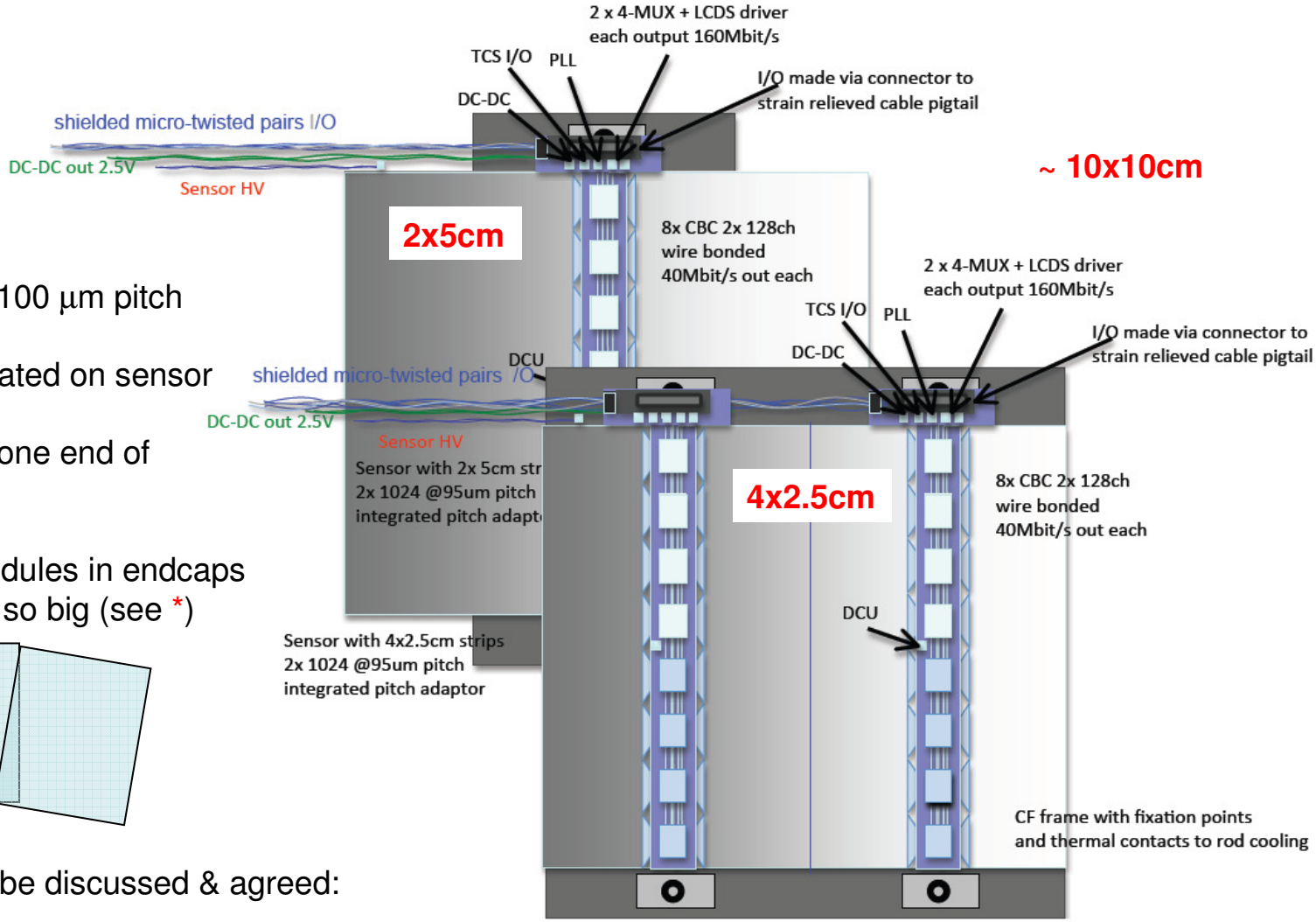
only 2 strip lengths
2.5 & 5 cm, ~100 µm pitch

pitch adapter integrated on sensor

DC-DC, PLL, … at one end of hybrid

could use same modules in endcaps
overlap penalty not so big (see *)





many details yet to be discussed & agreed:

DC-DC architecture, 128 vs 256 chan CBC, constructional details, bonding technology choices, cooling, electrical interface choices, …..

* from D.Abbaneo: http://indico.cern.ch/getFile.py/access?contribId=1&sessionId=2&resId=0&materialId=slides&confId=47298