# CBC status

last detailed report on electronic performance in May tracker week
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC_Tracker_Electronics_May_11.pdf

will not repeat details here, but briefly summarize

since then most of effort on tests with sensors
lab with beta source
recent test beam

progress on definition of next chip iteration for 2S-Pt modules

Tracker Phase 2 Upgrade Electronics, Oct. 2011.
Mark Raymond, Imperial College

# CBC overview

**features**

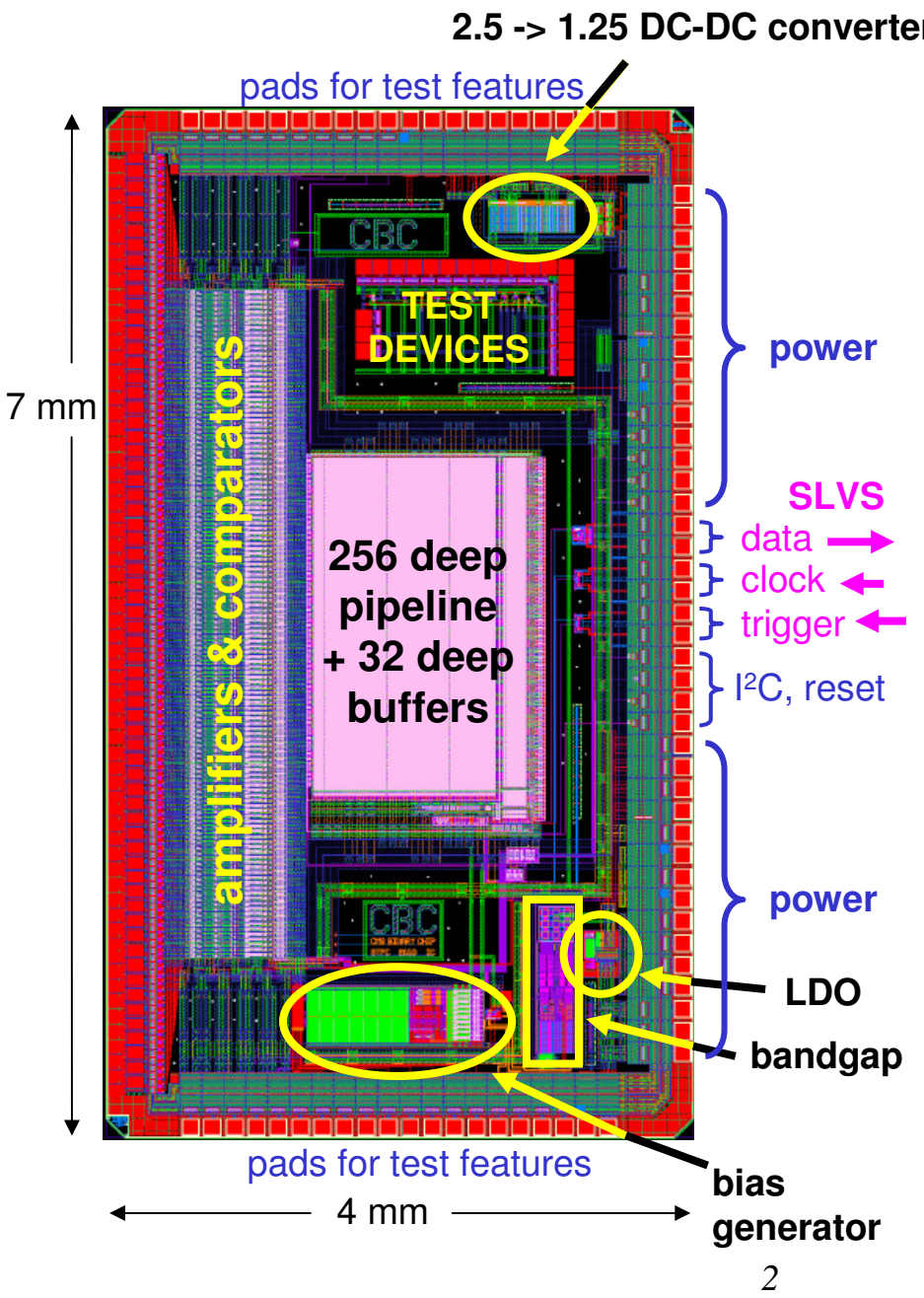
- designed for short strips, ~2.5–5cm, < ~ 10 pF
- full size prototype - 128 channels
  - 50 μm pitch wirebond
- binary un-sparsified readout
- powering test features
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analog FE

**main functional blocks**

- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- fast (SLVS) and slow (I2C) control interfaces

**front end**

- DC coupling to sensor – up to 1 uA leakage
- can be used for both sensor polarities



# CBC under test

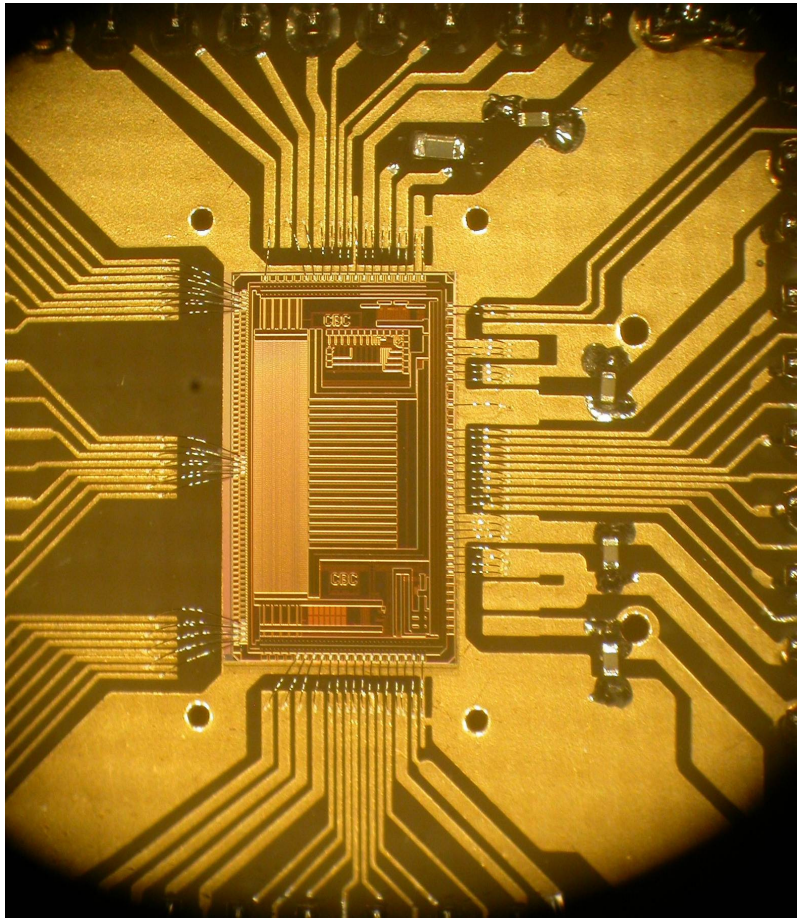
produced in IBM 130 nm CMOS process

2010 CERN MPW run

chips on test bench since Feb. 2011

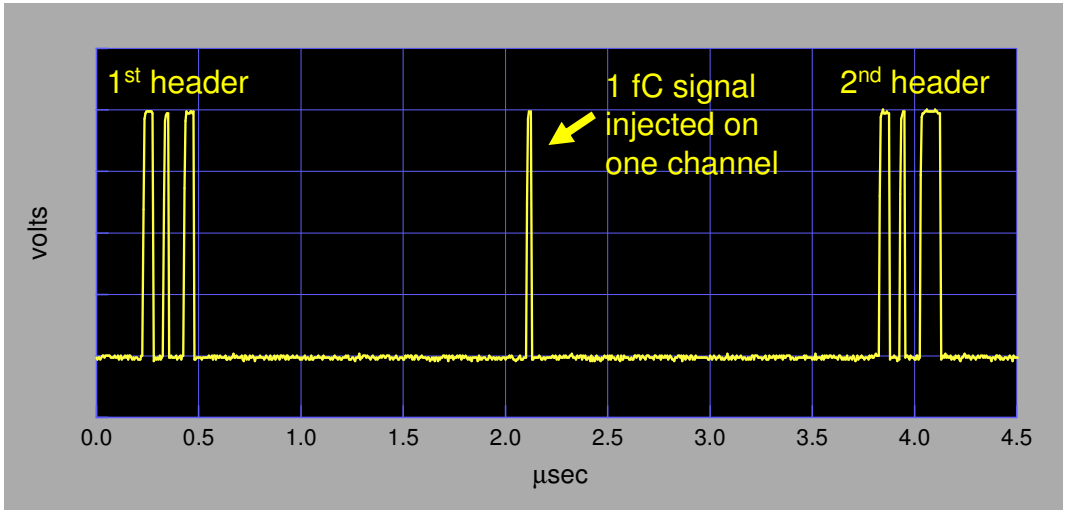
fully functioning chip

a few workarounds needed for biasing issues
(see previous talk)

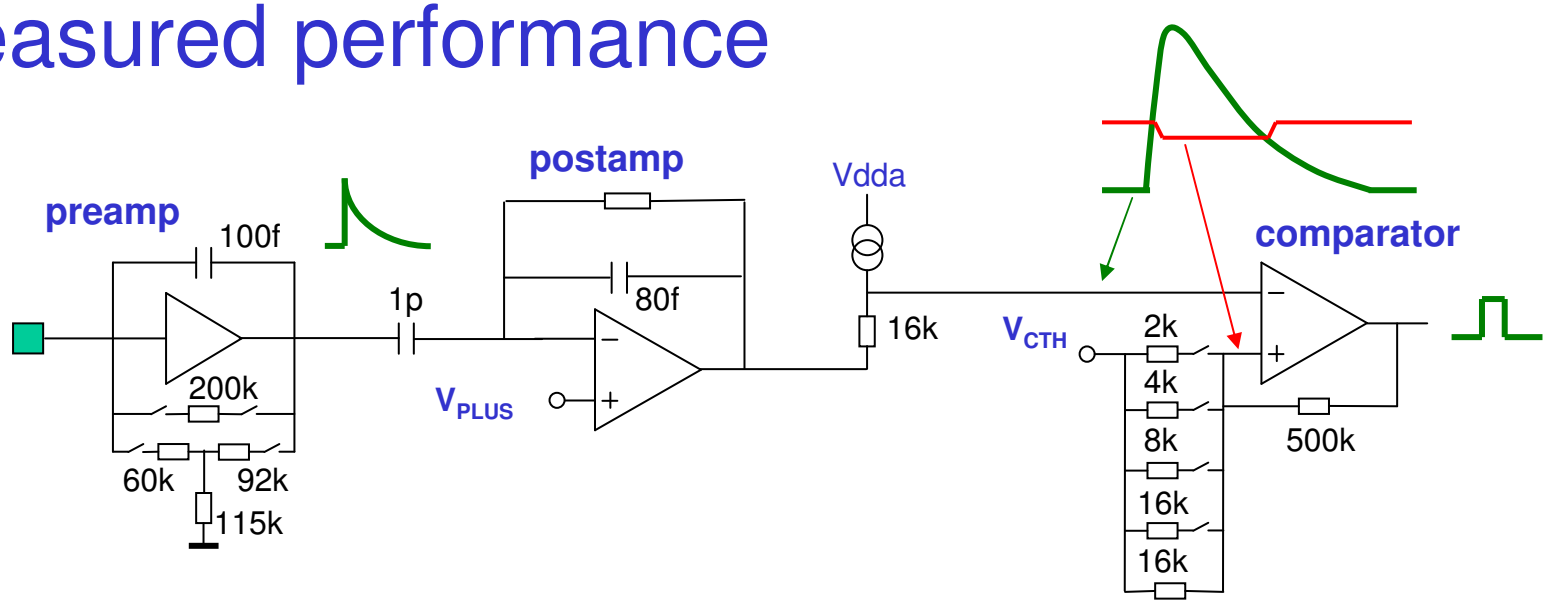


CBC on test board

**2 consecutive data frames (2 triggers)**



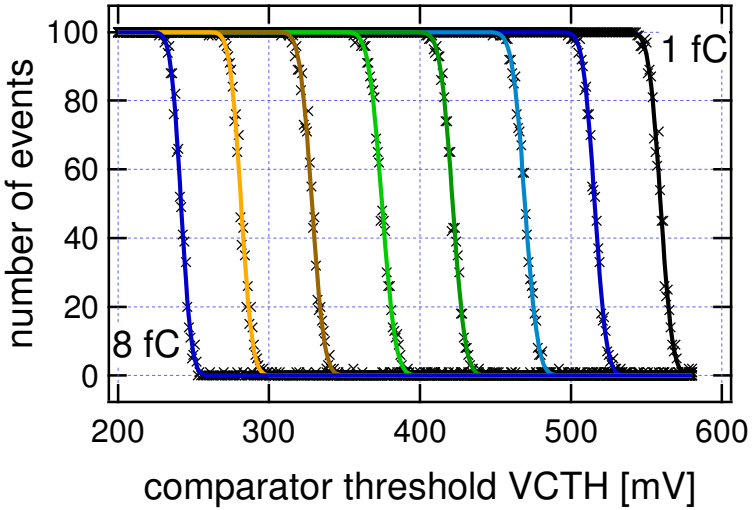
# measured performance



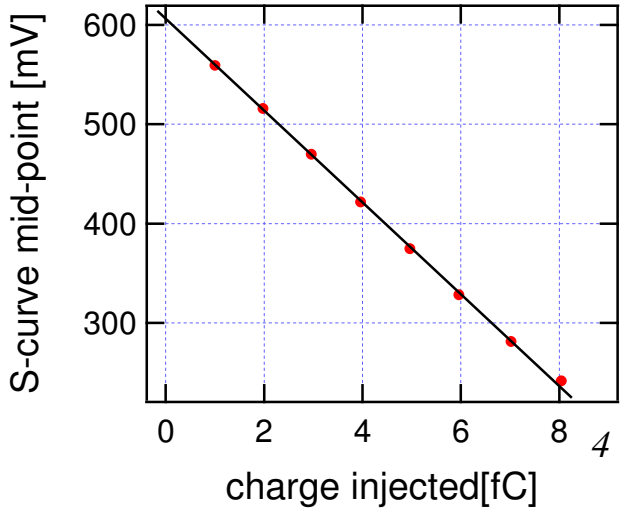

**preamp**: leakage tolerance 1μA verified, both polarities

**postamp**: gain: ~ 50 mV / fC

**s- curves for signals in range 1 - 8 fC : 1 fC steps**




**gain**



# comparator

**thresholds**

before tuning pk-pk threshold spread ~30 mV (~ 0.6 fC)

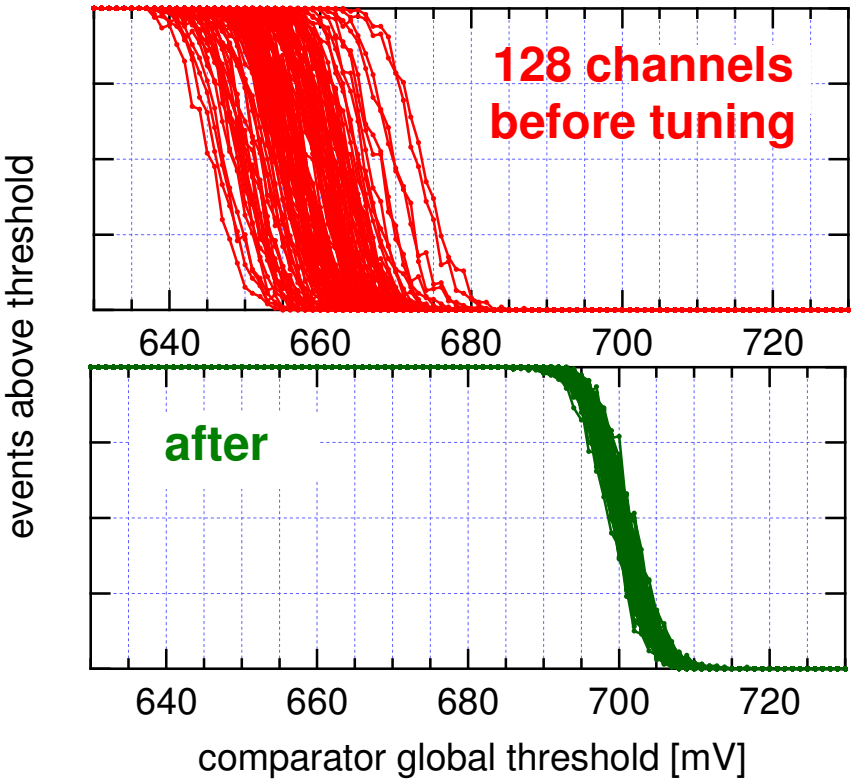
tuning reduces spread to ~ mV level

**timewalk**

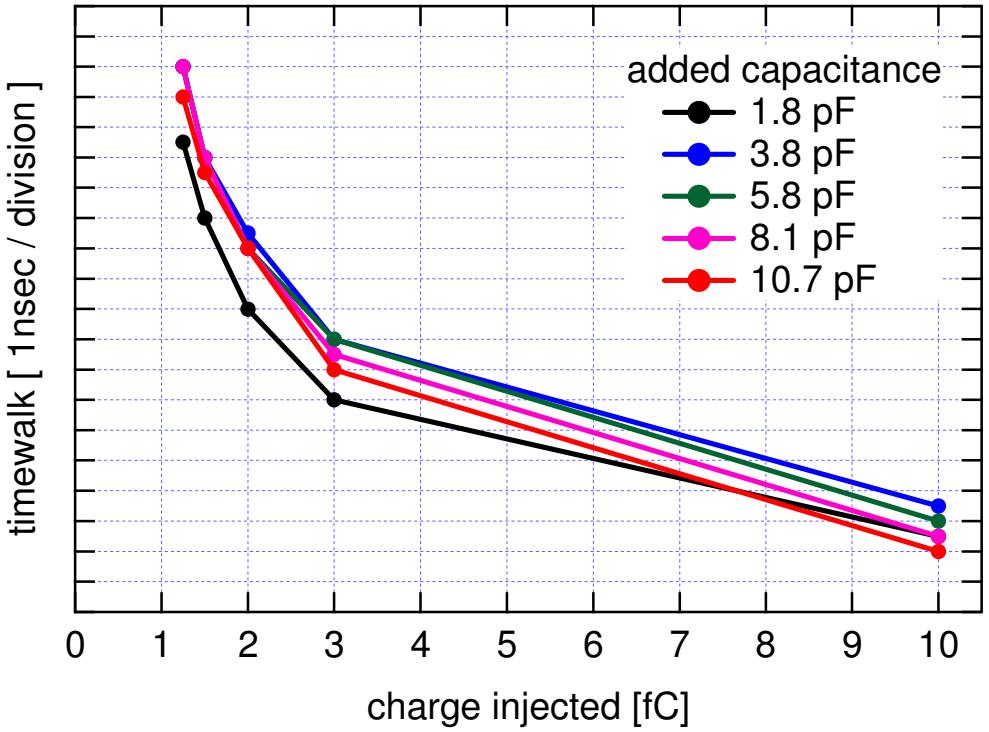
timewalk spec. < 16 ns between 1.25 and 10 fC signals, with comp. threshold set to 1 fC

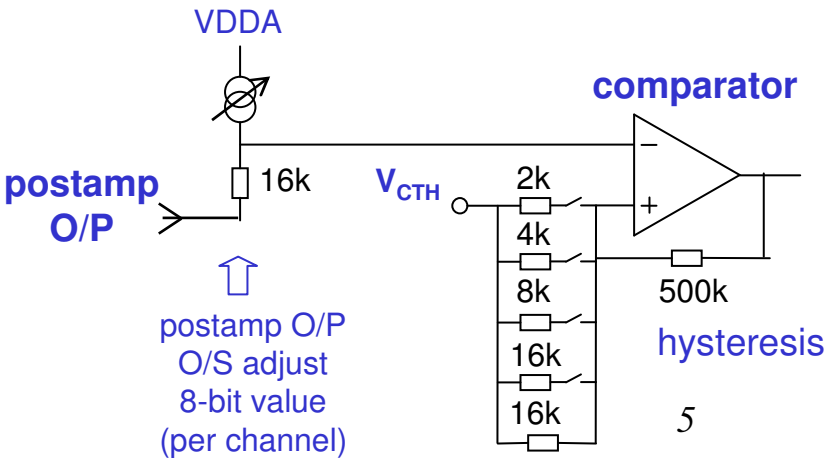
measurements just within spec.

**threshold uniformity**




**timewalk: threshold at 1 fC**



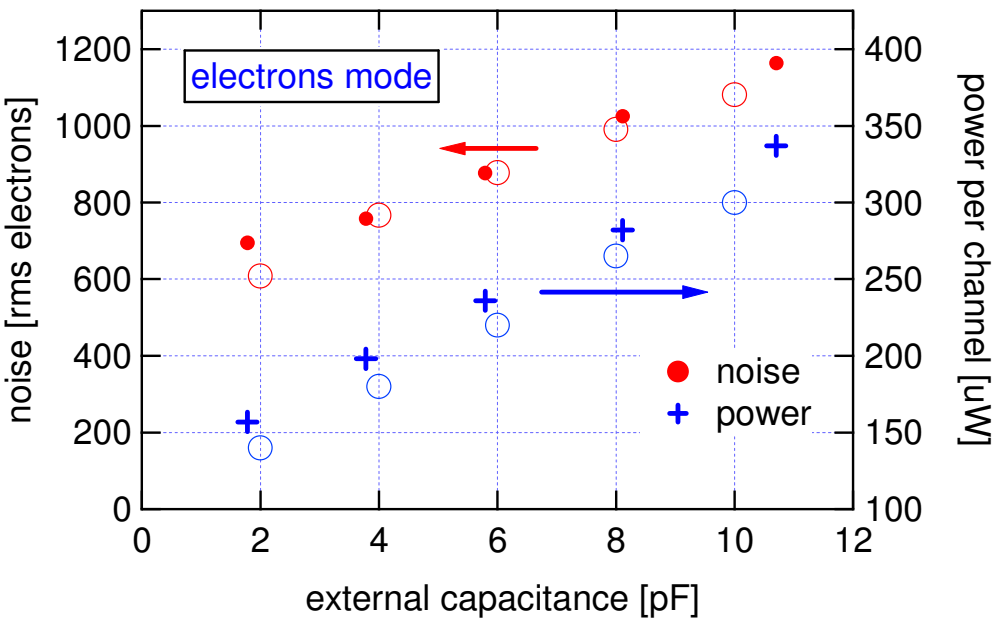
# noise and power

**measurement technique**

vary current in input transistor to keep pulse shape independent of C

=> analogue power consumption depends on C

close agreement between measurements (solid symbols) & simulations (open circles)




**results**

noise (rms electrons): ~ 500 + 64 / pF
**analogue power**: 130 + 21 / pF  µW / channel

e.g. ~ 800e  noise for  analog power ~ 250 µW/chan  for 5 pF input capacitance

no significant difference between electrons and holes modes

**overall power**

**digital:** $I_{VDDD}$ = 2.8 – 4.5 mA for whole chip  (depends on SLVS bias setting) **< 50 µW / channel**

**total:**

**180 + (21 x $C_{SENSOR}$[pF])  µW / channel**

**e.g. < 300 uW /channel  for 5 pF sensor capacitance**

# power features

### DC-DC switched capacitor converter

converts 2.5 -> ~ 1.2

clearly functioning

effect of switch noise needs careful study

### LDO linear regulator

provides clean,regulated rail to analog FE

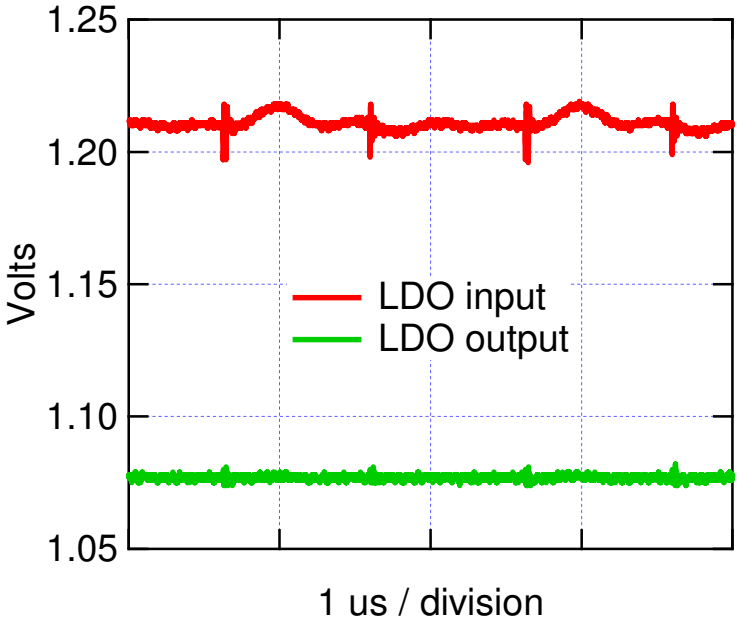
~ 1.2 Vin, 1.1 Vout

dropout ~ 40 mV for 60 mA load

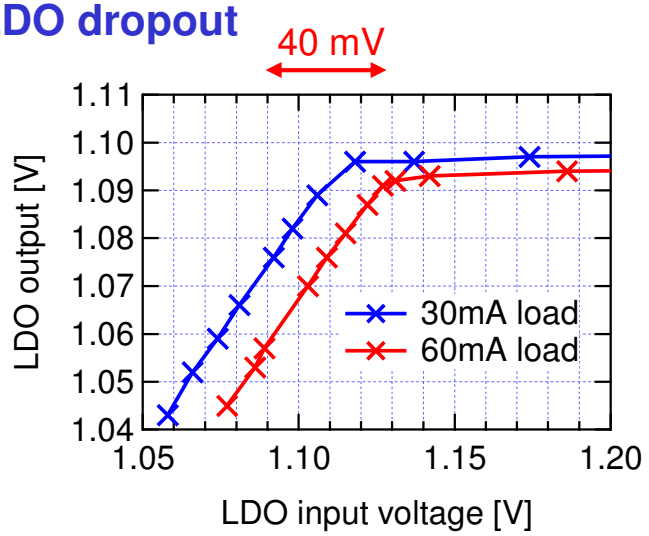
provides > 30dB supply rejection up to 10 MHz

(see May talk for more detail)

### DC-DC & LDO outputs



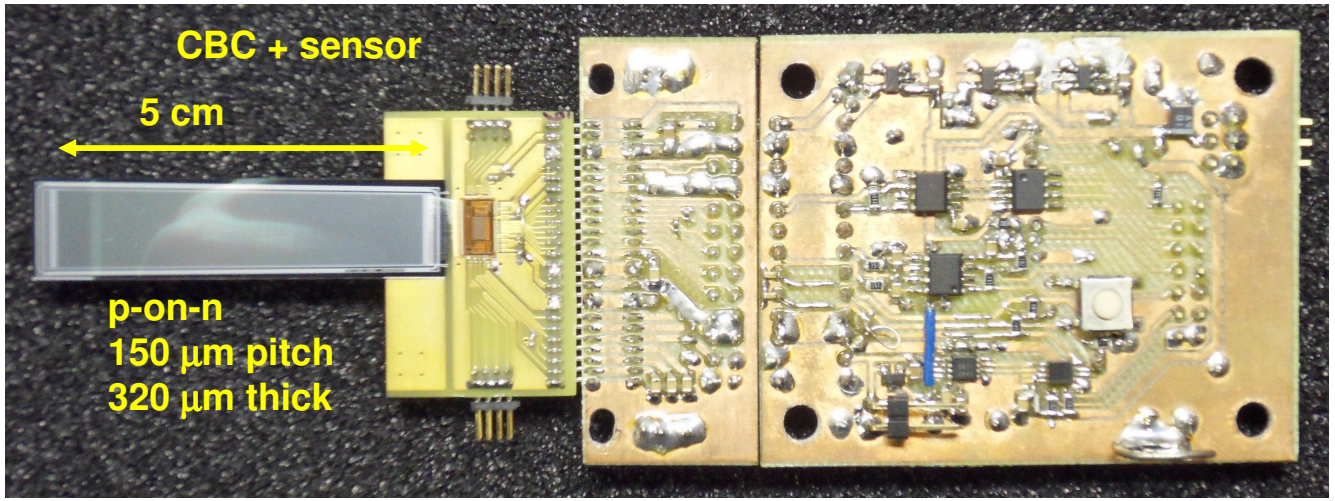

### LDO dropout



# results with sensors

preparations for (and tests with) sensors have dominated activities in recent months

**CBC module**

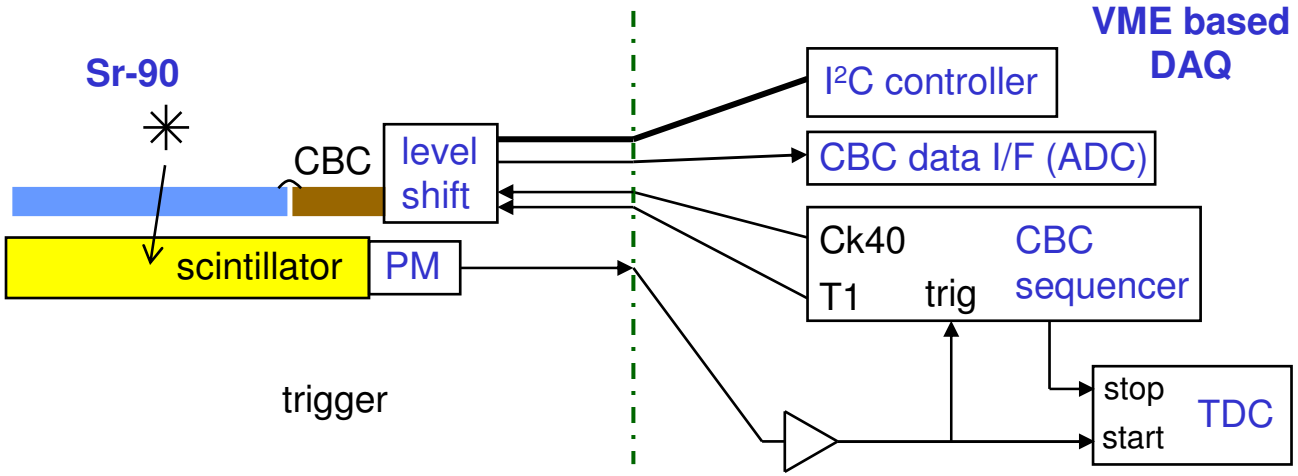



interface card for level shift and power supply

all signals LVDS
I2C at 5 / 3.3V levels

+/- 5V & sensor bias

**lab system for source measurements**




need TDC to timestamp scintillator trigger

can then select appropriately timed signals by TDC value

# beta source results

**method**

choose comparator threshold (programmable)

count number of clusters in CBC output signal for fixed number of scintillator triggers

repeat for range of comparator thresholds

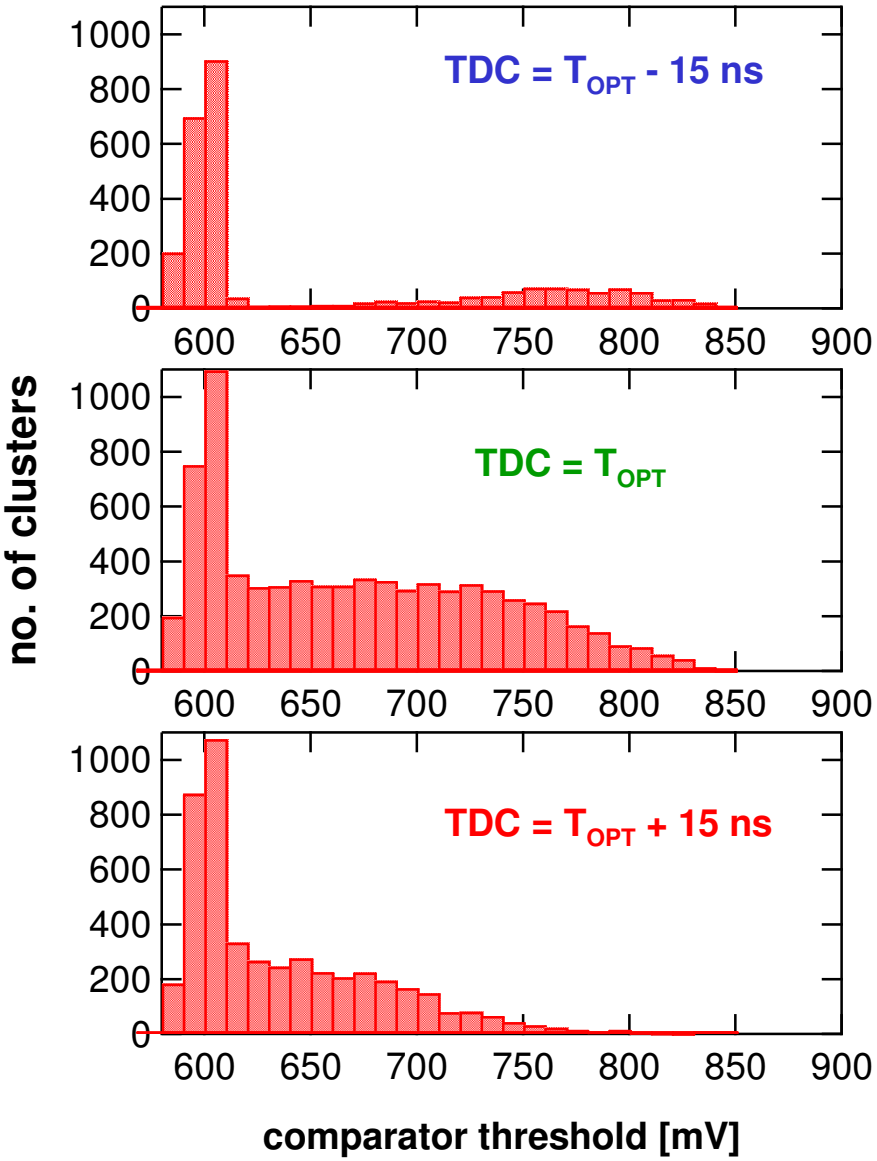
plot no. of clusters vs. comparator threshold →

shape depends on signal arrival time (TDC value)

need to select events by TDC value so that triggered timeslice contains all signal sizes ($T_{OPT}$)

if select signals occurring too early/late then get spectrum where some signals fire comparator in previous/subsequent timeslice

(see backup slides for more detailed explanation of histogram shapes)



# beta source - landau fitting

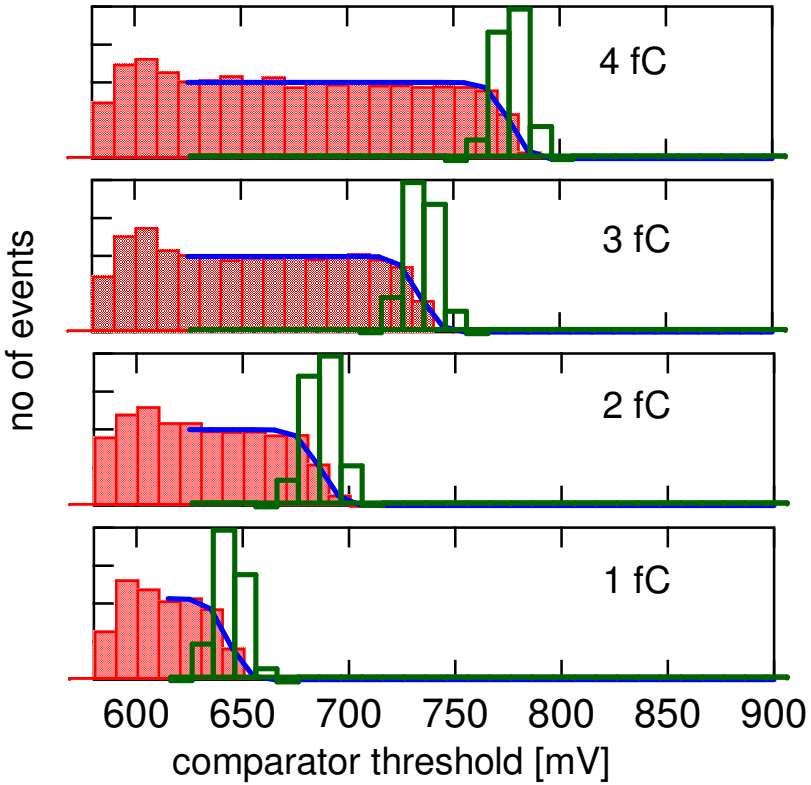
can fit raw data with curve generated from Landau distribution

compare most prob. signal size with electronic test charge injection

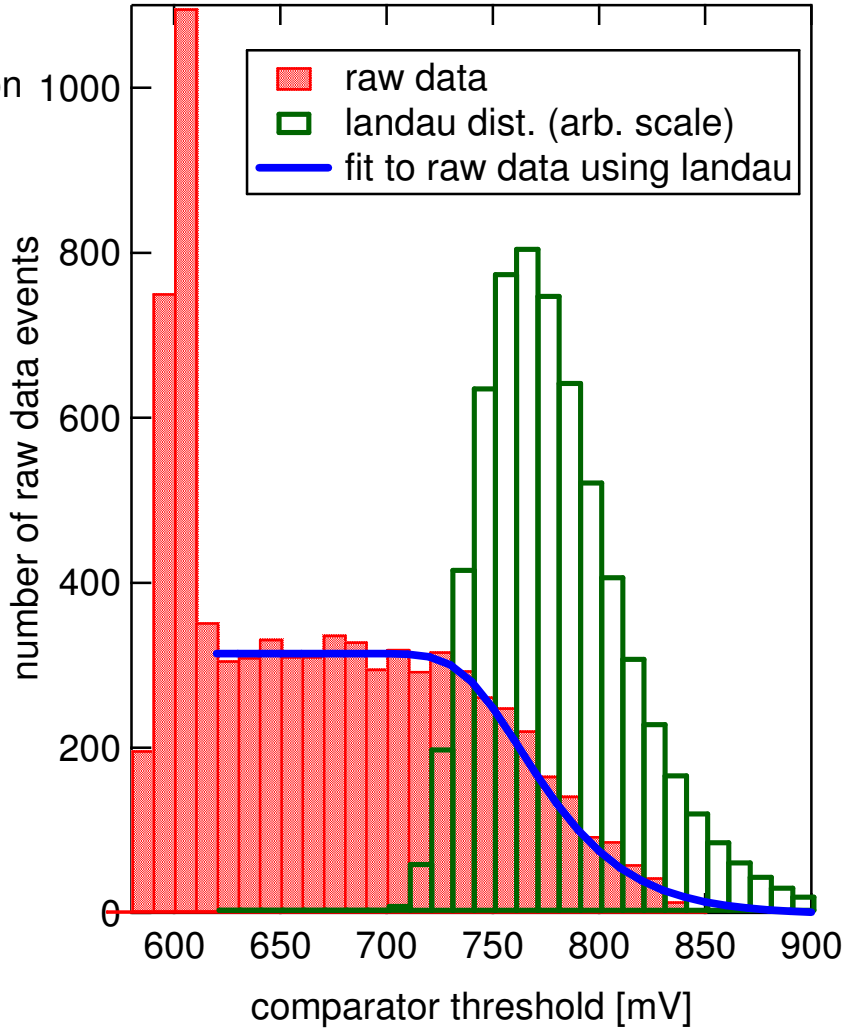
-> most prob. signal value ~3.7 fC (23,000 e)

840 electrons noise

**electronic charge injection**




**Sr-90 source**



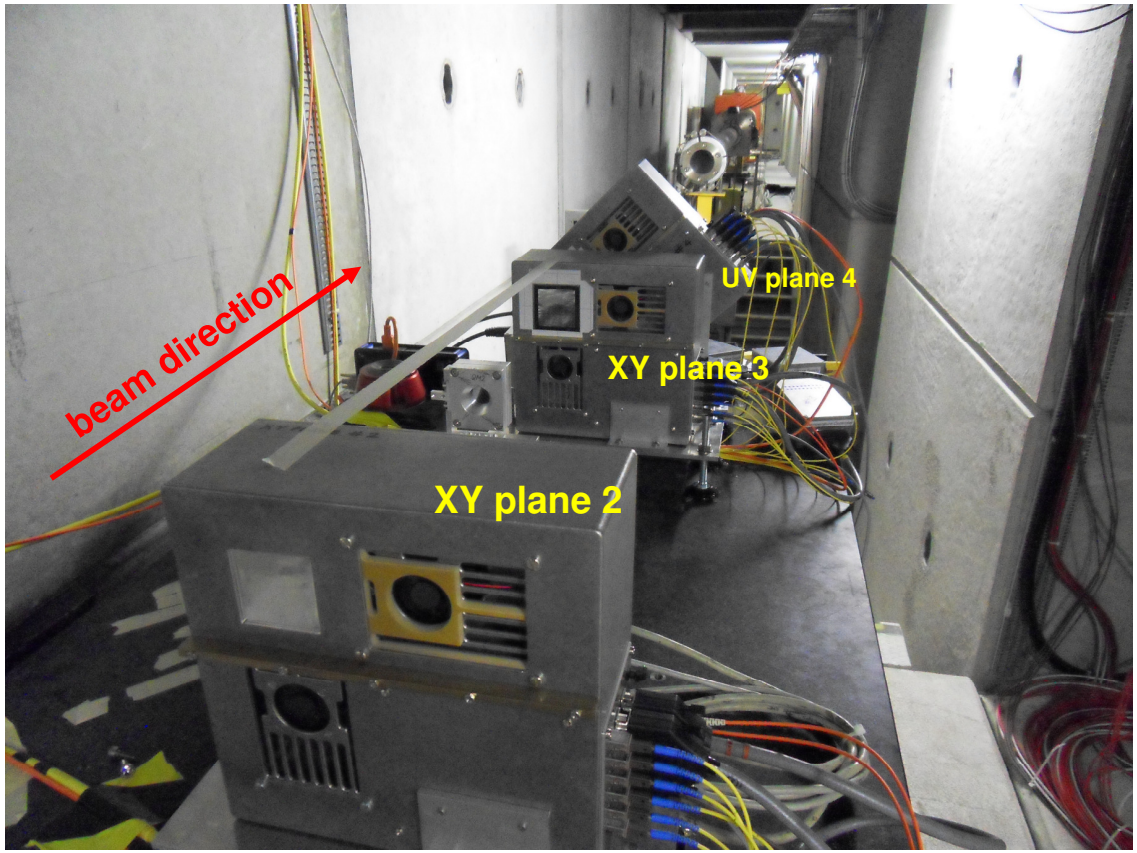
# test beam

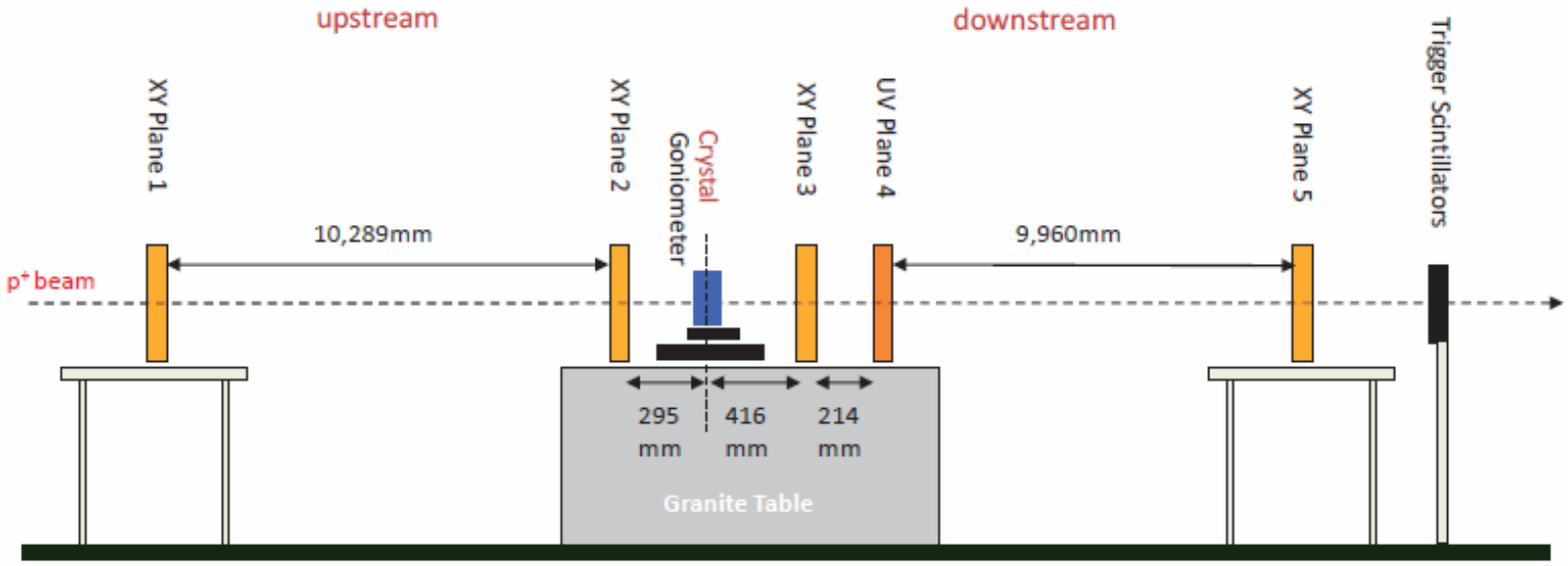
CBC module operated parasitically
in UA9 crystal collimation test beam
- September, 2011

H8 beam line, 400 GeV protons

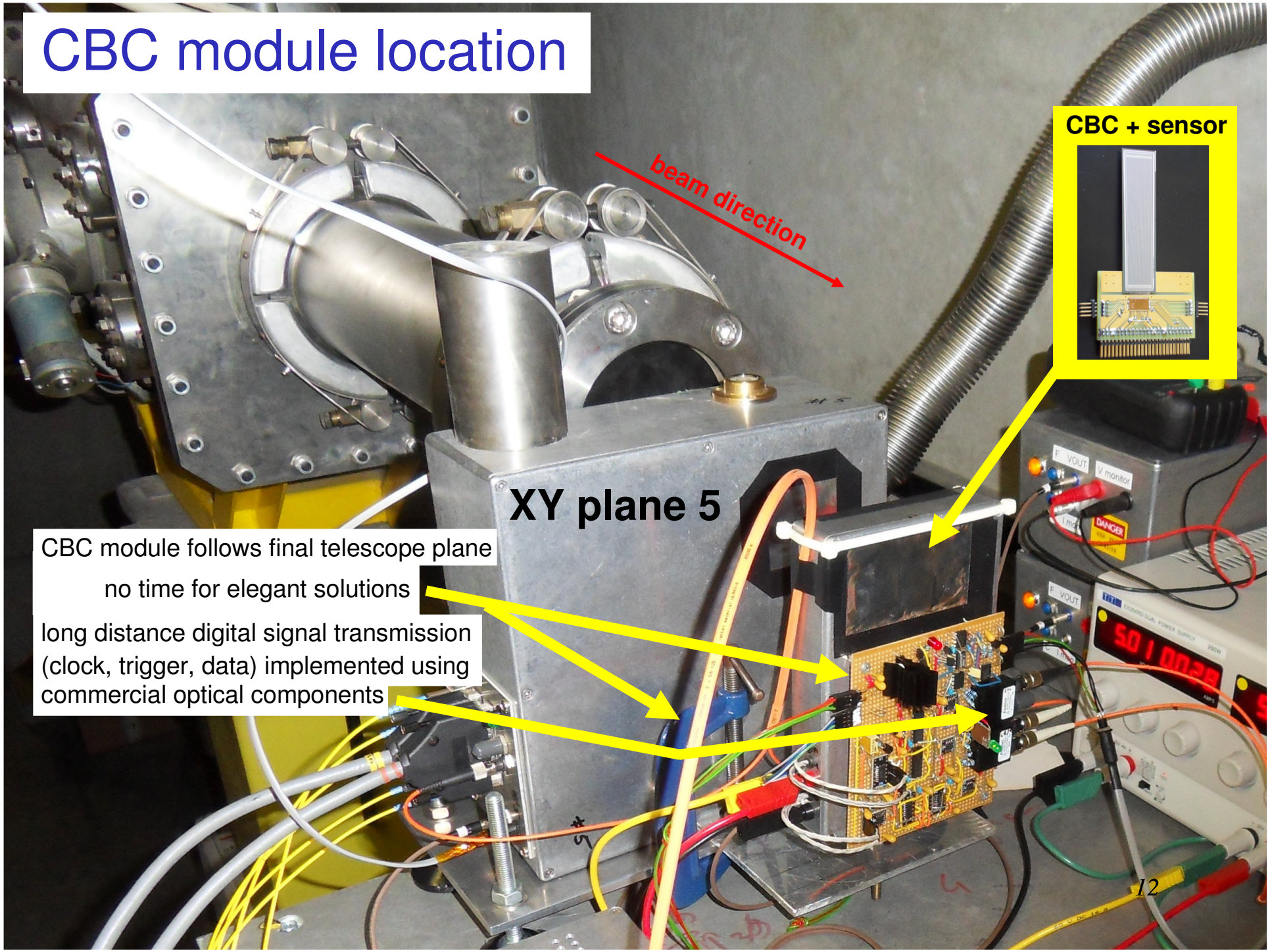
UA9 telescope implemented using CMS tracker readout
- D0 sensors + APV
- analog optical link
- CMS FED,…
- CMS DAQ software

for further details see:
M Pesaresi *et al* 2011 *JINST* **6** P04006

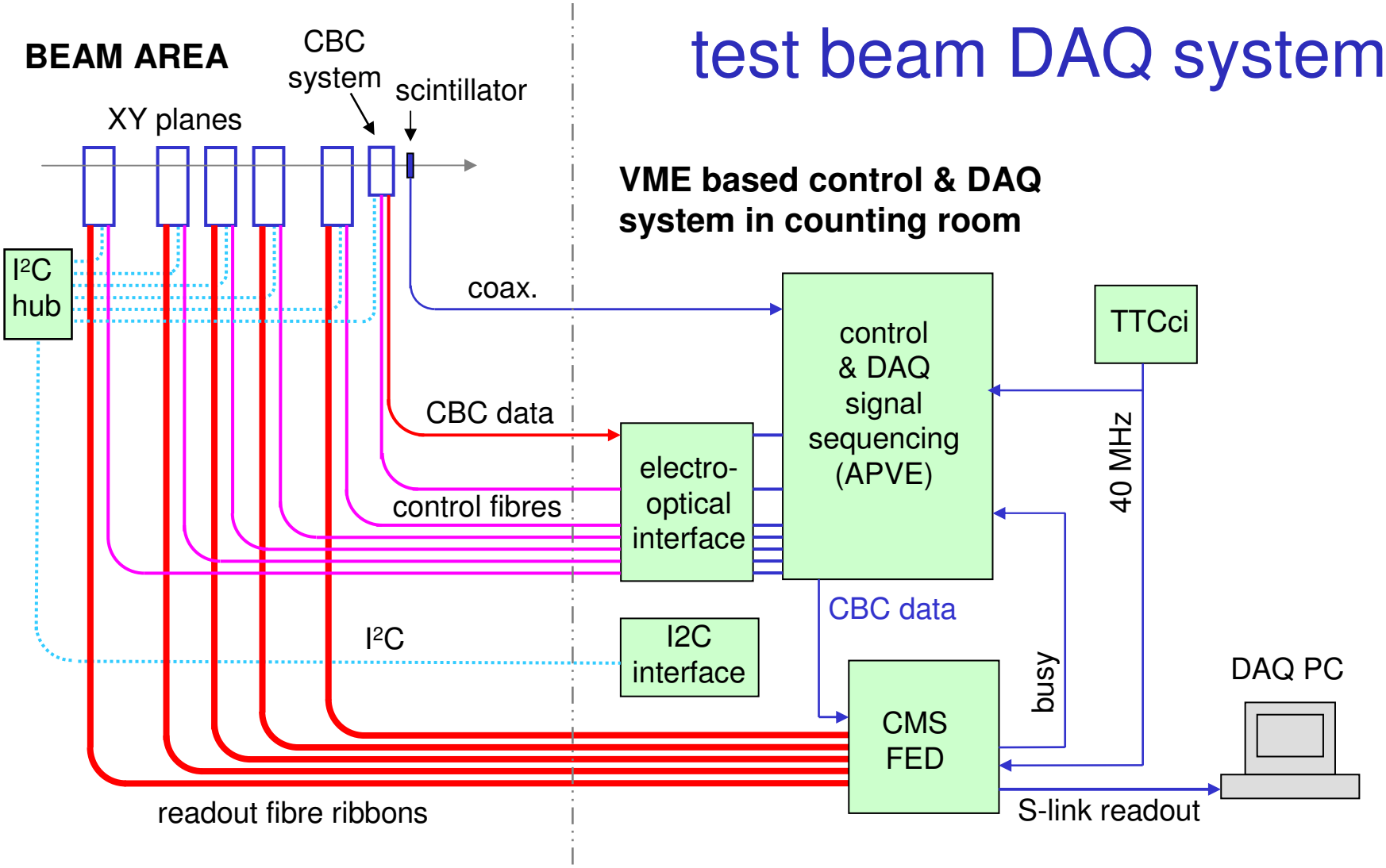


# CBC module location



# test beam DAQ system



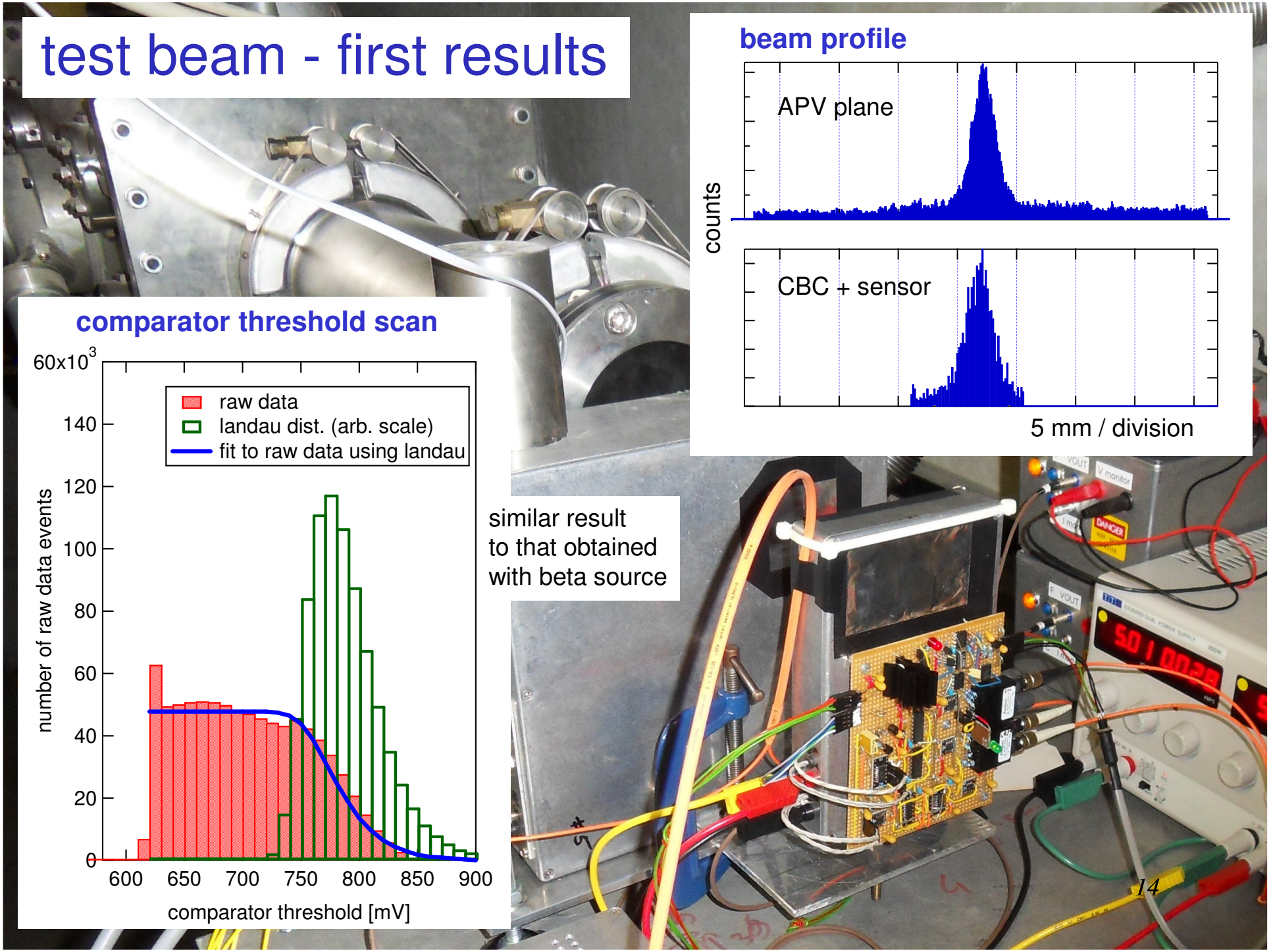

control and DAQ signal sequencing implemented in APVE FPGA board (also TDC functionality)
allows to delay & synchronize CBC data with APV - so FED sees CBC data as if from an APV

quite complicated thing to do but simplifies things from DAQ point of view

=> FED & DAQ can process CBC data as if from an APV (including zero suppression)

CBC data injected electrically into FED front end after optical receiver (before ADC)

# test beam - first results



**beam profile**

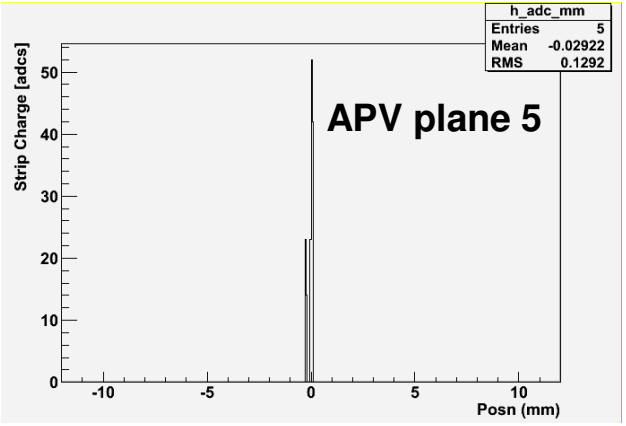



**comparator threshold scan**



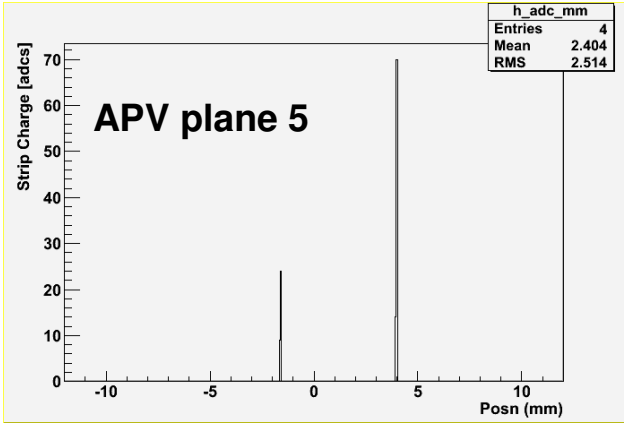

similar result
to that obtained
with beta source

# test beam - first results

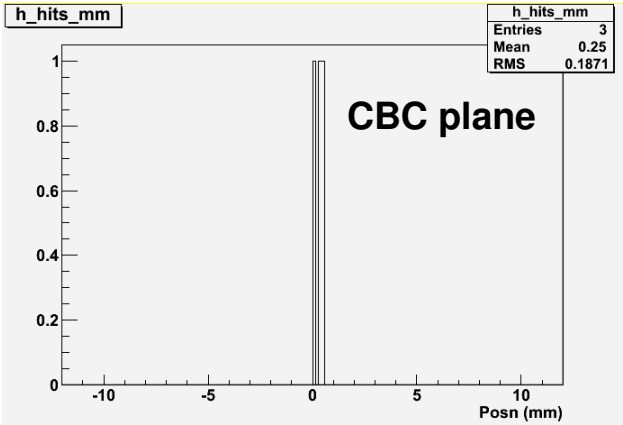



lots of data to look at

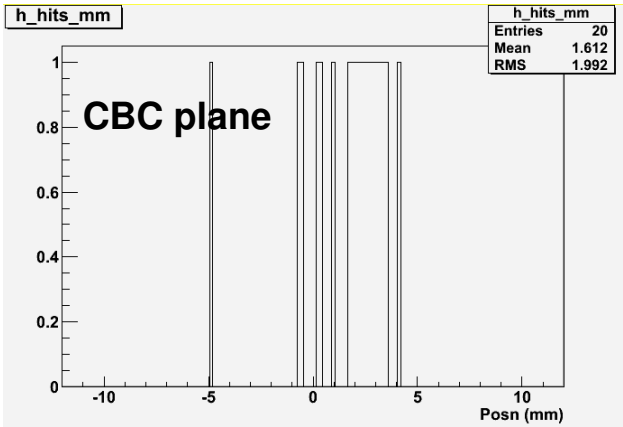
most events make sense like this one




some need better understanding

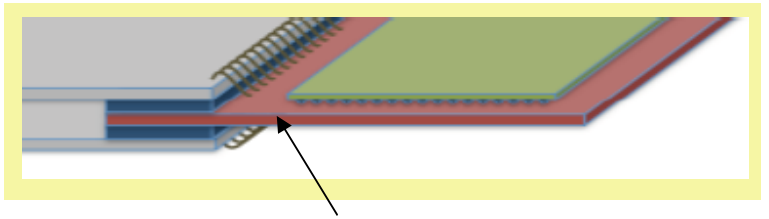



detailed study only just begun

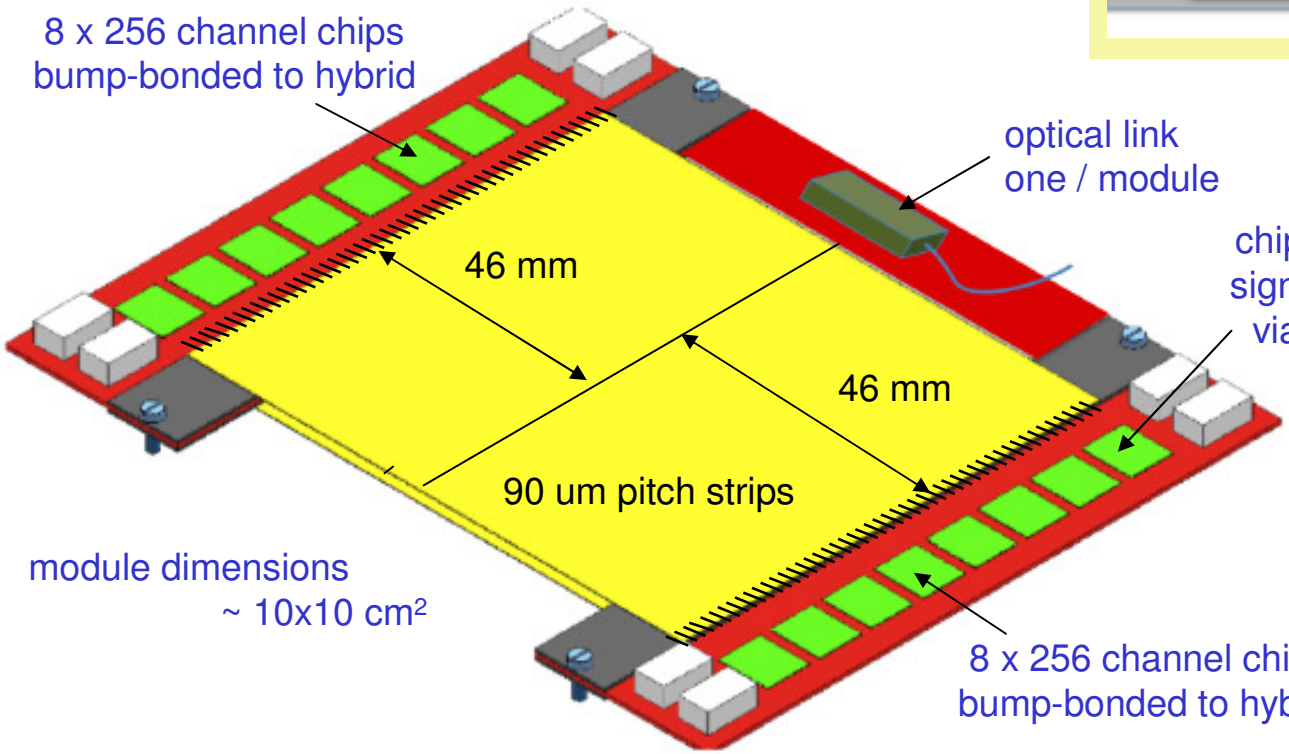



*plots provided by Will Ferguson (IC)*

# SS - Pt modules



sensors wire-bonded
above and below




"hi-tech" 2-in-1 module concept proposed for outer tracker layers
- bring signals from 2 strip (SS) sensor layers together in one chip
- look for cluster correlations to identify high Pt stub

plan to prototype logic to implement correlation in next CBC version
- allows to study issues involved with constructing such a module

=> 256 channel bump-bondable chip required

# next CBC version

design has begun
- 250 µm pitch C4 pads

some issues to confront:

- chip and hybrid design has to proceed in parallel - routing capabilities of substrate has impact on pad locations
  *(hybrid design - Georges Blanchot)*

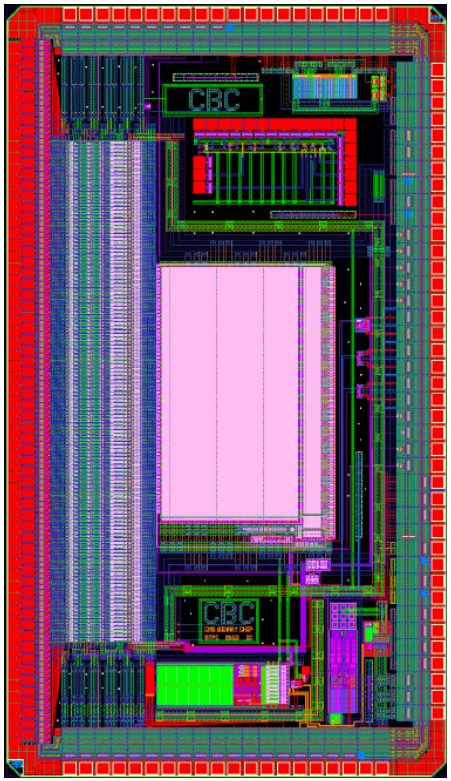
- how to test? - prototype and production

  - wafers for eventual bump-bond have to be kept in ultra-clean environment

  - but need to identify good chips for good multi-chip module yield

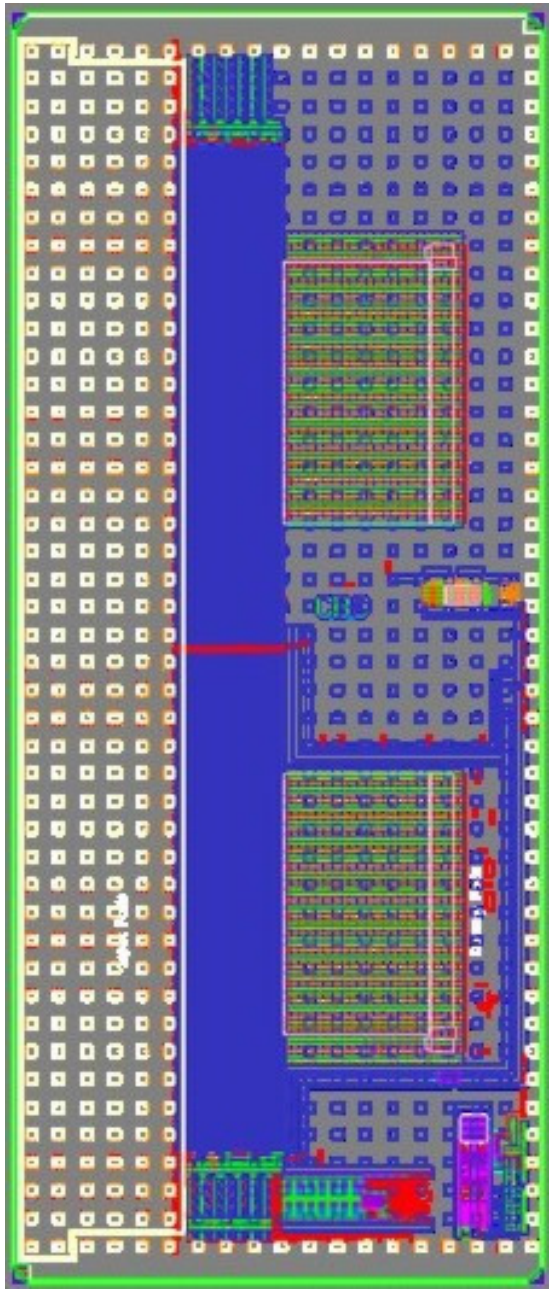
  - => wafer probing, but probably not possible in home labs

  - verify single chip performance on dedicated substrate - yield not important here




**existing chip**
128 channels
wirebond: 50 um pitch
7mm x 4mm

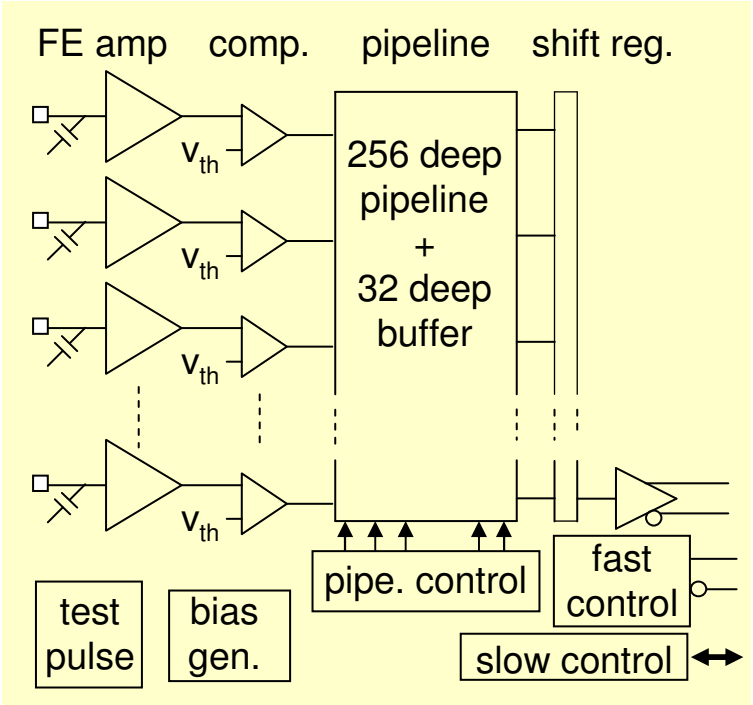
**next version**
256 channels
bump-bond: 250 um pitch
11.4mm x 4.75mm



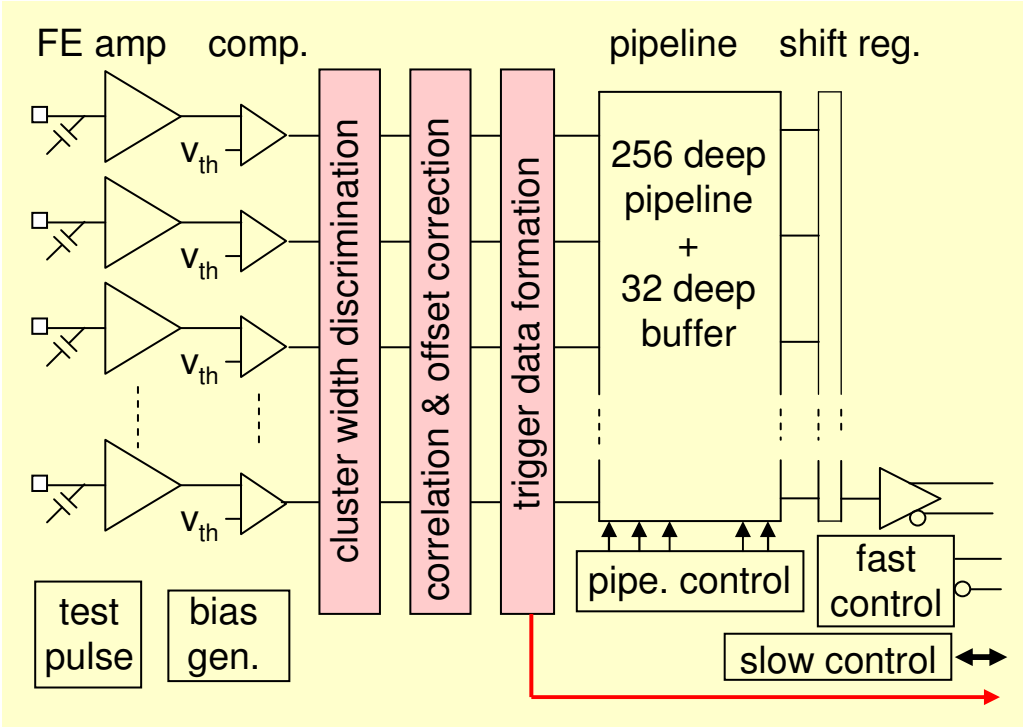
***layout by Davide Braga (RAL)***

# triggering logic

**current CBC**




**CBC + added triggering logic**




3 new blocks required

**cluster width discrimination**

simple logic to exclude wide clusters

**correlation & offset correction**

relatively simple logic to correct for phi offset across module and perform correlation

**trigger data formation and off-chip transmission**

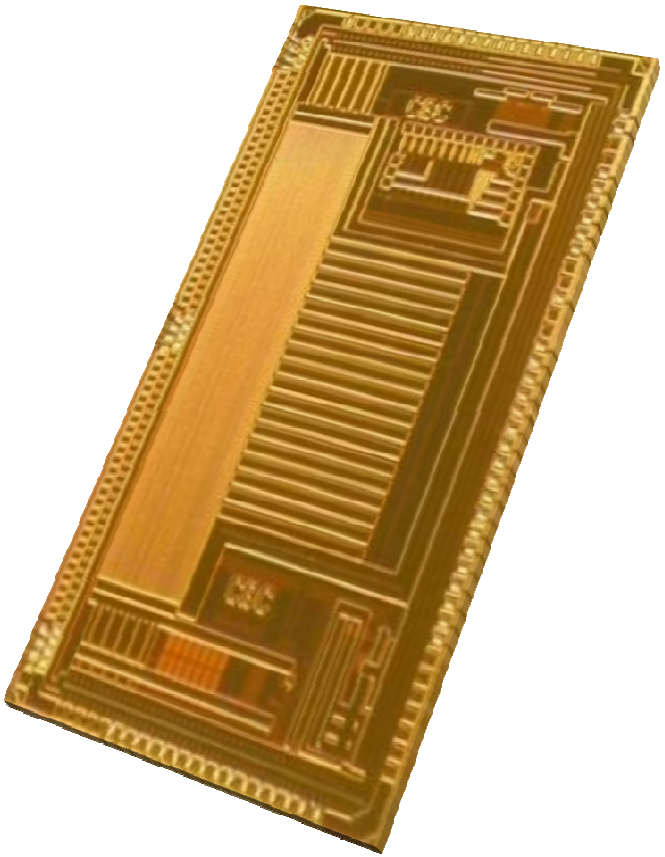
foreseen to be just simple OR for this chip version

=> 1 bit to signify high PT stub detected (no Pt stub address)

eventual requirements here still under consideration

synchronous or asynchronous options are possible

# summary



**CBC testing status**

tests with sensors have dominated activities in recent months
beta source measurements show results consistent with performance measured electronically

lab measurements also confirmed in test beam
further analysis of test beam data underway

**further chip testing**

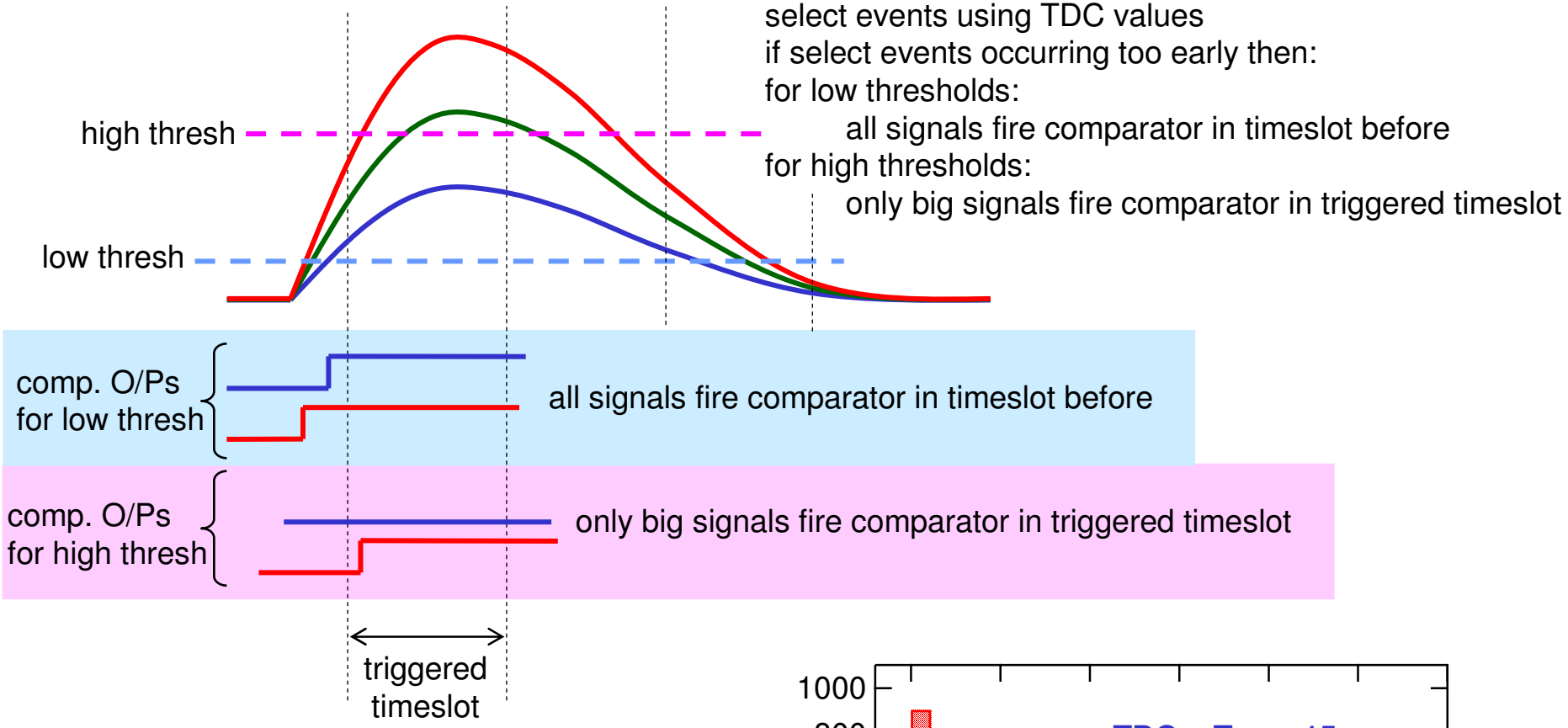
more detailed study of powering options
temperature effects
(work underway at Bristol - David Cussans)
radiation: ionizing and SEU

**next chip iteration**

plan to submit 256 channel bump-bondable version with triggering features, early 2012

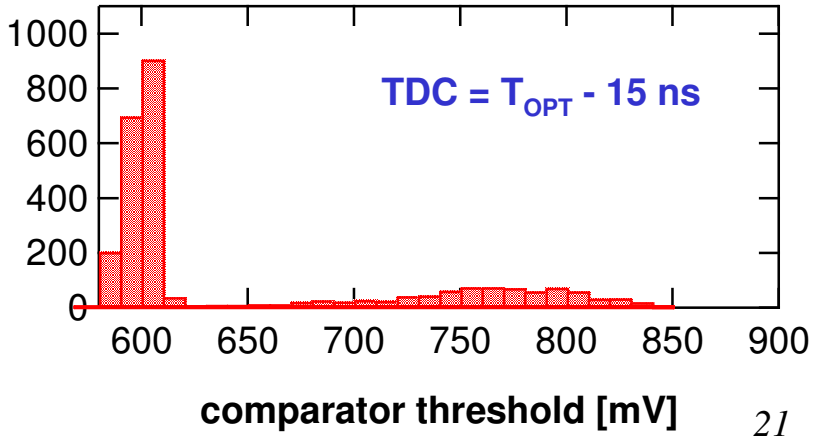
# extra slides

# comp. threshold scan explanation - early events

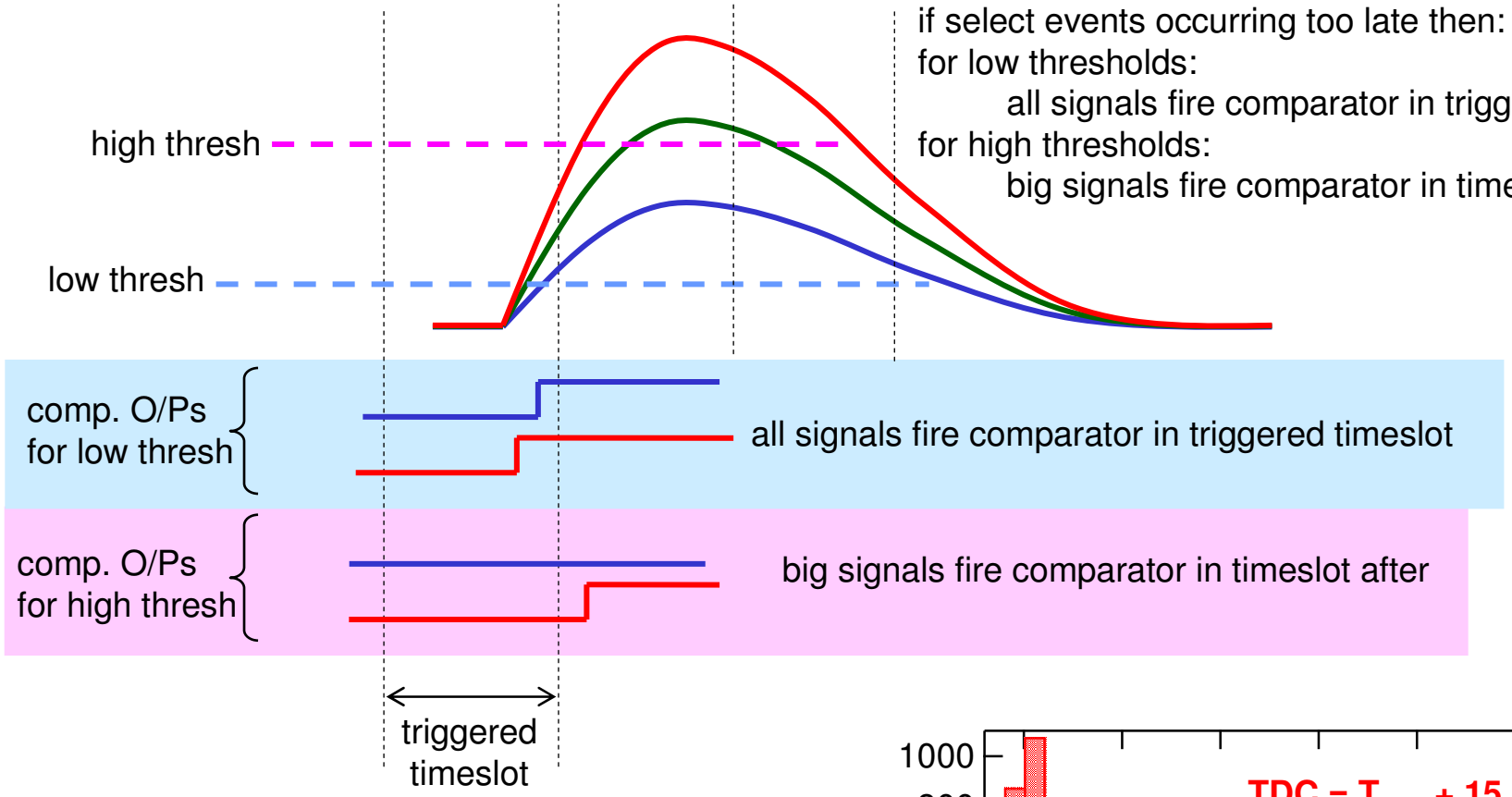



select events using TDC values
if select events occurring too early then:
for low thresholds:
all signals fire comparator in timeslot before
for high thresholds:
only big signals fire comparator in triggered timeslot

so counts inrease as comparator threshold increases →

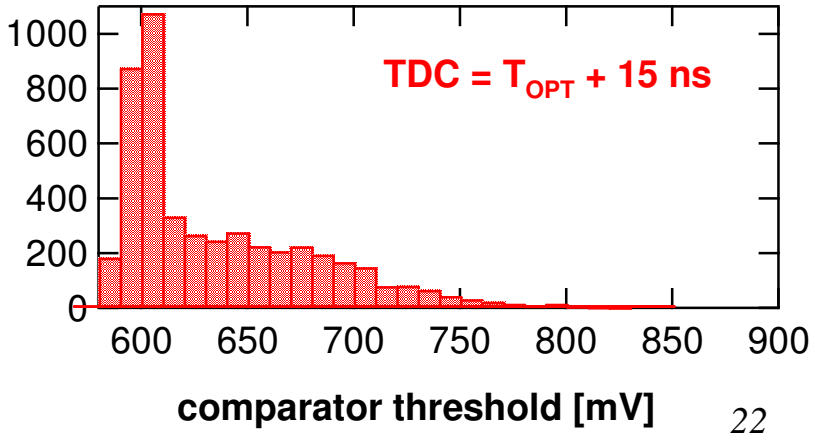


# comp. threshold scan explanation - late events

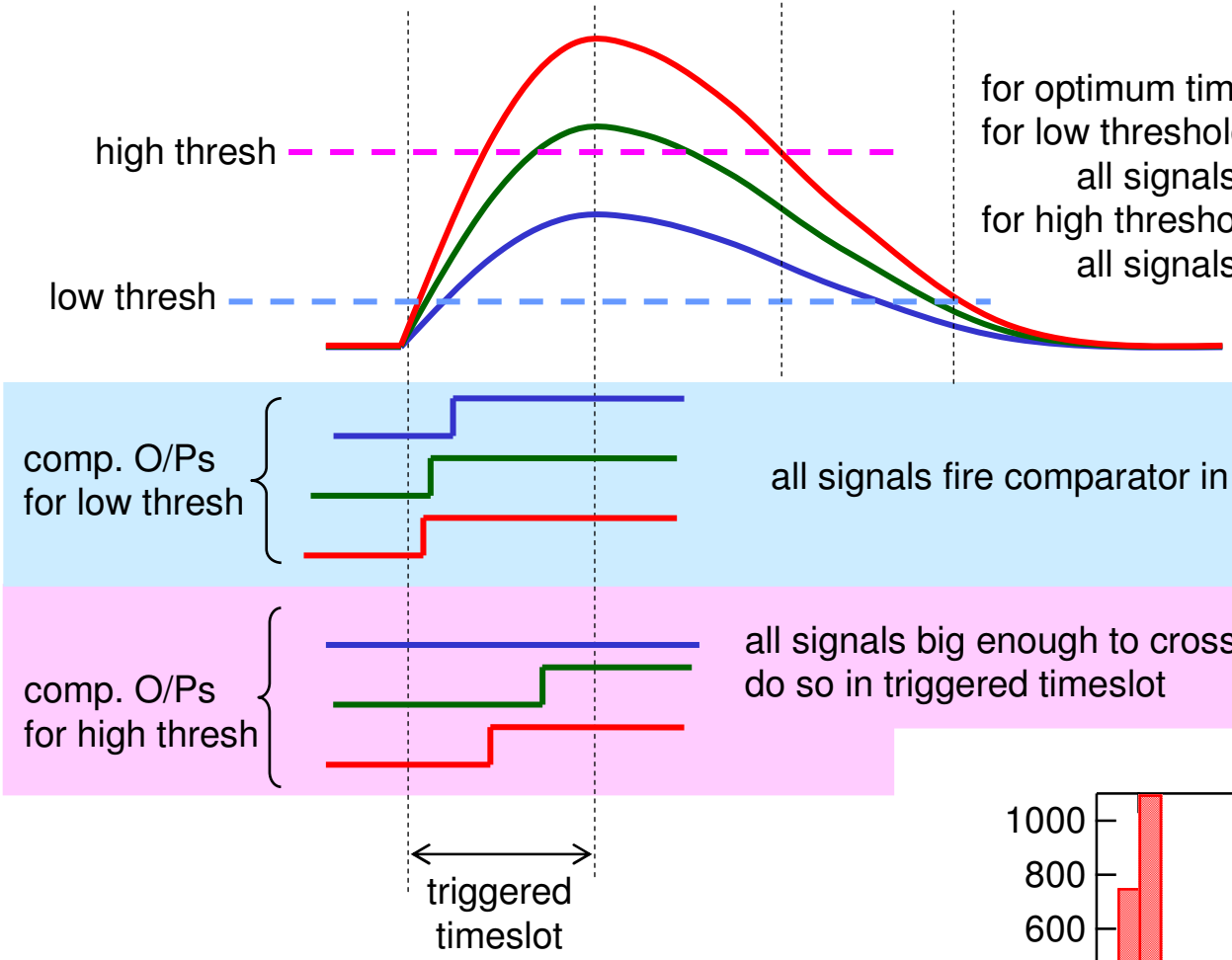



if select events occurring too late then:
for low thresholds:
all signals fire comparator in triggered timeslot
for high thresholds:
big signals fire comparator in timeslot after

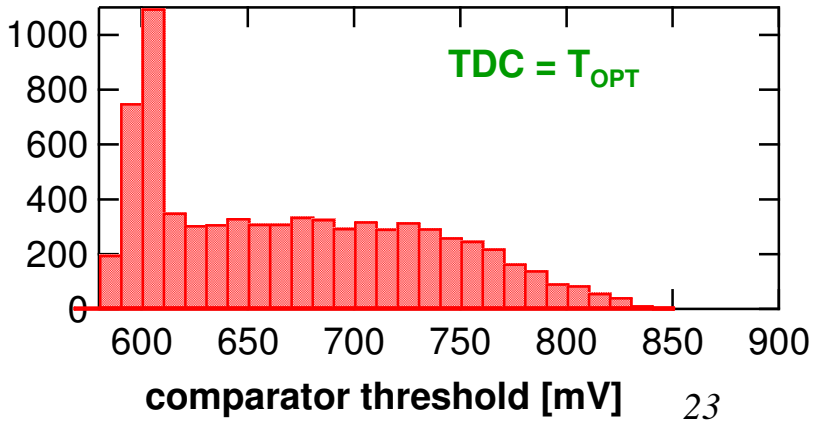
so counts drop quickly as comparator threshold increases →



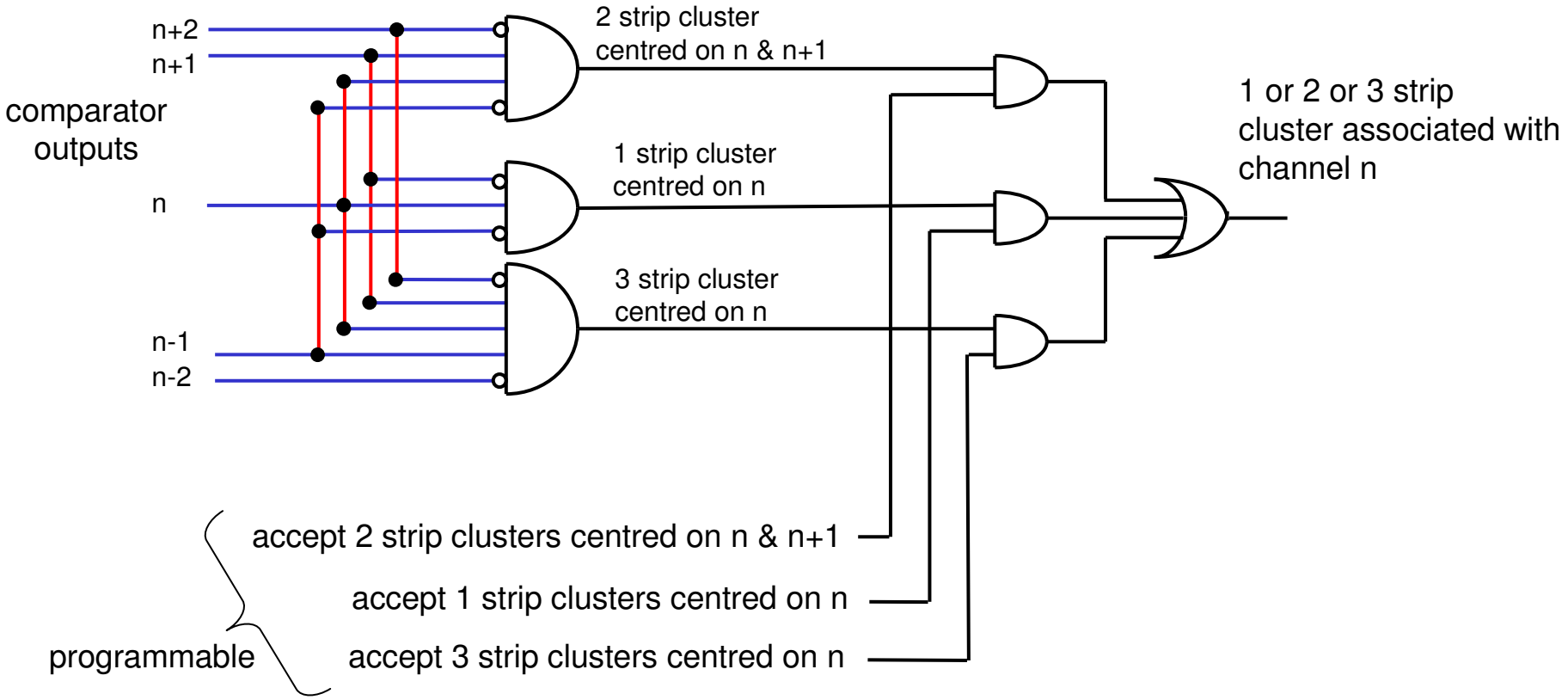
# comp. threshold scan explanation - optimum timing




for optimum time of trigger selection ($T_{OPT}$):
for low thresholds:
all signals fire comparator in triggered timeslot
for high thresholds:
all signals big enough to cross threshold do so in the triggered timeslot

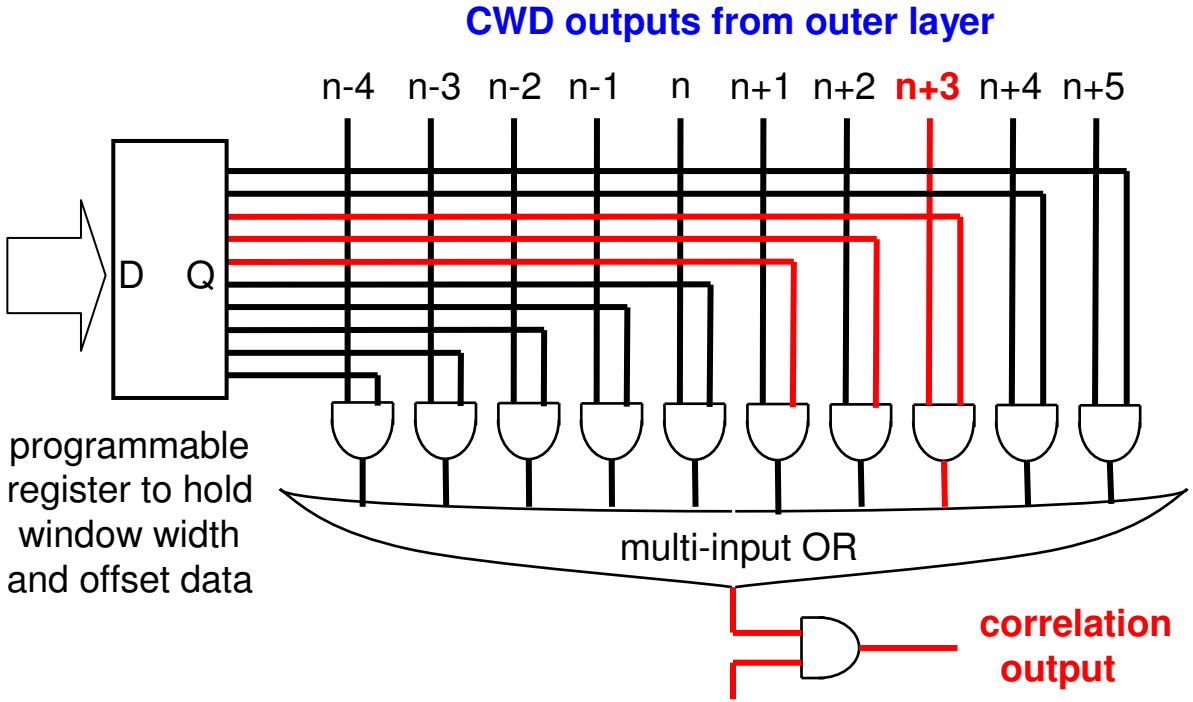


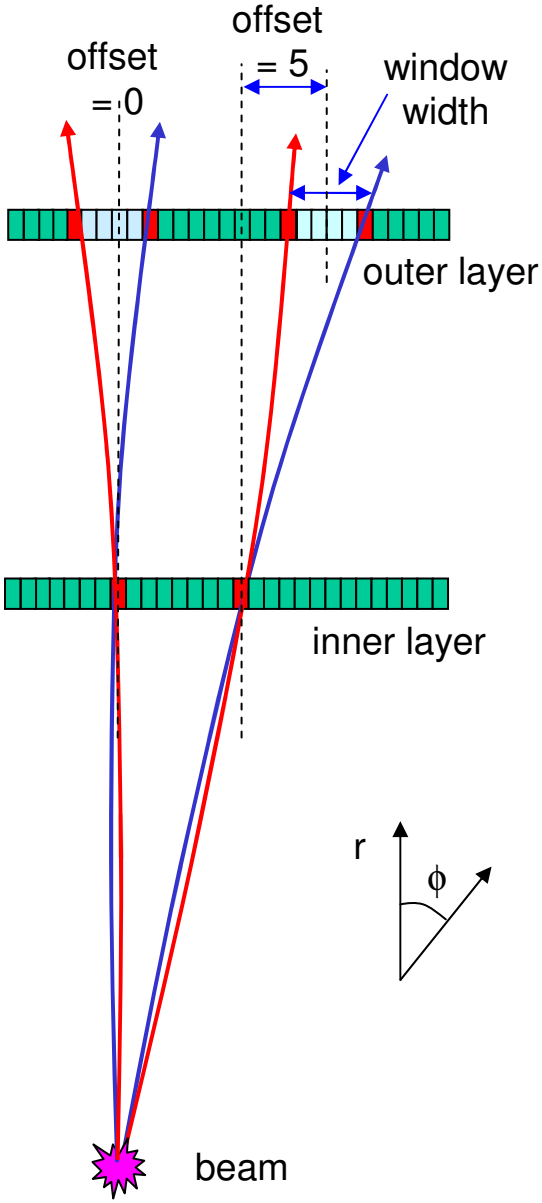
# CWD logic




**n-1, n, n+1, … are neighbouring channels on sensor layer (inner or outer)**
**but every other channel on chip**
**could increase to accept wider clusters if necessary**

# offset correction and correlation circuit




need one of these circuits on every channel

programmable register to allow for cluster window and offsets between layers

window width determines Pt cut

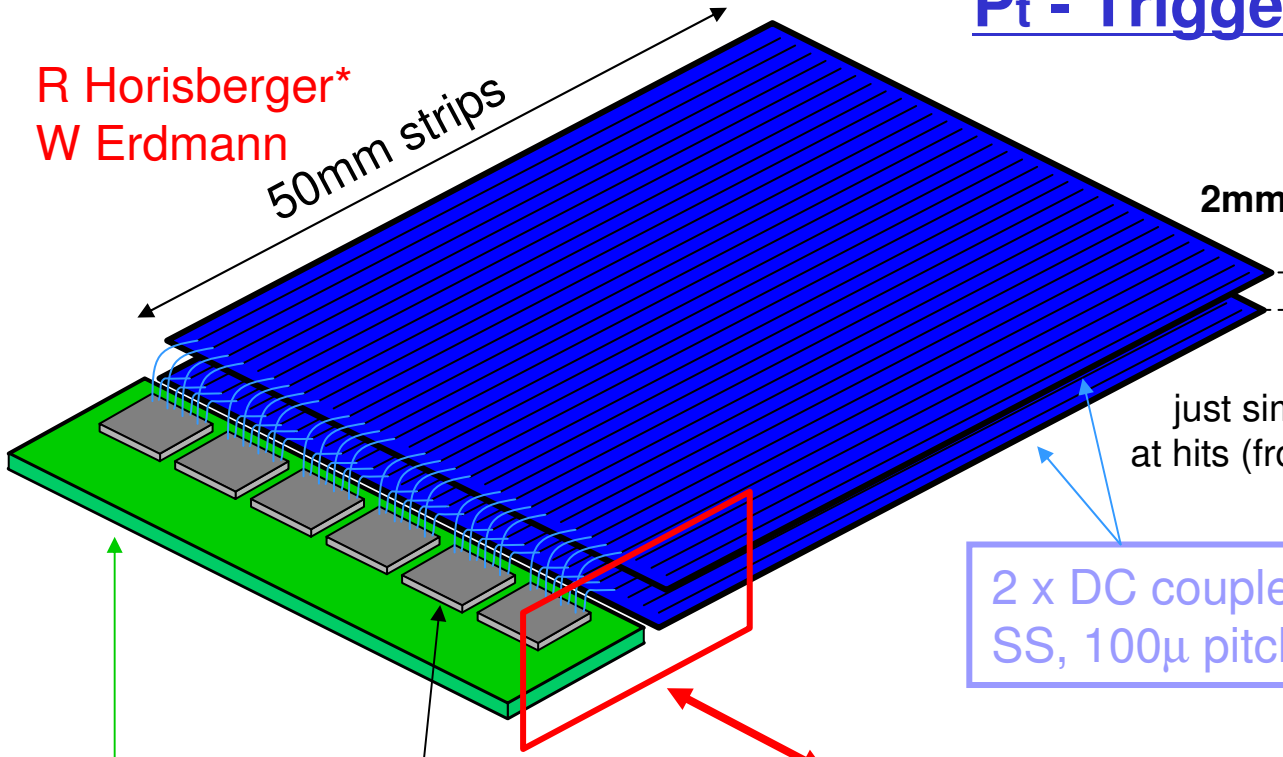
offset varies depending on location across sensor (& layer separation)

in above example 2 channel offset applied to 3 channel window in outer layer

cluster on channel **n+3** in outer layer correlates with cluster on channel **n** in inner layer

# $P_t$ - Trigger for TOB layers

R Horisberger*
W Erdmann




## Two-In-One Design

bond stacked upper and lower sensor channels to adjacent channels on same ASIC
no interlayer communication
no extra correlation chip
just simple logic on readout chip, looking at hits (from 2 layers) on adjacent channels

2mm

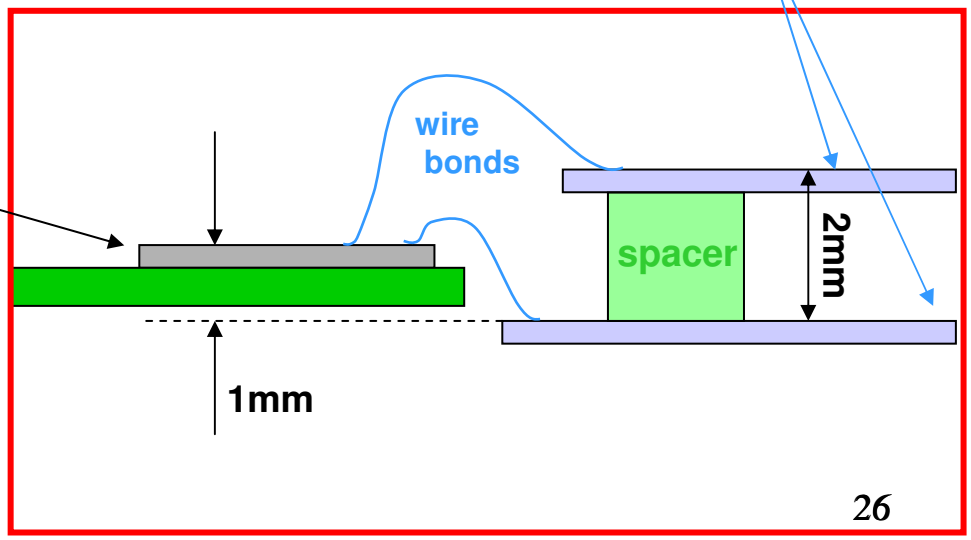
2 x DC coupled Strip detectors
SS, 100µ pitch ~8CHF/cm²

Strip Read Out Chip
2 x 100µ pitch with on-chip correlator

Hybrid

track angular resolution ~20mrad

→ good $P_t$ resolution






W.E. / R.H.

* *http://indico.cern.ch/getFile.py/access?contribId=3&sessionId=0&resId=0&materialId=0&confId=36580*