CMS Binary Chip development for the Outer Tracker High-Luminosity Upgrade

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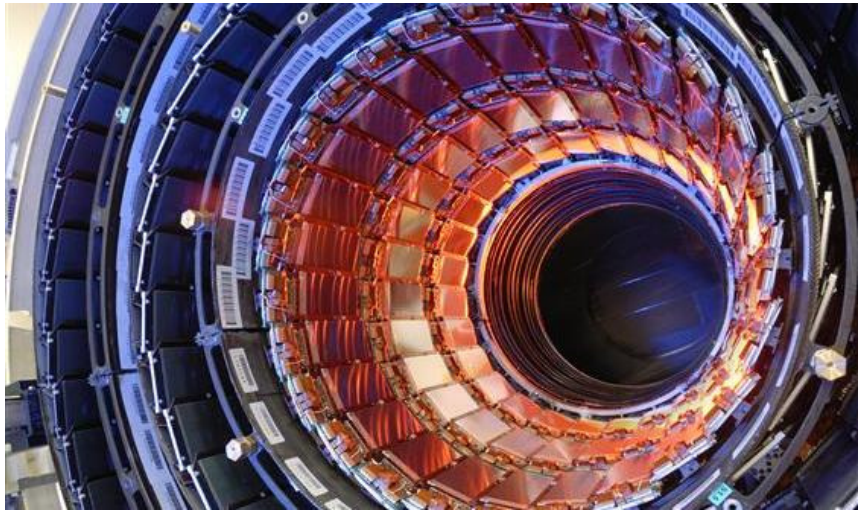
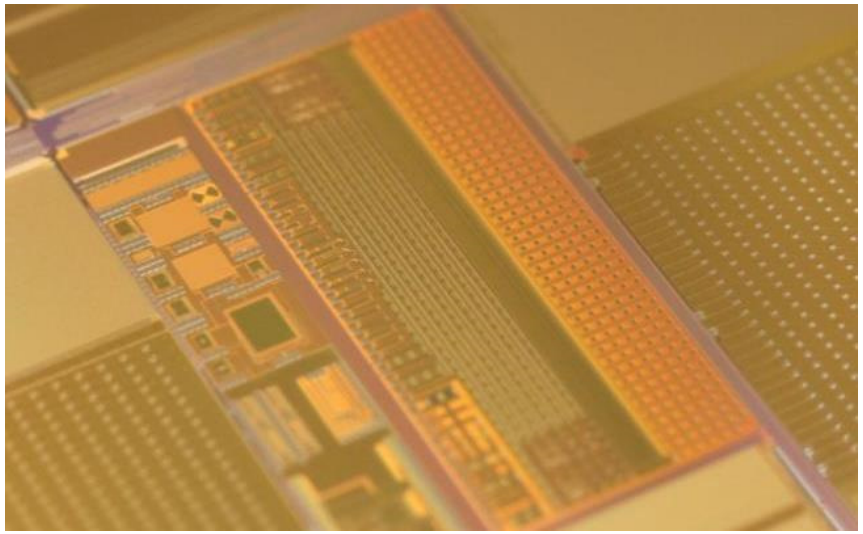
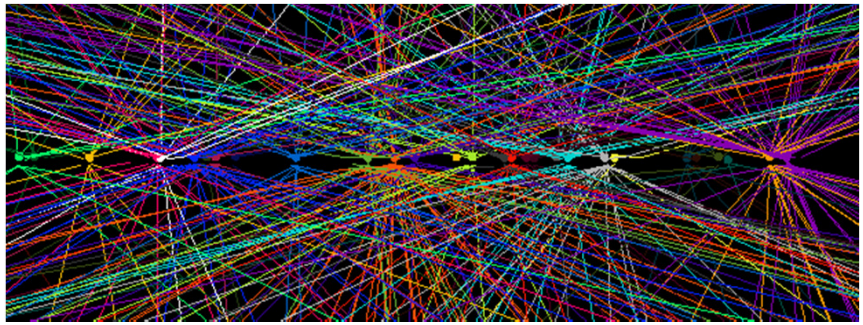
Imperial College: G. Hall, M. Raymond, M. Pesaresi

Imperial College London

Science & Technology Facilities Council



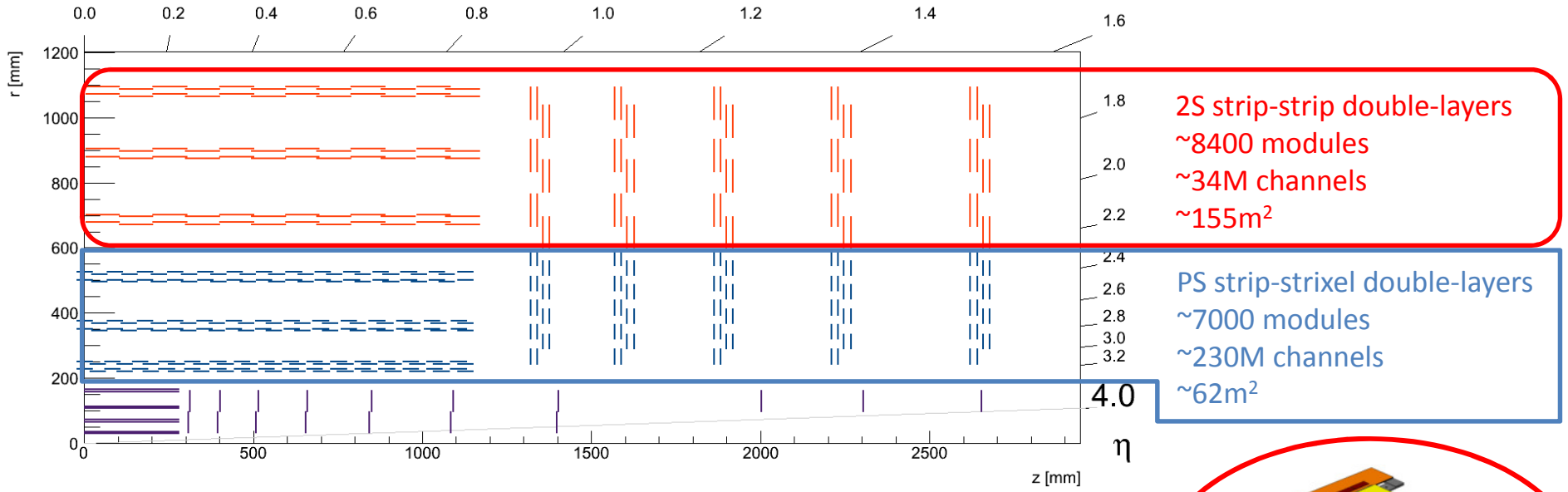




Outline

- Background
- CBC2 Features
- CBC2 Testing
- Future work
- Summary & Conclusion

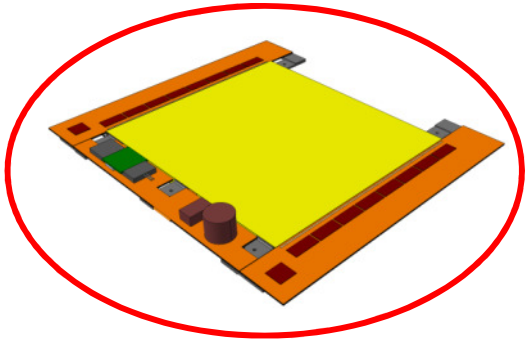
Phase-II Upgrade of the CMS Strip Tracker

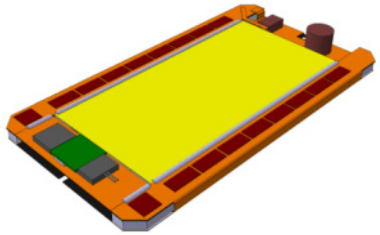


2S strip-strip double-layers
~8400 modules
~34M channels
~155m^2

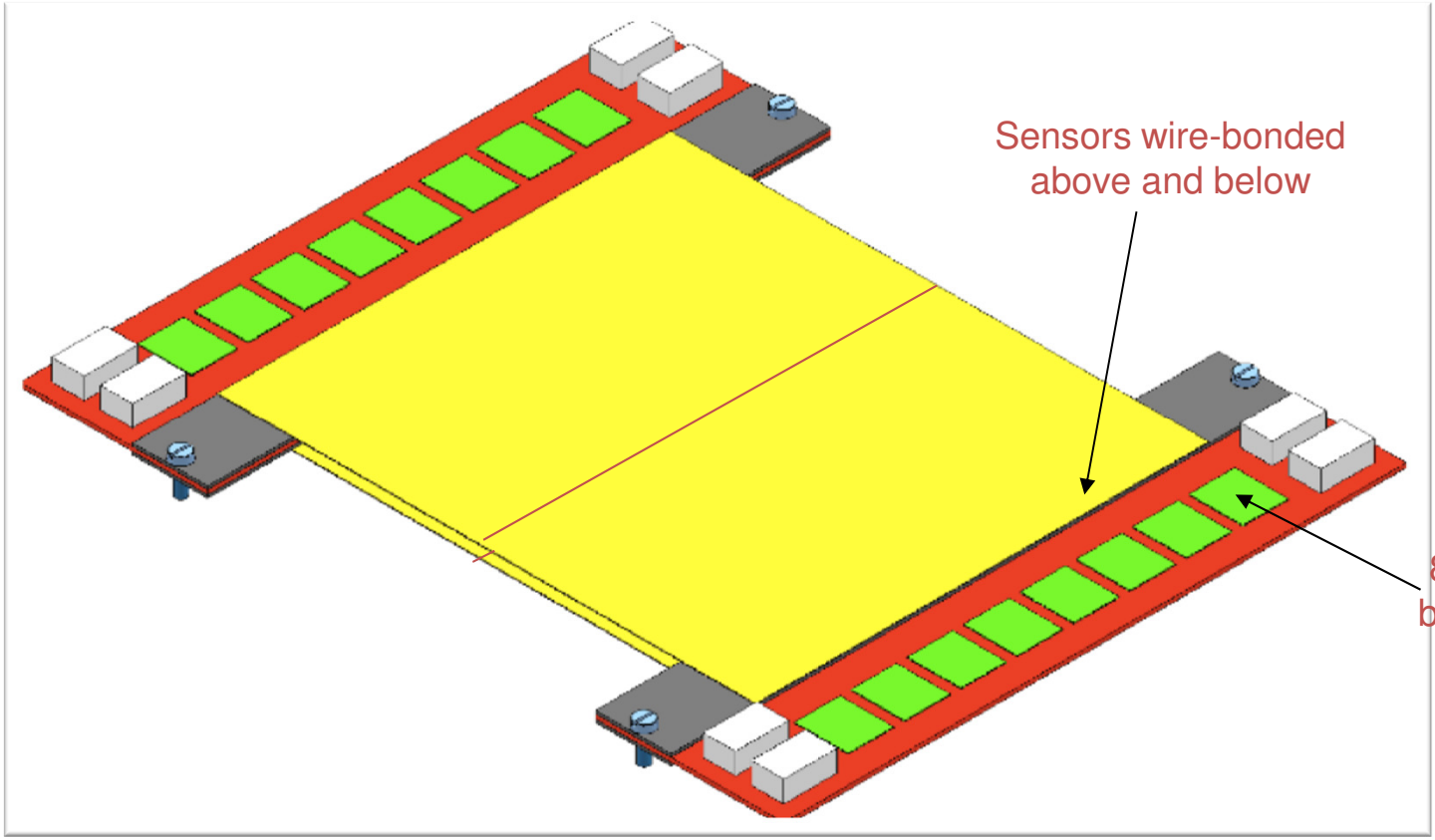
PS strip-strixel double-layers
~7000 modules
~230M channels
~62m^2

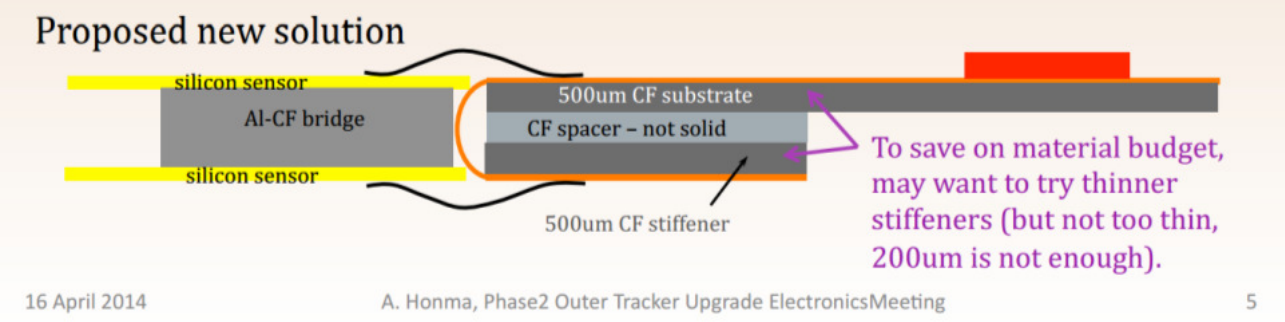
- Baseline design: Barrel+5Endcaps
- Based on 2 module types only
- Provides at the same time:
  - *readout data* upon receipt of L1 trigger
  - *trigger data* @40MHz



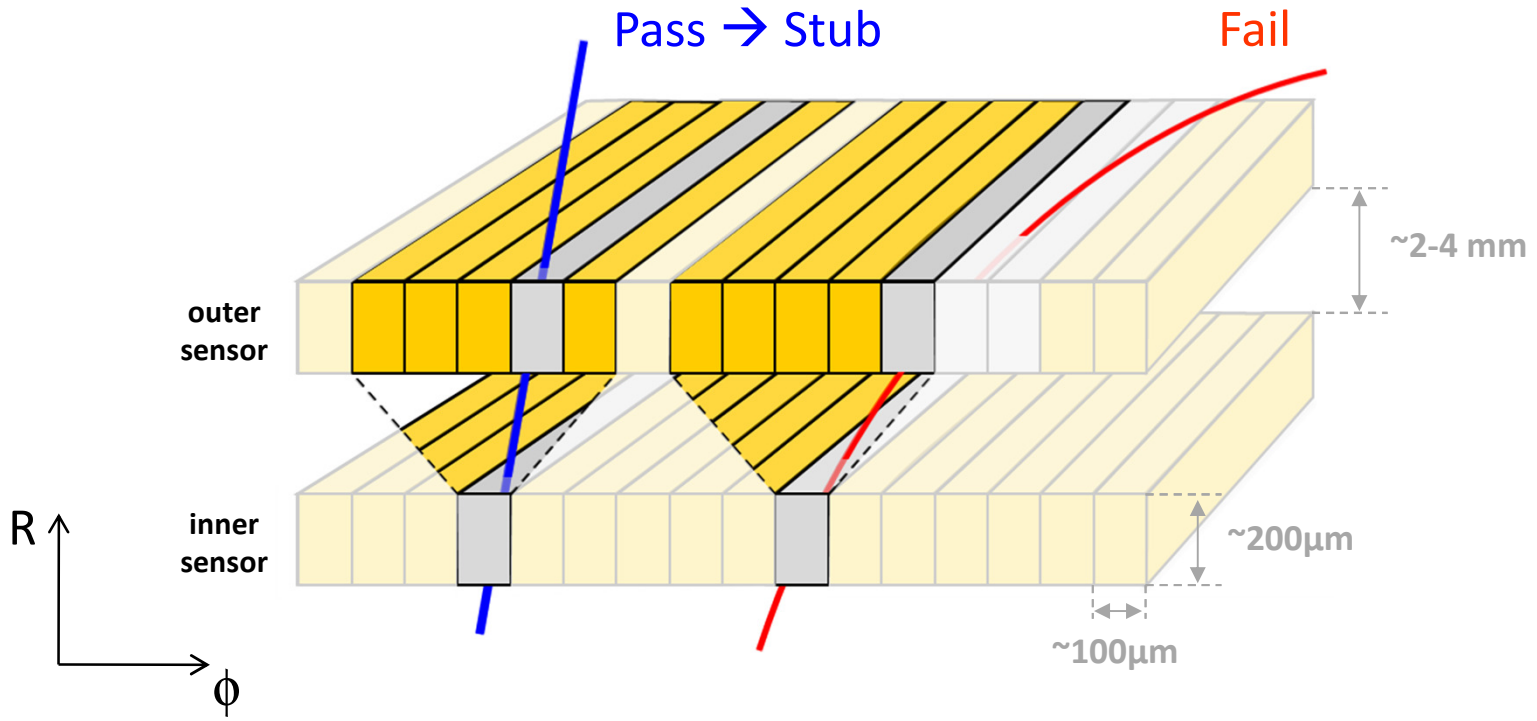


Basic Trigger Module Concept





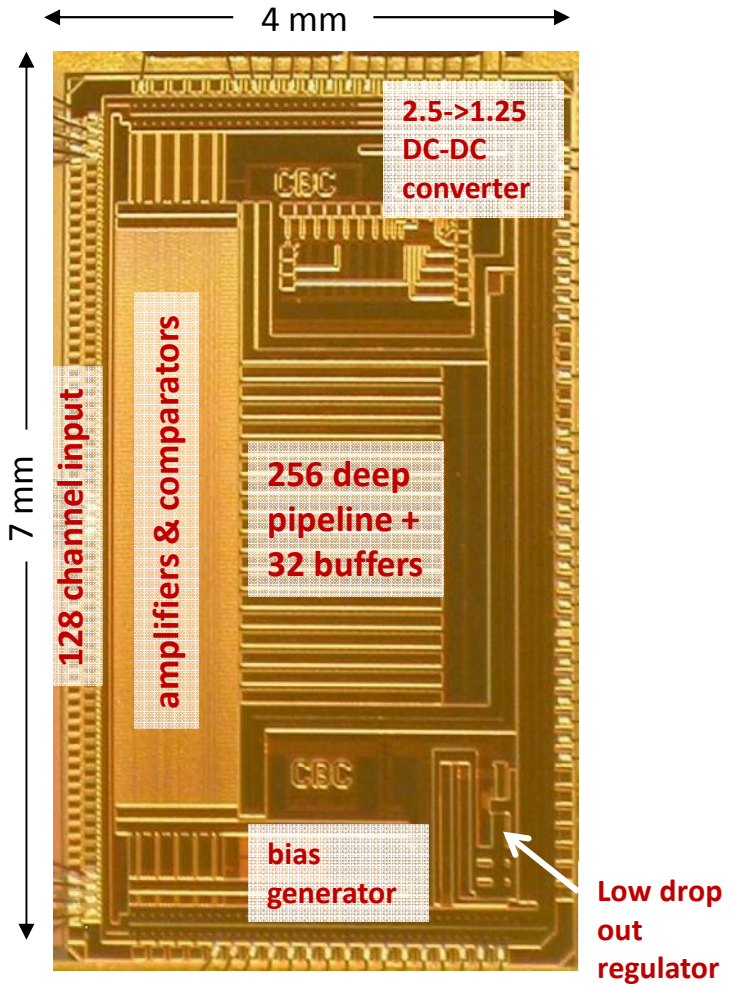
High Pt Track Identification Concept



- High-PT tracks (stubs) can be identified if cluster centre in top layer lies within a search window in R-Φ (rows)
- p_T cut given by: module radius (z), sensor separation and correlation window

First Version: CBC Main Features

- IBM 130nm CMOS process
- binary, unsparsified architecture
  - retains chip and system simplicity
  - but no pulse height data
- designed for ~2.5 - 5cm µstrips < ~ 10 pF
- 128 channels, 50 µm pitch wire-bond
  - either polarity input signal
- **not contributing** to L1 trigger
- powering test features:
  - 2.5 -> 1.2 DC-DC converter
  - LDO regulator (1.2 -> 1.1) feeds analogue FE
- fast (SLVS) and slow (I2C) control interfaces



CBC(1) Test Results

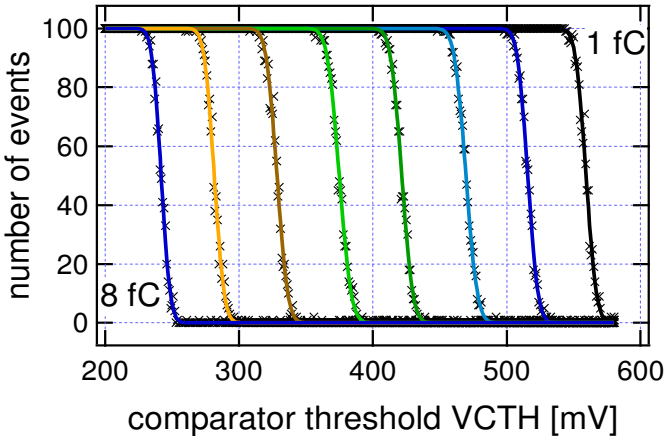
e.g. for 5pF input capacitance:

noise: ~ 800 e_{RMS}

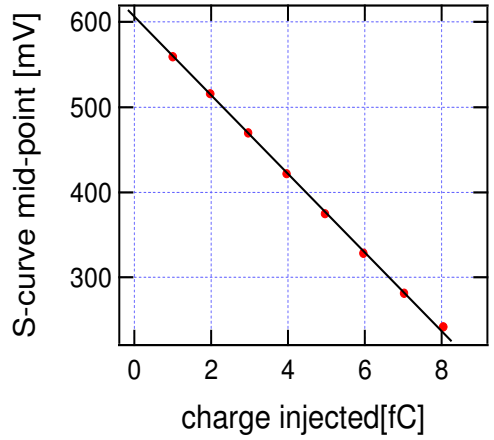
total power: < 300 µW/channel

see: "M.Raymond et al 2012 JINST 7 C01033"
"W.Ferguson et al 2012 JINST 7 C08006"

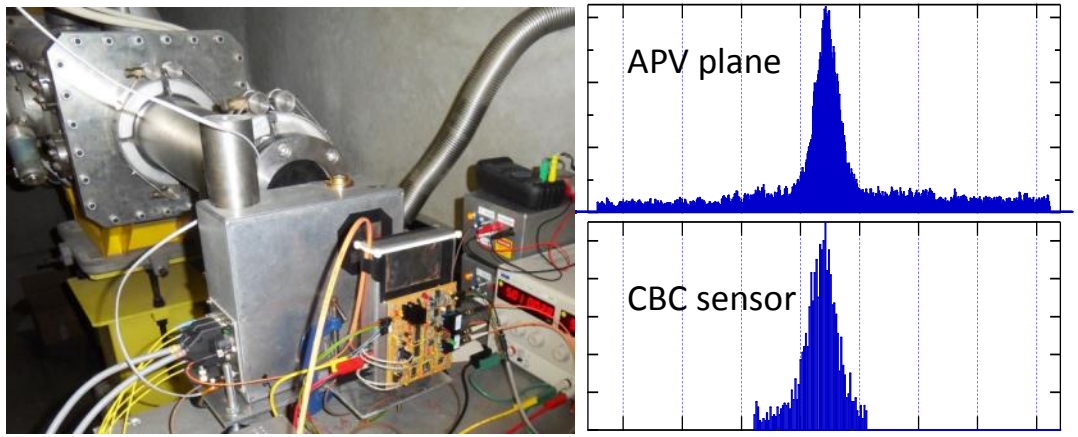
S-curves



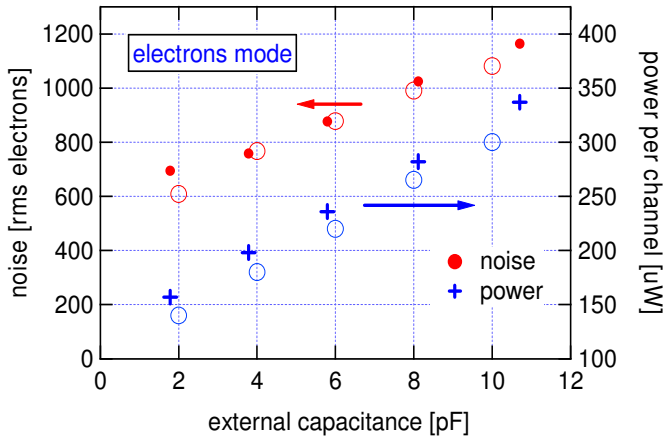
gain

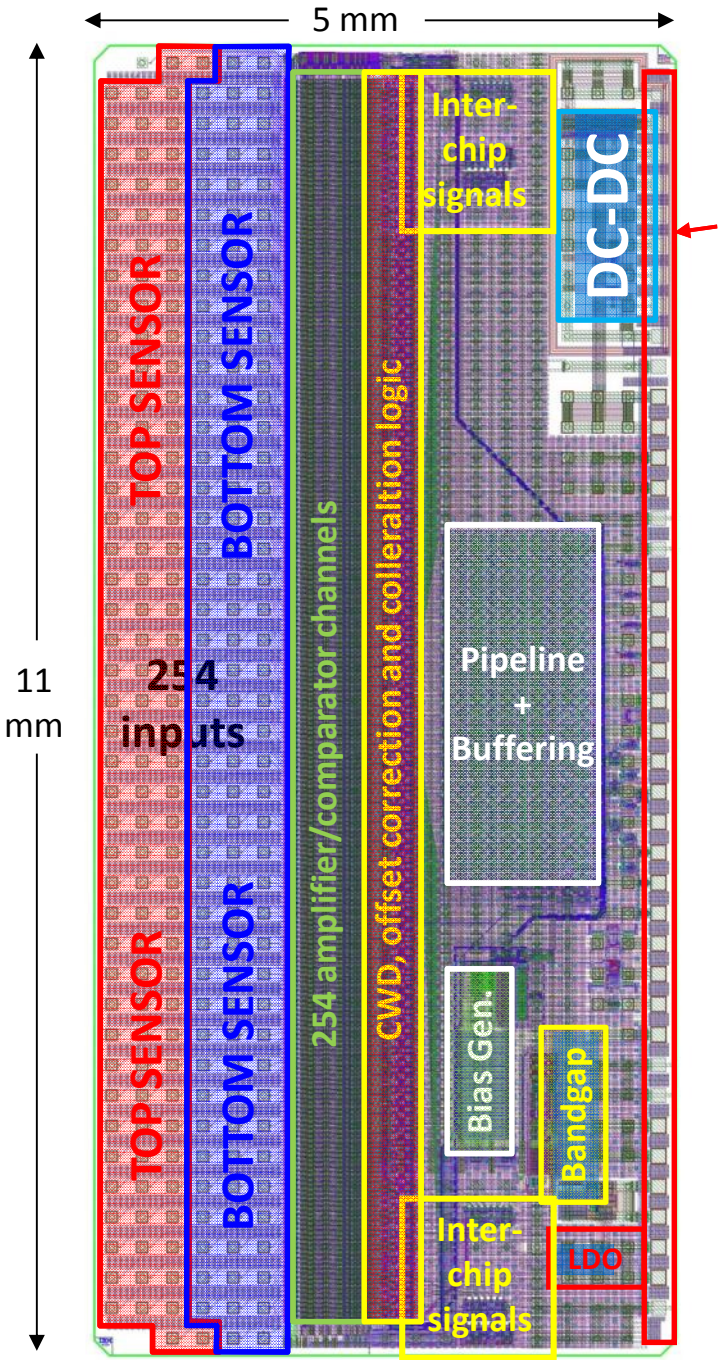


beam profile



noise/power





CBC → CBC2: New Features

250µm pitch C4 layout (for commercially assembled module)

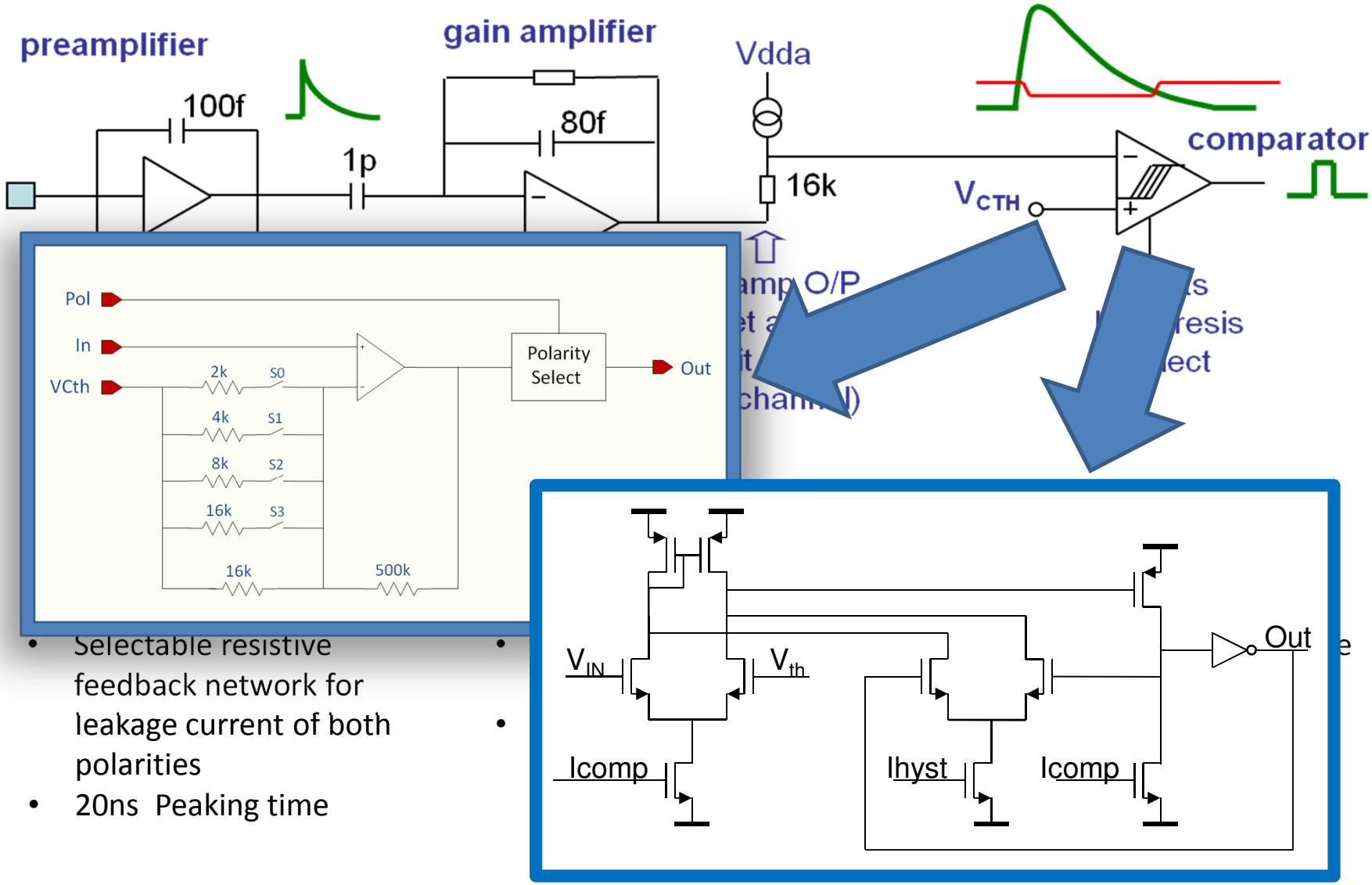
- 254 channels for 127 + 127 strips
- Vetoes of wide clusters
- Correlation logic for stub formation
- Front-end circuit improvements
- On-chip test pulse circuit with DLL for timing adjustment
- 4 bit direct input for controls (T1 trigger, Fast reset, Test pulse & I2C refresh)
- Analogue Multiplexer for bias monitoring
- Improved DC-DC (CERN)
- Back edge wire-bond pads for wafer probe
- Received Jan 2013 – fully functional

Analogue Front End

CBC2 Front End Specifications

Detector Type:	Silicon Strip
Signal Polarity:	both (electrons and holes)
Strip length:	2.5 – 5cm
Strip Capacitance:	< 10pF
Coupling:	AC or DC
Detector leakage:	up to 1uA leakage current compensation
Noise:	<1000e^-_{RMS} for 5pF sensor capacitance
Overload recovery:	normal response within ~ 2.5µs after 4pC signal
Power:	~500µW / channel (for 5pF strips)
Power supply:	1.1 V (front end supplied through LDO to get supply noise rejection)
Gain	50mV/fC
Dynamic range:	Linear up to 4fC
Timewalk:	<16ns for 1.25fC and 10fC signals with comp. thresh. set at 1fC

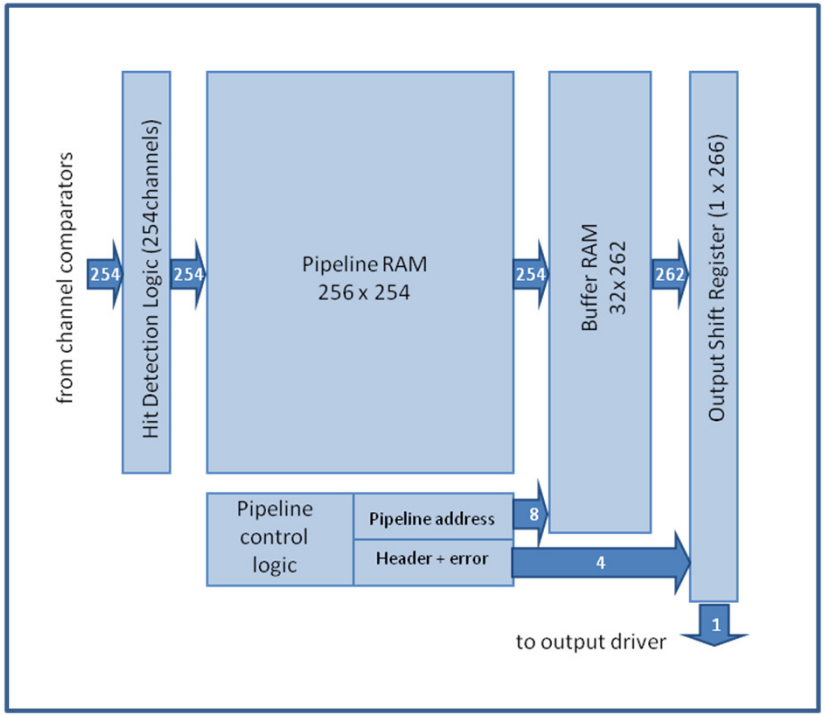
CBC 2 Front End

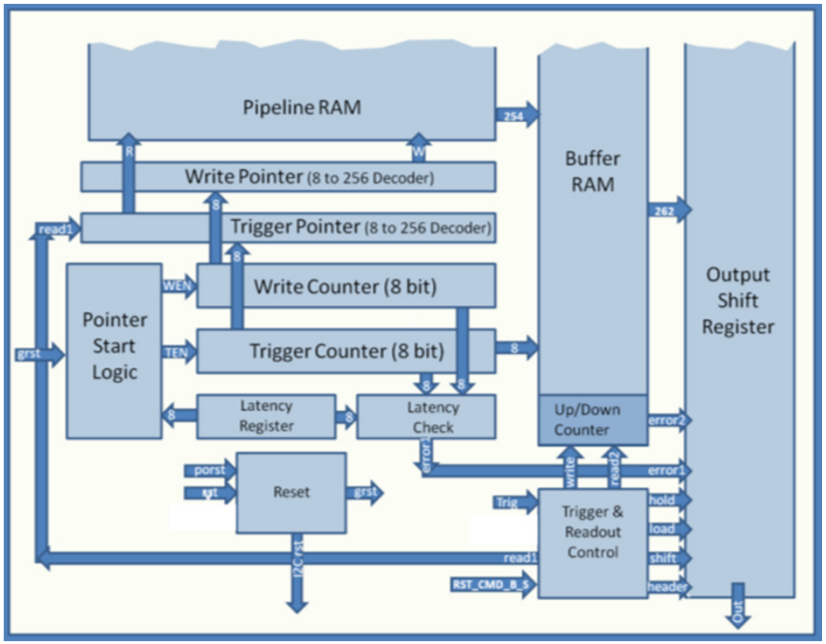


- Selectable resistive feedback network for leakage current of both polarities
- 20ns Peaking time

Digital Back End

Data buffer and Readout

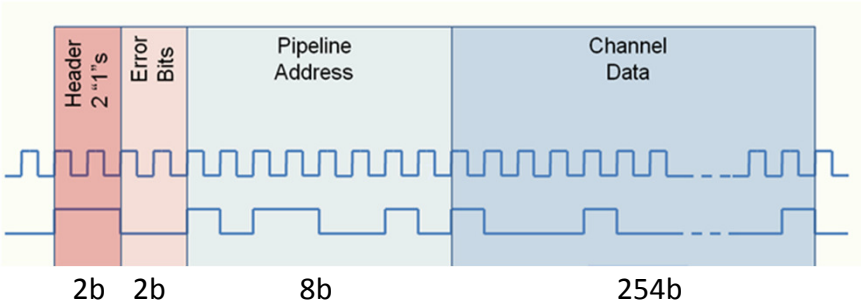




- 256-deep memory → max 6.4µs L1 trigger latency
- Dual-port SRAM (SEU considered tolerable for data)

- 32-deep additional buffer for events awaiting readout

- Data serialized in 266 bit long packets



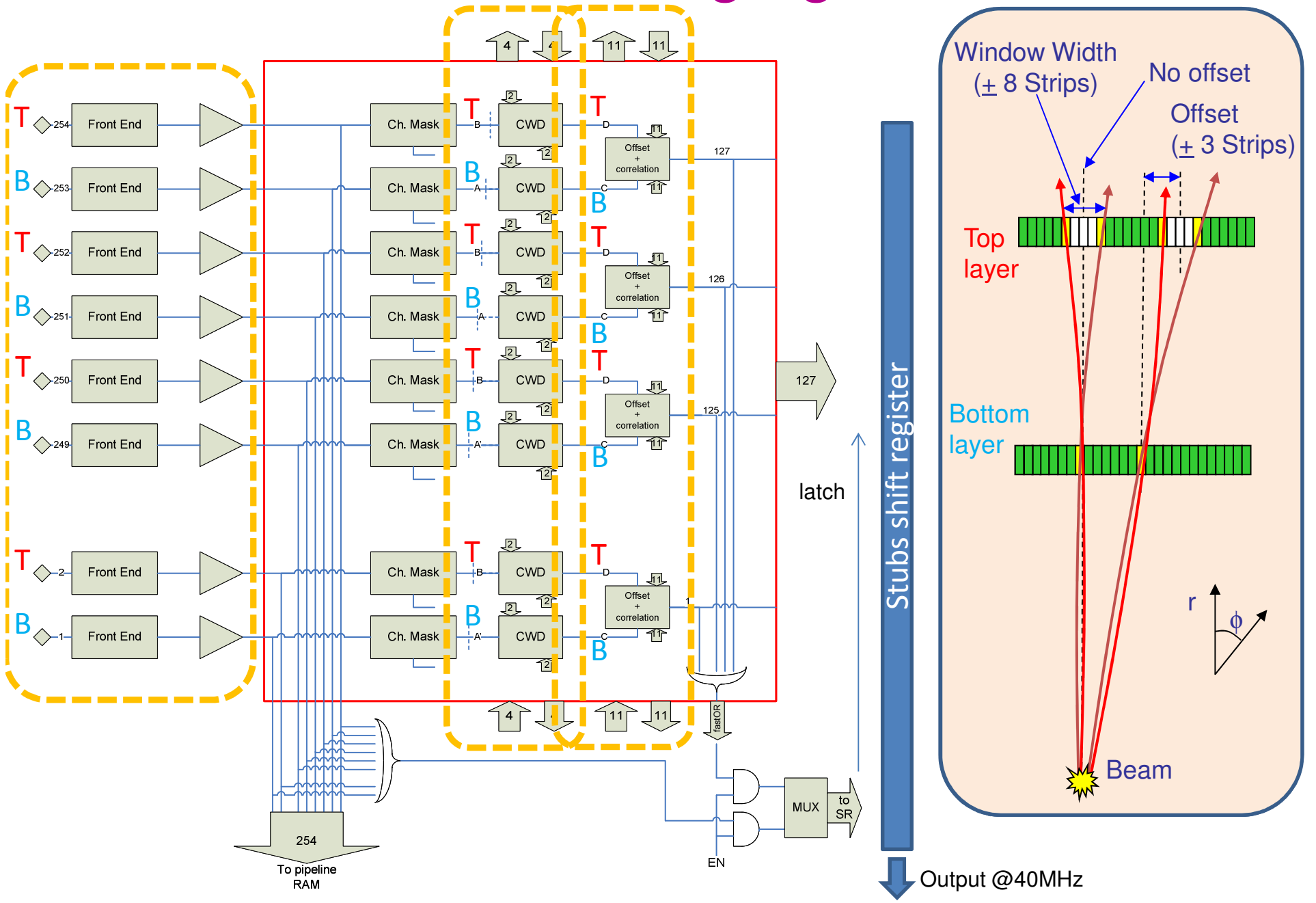
- Write and Read pointers separated by programmable latency

- 2 error bits:
  - Monitor the difference between Wr/Rd pointers against programmed latency
  - Buffer overflow
  - The address of the trigger counter is also a useful way to check the synchronization of different chips on the module

- Liu-Whitaker SEU-hardened Flip Flops for control logic

Stub Finding Logic

Stub Finding Logic

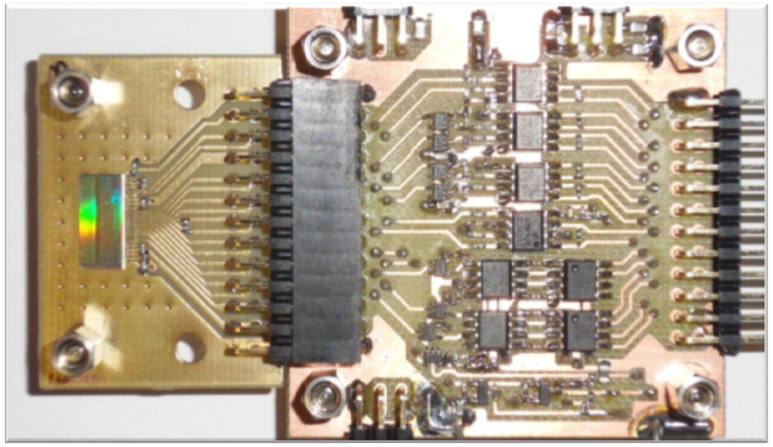


CBC2 Test Activities

CBC2 Test Activities

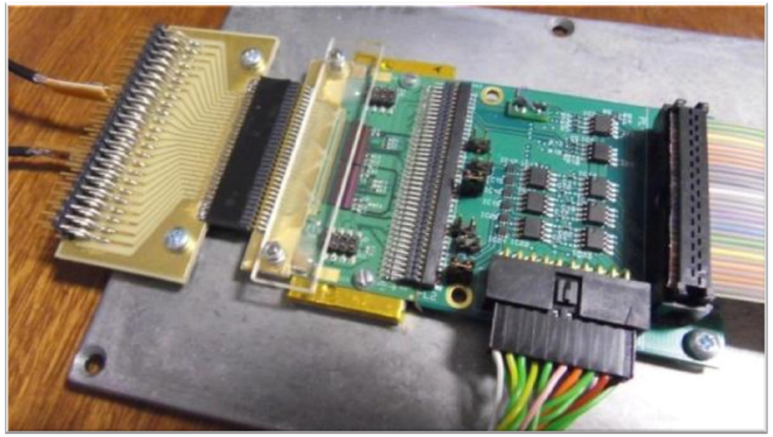
Wire-bond CBC2

- Useful to develop wafer probe procedures
- X-rays TID testing



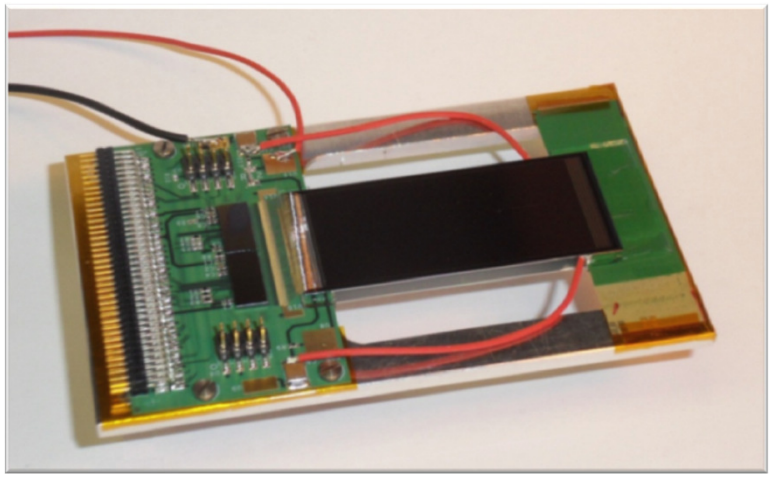
2xCBC2 hybrid

- Hybrid characterization and chip integration
- Bump-bonded ASICs
- Inter-chip links & logic



2xCBC2 mini-module + sensor

- Sr-90 source
- Cosmic rays
- Beam Test



Single Chip Results

Gain Measurements

M. Raymond, IC

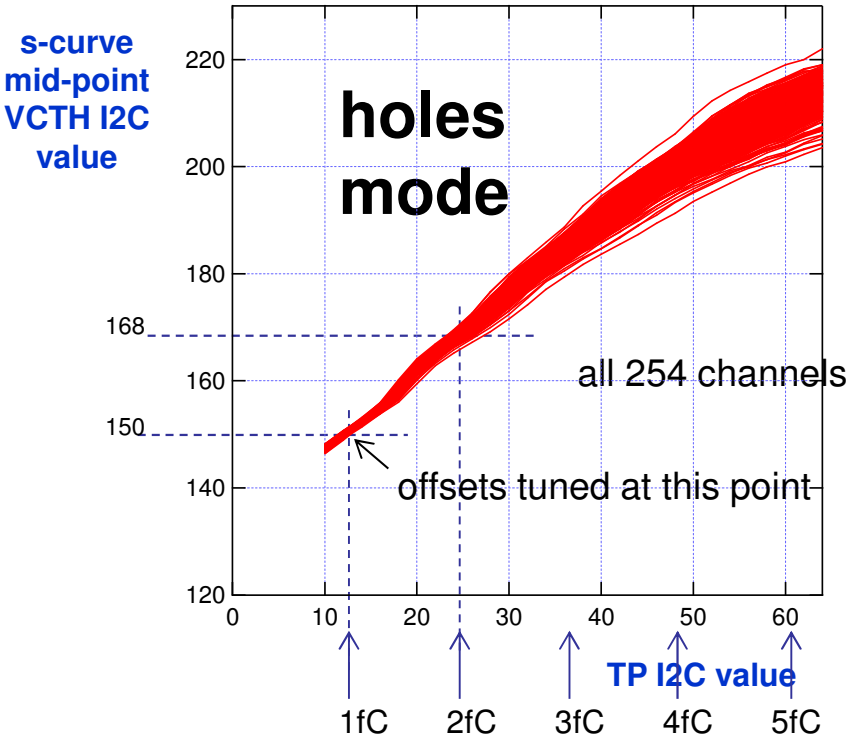
sweep global comparator threshold VCTH
to get s-curves for range of test pulse amplitudes

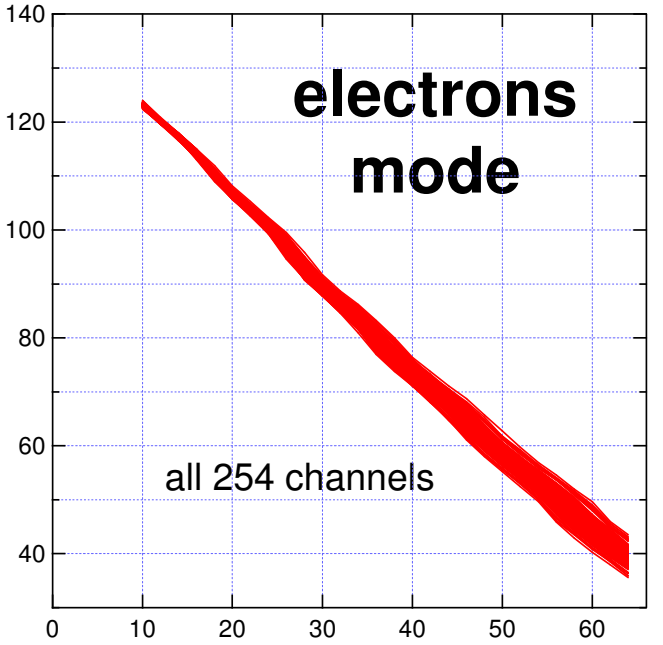
plot s-curve mid-points vs. TP amp

rough calculation in 1÷2fC region
(assumes TP value of 12 / fC)

(168 - 150) x 2.5 mV* = 45 mV/fC

(* from VCTH bias sweep measurements)

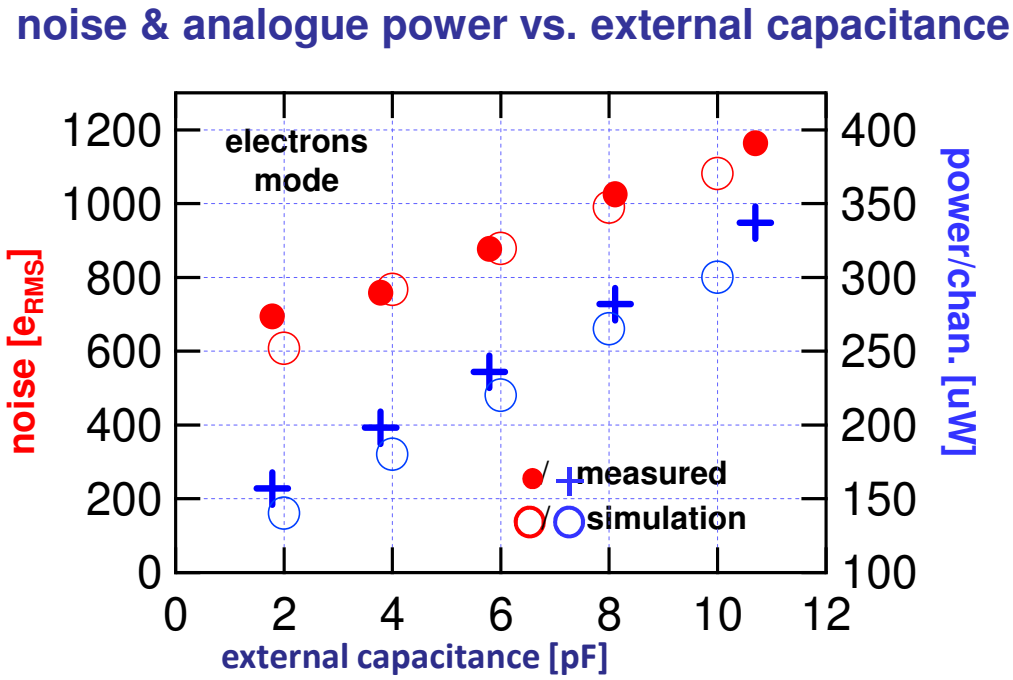




M. Raymond, Imperial College

Noise & Power

Analog:	130 + (21 x C_{in}[pF]) µW
Digital:	50µW
Trig. logic:	<50µW
Total:	<230 + (21 x C_{in} [pF]) µW
APV25	~2.6mW (long strips)



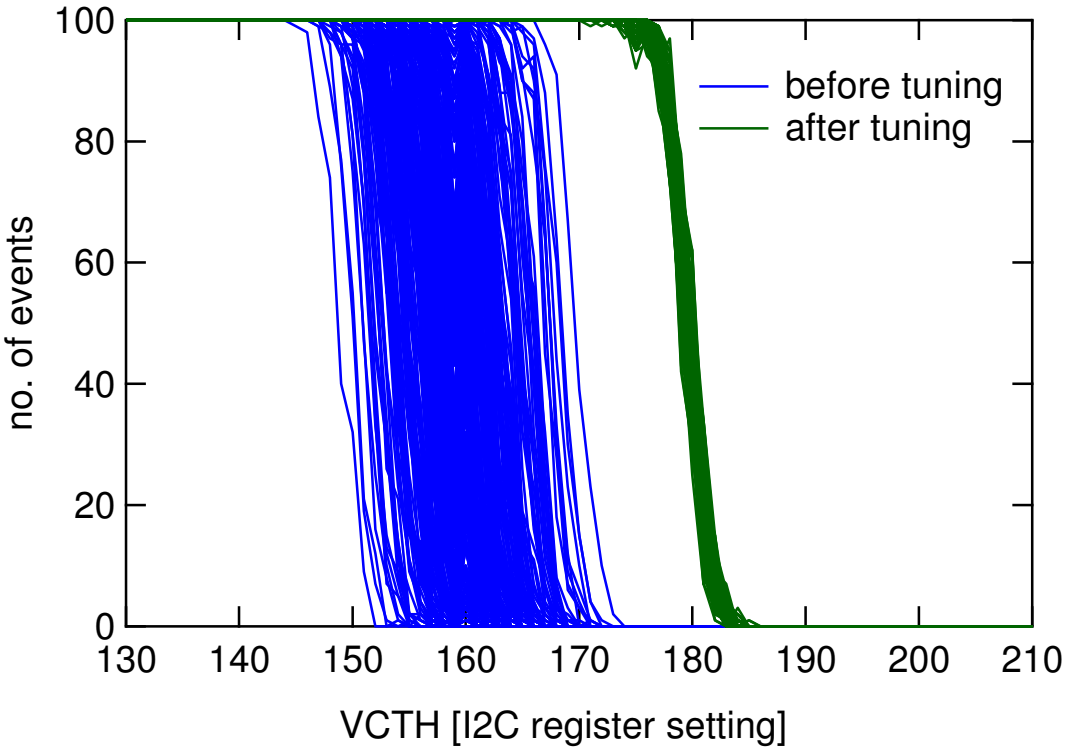
- Noise and power depends on external input capacitance
- The current settings in the front-end are adjusted to maintain the same pulse shape for different C_{in}
- Results almost identical for e^- and h^+

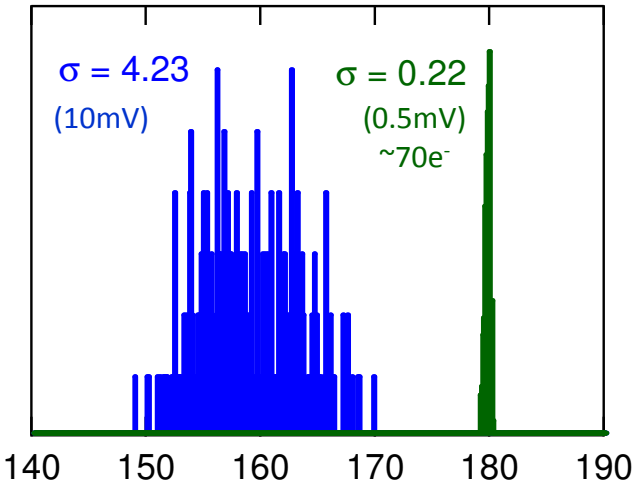
→ Within specification with ~800e^-_{RMS} for 5pF strips at <**325µW/channel**

S-Curves and Tuning

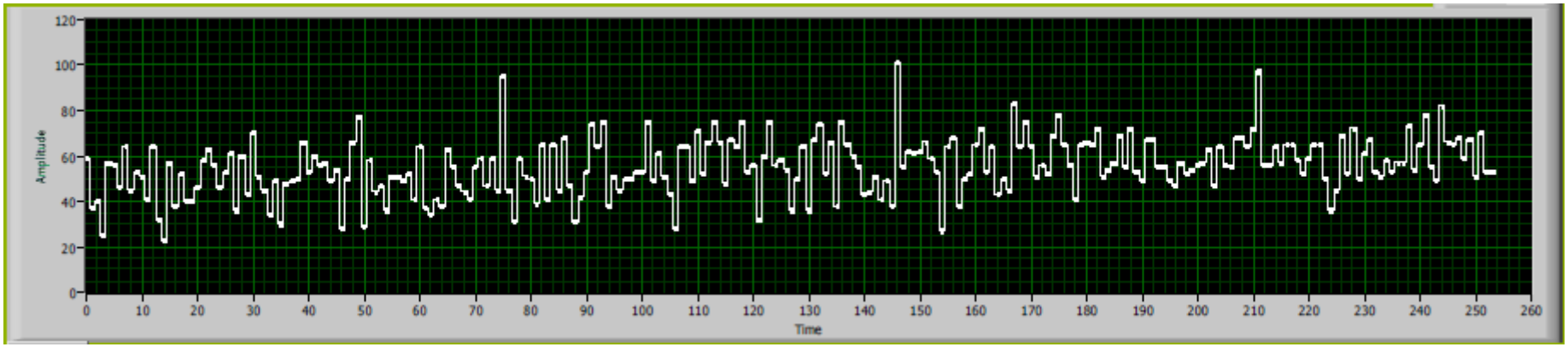
254 S-curves measured with on-chip test pulse

S-curve mid-points tuned to ~mV level

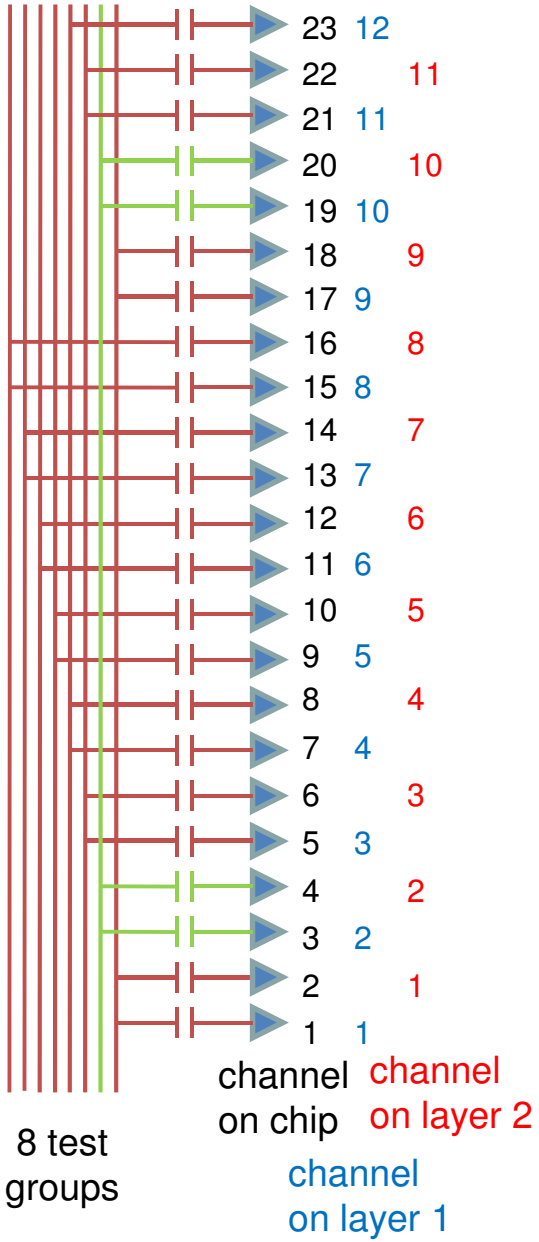


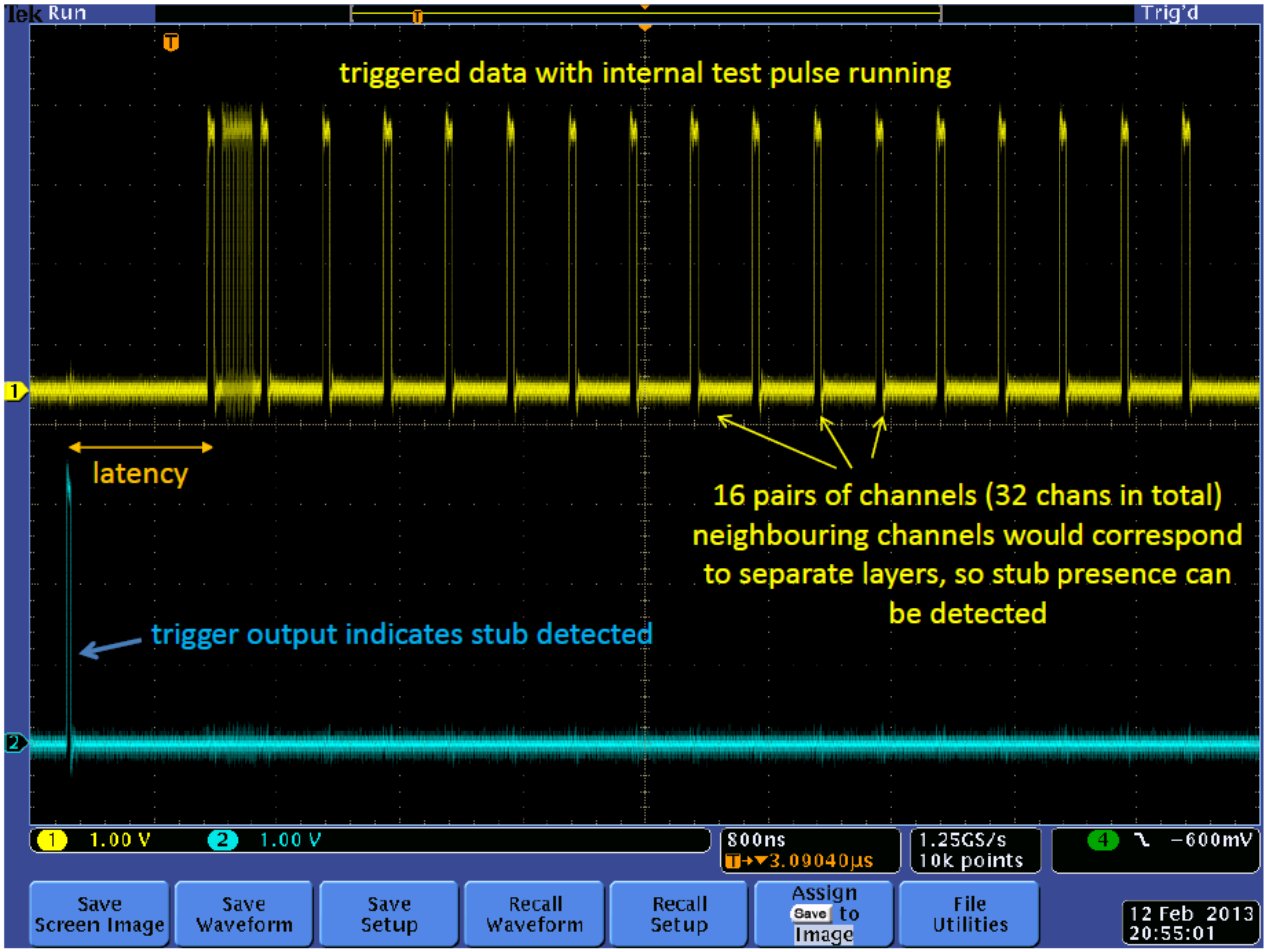


254 offset values after tuning



Results with On Chip Test Pulse

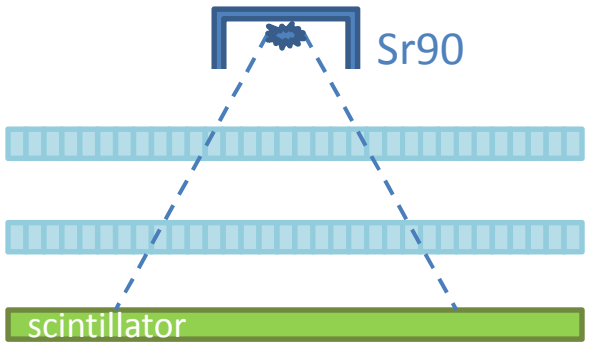


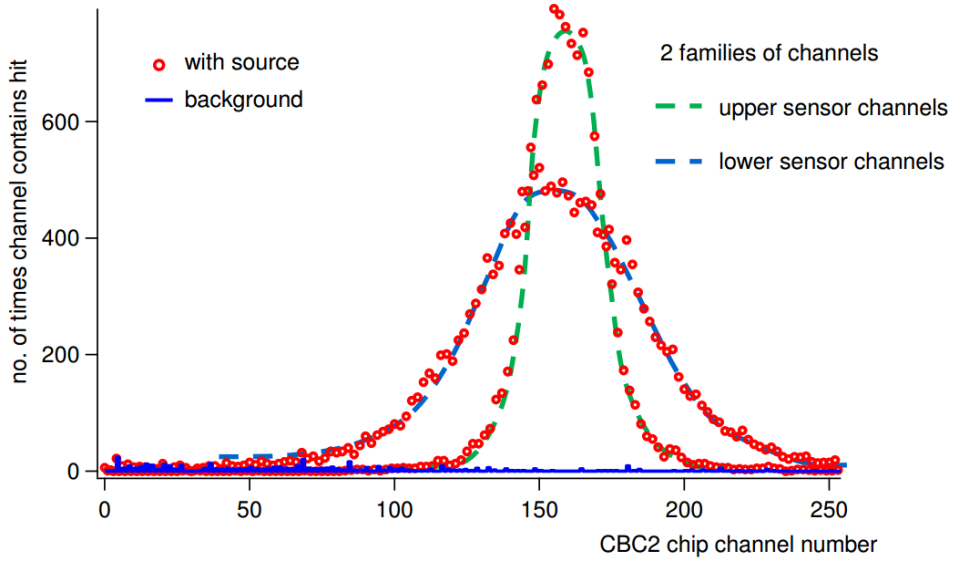


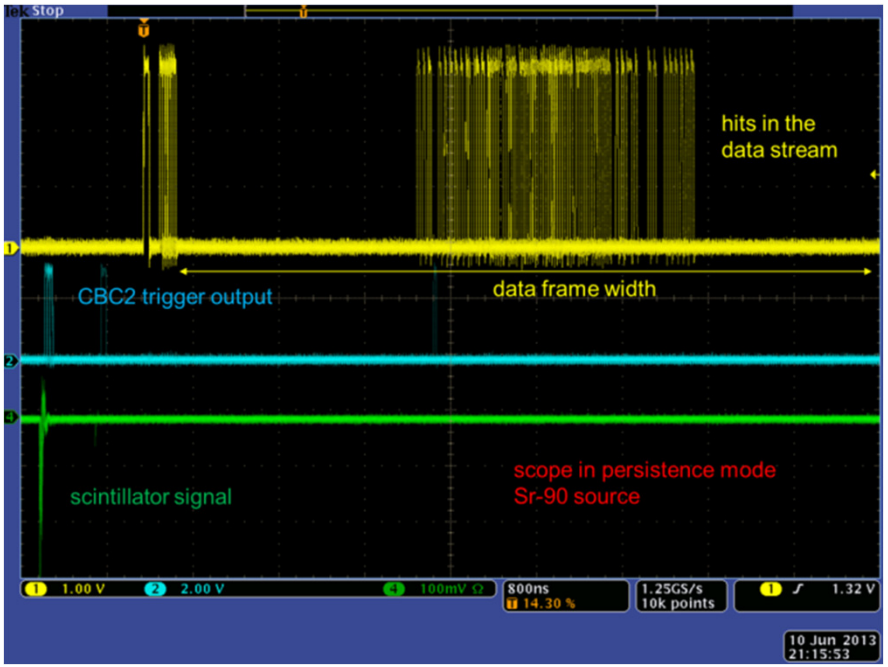
→ Test pulse together with individually-programmable channel masks can be used to fully exercise the coincidence logic

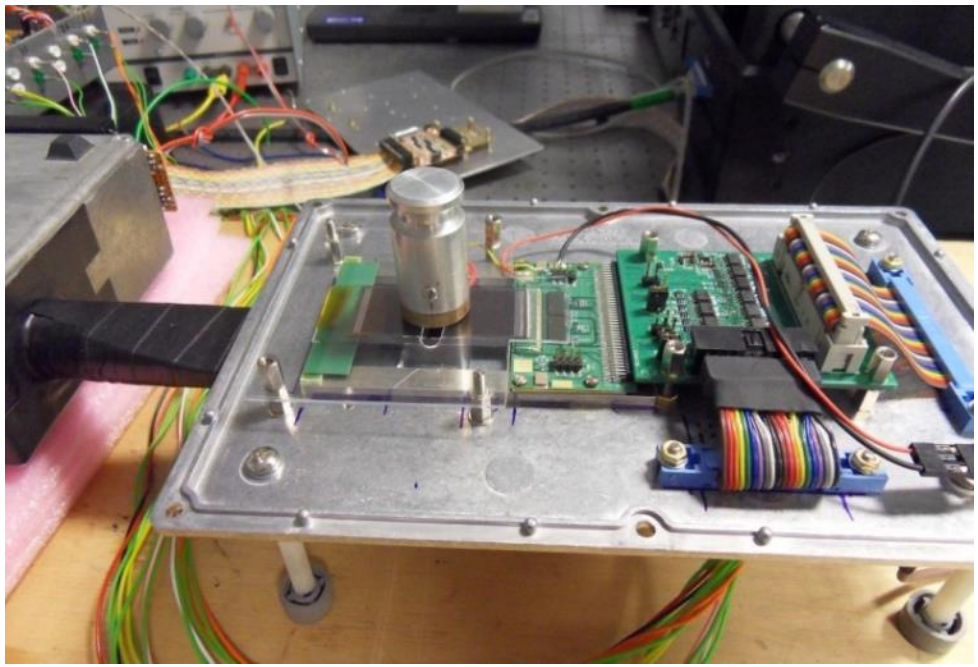
Mini Module Results

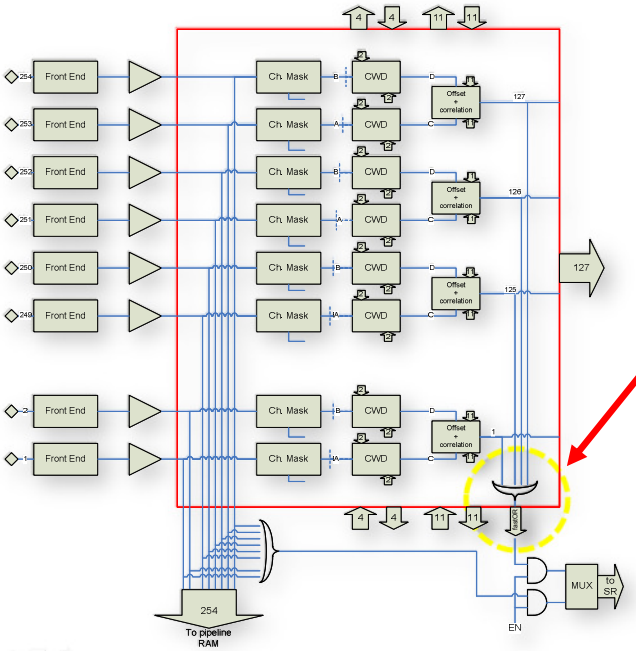
Logic tests using beta source

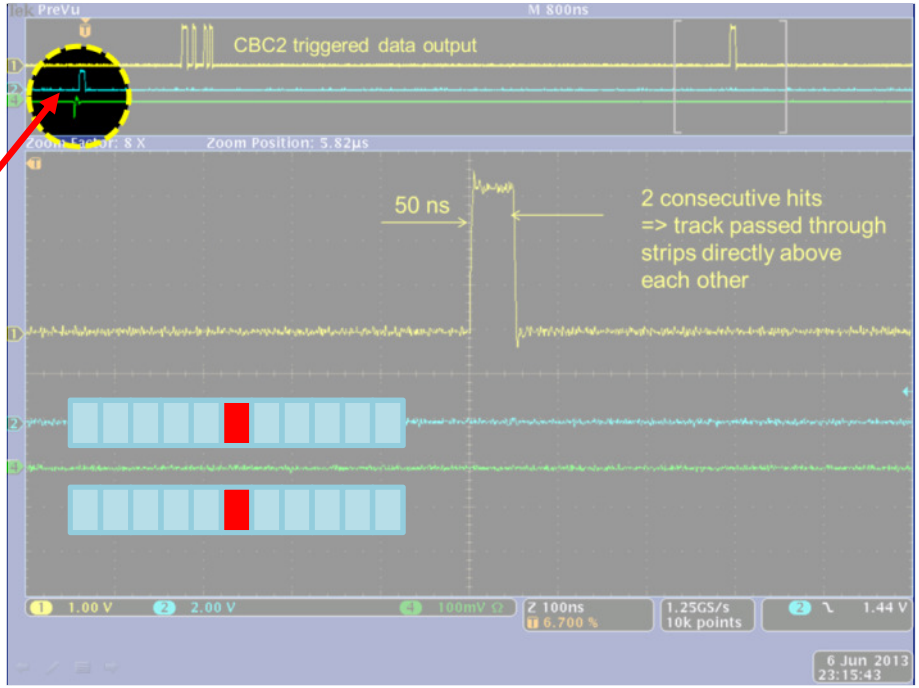


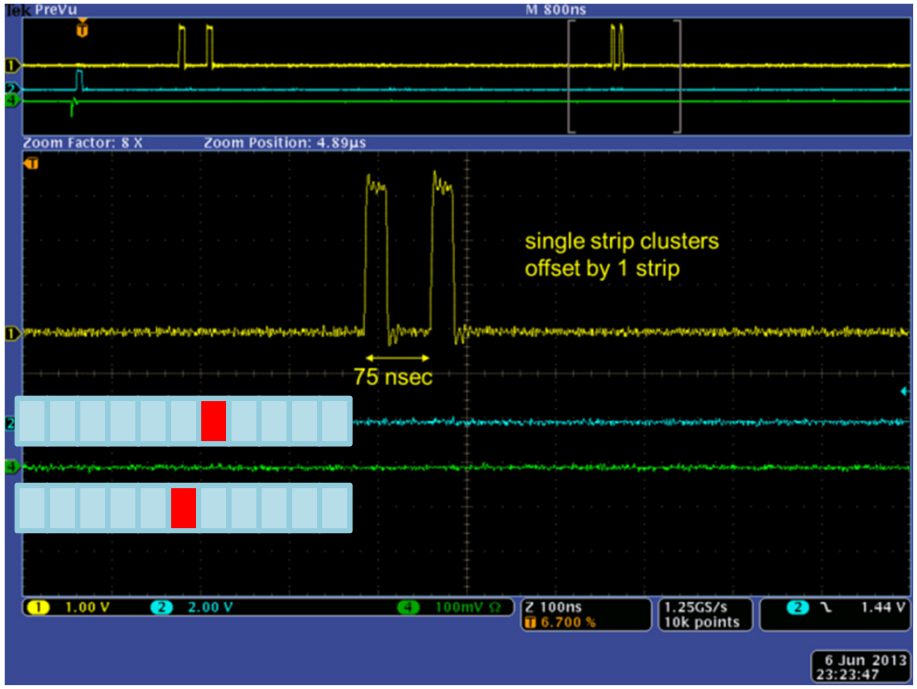


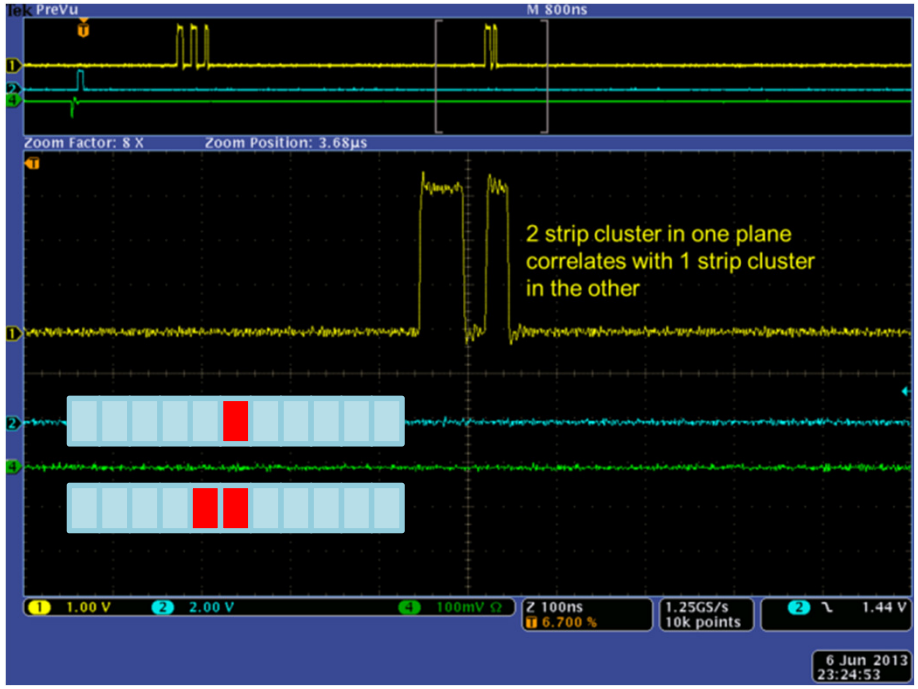





Front End
Ch. Mask
CWD
Offset + correlation
127
126
125
1
254
To pipeline RAM
MUX
To SR
EN

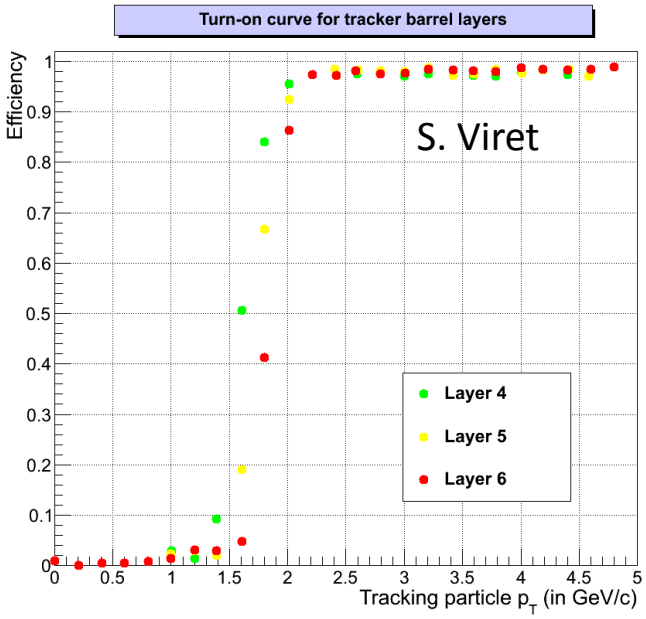

CBC2 triggered data output
Zoom Position: 5.82µs
50 ns
2 consecutive hits
=> track passed through
strips directly above
each other
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:15:43

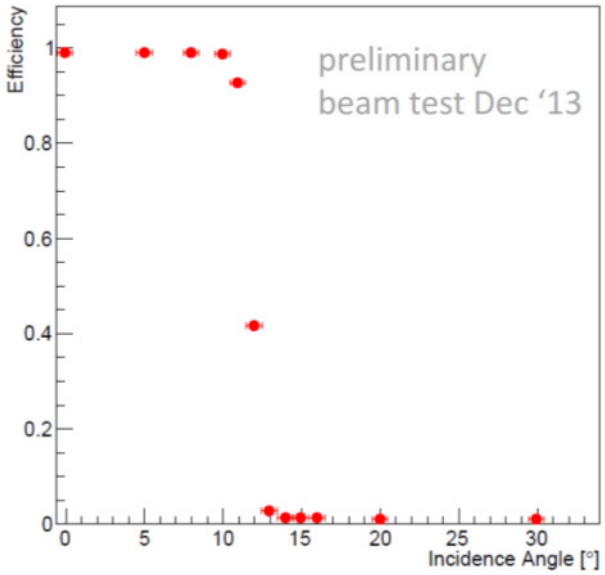

Zoom Factor: 8 X
Zoom Position: 4.89µs
single strip clusters
offset by 1 strip
75 nsec
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:23:47

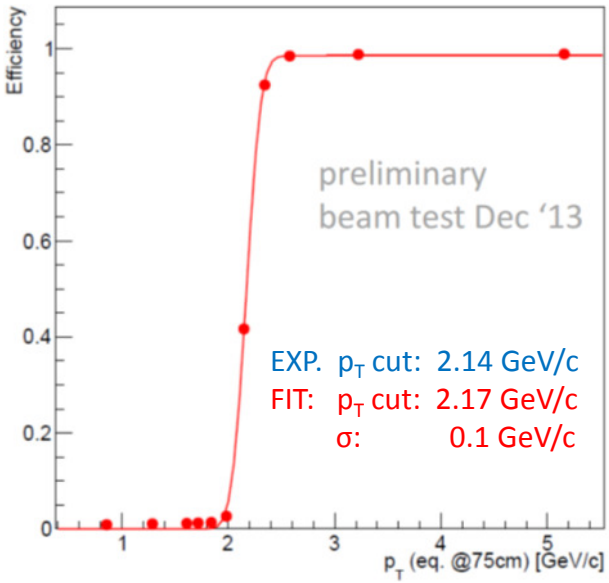

Zoom Factor: 8 X
Zoom Position: 3.68µs
2 strip cluster in one plane
correlates with 1 strip cluster
in the other
1.00 V
2.00 V
100mV Ω
Z 100ns
6.700 %
1.25GS/s
10k points
1.44 V
6 Jun 2013
23:24:53

Beam test results

M.Pesaresi, IC

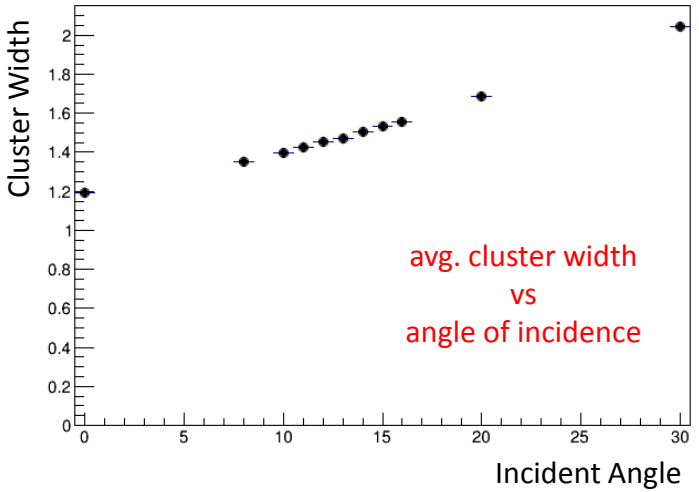






Pt Selection cut: simulation ⇨ **measured efficiency** ⇨ **reconstructed p_T cut of r=75cm layer**

- December 2013 beam test at DESY
- 4 GeV positron beam
- Datura telescope + 2 pT modules (1 rotatable to simulate B-field effect) + 2 different strip sensors
- Custom control and DAQ



Future Work

Future Work

- **Further testing of CBC2 up to 50 Mrad TID**
- **Testing for SE effects –** UC Louvain's cyclotron with protons (~50MeV)
- **CBC3 (Final Prototype)**
  - **Front End:**
    - Adjust pre-amp (1V operation, single polarity, AC coupled & larger sensor capacitance)
    - Extra Comparator -- 3σ Threshold
    - Additional circuit to suppress HIPs
  - **Increase Pipeline to 12μs (**possibly 25μs**)**
  - **Stub finding logic:**
    - ½ strip cluster resolution → 8 bit stub address
    - 5 bit bend information
    - Priority selection of 3 highest-pT stubs
    - Offset correction: 4 domains/chip (2 in CBC2)
  - **Stub readout**:
    - 13 bit/stub with up to 3 stubs/Bunch Crossing
    - Data Output: 6 SLVS differential pairs @ 320Mbps
  - **Possible change to bump pad layout (**Adjust for increased pitch**)**

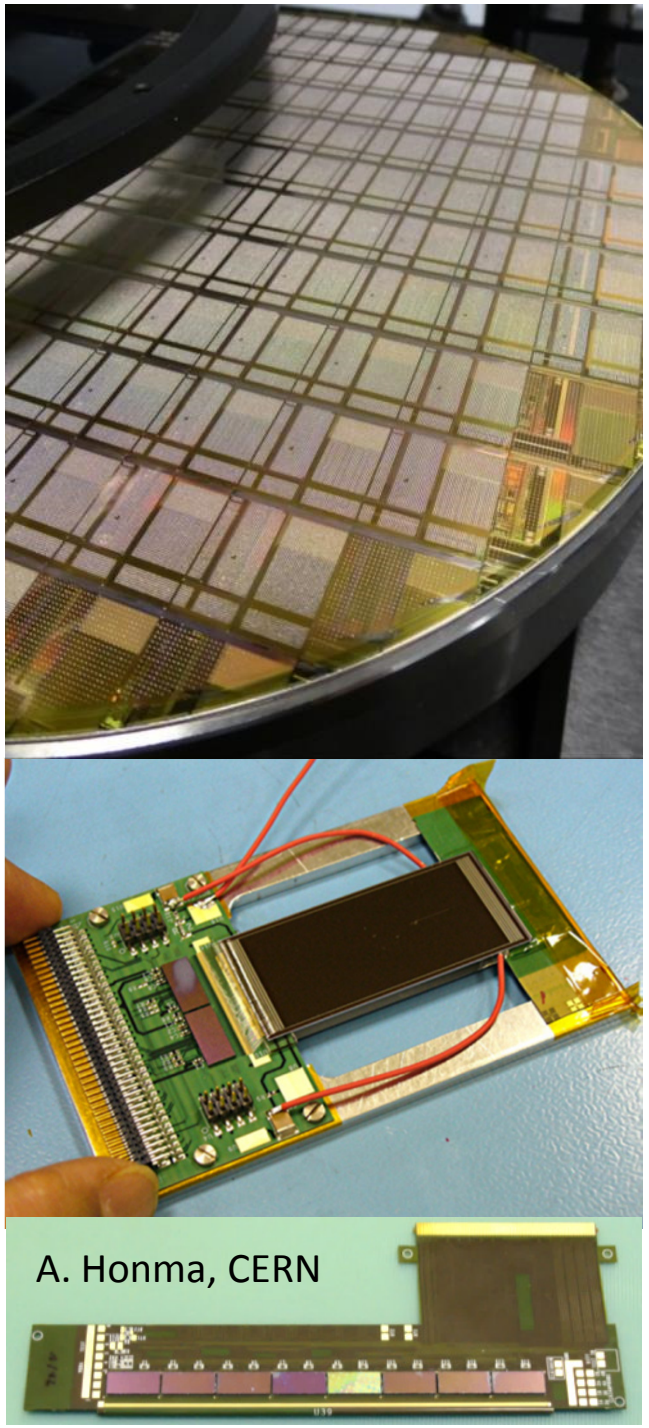
Summary & Conclusions

Two successful full-size prototypes of new Outer Tracker ASIC

- ✓ CBC2 working to specs
- ✓ Some front-end improvements over CBC1
- ✓ Stub finding logic functioning
- ✓ Power features (LDO & DC-DC) operational

First prototype version of 2S module in hand

- ✓ First demonstration of bump-bonded ASIC for strip readout
- ✓ Ready to be distributed to collaborating institutes
- ✓ First beam test followed by ionizing radiation studies



Acknowledgements

RAL: D. Braga, L. Jones, P. Murray

Imperial College: M. Raymond, G. Hall, M. Pesaresi.

CERN: S. Michelis, F. Faccio, K. Kloukinas

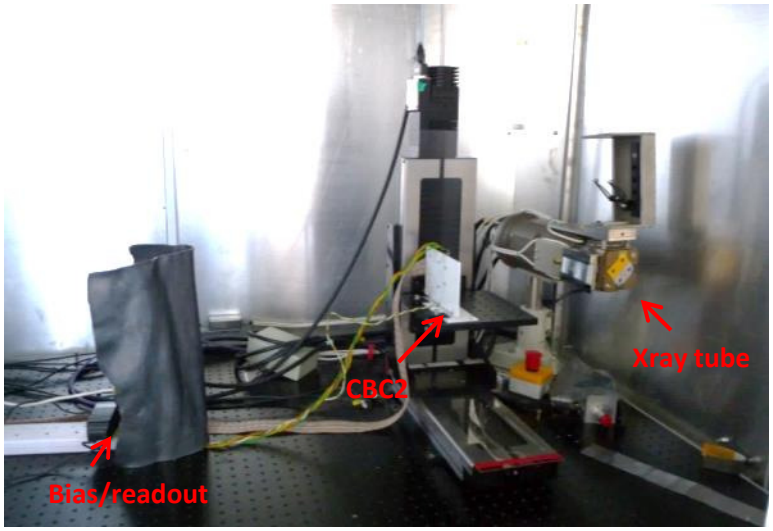
Many others for the beam test…

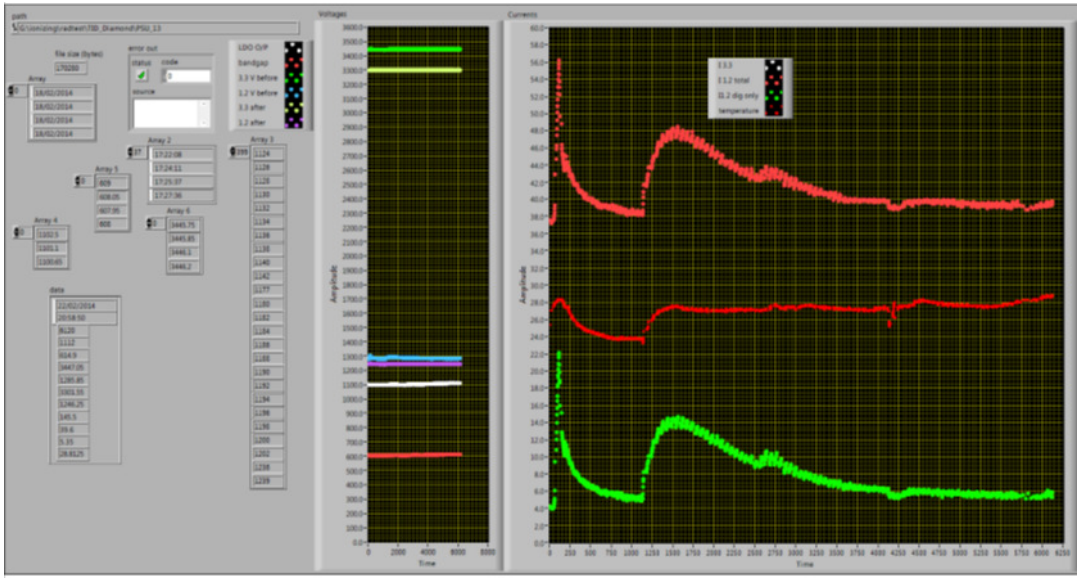
END


Backup slides

Total Ionizing Dose test

- First xray irradiation to 10 Mrads
- CBC2 operated continuously during irradiation
- monitored currents, biases, pedestal, noise
- no significant change in performance, moderate increase in current before annealing
- Next: TID test up to 50 Mrads

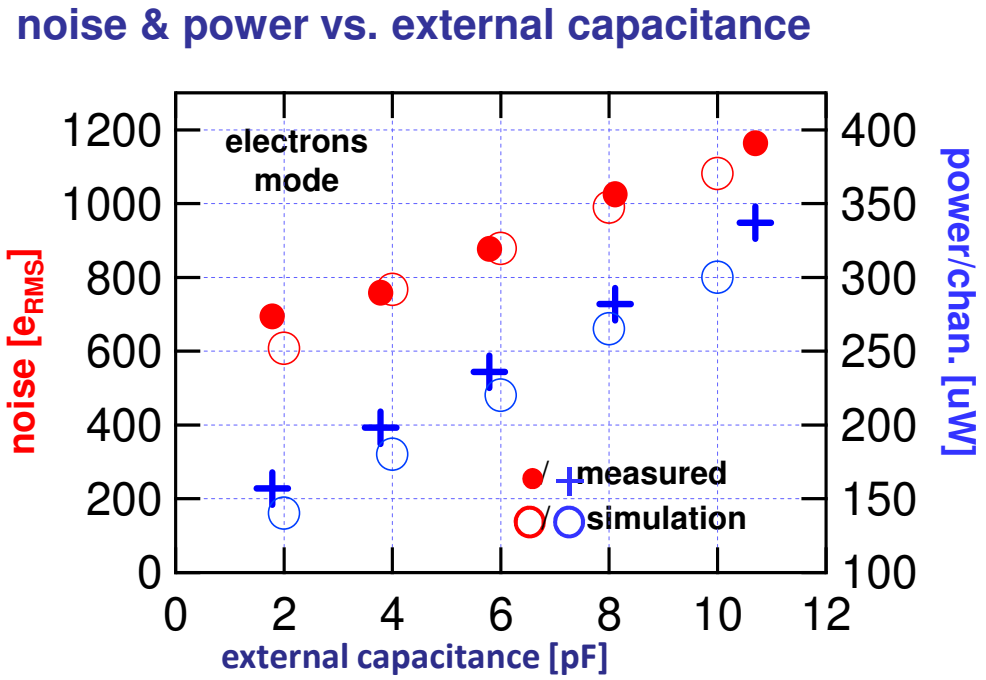




M. Raymond, Imperial College

Noise & Power

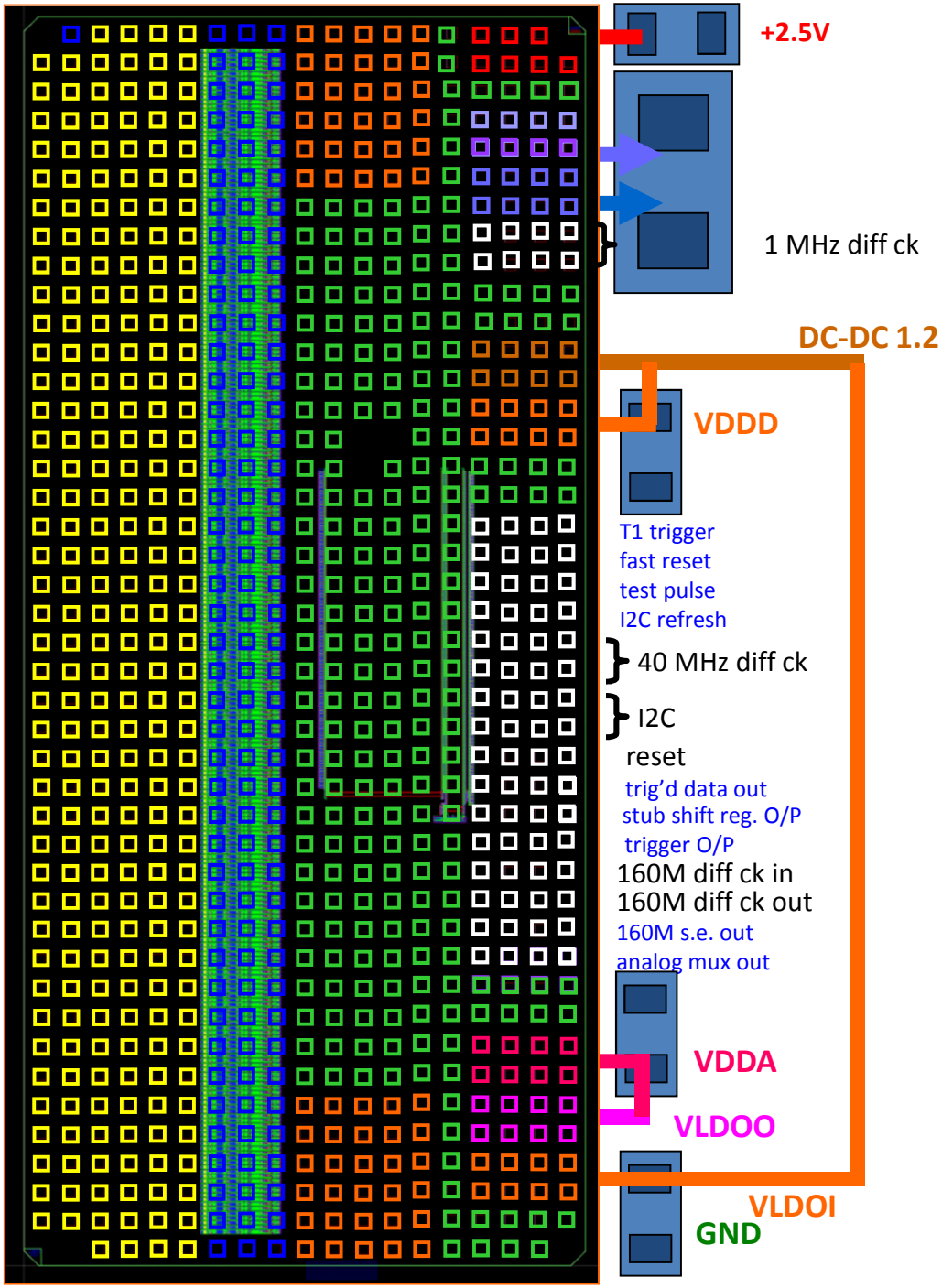
Analog:	130 + (21 x C_{in}[pF]) µW
Digital:	50µW
Trig. logic:	<50µW
Total:	<230 + (21 x C_{in} [pF]) µW
APV25	~2.6mW (long strips)



- Noise and power depends on external input capacitance
- The current settings in the front-end are adjusted to maintain the same pulse shape for different C_{in}
- Results almost identical for e^- and h^+

→ specification of **1000e^-_{RMS}** for 5cm strips met with **350µW/channel**

Power distribution



Inputs
dummy
prev/next chip
gnd

NB: the last column of PADs to the right are wire-bondable, they will not be routed on hybrid (->possible to reach the 3 pads to their left)

All but 160MHz output pads have redundancy

lines and arrows
show direction of power flow
(GND not shown)

note:

DC-DC 1.2 not connected
to VDDD or VLDOI on-chip

LDO output also connected to VDDA off-chip

(the idea is to maximise
possible effectiveness of
off-chip filtering)