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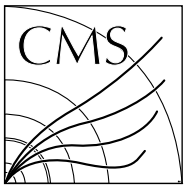

The Compact Muon Solenoid Experiment

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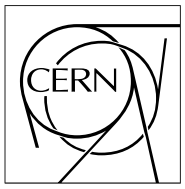

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Single Event Upset evaluations of CBC readout chips

K. Uchida, J. Borg, G. Hall, L. Jones, M. prydderch

Abstract

The Single Event Upset rate of the CMS Binary Chip (CBC) has been measured several times using different versions of the CBC in a series of tests in a 62 MeV proton beam to evaluate its sensitivity for use in the CMS tracker following the upgrade for High Luminosity LHC operation. Each version of the chip after the very first one has been subject to modest design improvements which affect the SEU tolerance. The main results are summarised, and the expected SEU rates in CMS 2S-modules at the HL-LHC are estimated.

1 Introduction

Single event upset (SEU) is a type of single event effect that arises from a significant localised ionisation energy deposit in a digital circuit. In the LHC environment, this mostly arises via knock-on silicon atoms generated in the chip by ionising particles or neutrons [1]. Light charged hadrons, leptons or light ions do not generally deposit enough localised charge to cause SEUs directly although occasional nuclear interactions with the silicon lattice in or near sensitive volumes are possible SEU sources. SEU is observed as a bit-flip in a register caused when the charge generated by an ionising particle is sufficient to change the state of the register. Depending on the detailed circuit design, multiple simultaneous bit-flips may be possible. Not many previous studies have been reported of SEU rates in front-end ASICs either at the LHC or in test beam evaluations (see e.g.[2–4]) although this will be an increasingly important consideration for operation at the High Luminosity LHC (HL-LHC).

The CBC ASICs have been manufactured using a Global Foundries 130nm CMOS technology and the pipeline control logic cells and I^2C registers are implemented with SEU-tolerant designs. Several versions of the CBC have been produced, as the requirements for operation in CMS have evolved. The first version, the CBC1, was a conventional LHC front-end readout chip containing amplifier, comparators and pipeline memory for each channel and multiplexed data output, but subsequent versions (denoted CBC2, CBC3.0 and CBC3.1) have been developed to meet the requirements of providing data to the track-finding processors and Level-1 trigger, using pT-modules [5], hence with cluster-finding and stub processing logic. (A stub is a pair of clusters in the two layers of sensors in the pT-module, which is consistent with a short track vector of interest.) Each version of the CBC has increased the amount of digital circuitry, with the largest increase between the CBC2 and CBC3.0 versions, thus potentially increasing the overall SEU susceptibility, even with improvements to the SEU tolerance.

It is not expected that the CBC designs should be totally immune to SEUs. Therefore an evaluation of each chip has been carried out in a 62 MeV proton beam line of a cyclotron at Louvain-la-Neuve. The results of those tests are summarised here. Typically, even with an exposure of around one or two working days, the number of SEUs observed is small so results are limited by statistics. The importance of an SEU also depends on its location in the CBC; most of the registers store values which have very limited consequences should they change, such as the fine tuning of the comparator threshold for each of the 254 CBC channels. A few values are more important for operation, such as the registers which store the latency value and the counters for pipeline read and write pointers. SEUs which affect hit data in the pipeline are expected to be unimportant, since the pipeline is regularly refreshed. However, once an SEU has corrupted a register, this will remain the case until a chip reset is issued, or the register is deliberately rewritten with its correct value; this is easily possible and even a low refresh rate should be sufficient to ensure the effect of SEUs on operation can be maintained at essentially negligible levels.

2 SEU measurements at Louvain

As explained in [1] the average SEU cross sections obtained with LHC secondary particle spectra in CMS are very similar to those from protons with energies of 60-200 MeV. Hence, the SEU tests of the CBC chips were all carried out in the Light Ion Irradiation Facility (LiF) at UC Louvain. The test beam was provided by a proton cyclotron in the LiF. The proton beam energy was set to the maximum, 62 MeV, and the tests were done with the maximum available intensity at the time, which was $\sim 2 \times 10^8\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, measured with a precision of 5%. Note that this

is considerably higher than the flux expected in the LHC which is explained later. Each test had a duration of 12 to 16 hours and CBCs in the beam received a radiation dose of 1-2 Mrad. The total dose behaviour of the CBC3 has been studied [6] and the consequences are insignificant at HL-LHC dose rates. At accelerated doses, an increase in the power consumption is observed, which does not affect operation. However, because of this, care was taken during the SEU studies to avoid any possible bias under different SEU test conditions. The beam conditions for each test are summarised in Table 1.

In the test system, a CBC was wire-bonded on a small board connected to a support board which provided differential buffering and driving of signals to and from backend electronics. For the CBC2, the backend electronics was located in a nearby control room connected to the support board by 5m of twisted pair cable. In the case of the CBC3.0 and CBC3.1, the back-end electronics was located on the floor in the beam line area behind a lead block because the twisted pair cable had to be shorter for the faster signals, clocked at 320 MHz compared to 40 MHz for the CBC2. In the CBC2 test, just one chip was placed in the beam. For the CBC3.0, one chip was placed in the beam and another outside the beam as a control, in case of external interference which could resemble an SEU. In the most recent test of the CBC3.1, three chips were placed in the beam, to increase statistics, and one outside the beam. The back end data acquisition system was based on the GLIB board [7] for the CBC2 and the FC7 [8] for CBC3.0 and CBC3.1.

Table 1: The beam parameters and exposure conditions

	CBC2	CBC3.0	CBC3.1
proton energy [MeV]	62	62	62
flux [10^8 cm^{-2}s^{-1}]	2.5	2.3	2.0
flux relative to HL-LHC	$\times$73.5	$\times$67.6	$\times$58.8
beam exposure time [h]	12	14.6	(3$\times$)15.6
total fluence [10^{13} cm^{-2}]	1.1	1.2	1.1
total radiation dose of CBCs in the beam [Mrad]	1.5	1.6	1.5

3 SEU sensitivity of the CBC

The overall design of the CBC is summarised in [9] and references therein. The first version of the CBC [10, 11] was a conventional 128 channel LHC readout chip, and was not subjected to an SEU test. The later versions, starting with the CBC2, included logic for stub-finding [12–15]. The CBC2 did not include all the circuitry required to transmit stub data off-chip at the full HL-LHC rate. This was done in the CBC3 [16, 17] which, following studies of CBC2 SEU resilience, also included modifications to further improve SEU robustness. The CBC3.1 design included some minor changes intended to finalise the chip for HL-LHC operation; some of them were intended to further reduce the SEU sensitivity. Following each new CBC version, SEU tests were carried out to evaluate the performance.

The chip has 254 front-end channels, with preamplifier, gain amplifier and comparator, and reads out microstrips from two sensors, with alternate CBC channels connected to either upper or lower sensor [14]. In this way, it is relatively simple to compare hit patterns between the two layers, to identify those which are compatible with a higher transverse momentum track candidate ($p_T \gtrsim 2$ GeV/c). The outputs of the comparators follow two separate data paths; in one of them data are stored in a pipeline memory buffer. When a L1 trigger is received, the data of interest are loaded into a 32-deep readout buffer before being read out serially, at 40 Mbps

in the CBC2, and at 320 Mbps in the CBC3. The L1 trigger counter is incremented on receipt of a trigger and transmitted with the data.

A second data path is responsible for identifying and reading out stubs through several stages of combinatorial logic. As explained elsewhere, this path runs at the LHC clock rate to transmit data from every beam crossing for use in the CMS L1 trigger by permitting real-time track reconstruction [18].

The digital circuitry is used to operate the pipeline memory, to store values in I^2C registers to program various operating parameters in the chip, and within the pipeline itself to store binary values representing hits until they can be read out after the latency period, which is up to 6.4 μs (CBC2) or 12.8 μs (CBC3). The most relevant CBC parameters for each chip are summarised in Table 2. Therefore possible types of error in the CBC are bit-flips in pipeline cells, pipeline logic upsets, and bit-flips in I^2C registers.

Table 2: Relevant CBC parameters

	CBC2	CBC3.0 / CBC3.1
Channels	254	254
Pipeline memory length	256	512
Storage buffer depth	32	32
I^2C registers	307	330 / 338
Data storage (memory) cells	73,536	138,592
Readout speed [MHz]	40	320
Data and header frame readout time [μs]	6.65	0.95
Stub resolution	1 strip	half strip
Stub readout	OR of all stubs	addresses & bends of up to 3 stubs

Bit-flips in pipeline cells should be unimportant as during CMS operation the memory cells are overwritten every 25 ns clock cycle, so every cell in the CBC3 pipeline is refreshed once every 12.8 μs. They can be detected in an SEU test by storing data at the start of a test with a high comparator threshold so that no channel hit is created and a logic 0 is written into all cells of the pipeline. Then later, if a logic 1 is detected, it must be due to a bit-flip in the pipeline cell. It can also be done in the converse way by initialising cells to logic 1 and checking for a logic 0, and this method was also used.

Although upsets in pipeline data should be unimportant for CMS operation, it was decided to confirm it by dedicating some time to such a test. In addition, hit data stored in the pipeline are transferred to a 32-deep buffer following a trigger. However, normally only a few cells of this buffer will be occupied because of the trigger rates expected in CMS p-p running. Data in the readout buffer could stay up to $\sim 200\mu$s (CBC2) or $\sim 30\mu$s (CBC3) in the very extreme case that 32 triggers are received very close together in time. At the maximum trigger rate of 750 kHz expected at HL-LHC, Poisson fluctuations mean that this will be very rare.

Pipeline logic upsets are detected by means of an error bit in the header preceding each frame of data read out from the CBC. There are two special counters in the pipeline logic, one for the read pointer and the other for the write pointer. The difference between their values corresponds to the trigger latency which is stored in an I^2C register. Any of the three values of read or write pointer, or stored latency value could be affected by an SEU. If the difference between the read and write pointer values is different from the value stored in the I^2C latency register, an error bit is set in the data header. This kind of error will then persist until the three values are reset.

In the case of I^2C registers, bit-flips are detected by comparing the read value with the written

value. Although there are more than 300 8-bit I^2C registers, 254 of them are used for channel offsets and each register affects only one channel so the impact of an SEU is still very minor. Some control registers which define analogue circuit parameters for the full 254 channels or which influence the digital logic for hit detection and stub identification might have a bigger impact on operational efficiency, but will not generally disable the chip. However, a small number of registers might generate a state which requires a reset for normal operation to continue; no error of this type has been detected.

Different means have been adopted to make these components SEU tolerant. The pipeline logic has been designed using Whitaker cells [19]. In this case SEU events can only corrupt the cell state while writing a value at a clock edge, which lasts for an extremely short time (much less than 1 ns). Whitaker cells were not originally used for I^2C registers, but this was adopted for the CBC3, as explained below.

A majority voting scheme was implemented for the I^2C registers in the CBC2, where each loaded bit state is triplicated and stored; the majority of the states in the three cells defines the state of the bit. This means that an SEU has to occur in at least two cells to flip the logical state of the bit. In addition, an external I^2C refresh signal was implemented. Once this signal is sent to the CBC, each register bit is set to the majority of the three relevant cells. If this refresh is carried out sufficiently often, it should be rare that more than one cell among the three has changed state, so the bit-flip rate is expected to be minimal. However, from the result of the SEU tests on the CBC2, the spatial separation of the triplicated logic was suspected to be too small. Therefore, in the CBC3, it was replaced by Whitaker cells.

To compute the rates in the HL-LHC environment, it is necessary to know the flux of particles where the CBCs will be located. This is explained in the tracker upgrade TDR [5]. The maximum total ionising dose in the Outer Tracker, in the vicinity of 2S-modules, is computed to be 9 Mrad for 3000 fb^{-1} of integrated luminosity. Assuming this is delivered over 10 years with an operational year of 10^7 s entirely by minimum ionising particles (MIPs), it corresponds to a maximum flux of 3.4×10^6 $cm^{-2}s^{-1}$. The statistical uncertainties were estimated to be less than 8% [5].

4 Method of SEU testing

In each of the tests, the detailed procedure was changed slightly to adapt to differences in the CBC versions or the readout system. However, the method was essentially the same in each case, and is described below.

4.1 Pipeline logic test

Once the CBC receives a signal denoted as a fast reset, the logic is reset, as is the error bit, and the write counter starts to increment. The trigger pointer starts after the trigger latency period which is stored (in clock cycles) in an I^2C register. The CBC writes data (the binary value corresponding to the signal from the front end amplifier, following a comparator and hit-detect logic) to the pipeline address at the write pointer value. The CBC reads out data from the location of the read pointer, which is the trigger counter value when it receives the trigger signal.

The pipeline logic was tested by checking the error bit in the triggered data header. If the error bit is not set (0), it means that no bit-flip occurred in either the read or write counters or the latency register during the interval between the last fast reset and the trigger signal. If the error bit changed from 0 to 1, a bit-flip must have occurred and that error persists until a fast reset

is sent. A trigger was sent multiple times after a fast reset to accumulate statistics. An upper limit was estimated for the pipeline logic error rate since this type of error was not observed.

4.2 Pipeline cell test

The pipeline and readout buffer cells were tested together with the pipeline logic. Triggers were sent periodically so that only data for a single event was present in the readout buffer. To increase sensitivity while limiting dead time in the CBC2 test, the 40 MHz clock was stopped for 260 cycles and started just before the next trigger. In this way, all the data stayed in the pipeline cells for at least 260 clock cycles (6.5μs). This was not possible for CBC3 tests due to the more complex control logic for the fast serial interface with its 320 MHz clock.

4.3 I^2C register test

The CBC chips have registers written to and read back via the I^2C serial interface. Three quarters of the registers are used for the fine adjustment of the offset level for each channel with respect to a single global threshold for the hit logic. There are 254 channels for both CBC2 and CBC3. For the SEU tests, the contents of the I^2C registers define the number of cells with logic 0 and 1. These could be chosen arbitrarily for offset values to populate 0s and 1s in a convenient way. However, control registers were configured for normal operation in all tests, which meant that arbitrarily chosen values of register settings could not be used.

Since the I^2C registers are implemented in different types of logic cell for CBC2 and CBC3, the testing methods were different. The following subsections describe them separately for each CBC version.

4.3.1 CBC2

I^2C register upsets were checked periodically by reading them at a time T_0 after setting their contents, as in Figure 1. The offset registers were set to values such that the numbers of logic 0 and 1 were roughly the same. The I^2C refresh signal was issued from the back end data acquisition.

The sequence in this test was as follows:

- a hard reset was sent from software,
- I^2C registers were configured,
- I^2C refresh signals were sent periodically from firmware or software,
- I^2C registers were read and recorded at time T_0 after configuration,

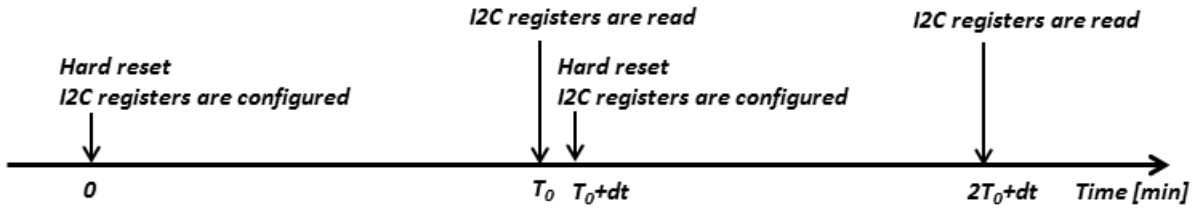

Figure 1: I^2C register test sequence.

4.3.2 CBC3

One relevant change between the CBC2 and CBC3 was an increase in the pipeline length to increase the latency. Although the memory cell circuit is fundamentally the same type, the

circuit was modified in three significant ways: read and write transistors were changed from NMOS to PMOS; NMOS transistors in back-to-back inverters were changed to an enclosed geometry, effectively increasing their size by a factor of 4.5; the cell layout was made more compact, so that the CBC3 memory area is less than 1.5 times larger than the CBC2 despite doubling the number of bits.

The second change probably enhanced the SEU tolerance, but the third one might have increased the SEU probability. In addition, the increased memory size required extra intermediate buffering in control and read/write lines so the memory is in manageable blocks. This introduced extra logic buffers which could be susceptible to SEU.

In the case of the CBC3, I^2C register upsets were checked by periodically reading them after an interval T. This was done for the CBC3.0 during the data taking run, in parallel with the pipeline logic and readout buffer test, and (for practical reasons) between runs for the CBC3.1.

The registers were configured once at the beginning of each run. The runs were stopped when necessary, especially when bit-flips which disturbed data taking were observed. In this version of the CBC, there are a small number of read-only bits for monitoring errors, and also some extra read-only bits added to the CBC3.1 to allow to test hit data transfer to the nearest neighbour chip. In total, 316 8-bit registers (of which a total of 5 bits were read-only) were checked in the CBC3.0 (14 registers were omitted), and 332 8-bit registers (of which 11 bits were read-only) were checked in the CBC3.1 (3 registers were omitted.) In both tests, control registers were configured with values for normal data taking.

Four different configurations of channel offsets were tested in the CBC3.0, as shown in Table 3. Configuration D used two values, 0x80 and 0x7f, with half the channels set to one of the values. Only configuration D was used for the CBC3.1 test.

Table 3: I^2C register offset settings for CBC3.0 and the total exposure time for each setting. The periodic read interval was set to 5 mins except for (*), where it was set to 5 sec. For run D, half the channels were set to each value.

Setting type	time [h]
A: all 0xff	4.64
B: all 0x00	1.62
C: all 0x0f	2.80
D: 0x80/0x7f	2.49
D: 0x80/0x7f (*)	0.42

5 SEU results from the CBC2

A detailed discussion of the CBC2 tests and results is given in [20]. No errors attributable to SEUs were observed in the pipeline logic in an interval of 1.2×10^4 s, which corresponds to 9.0×10^5 s, or 11 days, at HL-LHC. With a confidence level of 99%, this corresponds to a Poissonian upper limit on the rate per CBC of 0.019 SEU h^{-1}.

78 bit-flips were observed in I^2C registers during the test, which took place over two days in 2014. Of those, 21 were $0 \rightarrow 1$ and 57 were $1 \rightarrow 0$ bit-flips. There were a few examples of multiple bit-flips; 14 registers were affected in this way, comprising $5\times$ 2-bit-flips, $6\times$ 3-bit-flips and $3\times$ 4-bit-flips. The results are summarised in Tables 4 and 5. Run 9B was simply to verify that no bit-flips were observed without beam.

In both single and multiple upset cases, flips $0 \rightarrow 1$ were less frequent than those $1 \rightarrow 0$. Of the single bit-flips, there were $8\times$ $0 \rightarrow 1$ compared to $30\times$ $1 \rightarrow 0$. In the multiple bit-flips, there were $13\times$ $0 \rightarrow 1$ compared to $27\times$ $1 \rightarrow 0$. This could indicate a different SEU cross section for the p and n nodes. It was suspected that the multiple bit-flips might occur if the three cells used for triplication were too close to each other, so that a single SEU event could change the state of multiple cells in a register, but this was ruled out from an examination of the circuit layout. Later studies on the CBC3 suggest that it might be a result of I^2C registers being reset to the last written value or the default value, which is hard to verify from the CBC2 data.

Using the data from Run 4 and 12 in Tables 4 and 5, a total of 27 registers experienced a bit flip in 130 min exposure. Data from other runs was ignored, because of uncertainties in the efficiency of the refresh mechanism. Scaling this to the HL-LHC, in a flux of 3.4×10^6 $cm^{-2}s^{-1}$, would lead to an SEU event rate of approximately 0.17 $CBC^{-1}h^{-1}$ which was considered higher than desirable. Hence improvements to the design were sought.

There were no observed bit-flips in the pipeline control logic and it was therefore decided that Whitaker cells should be adopted for the next iteration of the design.

Table 4: Summary of CBC2 bit-flips in I^2C registers. N^{cycle} is the number of 10 min periods used for each run.

Run	Beam	Number of bit-flips					I^2C refresh	
		$0 \rightarrow 1$	$1 \rightarrow 0$	Total	N^{cycle}	Total/N^{cycle}	Hz	pulse length
Run 4	On	5	11	16	7	2.29±0.57	-	-
Run 6	On	1	5	6	7	0.86±0.35	1	1 msec
Run 8	On	6	4	10	6	1.67±0.53	10	1 msec
Run 9A	On	5	21	26	4	6.50±1.27	10	25 nsec
Run 9B	Off	0	0	0	3	0.00±0.00	10	25 nsec
Run 12	On	4	16	20	6	3.33±0.74	-	-
Total		21	57	78				

Table 5: I^2C register bit-flips in the CBC2, where multiple bit changes occurred. The page and address specify the 8-bit I^2C register.

Event	Run	Page	Address	Written value	Read value	Default value
1	4	2	0xfd	01101000	01010000	10000000
2	4	2	0x80	01011000	01010100	10000000
3	4	2	0x25	01011001	01010101	10000000
4	8	2	0xb1	01000110	01010101	10000000
5	8	2	0xe0	01010000	01010101	10000000
6	8	2	0x45	01001100	01000101	10000000
7	9A	2	0x1d	01001110	00000100	10000000
8	9A	2	0x64	01001100	10000000	10000000
9	9A	2	0x93	01011110	01010101	10000000
10	9A	1	0x28	11111111	01010101	00000000
11	9A	2	0x10	01000011	00000000	10000000
12	9A	2	0x29	01010000	01010101	10000000
13	12	1	0x28	11111111	01010101	00000000
14	12	2	0x33	01011011	01010101	10000000

6 SEU results from the CBC3.0

This test was carried out in 2017. As explained the principal change relevant for SEU performance was to replace triplicated logic in the I^2C registers by Whitaker cells.

12.4 hours were dedicated to measure the SEU rates. However, a wrong procedure for most of the data taking resulted in a fast reset being sent just before the L1 trigger for 11 hours of data taking so only 1.4 hours could be used to estimate the SEU rate in the pipeline logic. No errors were observed in an interval of 5040 s, which corresponds to 3.4×10^5 s at HL-LHC. With a confidence level of 99%, this corresponds to a Poissonian upper limit on the rate of 0.049 SEU h^{-1}.

Because of the error in the operation procedure, only the 1.4 hours of data taking could be used to estimate the error rate on hit data in the pipeline. In 5.1×10^6 triggers, no fake hits were detected.

In the case of I^2C registers, the test was not affected by the wrong procedure and the entire 12.4 hours of data could be used. The results are given in Table 6 and in detail in the Appendix. 25 bit-flips were observed. All of them were of single bits. Again $0 \rightarrow 1$ flips were less frequent than $1 \rightarrow 0$, here by a ratio of 1:24. Most bits experienced a flip, but lower order bits appear to be more frequent, particularly bit-4 of [0:7].

The rate corresponds to 8.6×10^{-6} s^{-1} or 0.031 ± 0.006 $CBC^{-1}h^{-1}$ in CMS. This is significantly lower than in the CBC2, as expected, but is not zero. This is because there are still some SEU-sensitive nodes in the register circuitry. An SEU on a write node causes the storage cell to flip to the last write transaction on the bus. An SEU on the reset node causes the cell to flip to its default value.

Table 6: Summary of CBC3.0 bit-flips in I^2C registers.

Setting type	duration [h]	Number of bit-flips		
		Total	$0 \rightarrow 1$	$1 \rightarrow 0$
A (all 0xff)	4.64	14	0	14
B (all 0x00)	1.62	2	1	1
C (all 0x0f)	2.80	4	0	4
D (0x80/0x7f)	2.91	5	0	5
Total	11.97	25	1	24

6.1 Direct exposure to heavy ions

During the course of other tests, data have been collected with prototype modules read out by the CBC3.0 exposed to heavy ions in the CERN H8 test beam. Although these do not generate such large localised charge deposits in the CBC ASIC as atomic knock-on events, they do generate very large ionisation signals in the sensors and are of interest because they resemble knock-on ion events within the sensors, for light ions at least. A fully stripped ion will generate a charge signal in silicon Z^2 times larger than a singly charged hadron, where Z is the atomic number of the ion. For example, xenon ions ($Z = 54$) with 150A GeV/c, which were used in H8, will generate signals in the sensors of almost 3000 MIPs ($\sim$12 pC in 300 μm silicon), which is well beyond the linear dynamic range of the CBC. The response to such sensor signals was studied to verify that the recovery time of the amplifier circuit was sufficiently fast. The response to such signals was observed to be limited to a localised overload affecting only a few nearby channels, with the size diminishing significantly away from the central core, from which they recover within 3 μs at the centre, and shorter times for the peripheral signals.

This also provided an opportunity to expose the CBC directly to a xenon beam in November 2017. The main difference between SEU-type events and exposure to a high energy ion beam is that the beam traverses the ASIC so the energy deposited is distributed approximately uniformly along the path of the beam, rather than in a very small volume as is the case when a knock-on ion comes to rest. This would imply a deposit of $\sim$40 fC in 1 μm depth, using the figures above.

The conditions in the beam did not permit a qualitative evaluation of SEU rates, since the flux was not well measured. However, a number of SEUs were observed, but no damage to the exposed CBCs resulted. In any case, such an exposure is not expected in CMS.

7 SEU results from the CBC3.1

The CBC3.1 is expected to be the final version of the CBC, having included a small number of minor changes to correct or improve small details of performance.

The I^2C registers for the CBC3 were designed in such a way that the SEU-tolerant Whitaker register cell for each bit of an 8-bit register employs its own set of standard inverters to buffer the reset and write signals, and produce their inverse for the purpose of controlling both n and p-type transistor switches in the circuit. These inverters are small in dimension, resulting in small node capacitances that make the circuit more susceptible to upset when an ionising particle deposits charge on the sensitive nodes. This was reasoned to be the cause of the single bit-flips observed during testing of the CBC3. To counter this without major changes to the ASIC, it was shown by simulation that by merging together all of the reset lines, and likewise all of the write lines, for every bit across the 8-bit register, the effective capacitance of the sensitive nodes was multiplied eight times and required a greater charge deposit to cause an upset. The registers in CBC3.1 were re-wired to implement this strategy.

A consequence of this modification is that any particle depositing enough charge on either the reset or write line to the 8-bit register will potentially cause all eight bits to upset. To increase further the capacitance and hence the resistance to SEU, the size of the inverter cells used on CBC3.1 was also increased as much as possible within the constraints of the existing layout, leading to devices three times their original size. Simulations of the modified circuit using standard corner models for the technology showed the modified circuit to be resistant up to a deposited charge of 864 fC, over thirty times greater than for the unmodified circuit.

The CBC3.1 test was carried out in 2019. As statistics had regularly been a limit to the measurements, they were increased by equipping the setup with four CBC3.1 chips, three of which were exposed to the beam, with the fourth control chip outside the beam.

An unexpected event was observed once in each of the three chips in the beam but not attributed to an SEU during the 15.4 hours of data taking. In each case, a small group of consecutive I^2C registers was reset to their default values. It was believed that this was caused by an upset in the nearby interface electronics which was only partially shielded from the beam and not radiation hard. However, it was not possible conclusively to rule them out as SEUs occurring in the CBCs themselves, even though the behaviour was not believed to be consistent with the design of the CBC register control distribution. This remains a subject for further investigation.

No pipeline logic errors were observed in 3662 seconds in the three exposed CBC3.1s. Combined with the results from the CBC3.0, this leads to a 99% confidence level Poisson upper limit

on the rate per CBC of 0.017 SEU h^{-1}. This is only slightly less than the limit established for the CBC2 but the memory is twice the size, with more extensive control logic.

A small number of errors in the pipeline memory data were observed. Triggers were sent at 20 kHz with the latency between the write and read pointers set to 12.5 μs, which is almost the maximum value which will be allowed in CMS, checking for both $1 \rightarrow 0$ and $0 \rightarrow 1$ types of error. 74 unexpected values in the three CBCs were observed in the 7.32×10^7 triggers. Taking into the account the flux relative to HL-LHC this corresponds to a false hit rate of 2.2×10^{-11} per trigger in CMS, which can be compared with an expected occupancy $\sim$1-2%.

15.4 hours were dedicated to measuring the SEU rate in the I^2C registers, which was where possible changes compared to the CBC3.0 were expected. In the entire test, the content of each register remained unchanged, and the 254 offset registers were all configured so that half of them took the value 0x80 and the other half 0x7f. In this way the offset was in both cases in the middle of the range but with seven 0s in one case and seven 1s in the other. While the numbers of logic 0 and 1 in the configuration used in the test were almost equal, the default values are dominated by 0, as shown in Table 7. Table 8 shows the number of bits for different configurations which could be checked during each test.

Table 7: The number of logic 0 and 1 in the 330 8-bit registers for the default settings of the CBC3.1 and for the configuration used in the test. Eight registers which were not checked are ignored.

	Number of logic 0	Number of logic 1
Default settings	2026	614
Test configuration	1234	1406

Table 8: The number of logic 0 and 1 in the 330 8-bit registers which could be compared with the value in the first column for different test configurations of the CBC3.1. A bit which is set to 1 can only be checked for a $1 \rightarrow 0$ transition, for example.

	Number of logic 0	Number of logic 1
Default settings	153	945
0xc1	462	878
0x55	610	696
0x00	0	1406
0xff	1234	0
0x41	306	1053

For the CBC3.0 test, the last written value to the I^2C register was always the same (0x41) but different values were used in the CBC3.1 exposures, as listed in Table 9, to study its influence more carefully. One register was written with the chosen value, e.g. 0x55, after all the registers had been read to check their contents. Then, 0x55 stayed in the latch and if the write line of any register were to experience an SEU, that value would be written to the register.

81 register value changes were observed, of which 38 altered a single bit. The three CBC3.1s appeared to behave similarly with 34, 23 and 24 SEUs observed in each of them. The detailed results are shown in the Appendix. In summary, there were 10×2-bit, 3×3-bit, 9×4-bit, 4×6-bit, 14×7-bit and 3×8-bit flips. This behaviour was more complicated than originally expected and the register content changes were studied to seek any patterns which could explain it. As explained earlier for the CBC3.0, two types of expected correlation were with the default value of the register setting, and the last written I^2C value transmitted to the CBC. In most cases, the bits which changed took a value which was consistent with the same bits in either the default setting, or the last written value.

Table 9: The conditions of each CBC3.1 test and numbers of SEUs observed. The periodic read interval was 2 sec. As explained in the text, several runs were taken alternating the last written value between 0x00 and 0xff.

Run ID	Last written value	duration [h]	No. SEU	rate [h^{-1}]
1	0xc1	0.45	6	13.4 ± 5.5
2	0xc1	1.21	10	8.2 ± 2.6
3	0x55	2.01	13	6.5 ± 1.8
4	0x00	0.96	0	0.0 ± 0.0
5	0xff	0.72	6	8.4 ± 3.4
6	0x00/0xff	1.37	10	7.3 ± 2.3
7	0x00/0xff	0.88	3	3.4 ± 2.0
8	0x00/0xff	0.91	5	5.5 ± 2.5
9	0x00/0xff	0.62	5	8.1 ± 3.6
10	0x00/0xff	1.06	2	1.9 ± 1.3
11	0x41	0.94	2	2.1 ± 1.5
12	0x41	0.99	0	0.0 ± 0.0
13	0x00/0xff	3.25	19	5.8 ± 1.3
total		15.36	81	5.3 ± 0.6

It was found that the rate of bit-flips depended most strongly on the last written value. In particular, if the value was 0x00, the rate was significantly lower than when it was 0xff. Therefore, to improve the statistics under those conditions, each periodic I^2C register check, carried out at 2 s intervals, was followed by writing a register with either 0x00 and 0xff, toggling so that the last value alternated between 0x00 and 0xff, for a total of 8.1 hours. This method was adopted to avoid any risk of radiation effects from the accumulated dose biasing the result. The conditions for each configuration and the numbers of SEUs observed are summarized in Table 9.

72 events were consistent with bit-flips to the last written value, while 31 events were consistent with bit-flips to the default value (see Figure 2 where the register changes are categorized according to the new flipped values). For many of the flipped bits, the default and the last written value were the same, thus indistinguishable. All of the four SEUs which were not consistent with either a flip to the default or last written value were single $1 \rightarrow 0$ bit-flips.

Combining the data from Runs 4-10 and 13, 47 SEUs were observed in 4.76 h when the last written value was 0xff, while only 3 SEUs were observed in 5.00 h when the last value was 0x00, a ratio of 16.5, with a large statistical error because of the small number of 0x00 SEUs. Of these 3 events, 2 are single bit-flips while the third is an 8-bit transition from 0xff to 0x00; all three are consistent with the last written value, while the two single bit-flips are also consistent with the default value.

From these results it is possible to compute the expected SEU rate in CMS at the HL-LHC, for different choices of the last written value, which are shown in Table 10. By choosing a value of 0x00, it should be possible to operate in CMS with an SEU rate of 0.010 ± 0.006 $CBC^{-1}h^{-1}$. If the anomalous events mentioned earlier are also attributed to genuine CBC SEUs and not the interface circuitry, then this would increase the rate in CMS to 0.014 ± 0.006 $CBC^{-1}h^{-1}$.

7.1 Operation in CMS

Although SEUs in CMS during the HL-LHC era may be more troublesome than in the past, there is no specification for an acceptable rate, and SEU effects will in any case clearly depend on the specific consequences for the affected ASIC and its location. Atomic knock-ons will in-

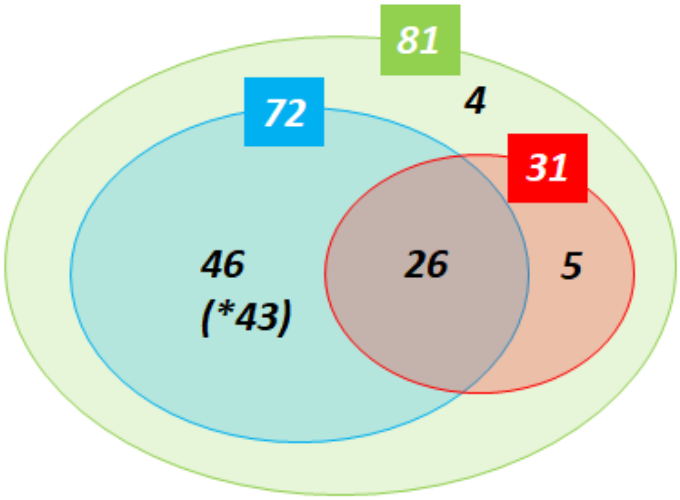

Figure 2: The 81 SEU events in I^2C registers categorized according to the new (flipped) value: the default value (red), the last written value (blue), or neither. Of the 72 events where the register changed to the last written value, 43 had multiple bit-flips. The 4 events inconsistent with both the last written value and the default value were all single $1 \rightarrow 0$ bit-flips.

Table 10: Comparison of SEU rates in the CBC3.0 and CBC3.1 I^2C registers depending on the last written register value.

CBC version	Last written value	SEU rate at HL-LHC [$CBC^{-1}h^{-1}$]
CBC3.0	–	0.031 ± 0.006
CBC3.1	all used	0.090 ± 0.010
CBC3.1	0xff	0.168 ± 0.025
CBC3.1	0xc1	0.164 ± 0.041
CBC3.1	0x55	0.110 ± 0.030
CBC3.1	0x41	0.018 ± 0.012
CBC3.1	0x00	0.010 ± 0.006

evitably be more frequent closer to the beam but the innermost detector ASICs are presently at a relatively early stage of development. The impact of SEUs may be most strongly felt on control functions, rather than on data corruption, which has been demonstrated by these measurements to be trivial for the CBC data. In the CBC, an upset affecting the stored value of the latency or the read or write counters would force that chip out of synchronisation which would corrupt the data until the correct values have been restored. However, a significant number of chips would need to go out of sync before there is a noticeable effect on data quality, given the redundancy in the track finding, and large number of tracks being measured in each interaction.

It is also difficult to be guided by experience from the present silicon strip tracker. SEUs were not explicitly monitored during data taking, except by counting the front-end ASICs which went out of sync during a run. However, this was difficult to correlate with luminosity, since global CMS resets were issued during data taking in response to unexpected conditions in a wide range of sub-systems which had not been foreseen.

In future, it seems wise to monitor the status of the registers on (all) the ASICs to keep a record of the rate of SEUs, and react if required. About twenty CBC registers have a global effect on the chip, hence should be monitored most frequently, e.g. at $\sim$1 Hz. Conversely, it does not seem useful to continuously monitor the 254 threshold offset values, which affect only a single channel, but the pipeline logic could also be monitored at $\sim$1 Hz, especially since the error bit in the CBC header may be ambiguous when it reaches the data acquisition.

Monitoring the register contents requires an I^2C read transaction, which takes about 40 μs at the 1 MHz I^2C clock frequency used. There are 7,680 2S-modules in CMS [5], each containing 16 CBC chips, so 122,880 CBCs in total. An upset rate of 0.01 SEU $CBC^{-1}h^{-1}$, monitoring 20 of the 338 registers, implies 0.02 registers s^{-1} in the entire system would require a reset. This can easily be accomplished by rewriting the value at a convenient moment in data taking, such as a pause for system resets or during a calibration operation in another sub-system, once the actual operating conditions are better established.

8 Conclusions

SEU tests have been carried out on several versions of the CBC readout ASIC. In the final version of the chip, the CBC3.1, no pipeline logic error was observed in the equivalent of 11 days of continuous operation in CMS at the HL-LHC and gives a 99% Poisson upper limit of 0.017 SEU $CBC^{-1}h^{-1}$. A fake hit rate in any channel of 2.2×10^{-11} per trigger in CMS was inferred from the measurements, which can be compared with an expected occupancy of 1-2%. 3 SEU events were observed in I^2C registers in the equivalent of 903 h, or 38 days, of HL-LHC operation, providing the last value written to an I^2C register on the chip was set to be 0x00, which is a rate of 0.010 ± 0.006 $CBC^{-1}h^{-1}$.

Only a handful of I^2C registers have a significant effect on the chip by, for example, controlling latency values, amplifier bias settings or global values of the comparator thresholds. Most of the I^2C registers store comparator offset values which are for the fine tuning of signal thresholds for a single channel and hence will have little effect on operation should they be disturbed. However, it will be desirable to monitor SEU rates in the experiment to ensure expectations are met. Checking the contents of the most sensitive registers and recording changes will be useful, and correction can be undertaken with no impact on operation during data taking.

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Appendix

Table 11: The complete list of I^2C register bit-flips in the CBC3.0. The page and address specify the 8-bit I^2C register. The last written value was always 0x41. A, B, C and D refer to the channel offset values used and are specified in Table 3.

Setting type	Page	Address	Written value	Read value	Default value
A	2	0x17	11111111	11111011	10000000
A	2	0x2d	11111111	11011111	10000000
A	2	0xc4	11111111	11111101	10000000
A	2	0x5d	11111111	11111101	10000000
A	2	0xd3	11111111	11110111	10000000
A	2	0x4f	11111111	10111111	10000000
A	2	0x97	11111111	11110111	10000000
A	2	0x01	11111111	11110111	10000000
A	2	0x08	11111111	11110111	10000000
A	1	0x29	11111111	11111101	11111111
A	2	0x6d	11111111	11110111	10000000
A	2	0xa6	11111111	11110111	10000000
A	2	0xab	11111111	11110111	10000000
B	1	0x1b	00000100	00000000	00000000
B	2	0x37	00000000	10000000	10000000
C	2	0xc8	00001111	00001110	10000000
C	2	0xef	00001111	00001011	10000000
C	2	0xdc	00001111	00001101	10000000
C	2	0xfa	00001111	00000111	10000000
D	2	0x99	01111111	01110111	10000000
D	2	0xda	01111111	00111111	10000000
D	2	0xda	01111111	01110111	10000000
D	2	0xa0	01111111	01110111	10000000
D	2	0xa4	01111111	01110111	10000000

Table 12: CBC3.1 bit-flips in I^2C registers. Columns I and II show if the bit-flips are consistent with the default value or the last written value. 1 = consistent, 0 = inconsistent.

Evt.	Page	Addr.	Written	Read	Default	Last written	I	II	1→0	0→1	# bfs
Run ID 1											
1	2	0x7e	10000000	11000001	10000000	11000001	0	1	0	2	2
2	2	0xac	01111111	00111111	10000000	11000001	1	0	1	0	1
3	1	0x4d	01100110	11100111	01100110	11000001	0	1	0	2	2
4	2	0xfe	01111111	11111111	10000000	11000001	1	1	0	1	1
5	1	0x3c	11111111	01111111	11111111	11000001	0	0	1	0	1
6	2	0xdf	01111111	11111111	10000000	11000001	1	1	0	1	1
Run ID 2											
7	1	0x3d	11111111	10111111	11111111	11000001	0	0	1	0	1
8	2	0x27	10000000	11000001	10000000	11000001	0	1	0	2	2
9	1	0x1c	10000100	10000101	00000000	11000001	0	1	0	1	1
10	2	0xfb	01111111	11111111	10000000	11000001	1	1	0	1	1
11	2	0xa7	01111111	11111111	10000000	11000001	1	1	0	1	1
12	2	0x70	10000000	11000001	10000000	11000001	0	1	0	2	2
13	1	0x13	00000000	11000001	00000000	11000001	0	1	0	3	3
14	2	0x7b	10000000	11000001	10000000	11000001	0	1	0	2	2
15	1	0x41	10101010	11101010	10101010	11000001	0	1	0	1	1
16	2	0x5a	10000000	11000001	10000000	11000001	0	1	0	2	2
Run ID 3											
17	2	0x4d	10000000	11010101	10000000	01010101	0	1	0	4	4
18	2	0x73	10000000	11010101	10000000	01010101	0	1	0	4	4
19	2	0x9f	01111111	01111011	10000000	01010101	1	0	1	0	1
20	2	0x4f	10000000	11010101	10000000	01010101	0	1	0	4	4
21	1	0x15	00000000	01010100	00000000	01010101	0	1	0	3	3
22	2	0x57	10000000	11010101	10000000	01010101	0	1	0	4	4
23	2	0x25	10000000	11000101	10000000	01010101	0	1	0	3	3
24	1	0x51	00000000	01010101	00000000	01010101	0	1	0	4	4
25	2	0x08	10000000	11010101	10000000	01010101	0	1	0	4	4
26	1	0x06	01010000	01010101	01101010	01010101	0	1	0	2	2
27	2	0x0c	10000000	11010101	10000000	01010101	0	1	0	4	4
28	1	0x03	00101101	01111101	00001010	01010101	0	1	0	2	2
29	2	0x19	10000000	11010101	10000000	01010101	0	1	0	4	4
Run ID 4											
none observed											
Run ID 5											
30	2	0x5a	10000000	10111111	10000000	11111111	0	1	0	6	6
31	2	0x8c	01111111	11111111	10000000	11111111	1	1	0	1	1
32	2	0xb1	01111111	11111111	10000000	11111111	1	1	0	1	1
33	2	0x69	10000000	11111111	10000000	11111111	0	1	0	7	7
34	2	0x0a	10000000	11111111	10000000	11111111	0	1	0	7	7
35	2	0x92	01111111	11111111	10000000	11111111	1	1	0	1	1
Run ID 6											
36	2	0xfd	01111111	11111111	10000000	11111111	1	1	0	1	1
37	2	0x6d	10000000	11111111	10000000	11111111	0	1	0	7	7
38	2	0x45	10000000	11111111	10000000	11111111	0	1	0	7	7
39	2	0x94	01111111	11111111	10000000	11111111	1	1	0	1	1
40	2	0x4a	10000000	11111111	10000000	11111111	0	1	0	7	7
41	2	0x86	01111111	11111111	10000000	11111111	1	1	0	1	1
42	2	0xc5	01111111	11111111	10000000	11111111	1	1	0	1	1
43	2	0xba	01111111	01111011	10000000	11111111	1	0	1	0	1
44	1	0x50	00000001	11111111	00000010	11111111	0	1	0	7	7
45	1	0x53	00000000	11111100	00000000	11111111	0	1	0	6	6

Table 13: CBC3.1 bit-flips in I^2C registers continued. Columns I and II show if the bit-flips are consistent with the default value or the last written value. 1 = consistent, 0 = inconsistent.

Evt.	Page	Addr.	Written	Read	Default	Last written	I	II	1→0	0→1	# bfs
					Run ID 7						
46	2	0xb6	01111111	11111111	10000000	11111111	1	1	0	1	1
47	2	0xe0	01111111	01011111	10000000	11111111	1	0	1	0	1
48	2	0x0b	10000000	11111111	10000000	11111111	0	1	0	7	7
					Run ID 8						
49	2	0x30	10000000	11111111	10000000	11111111	0	1	0	7	7
50	2	0xf9	01111111	11111111	10000000	11111111	1	1	0	1	1
51	1	0x0e	11110011	11111111	00000000	11111111	0	1	0	2	2
52	2	0xfb	01111111	01111011	10000000	11111111	1	0	1	0	1
53	1	0x04	01010000	11111111	00101110	11111111	0	1	0	6	6
					Run ID 9						
54	2	0xa9	01111111	01101111	10000000	00000000	1	1	1	0	1
55	2	0x15	10000000	11111111	10000000	11111111	0	1	0	7	7
56	2	0x01	10000000	11111111	10000000	11111111	0	1	0	7	7
57	2	0x55	10000000	11111111	10000000	11111111	0	1	0	7	7
58	1	0x0c	00010000	00000000	00010000	11111111	0	0	1	0	1
					Run ID 10						
59	2	0xe0	01111111	11111111	10000000	11111111	1	1	0	1	1
60	1	0x41	10101010	11111111	10101010	11111111	0	1	0	4	4
					Run ID 11						
61	2	0x23	10000000	10000001	10000000	01000001	0	1	0	1	1
62	2	0x24	10000000	11000001	10000000	01000001	0	1	0	2	2
					Run ID 12						
					none observed						
					Run ID 13						
63	2	0x80	01111111	11111111	10000000	11111111	1	1	0	1	1
64	2	0x63	10000000	11111111	10000000	11111111	0	1	0	7	7
65	1	0x04	01010000	11111111	00101110	11111111	0	1	0	6	6
66	2	0x9c	01111111	11111111	10000000	11111111	1	1	0	1	1
67	2	0x94	01111111	11111111	10000000	11111111	1	1	0	1	1
68	2	0xd2	01111111	11111111	10000000	11111111	1	1	0	1	1
69	2	0x50	10000000	11111111	10000000	11111111	0	1	0	7	7
70	2	0x37	10000000	11111111	10000000	11111111	0	1	0	7	7
71	1	0x0c	00000000	11111111	00010000	11111111	0	1	0	8	8
72	1	0x0c	11111111	00000000	00010000	00000000	0	1	8	0	8
73	2	0xec	01111111	00111111	10000000	00000000	1	1	1	0	1
74	2	0xed	01111111	11111111	10000000	11111111	1	1	0	1	1
75	2	0xe7	01111111	11111111	10000000	11111111	1	1	0	1	1
76	1	0x51	00000000	11111111	00000000	11111111	0	1	0	8	8
77	2	0xdd	01111111	11111111	10000000	11111111	1	1	0	1	1
78	2	0xf0	01111111	11111111	10000000	11111111	1	1	0	1	1
79	1	0x46	11111111	11110111	11111111	11111111	0	0	1	0	1
80	2	0xa2	01111111	11111111	10000000	11111111	1	1	0	1	1
81	2	0xe2	01111111	11111111	10000000	11111111	1	1	0	1	1

Table 14: Summary of CBC3.1 bit-flips in I^2C registers for chip 1.

Evt	Page	Addr	Written	Read	Default	Last written	I	II	$1 \rightarrow 0$	$0 \rightarrow 1$	# bitflips
1	2	0x7e	10000000	11000001	10000000	11000001	0	1	0	2	2
2	2	0xac	01111111	00111111	10000000	11000001	1	0	1	0	1
6	2	0xdf	01111111	11111111	10000000	11000001	1	1	0	1	1
9	1	0x1c	10000100	10000101	00000000	11000001	0	1	0	1	1
11	2	0xa7	01111111	11111111	10000000	11000001	1	1	0	1	1
13	1	0x13	00000000	11000001	00000000	11000001	0	1	0	3	3
15	1	0x41	10101010	11101010	10101010	11000001	0	1	0	1	1
17	2	0x4d	10000000	11010101	10000000	01010101	0	1	0	4	4
20	2	0x4f	10000000	11010101	10000000	01010101	0	1	0	4	4
22	2	0x57	10000000	11010101	10000000	01010101	0	1	0	4	4
23	2	0x25	10000000	11000101	10000000	01010101	0	1	0	3	3
26	1	0x06	01010000	01010101	01101010	01010101	0	1	0	2	2
28	1	0x03	00101101	01111101	00001010	01010101	0	1	0	2	2
30	2	0x5a	10000000	10111111	10000000	11111111	0	1	0	6	6
33	2	0x69	10000000	11111111	10000000	11111111	0	1	0	7	7
35	2	0x92	01111111	11111111	10000000	11111111	1	1	0	1	1
37	2	0x6d	10000000	11111111	10000000	11111111	0	1	0	7	7
43	2	0xba	01111111	01111011	10000000	11111111	1	0	1	0	1
48	2	0x0b	10000000	11111111	10000000	11111111	0	1	0	7	7
51	1	0x0e	11110011	11111111	00000000	11111111	0	1	0	2	2
52	2	0xfb	01111111	01111011	10000000	11111111	1	0	1	0	1
56	2	0x01	10000000	11111111	10000000	11111111	0	1	0	7	7
58	1	0x0c	00010000	00000000	00010000	11111111	0	0	1	0	1
59	2	0xe0	01111111	11111111	10000000	11111111	1	1	0	1	1
60	1	0x41	10101010	11111111	10101010	11111111	0	1	0	4	4
65	1	0x04	01010000	11111111	00101110	11111111	0	1	0	6	6
66	2	0x9c	01111111	11111111	10000000	11111111	1	1	0	1	1
68	2	0xd2	01111111	11111111	10000000	11111111	1	1	0	1	1
69	2	0x50	10000000	11111111	10000000	11111111	0	1	0	7	7
71	1	0x0c	00000000	11111111	00010000	11111111	0	1	0	8	8
72	1	0x0c	11111111	00000000	00010000	00000000	0	1	8	0	8
75	2	0xe7	01111111	11111111	10000000	11111111	1	1	0	1	1
76	1	0x51	00000000	11111111	00000000	11111111	0	1	0	8	8
80	2	0xa2	01111111	11111111	10000000	11111111	1	1	0	1	1

Table 15: Summary of CBC3.1 bit-flips in I^2C registers for chip 2.

Evt	Page	Addr	Written	Read	Default	Last written	I	II	$1 \rightarrow 0$	$0 \rightarrow 1$	# bitflips
3	1	0x4d	01100110	11100111	01100110	11000001	0	1	0	2	2
5	1	0x3c	11111111	01111111	11111111	11000001	0	0	1	0	1
8	2	0x27	10000000	11000001	10000000	11000001	0	1	0	2	2
16	2	0x5a	10000000	11000001	10000000	11000001	0	1	0	2	2
19	2	0x9f	01111111	01111011	10000000	01010101	1	0	1	0	1
29	2	0x19	10000000	11010101	10000000	01010101	0	1	0	4	4
36	2	0xfd	01111111	11111111	10000000	11111111	1	1	0	1	1
38	2	0x45	10000000	11111111	10000000	11111111	0	1	0	7	7
39	2	0x94	01111111	11111111	10000000	11111111	1	1	0	1	1
40	2	0x4a	10000000	11111111	10000000	11111111	0	1	0	7	7
41	2	0x86	01111111	11111111	10000000	11111111	1	1	0	1	1
46	2	0xb6	01111111	11111111	10000000	11111111	1	1	0	1	1
49	2	0x30	10000000	11111111	10000000	11111111	0	1	0	7	7
54	2	0xa9	01111111	01101111	10000000	00000000	1	1	1	0	1
55	2	0x15	10000000	11111111	10000000	11111111	0	1	0	7	7
61	2	0x23	10000000	10000001	10000000	01000001	0	1	0	1	1
62	2	0x24	10000000	11000001	10000000	01000001	0	1	0	2	2
63	2	0x80	01111111	11111111	10000000	11111111	1	1	0	1	1
64	2	0x63	10000000	11111111	10000000	11111111	0	1	0	7	7
73	2	0xec	01111111	00111111	10000000	00000000	1	1	1	0	1
77	2	0xdd	01111111	11111111	10000000	11111111	1	1	0	1	1
78	2	0xf0	01111111	11111111	10000000	11111111	1	1	0	1	1
81	2	0xe2	01111111	11111111	10000000	11111111	1	1	0	1	1

Table 16: Summary of CBC3.1 bit-flips in I^2C registers for chip 4.

Evt	Page	Addr	Written	Read	Default	Last written	I	II	$1 \rightarrow 0$	$0 \rightarrow 1$	# bitflips
4	2	0xfe	01111111	11111111	10000000	11000001	1	1	0	1	1
7	1	0x3d	11111111	10111111	11111111	11000001	0	0	1	0	1
10	2	0xfb	01111111	11111111	10000000	11000001	1	1	0	1	1
12	2	0x70	10000000	11000001	10000000	11000001	0	1	0	2	2
14	2	0x7b	10000000	11000001	10000000	11000001	0	1	0	2	2
18	2	0x73	10000000	11010101	10000000	01010101	0	1	0	4	4
21	1	0x15	00000000	01010100	00000000	01010101	0	1	0	3	3
24	1	0x51	00000000	01010101	00000000	01010101	0	1	0	4	4
25	2	0x08	10000000	11010101	10000000	01010101	0	1	0	4	4
27	2	0x0c	10000000	11010101	10000000	01010101	0	1	0	4	4
31	2	0x8c	01111111	11111111	10000000	11111111	1	1	0	1	1
32	2	0xb1	01111111	11111111	10000000	11111111	1	1	0	1	1
34	2	0x0a	10000000	11111111	10000000	11111111	0	1	0	7	7
42	2	0xc5	01111111	11111111	10000000	11111111	1	1	0	1	1
44	1	0x50	00000001	11111111	00000010	11111111	0	1	0	7	7
45	1	0x53	00000000	11111100	00000000	11111111	0	1	0	6	6
47	2	0xe0	01111111	01011111	10000000	11111111	1	0	1	0	1
50	2	0xf9	01111111	11111111	10000000	11111111	1	1	0	1	1
53	1	0x04	01010000	11111111	00101110	11111111	0	1	0	6	6
57	2	0x55	10000000	11111111	10000000	11111111	0	1	0	7	7
67	2	0x94	01111111	11111111	10000000	11111111	1	1	0	1	1
70	2	0x37	10000000	11111111	10000000	11111111	0	1	0	7	7
74	2	0xed	01111111	11111111	10000000	11111111	1	1	0	1	1
79	1	0x46	11111111	11110111	11111111	11111111	0	0	1	0	1