

Tests with the CMS Binary Chip (CBC)

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Tests with the CMS Binary Chip (CBC)

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ABSTRACT: The CMS Binary Chip is an ASIC designed for the readout of silicon strip sensors. Tests have been performed to verify that it operates correctly over a range of temperatures from -40°C – 40°C . The results of these tests are presented.

KEYWORDS: Front-end electronics for detector readout; Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons); Particle tracking detectors (Solid-state detectors)

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1 Introduction

The silicon strip tracker at the CMS experiment [1] uses the APV [2], a multiplexing readout chip with an analogue storage pipeline. Plans for an upgraded “High Luminosity LHC” (HL-LHC) [3] mean that development of a new readout ASIC is required. A first prototype of this chip, the CMS Binary Chip (CBC) has been produced. This article describes initial tests of the CBC over its full operating temperature range.

Operation at HL-LHC implies a greatly increased flux of particles through the tracking detectors with respect to the LHC. In order to keep the occupancy on each readout channel low enough for effective track reconstruction the granularity of the detector and hence the number of readout channels will have to be increased. However the amount of material, especially high-Z material, must be kept constant or preferably be reduced. This implies that the tracker power consumption must stay constant or reduce, since the cables needed to supply power and the cooling pipes needed to remove the resulting heat are a significant component of the tracker dead-material. Reducing the power consumption per channel implies moving to a smaller feature size IC technology than the 250nm used for the APV. It is anticipated that the eventual design for the CBC will include circuitry to generate information for the trigger system. However, the first version does not include any trigger functionality.

To reduce the effects of radiation damage a CMS tracker for HL-LHC is likely to be run at a lower temperature than the current tracker. Hence the performance of the CBC needs to be characterized over a wide temperature range.

1.1 CMS Binary Chip (CBC)

The CBC is described elsewhere [4], so only brief details are given here. The CBC is manufactured in a 130nm IBM CMOS process. The APV has an analogue storage pipeline and readout. However the move to digital rather than analogue fibre optic links means that this approach is not possible for the CBC and a binary, non-sparsified readout has been chosen instead. This is similar to the approach taken by the VFAT [5] readout ASIC.

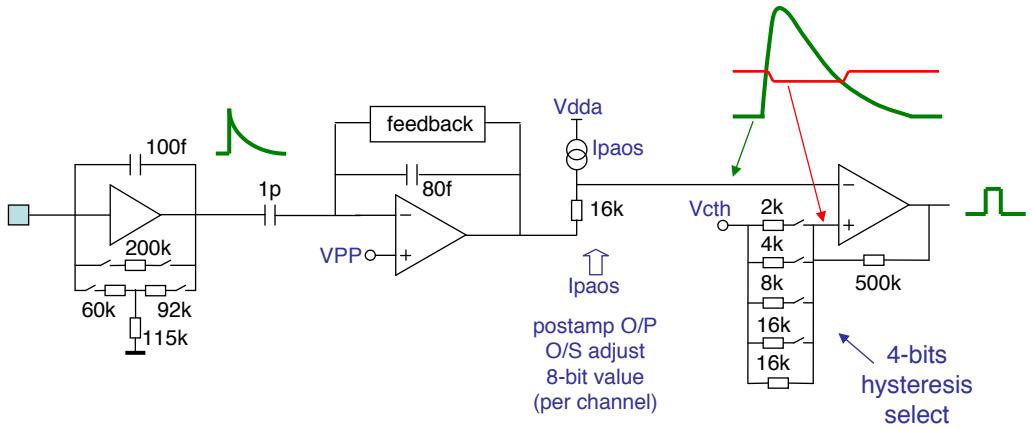


Figure 1. Block diagram of CBC front-end.

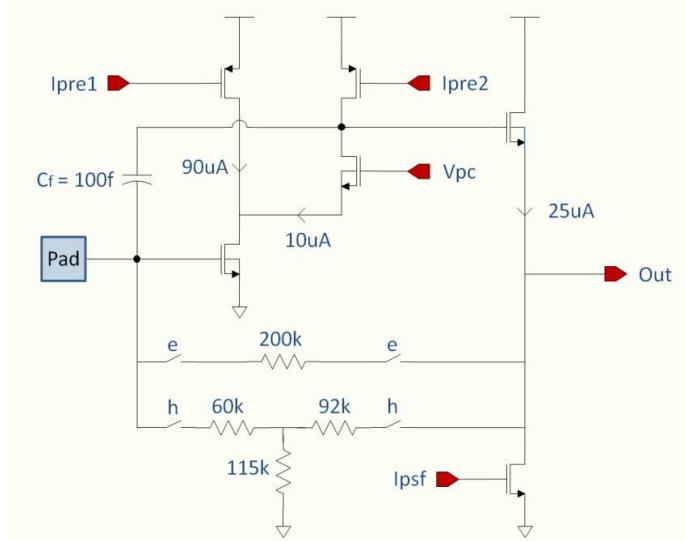


Figure 2. Outline of CBC pre-amplifier.

The analogue front-end of each channel is illustrated in figure 1 (taken from [6]). The front end has a fast impulse response function (approximately 20 ns peaking time) to cope with high occupancy and to reduce the time-walk generated in the fixed threshold discriminator. It can tolerate a leakage current of up to $1\mu\text{A}$ and so it can be DC coupled to the sensor. The front end can be switched between sensor polarities. Figure 2 shows an outline of the pre-amplifier (taken from [4]).

The supply voltage of the CBC is approximately 1.2 V, which precludes the use of LVDS, so the SLVS [7] standard is used for fast I/O signals. As with the APV, setup and control is done via an I2C interface.

2 Measurements

The CBC has a binary readout, but by repeatedly triggering and recording the fraction of hits whilst scanning the comparator threshold it is possible to build up a picture of analogue behaviour. By using an environmental chamber variation of the parameters that characterize the circuit response can be evaluated. The chamber used is capable of operation between -70°C and $+180^{\circ}\text{C}$ but for these tests a range of -40°C – $+40^{\circ}\text{C}$ was used. A voltage step of adjustable amplitude applied across a $1.5\text{ pF} \pm 10\%$ capacitor was used to inject charge into a channel. The timing of the pulse with respect to the trigger could be varied either by changing the pipeline latency inside the CBC or the pulse generator delay between the trigger signal and the pulse output. A single CBC was used to take the measurements presented here.

2.1 Measuring “turn-on” (S-Curves)

In general, plotting the fraction of hits (the fraction of triggers that return a “1” from a particular channel) as a function of the threshold voltage gives a sigmoid (an “S-Curve”). By fitting a function to the curve the mid-point of the “turn-on” can be measured and the noise estimated from the width of the turn-on. The error function (erf) or complementary error function (erfc), as appropriate, is fitted. Figure 3 shows S-curves for a range of different injected charges. Due to issues with the CBC internal threshold voltage generator an external voltage source was used. In all cases the minimum hysteresis setting was used.

2.2 Rise time

The voltage as a function of time at the output of a CBC post-amplifier can be investigated by varying the time delay between the trigger input to the pulse generator that produces the charge injection signal. At each value of the pulse delay an S-curve is taken and the mid-point of the turn-on measured. This gives a measure of the voltage at the output of the post-amplifier convoluted with the time response and voltage offset of the comparator. In essence the CBC is being used like a “sampling oscilloscope” using the S-Curve mid-point as the ADC. Figure 4 shows the S-Curve mid-point as a function of delay for a single pulse-height. Curves are shown for two different values of bias current through the front-end transistor. The curves correspond to a nominal current of $4\text{ }\mu\text{A}$ through the preamp cascode branch and current of $10\text{ }\mu\text{A}$ and $90\text{ }\mu\text{A}$ through the input branch. The 10%–90% rise time is $25 \pm 3\text{ ns}$, $28 \pm 3\text{ ns}$ for $10\text{ }\mu\text{A}$, $90\text{ }\mu\text{A}$ respectively through the preamplifier input branch.

2.3 Linearity

Figure 5 shows the S-Curve mid-point as a function of delay for a range of different pulse heights. Figure 6 shows the peak-pedestal shift in the S-Curve mid-point as a function of injected charge. The delay (in 30 ns units) was set to give maximum response. For electrons (negative pulse) at $T=273\text{ K}$ the gain was measured as 40 ± 0.5 (statistical) ± 5 (systematic) mV/fC . This indicates that when the pulse is correctly timed the relationship between pulse size and comparator threshold is sufficient for operation as a binary strip-tracker readout.

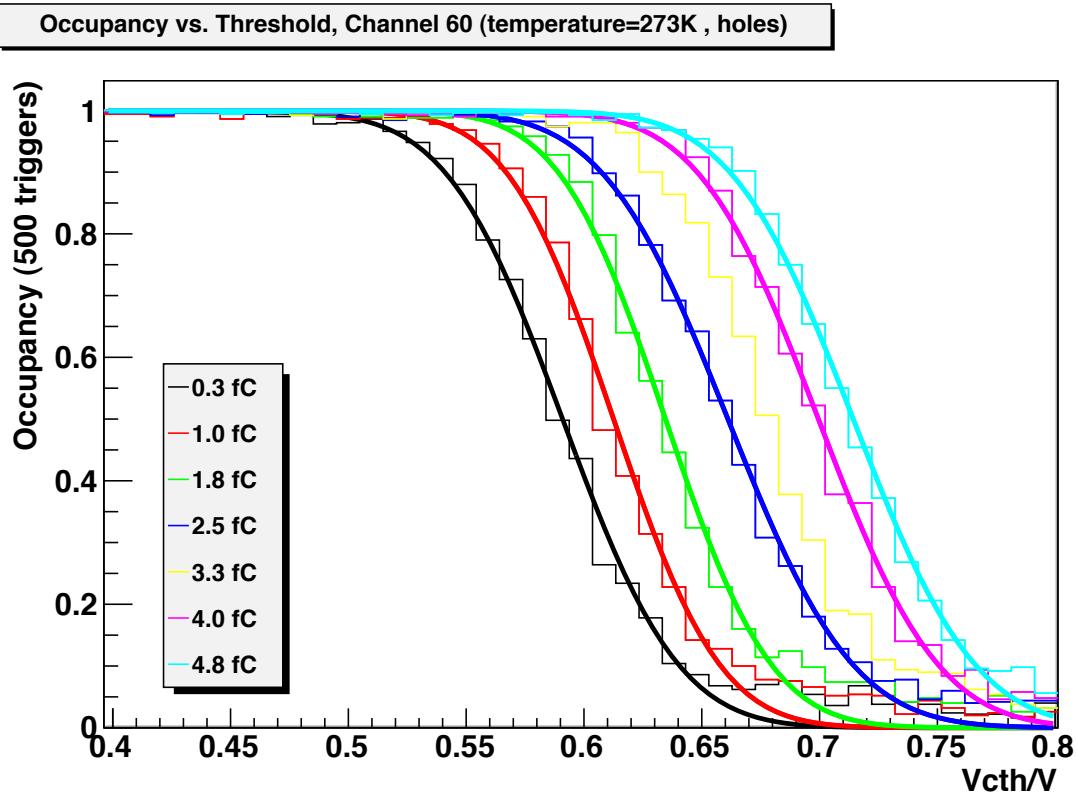


Figure 3. Occupancy as function of threshold voltage (“S-Curve”) for different pulse-heights, together with fit to complementary error function for each S-Curve.

2.4 Temperature variation of pedestal and noise

To characterize the variation with temperature of the post-amp pedestal position S-Curves were taken between -40°C – $+40^{\circ}\text{C}$.

Figure 7 shows the S-Curve mid-position and the width of the S-Curve for an unconnected input channel as a function of temperature. For this unconnected channel the width of the S-Curve, which is related to the RMS fluctuation on the post-amplifier output, is $2.9 \pm 0.2\text{mV}$ and does not change significantly with temperature. This corresponds to an equivalent noise charge of 450 ± 75 electrons. The S-Curve mid-point, for a fixed set of I2C configuration values, changes by $1.4\text{mV}/K$ over the temperature range -40°C – $+40^{\circ}\text{C}$. This is consistent with simulation results [8].

3 Conclusion

Basic CBC functionality was tested over the temperature range needed for a CMS tracker at the HL-LHC. No adverse changes in performance were observed. However, the operating point changes slightly with temperature. Further work to characterize the variation with temperature is needed, including taking measurements from a sample of devices, rather than the single device characterized here.

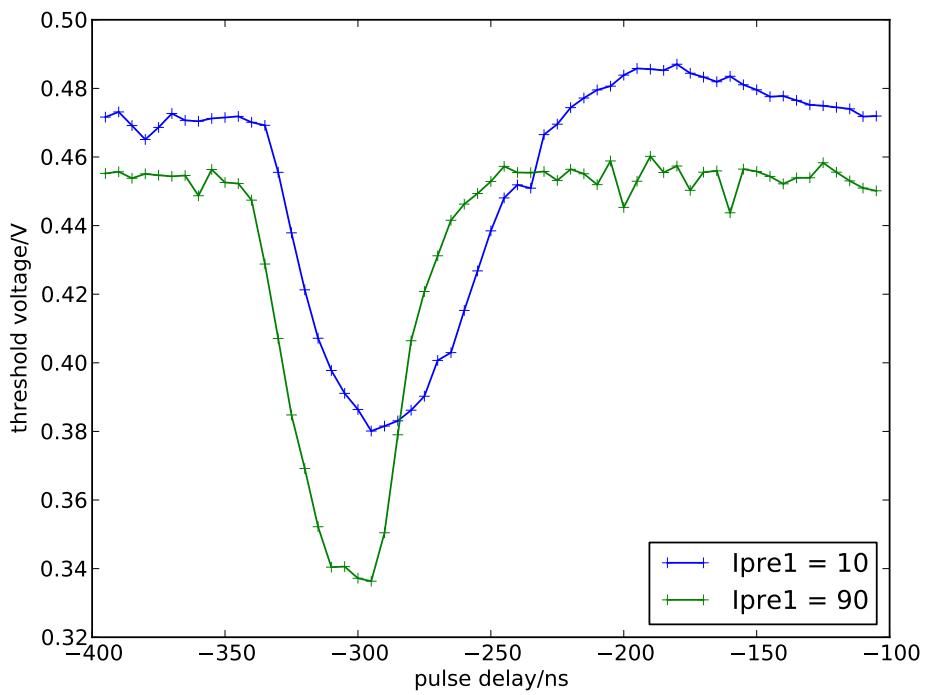


Figure 4. S-Curve mid-point as a function of delay for two different input transistor bias currents, 5ns steps.

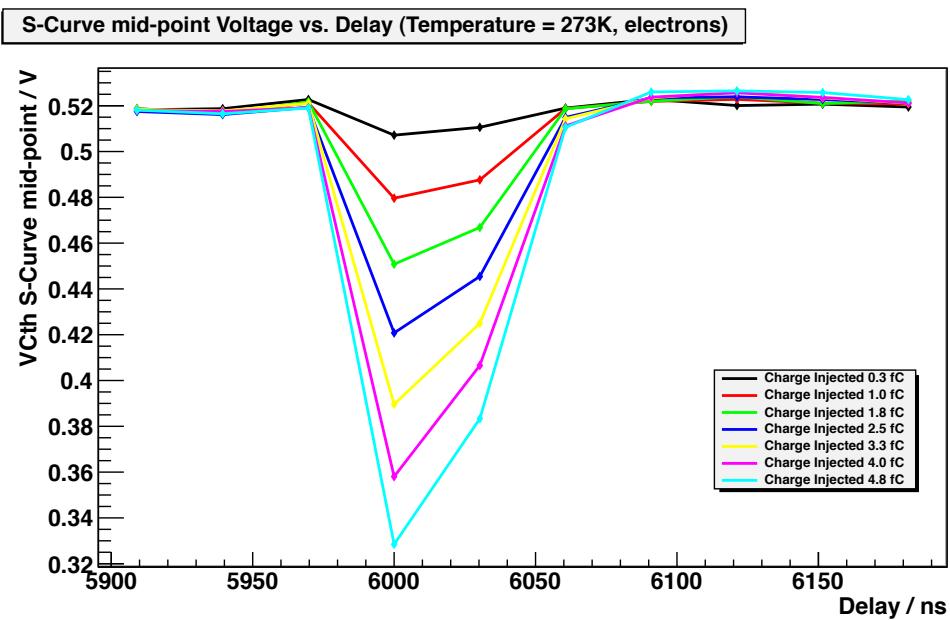


Figure 5. S-Curve mid-point as a function of delay for different pulse-heights.

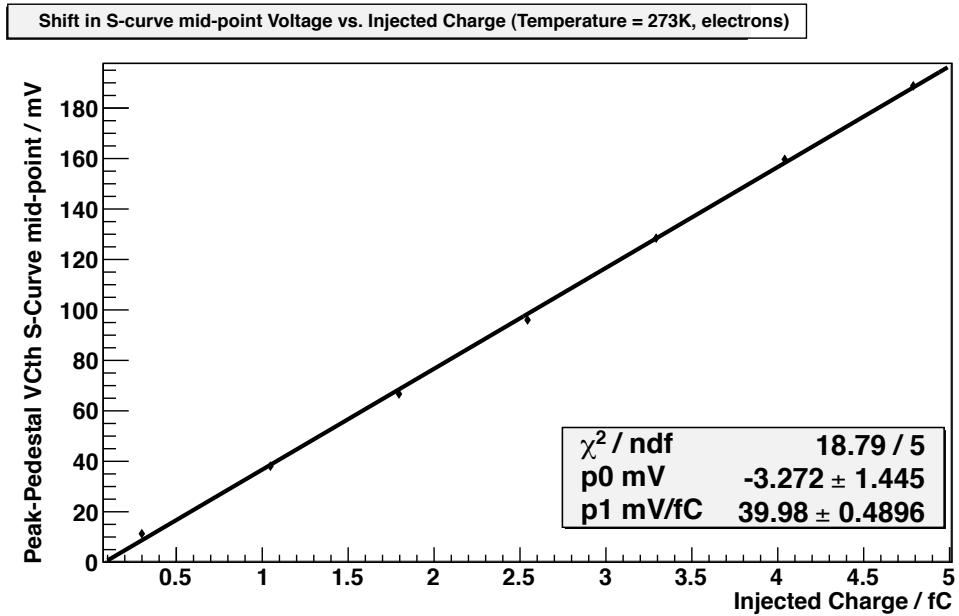


Figure 6. Shift in S-Curve mid-point for different pulse-heights.

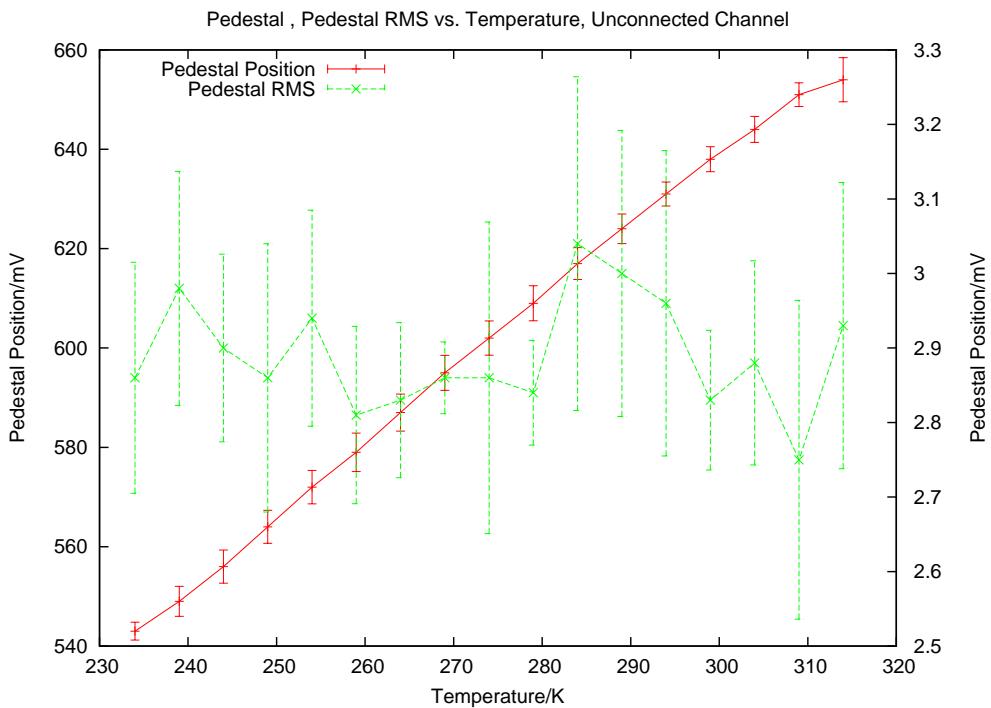


Figure 7. Shift in S-Curve mid-point and width with temperature.

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