Electronics for 2S-Pt modules: CBC2

D.Braga, M.Prydderch (STFC RAL)

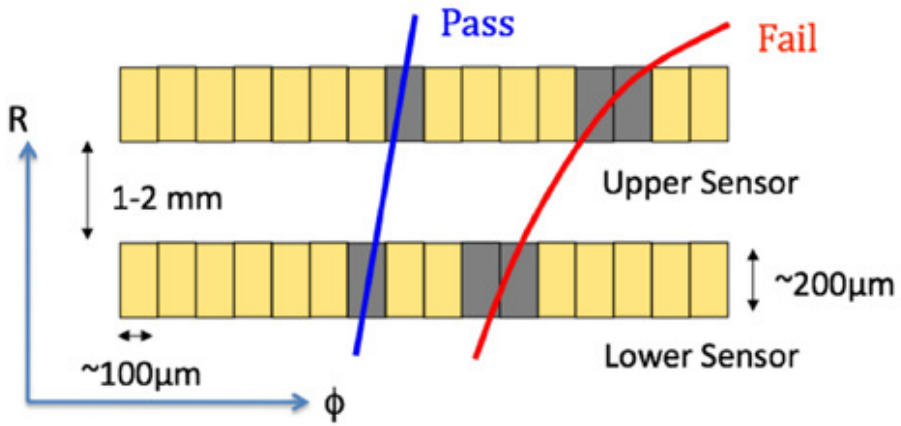
G.Hall, M.Pesaresi, M.Raymond (IC)

Tracker Week Phase II Electronics Meeting, 26 April 2012

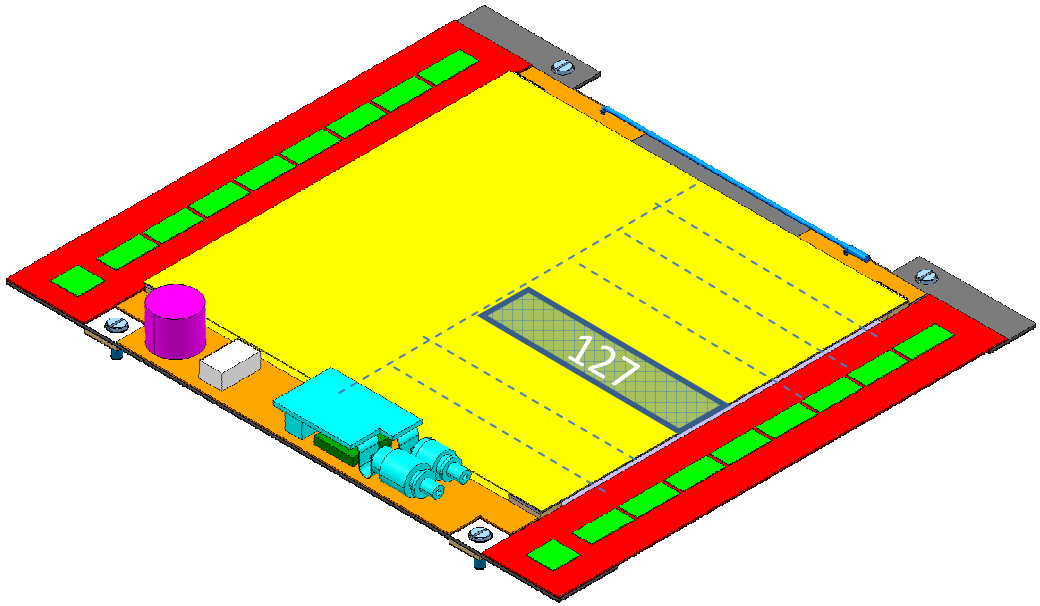
Imperial College London

Science & Technology Facilities Council

P_T Discrimination



CBC2 to correlate hits in two closely separated sensors to discriminate between high and low P_T tracks

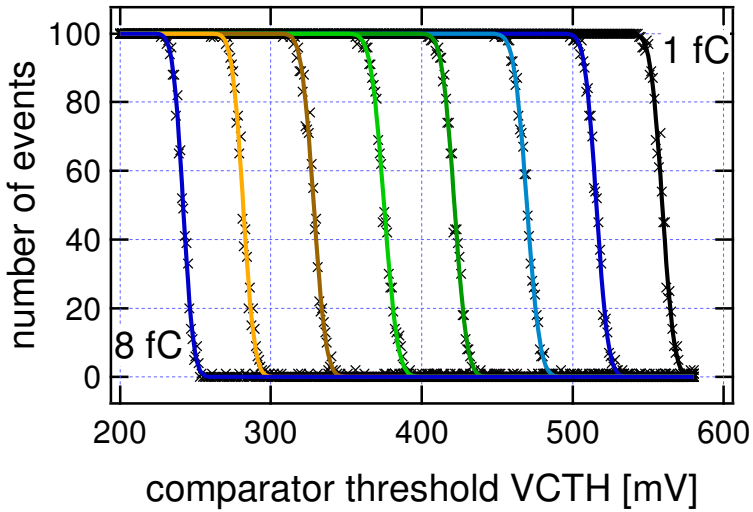


2S (Strips-Strips) module:

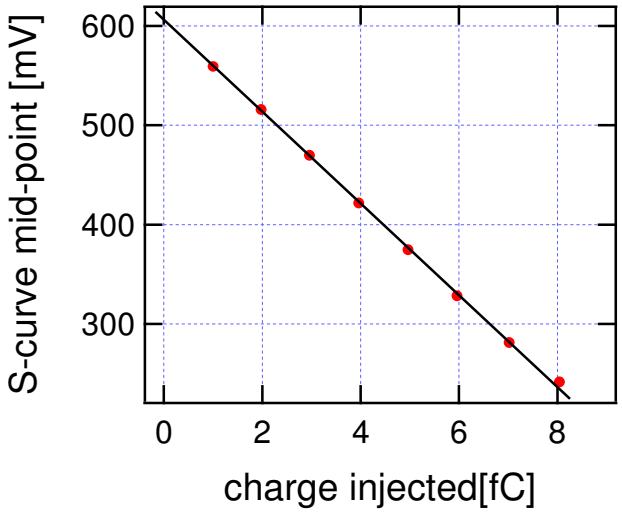
- 16 readout ASICs
- each reading 127 strips from bottom sensor and 127 from top s.

CBC Test Results

s- curves for range 1 - 8 fC : 1 fC steps



gain



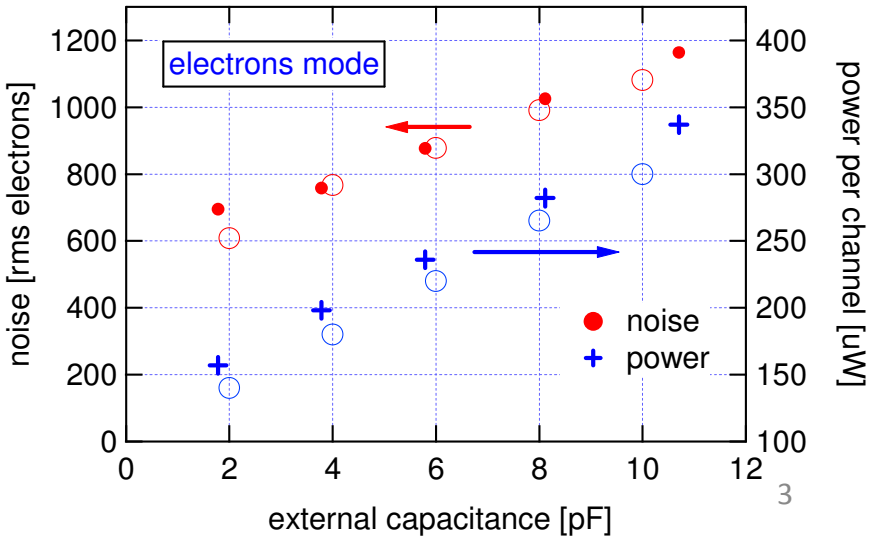
e.g. for 5pF input capacitance:

noise: ~ 800 e_{RMS}

total power: < 300 µW/channel

CBC2 coincidence logic estimated consumption: ~50uW/channel

Noise and power



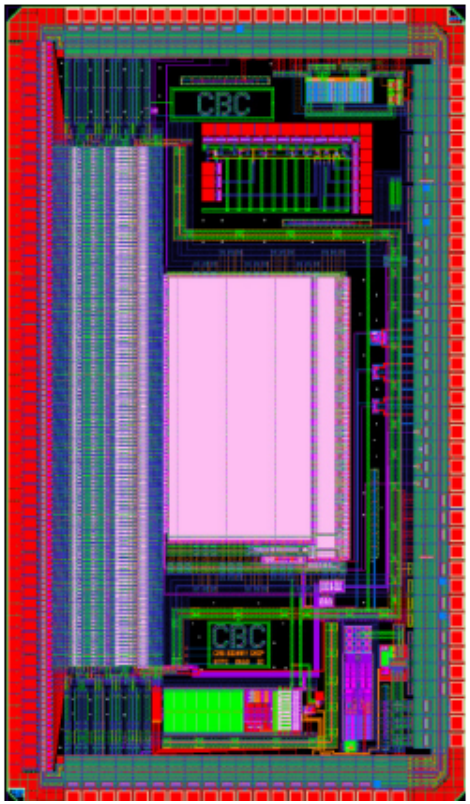
CBC(1) -> CBC2

Features kept:

- **L1 triggered readout**
- **Powering features (DC-DC and LDO)**

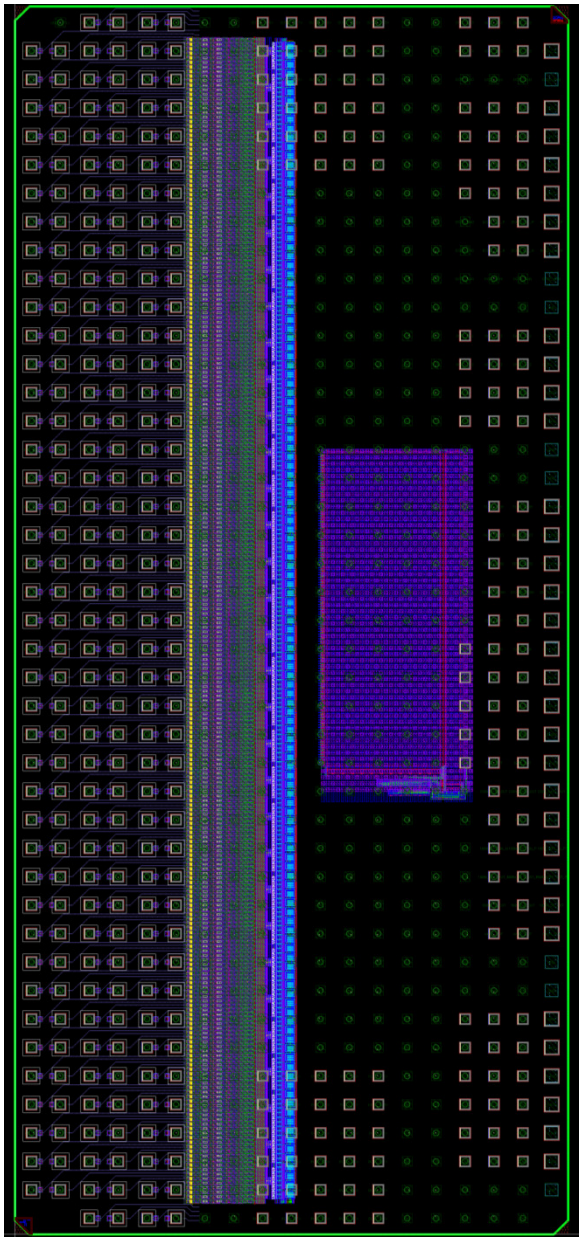
New features:

- **250um C4 bump-bonding**
- **254 channels (not 256): allows correlation between 127 strips on top and bottom sensors (one spare binary code)**
- **Internal test pulse**
  programmable amplitude and delay
- **Trigger output if correlation between clusters**
  programmable window and offset



CBC
128 channels
wirebond: 50 um pitch
7mm x 4mm

CBC2
254 channels
C4 bump-bond: 250 um pitch
10.75mm x 4.75mm



Top Level status

Analog channels completed

Coincidence logic completed, now working on readout

Pipeline memory completed

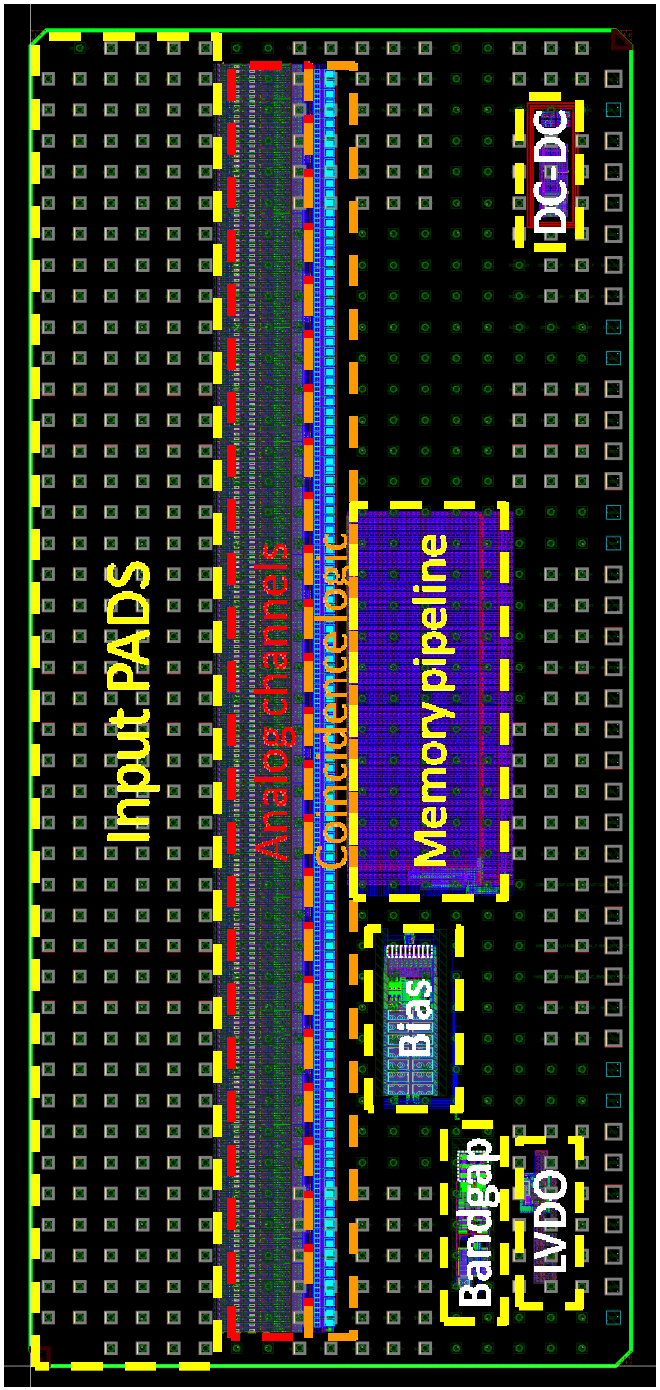
Bandgap reference as in CBC1

DCDC converter supplied by CERN, almost ready

Low Voltage Dropout Regulator as in CBC1

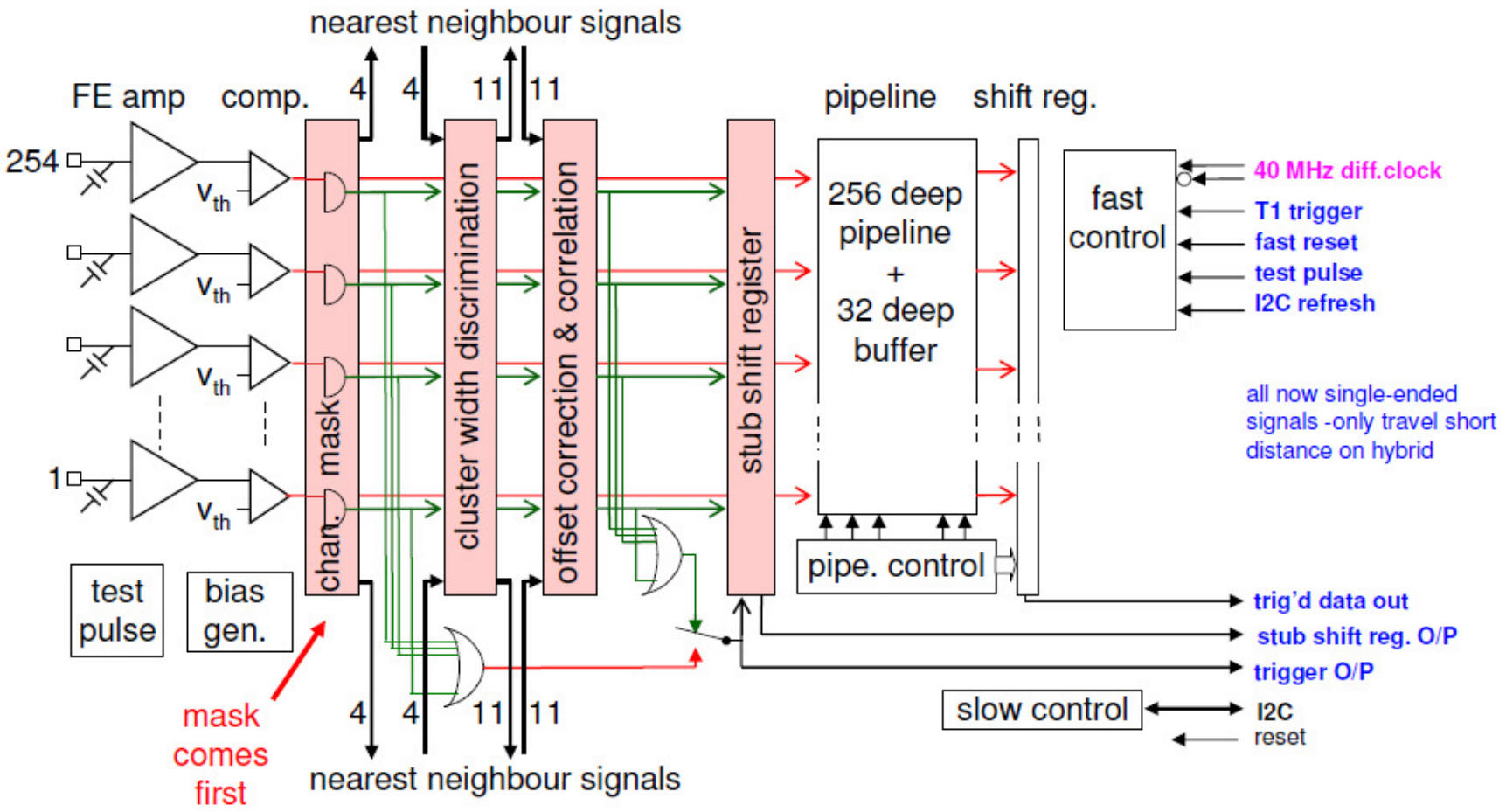
Bias, Test Pulse circuit, Readout, top level integration

not completed



CBC2 architecture

(M.Raymond: 2S-Pt module systems meeting, CERN, 22nd March, 2012)



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)
cluster width discrimination: exclude wide clusters
offset correction and correlation: correct for phi offset across module and correlate between layers
stub shift register: test feature - shift out result of correlation operation at 40 MHz
fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip
for normal operation choose correlation O/P

neighbour chip signals - CWD O/Ps

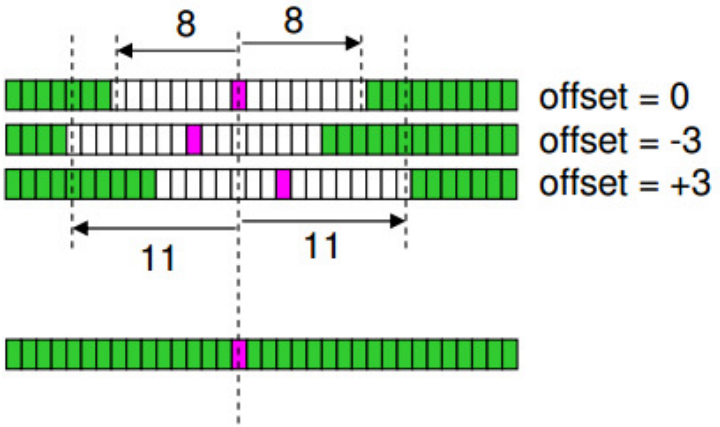
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

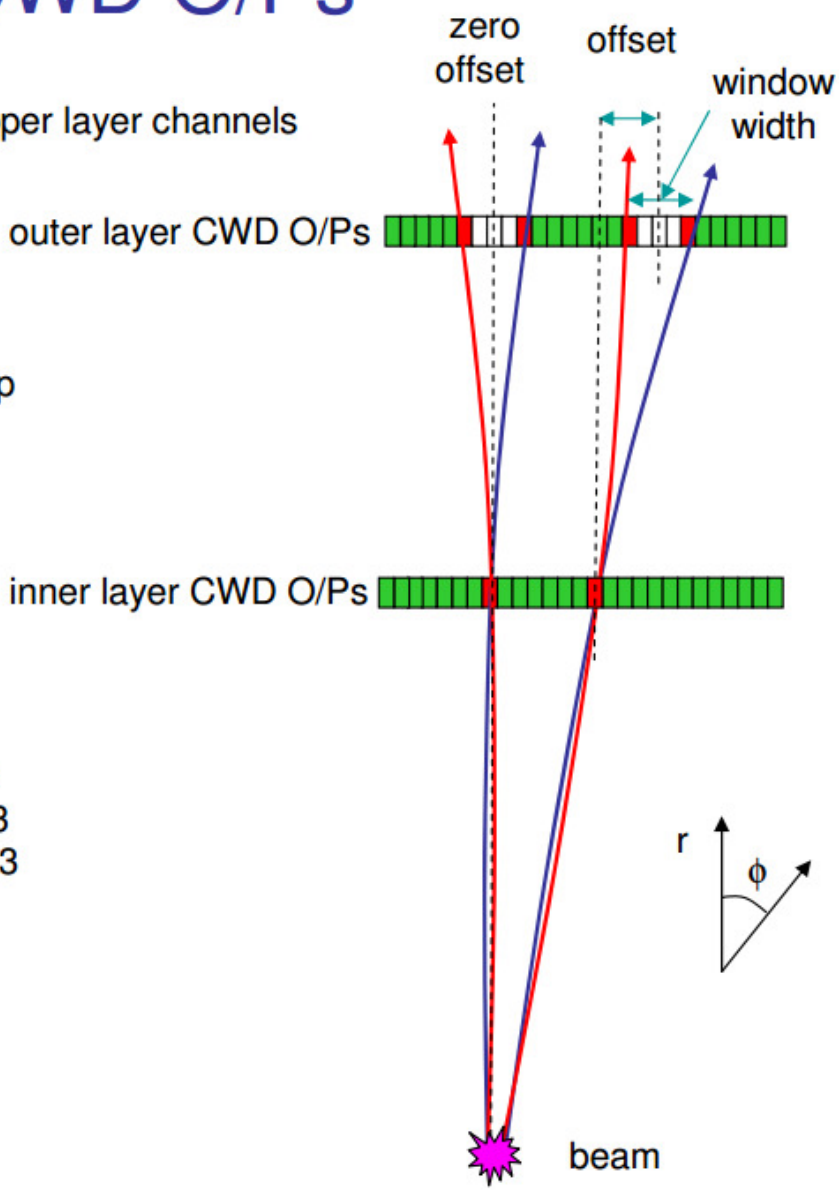
window defines Pt cut
width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
11 to receive from neighbouring chip

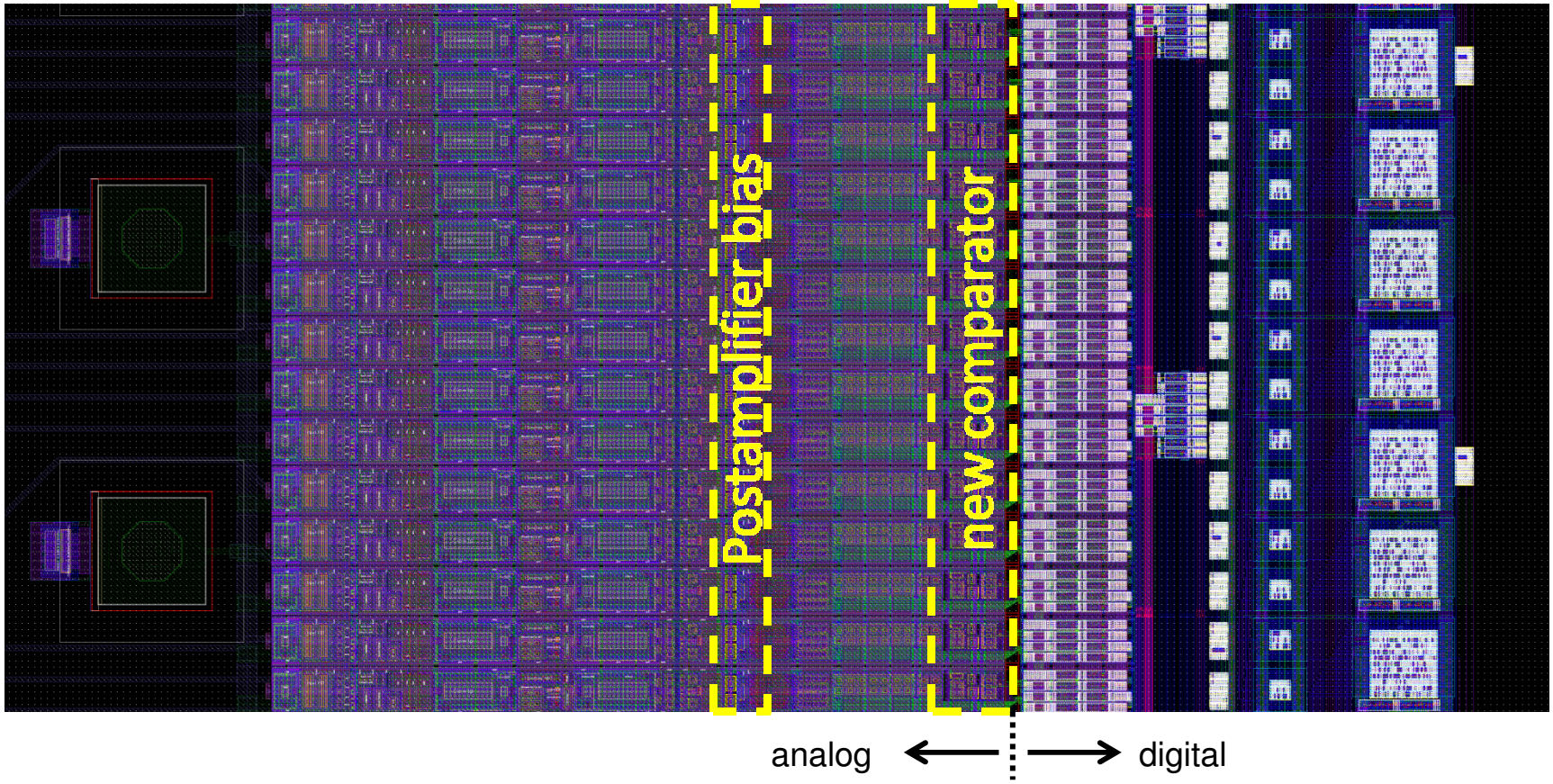
= 22 signals





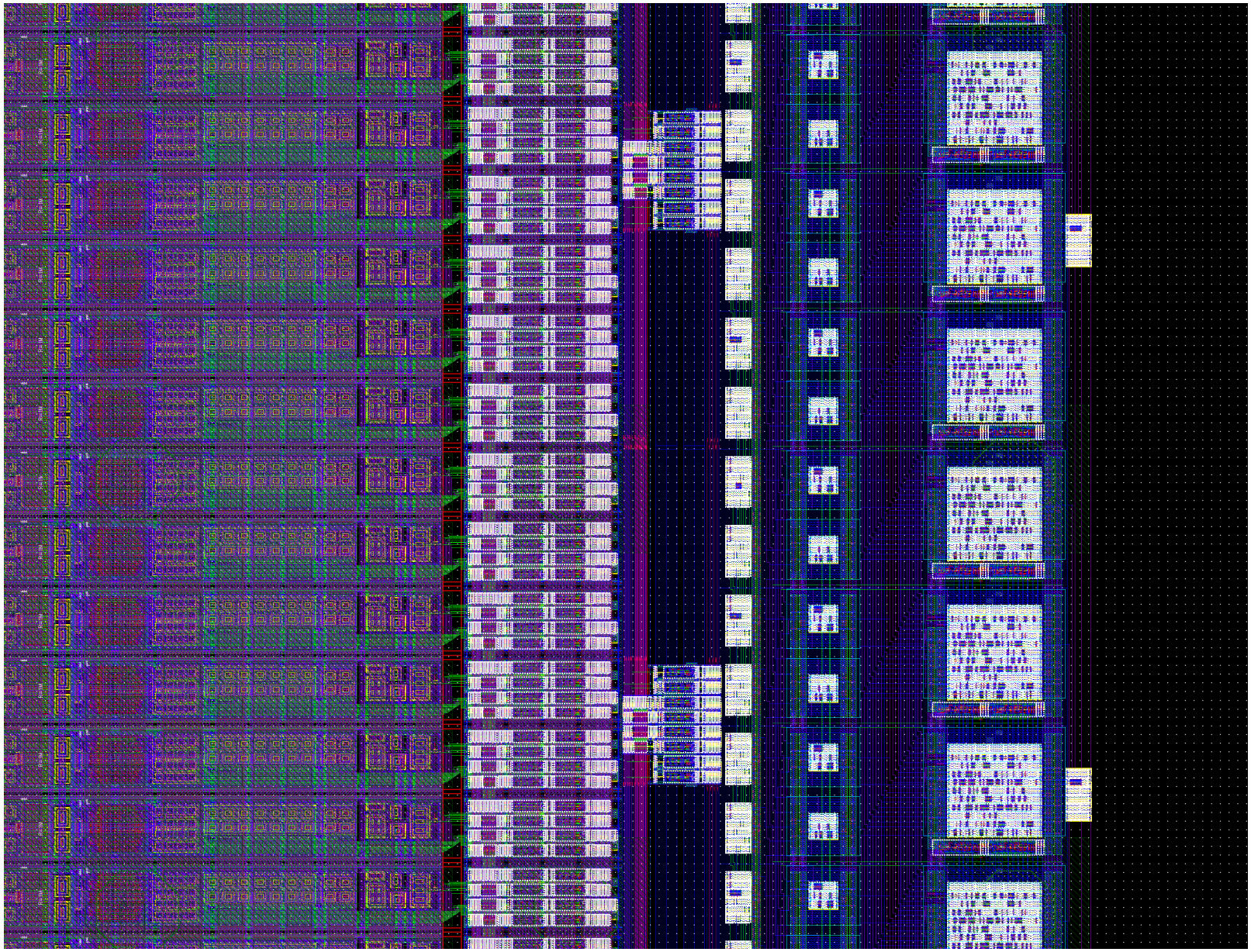
adding comp O/Ps -> 30 signals altogether, top and bottom of chip

Channel layout

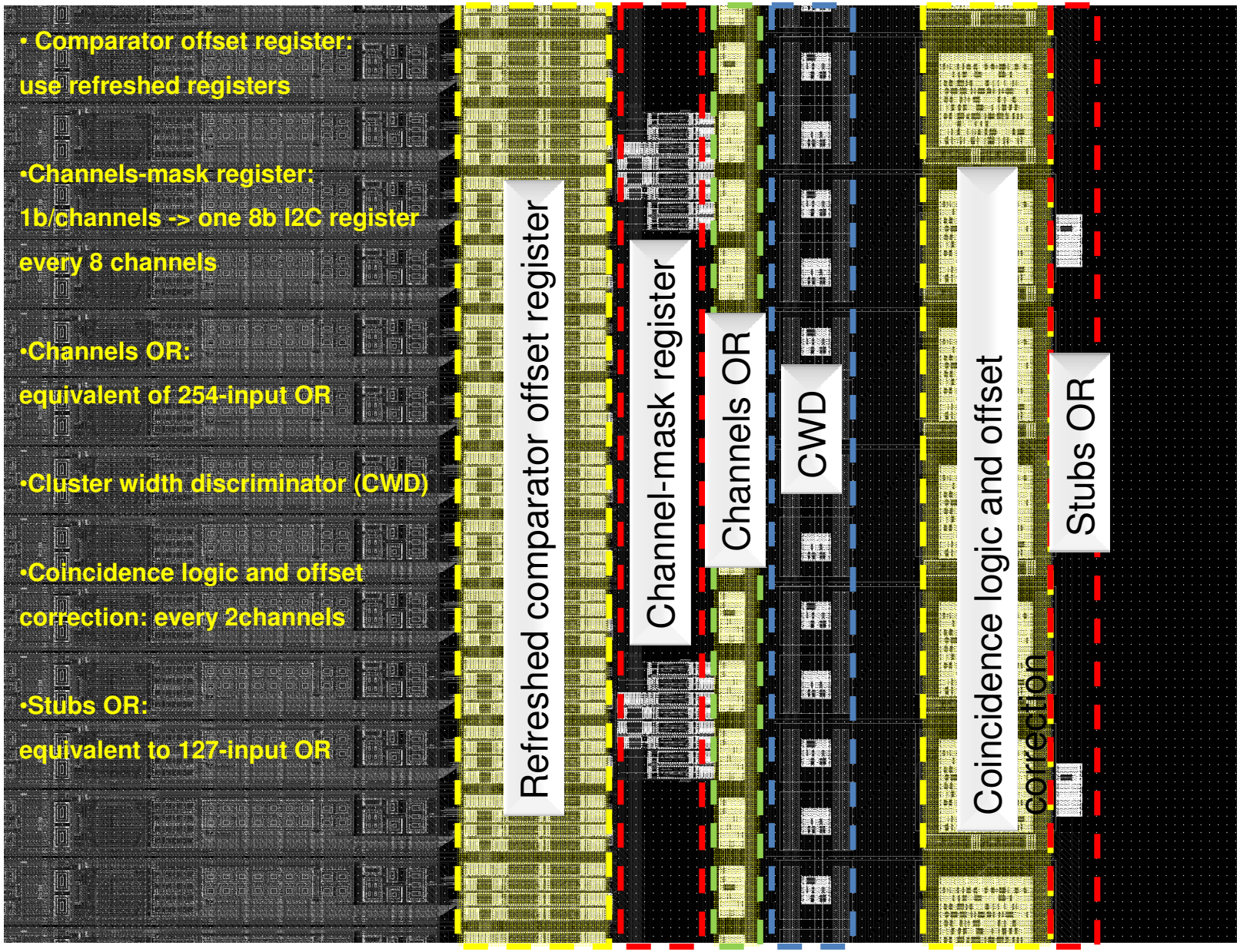


- **Power distribution optimized (made use of wider pitch)**
- **Postamplifier feedback network bias: local buffer to avoid effect of CM shift (additional ~5uW/channel)**
- **Comparator: internal hysteresis to solve drive issue of previous resistive network**

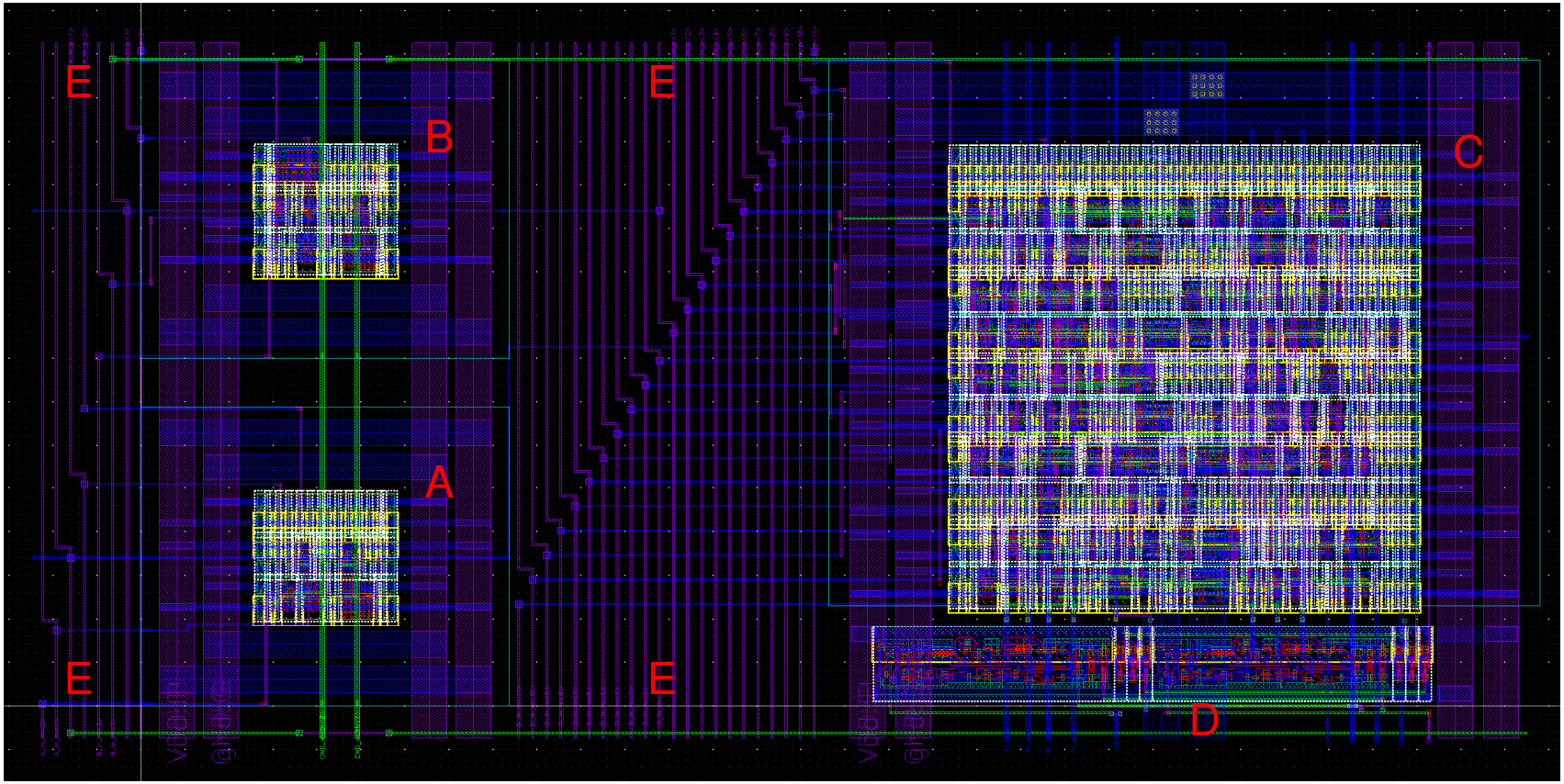
Digital part - Detail



Digital part - Detail



Coincidence logic - Detail



A: Cluster width discrimination for bottom sensor hits

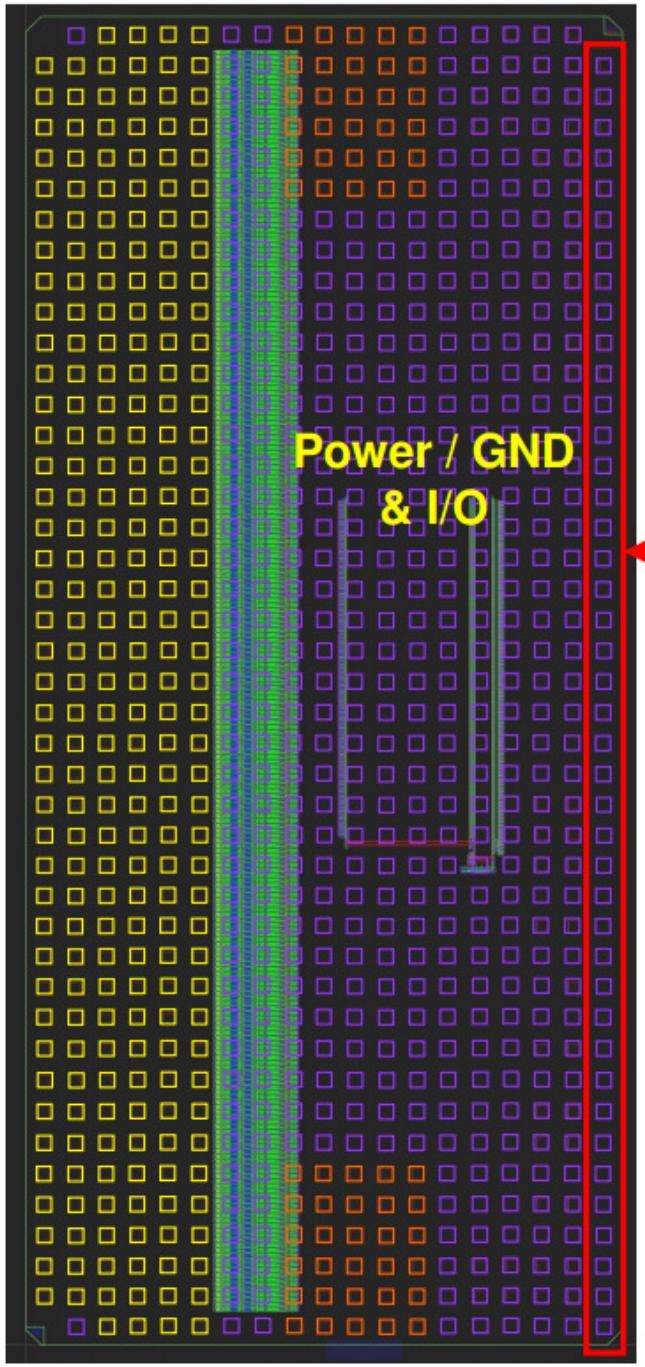
B: Cluster width discrimination for top sensor hits

C: Coincidence logic (with programmable window and offset correction)

D: Shift register for stubs readout and shadow SR for readout control

E: lines to/from previous/next channels (propagate for ~1mm (11*80um))

PAD scheme



43 rows x 19 cols = ~ 800 bumps

10.75 x 4.75 mm²

inputs

outputs to / inputs from neighbours

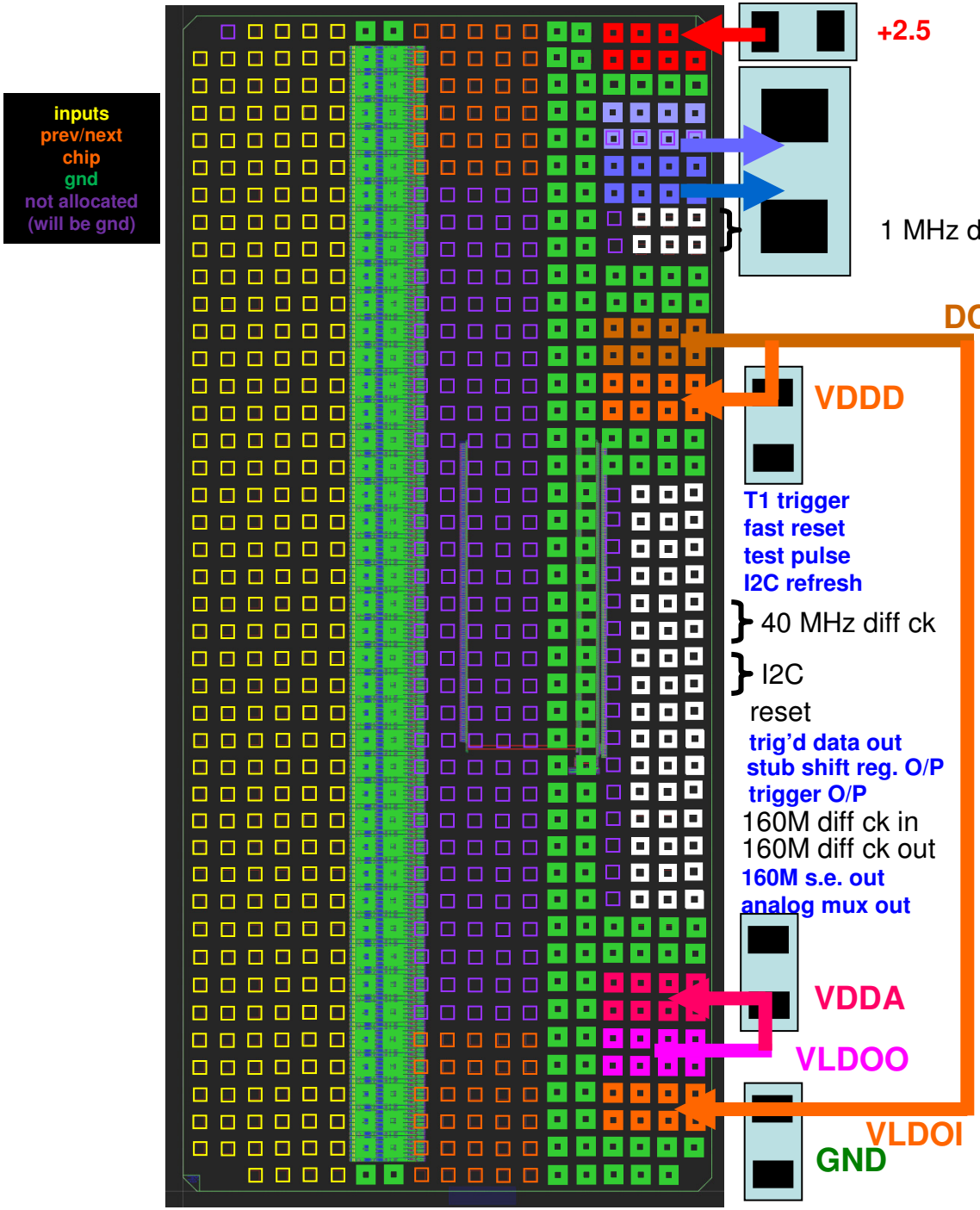
probe-able pads for wafer test

access to:
- power
- fast control
- I2C
- outputs

should be able to provide quite thorough test of chip functionality

NB: at least 2 columns of gnd pads must separate input pads and pads for digital inter-chip signals (orange)

Power distribution



NB: the last column of PADs to the right are wire-bondable, they will not be routed on hybrid (->possible to reach the 3 pads to their left)
Except for 160M diff pads all the other signals have 2 or more pads shorted together for reliability.

lines and arrows
show direction of power flow
(GND not shown)

note:

DC-DC 1.2 not connected
to VDDD or VLDOI on-chip

LDO output also connected to VDDA off-chip

(the idea is to maximise possible effectiveness of off-chip filtering)