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CBC2: a microstrip readout ASIC with coincidence logic for trigger primitives at HL-LHC

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ABSTRACT: We present the design of CBC2, the new version of the CMS Binary Chip ASIC for the readout of CMS Tracker Phase-two upgrade. CBC2, designed in 130nm CMOS, doubles the input channels to 254 and will be bump-bonded to the substrate. The ASIC is designed to instrument double layer modules in the outer tracker, consisting of two overlaid silicon sensors with aligned microstrips, and incorporates the logic to identify L1 trigger primitives in the form of “stubs”: high transverse-momentum candidates which are isolated from the low momentum background by selecting correlated hits between two closely separated microstrip sensors. The functionality of the coincidence logic, which includes rejection of wide clusters and offset correction to account for the position of the module in the R - ϕ plane, is described in detail.

KEYWORDS: Front-end electronics for detector readout; Trigger concepts and systems (hardware and software); VLSI circuits

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1 Phase-II upgrade of the CMS silicon tracker

The high-luminosity (HL) upgrade of the LHC will set stringent requirements for the CMS silicon tracker, such as higher granularity, new power distribution and trigger capabilities. To maintain the first level trigger (L1) average rate at 100 kHz, it is envisaged that the silicon tracker will contribute to the L1 trigger by providing basic tracking information in the form of high transverse momentum (Pt) track primitives called stubs. A promising way to identify stubs is the stacked module approach, by which high-Pt tracks are isolated from the low-Pt background by looking at the coincidence between hits on two closely separated sensors (figure 1a) [1, 2]. The current tracker analogue readout based on the 0.25 μm CMOS APV25 ASIC cannot be used to build stacked modules for the HL-LHC. The CBC (CMS Binary Chip) is a 128 channel binary unsparified prototype ASIC for the trigger readout of short silicon microstrips. The CBC was fabricated in the second half of 2010, and chips have been under test since February 2011. For a 5 pF input capacitance the ASIC achieves ≈ 800 e- RMS noise with a total power of less than 300 μW /channel. Design, performance and test results of CBC are reported in detail in [3–5]. CBC2 incorporates the logic to identify high-momentum stubs, doubles the number of input channels and introduces a bump-bonded layout and several other improvements.

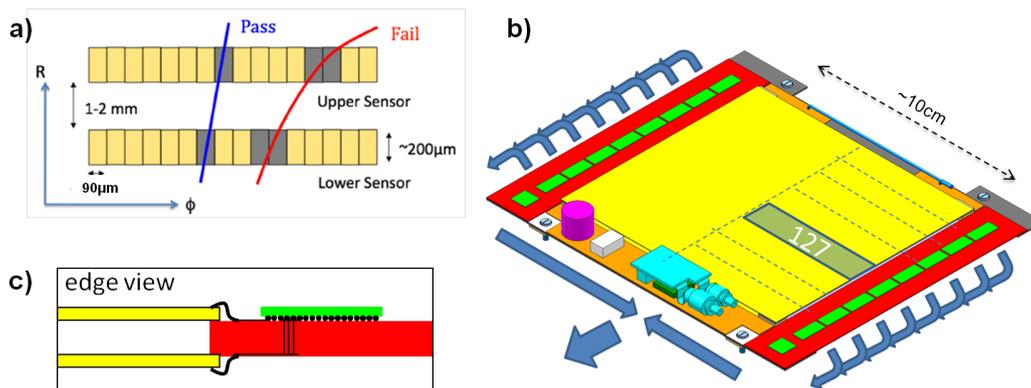


Figure 1. a) Pt selection concept. b) Stacked module for strip sensors and data transfer (ASICs in green). c) Edge view of sensor connections.

1.1 Module design

Several geometries have been considered for the new tracker, having six barrel layers with a radial range between 230 mm and 1080 mm [2]. The CBC2 is designed for the readout of silicon strips with a pitch of $90\ \mu\text{m}$ in the outer barrel ($R > 500\ \text{mm}$). Figure 1b shows one of the stacked modules currently being developed, designed to be lightweight and rely on commercial interconnection technologies [2, 6]. The optimal sensor separations vary in the range 1mm-4mm in the barrel and 1mm–5mm in the endcaps, depending on the Pt cuts required and the radius of the layer/disk. The strip sensors are wire-bonded to the substrate and read out by 16 readout ASICs. Two additional “Concentrator” ASICs (to be designed) at the base of the module collect the data from the readout chips for data formatting. A hybrid module consisting of one strip and one pixel detector is being considered for the inner tracker, where higher segmentation in η is necessary to maintain acceptable occupancy and resolution [7]. Another approach based on 3D vertical interconnections is described in [8], whilst a stub-finding readout scheme for ATLAS is presented in [9].

2 Design architecture

CBC2, designed in a 130 nm CMOS process, has 254 input channels, to correlate between 127 strips on top and bottom sensors, leaving one spare binary code for null-event encoding.

One of the new features introduced in this version is the adoption of bump-bonded C4 pads, so that routing and pitch adaptation of the input signals from the sensors can be made in an advanced hybrid technology. A conservative pitch of $250\ \mu\text{m}$ was chosen to ensure good production yield, and no active circuits were placed under the input pads to avoid possible noise injection (figure 2).

2.1 Overview

The CBC2 block diagram is shown in figure 3. Binary data from the front-end comparators are synchronized with the bunch crossing clock and then follow two parallel paths: one for trigger readout and the other for stub finding. In the former data are continuously written into a 256-deep FIFO pipeline RAM, for a maximum trigger latency of $6.4\ \mu\text{s}$. When a L1 trigger is received, the pipeline control logic transfers the relevant data to a 32-deep buffer memory, where it is stored

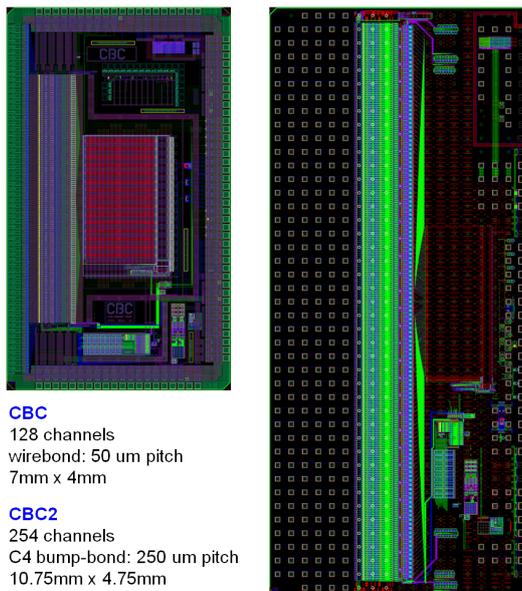


Figure 2. CBC and CBC2.

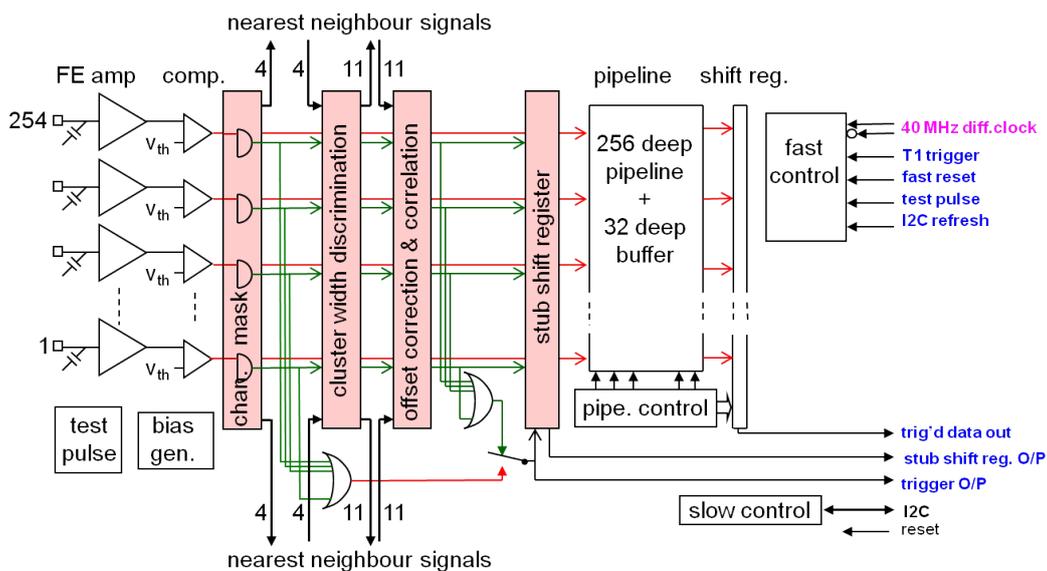


Figure 3. CBC2 block diagram.

before being serialized with its 8-bit column address (identifying the triggered pipeline time-slice) and read out, unsparsified, at 40 MHz. This additional memory buffer is needed to cope with the random nature of the trigger and the possibility of several triggers arriving within the same average trigger interval. In the other data path several blocks of combinatorial logic, described in section 2.3, identify stub candidates before writing them into a shift register for serial read out.

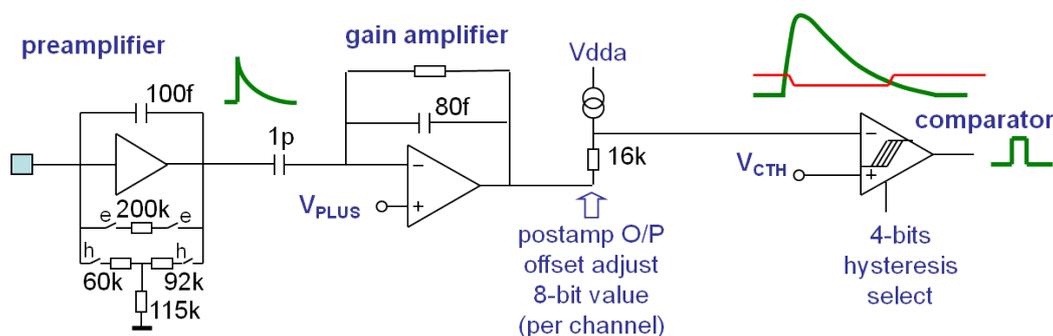


Figure 4. Front end channel.

2.2 Front-end circuitry

The front-end channel consists of preamplifier, gain amplifier and comparator (figure 4), and re-uses much of the circuits present on the previous version and described in detail in [3].

The charge preamplifier is designed to be DC coupled to sensors of either polarity up to ~ 10 pF, with leakage current up to $\sim 1 \mu\text{A}$ absorbed by a resistive feedback. It is AC coupled to a second amplifier which removes residual DC components due to the leakage current and provides the necessary gain for the following comparator. The output pulse shape has a peaking time of approximately 20 ns, and feeds the comparator via a resistor. An 8bit programmable current source in each channel produces a DC offset at the comparator input used to correct pedestal variation across the chip. CBC2 addresses a problem in the CBC gain amplifier feedback network, where a high-impedance node was found to be influenced by common mode movements of the comparator output. The solution was to buffer this node with a source-follower in every channel. The programmable hysteresis resistive network in the comparator was also replaced by an internal network to avoid common mode effects.

2.3 Stub-finding logic

The operation of the stub-finding logic is based on a simple procedure: the first stage rejects wide clusters of hits on both inner and outer sensors; subsequently for every valid cluster on the inner sensor the logic looks for a hit in a coincidence window on the outer sensor. If a hit is present within this window, the inner strip is considered a valid stub. In this version of the ASIC, the binary output of all the coincidence logic channels is ORed, and, when a stub is found, it is then latched into a shift register and read out at 40 MHz. The coincidence logic is structured into combinatorial blocks, which repeat every two adjacent channels (corresponding to one inner strip and the outer strips directly above it) and result in a uniform layout across the ASIC (figure 5). Noisy channels can be individually masked from the coincidence logic, without affecting the values written into the pipeline RAM.

2.3.1 Cluster-width discrimination (CWD)

The first stage of the combinatorial logic analyses adjacent strips from the same sensor to reject wide clusters of hits, which are typically associated with low-momentum tracks. A global 2 bit register sets the value of the maximum cluster width to one, two or three adjacent strips. Clusters

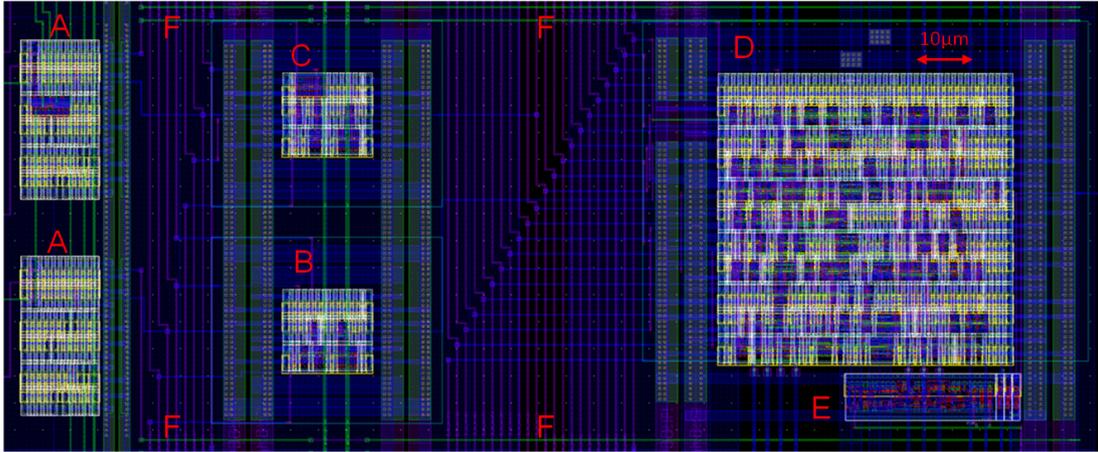


Figure 5. Stub-finding logic blocks: A: mask and channel outputs OR; B: cluster width discrimination for inner sensor channel; C: cluster width discrimination for outer sensor channel; D: offset correction and coincidence logic; E: flip-flop for stubs readout shift register; F: lines to/from previous/next channels.

wider than this value are suppressed. The same register allows for the CWD to be disabled and to pass every single hit to the subsequent stage. At the output of the CWD only the central strip of a cluster is active; in the case of a two-strip cluster, the centre is assigned to the strip with lower address. This choice was made to reduce the number of bits per stub to a minimum, to accommodate more stubs in the output bandwidth available. The readout scheme has since been revised and currently the plan is to adopt half-pitch segmentation in the next version of the ASIC, together with bend information for each stub.

2.3.2 Φ -shift correction and correlation logic

For every central strip of a valid cluster in the inner layer, the logic block following the CWD looks for valid clusters in a coincidence window in the outer layer. If there is any, then the output is true which indicates that the inner strip corresponds to a valid stub. The window in the outer layer channels is what defines the Pt-cut. For a given Pt, the displacement between the hits in the two sensors depends on the position of the module in the tracker, decreasing at larger radii in the case of the barrel. In order to obtain a uniform Pt cut in the tracker volume it is possible to adjust both the sensor spacing during assembly and the width of the coincidence window, which for a single chip is programmable in the range ± 8 strips (symmetrical around the central strip). Also depending on the position of the strip along the module in the r - ϕ plane, the coincidence window must be adjusted to account for the geometrical lateral displacement across the same module as illustrated in figure 6a. This offset is independently programmable in the range ± 3 strips in the two halves of the ASIC. Every module is therefore divided into 16 regions of programmable offset.

2.3.3 Stubs readout

When a stub is found, the output of the combinatorial logic for each channel is latched into a parallel-input serial-output shift register, which is then read out at 40 MHz. A future version of the ASIC will output the address of the stubs to four fast parallel outputs for low-latency input to

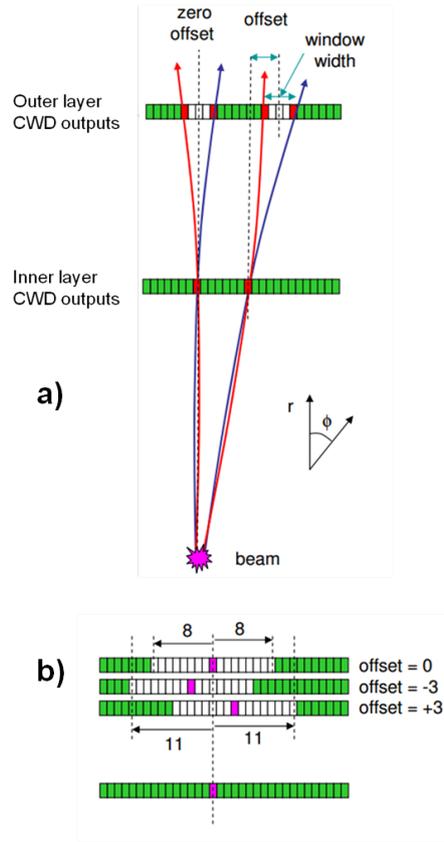


Figure 6. a) ϕ -shift offset; b) effect of offset on coincidence window.

the L1 trigger. The readout is controlled by the OR of all the correlations outputs, which is also transmitted off-chip as “signal ready”. As a test feature the OR of all the channels outputs can also be selected to control the stubs readout.

2.3.4 Inter-chip boundaries

As described above, both the cluster-width discrimination and the offset correction and correlation logic rely on inputs from neighbouring channels. In particular, the numbers of links required are:

- CWD inner sensor channels: ± 2 adjacent inner-channels;
- CWD outer sensor channels: ± 2 adjacent outer-channels;
- Offset correction: ± 3 adjacent coincidence logic channels;
- Coincidence logic: ± 8 adjacent coincidence logic channels.

In total every coincidence logic channel needs the inputs of the adjacent 30 channels. On both the top and the bottom sides of the ASIC there are therefore 15 input pads and 15 output pads assigned to inter-chip links. Modules are designed as independent units and there is no plan for a similar data transmission scheme between adjacent modules. The overlap of modules in η will ensure that high-Pt tracks straddling two adjacent modules are not lost, whereas the acceptance

loss due to stubs straddling the two halves of the same module in η should be limited if the sensor separations are kept sufficiently small. The use of interdigitated strips in the z direction is also being investigated to resolve this issue.

2.3.5 Logic power consumption

The power consumption of the stub finding logic depends on occupancy, maximum cluster width and coincidence window width; however simulations in pessimistic conditions (4% strip occupancy, maximum cluster and coincidence widths) indicate a value of less than $50 \mu\text{W}/\text{channel}$.

3 On-chip powering circuitry

As with its predecessor, CBC2 incorporates a switched capacitor DC-DC converter, provided by CERN, to power the digital circuits of the ASIC (1.2 V) from the 2.5 V supply present on the module. An on-chip low-dropout regulator (LDO) can be used to provide a clean 1.1 V supply for the front-end analog circuitry. The different power domains are connected off-chip to maximise the effectiveness of external filtering components. Improvements introduced in the powering of CBC2 include the adoption of enclosed-layout transistors in the DC-DC converter for enhanced radiation hardness, and on-chip filtering of the bandgap output to improve PSRR.

4 Conclusions and future developments

CBC2, the next version of the CMS Binary Chip for the silicon tracker microstrip readout, was submitted for production in August 2012. It represents a significant step forward towards the development of the final system by incorporating the functionality needed to perform stub selection and Pt-cut into a full-scale prototype that can be integrated on the module and tested under realistic conditions. The test plan includes single-die functional test at first, followed by bump-bonding to a two-die hybrid currently in development at CERN [7, 10]. This will be connected to stacked sensors to assess the performance of the stub finding logic under irradiation, and to evaluate efficiency, optimum separation between silicon sensors and effect of angle of incidence. It will also fully exercise the links between adjacent chips. Finally, an eight-die hybrid will be assembled to model one half of the module, and to study manufacturing yield. A further version of the ASIC is foreseen to include low-latency readout of stubs for input to the L1 trigger.

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References

- [1] M. Pesaresi and G. Hall, *Simulating the performance of a PT tracking trigger for CMS*, [2010 JINST 5 C08003](#).
- [2] S. Mersi, D. Abbaneo, N.D. Maio and G. Hall, *CMS tracker layout studies for HL-LHC*, in the proceedings of the *Technology and Instrumentation in Particle Physics 2011 (TIPP2011)*, June 9–14, Chicago, U.S.A. (2011), [CMS-CR-2011-362](#).
- [3] M. Raymond et al., *The CMS binary chip for microstrip tracker readout at the SLHC*, [2012 JINST 7 C01033](#).
- [4] W. Ferguson et al., *The CBC microstrip readout chip for CMS at the High Luminosity LHC*, [2012 JINST 7 C08006](#).
- [5] D.G. Cussans, J.A. Jacob and D.M. Newbold, *Tests with the CMS Binary Chip (CBC)*, [2012 JINST 7 C03016](#).
- [6] D. Abbaneo, *Upgrade of the CMS tracker with tracking trigger*, [2011 JINST 6 C12065](#).
- [7] D. Abbaneo and A. Marchioro, *A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC*, [2012 JINST 7 C09001](#).
- [8] J. Hoff, M. Johnson, R. Lipton and G. Magazzu, *Readout chip for an L1 tracking trigger using asynchronous logic*, [2012 JINST 7 C08004](#).
- [9] N. Dressanandt, A. Halgeri, M. Kamat, V. Koppal and M. Newcomer, *Prompt trigger primitives for a self-seeded track trigger*, [2012 JINST 7 C10001](#).
- [10] G. Blanchot, *Hybrid circuits and substrate technologies for the CMS tracker upgrade*, talk given at the *Workshop on Intelligent Trackers (WIT2012)*, May 3–5, Pisa, Italy (2012).