Front End Readout Electronics – for strips

OUTLINE

UK programme incorporates development of 130 nm readout chip for short strips

early thoughts were to develop digital APV type chip

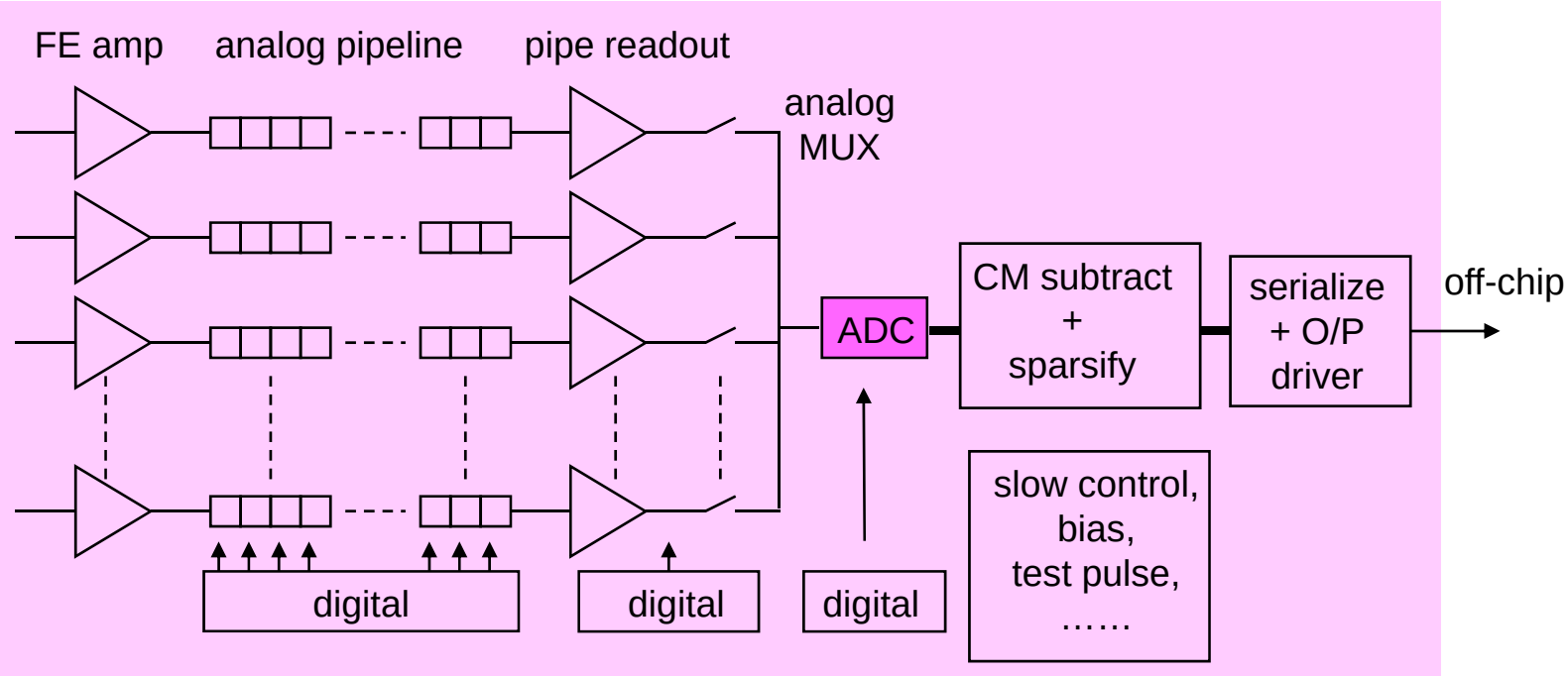
have decided to go for a binary un-sparsified architecture

will go through arguments briefly again here

have also decided to go for full-size chip on first iteration

will explain reasoning and present preliminary specifications

digital APV architecture



assumption has been that ADC on every channel (before pipeline) needs too much power

still valid? maybe not in future processes (90, 65 nm)

some new ADC architectures are beating previous power predictions *

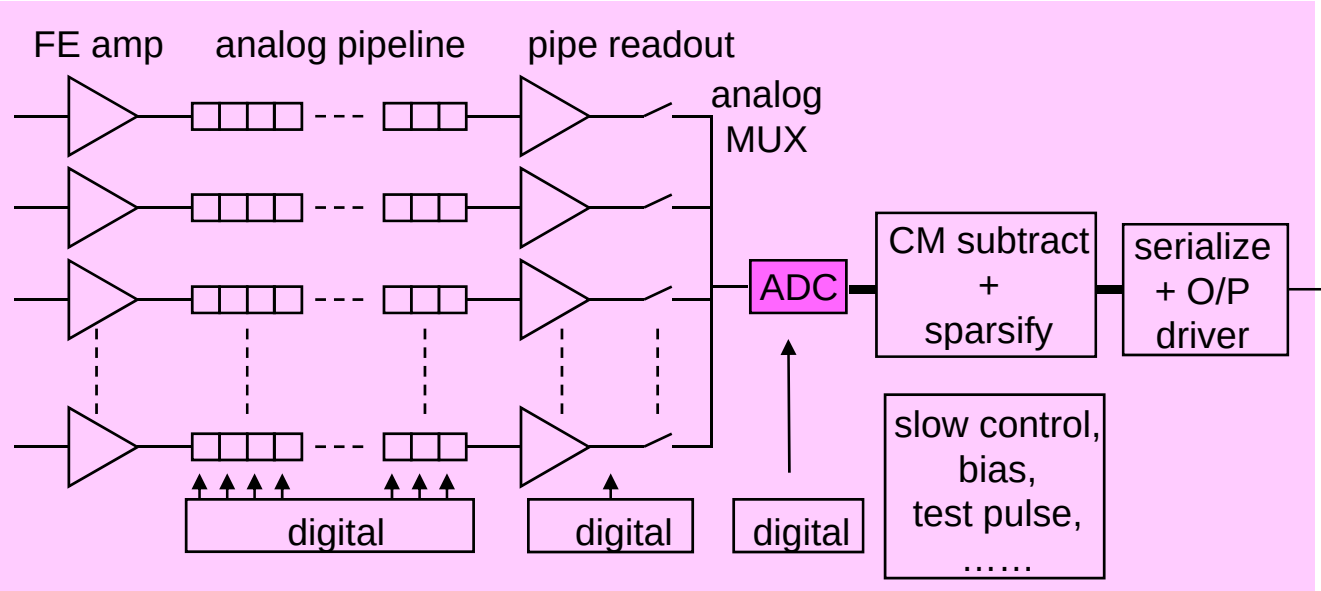
but negligible power / channel still seems long way off

negligible power/channel **is** achievable if relatively high power ADC shared between all front end channels

but this architecture still brings some disadvantages

*see - *A. Marchioro - http://indico.cern.ch/getFile.py/access?contribId=26&resId=0&materialId=slides&confId=41832*

digital APV architecture disadvantages



very complicated chip – all the complexity of APV + more
- fast ADC required
- sparsification necessary to keep data at manageable levels
- on-chip CM subtraction probably necessary (analogue pipeline contributes)

off-detector FED features in existing system

analogue pipeline using gate capacitance may still be possible in 130nm –not in finer processes

analogue circuitry throughout chip – harder to achieve supply noise rejection

sparsification leads to on-detector system complexity
- extra de-randomising buffering required (another chip) to cope with varying trigger-to-trigger data volume
- front-end timestamping
- loss of external emulation capability (like in present simple synchronous system)

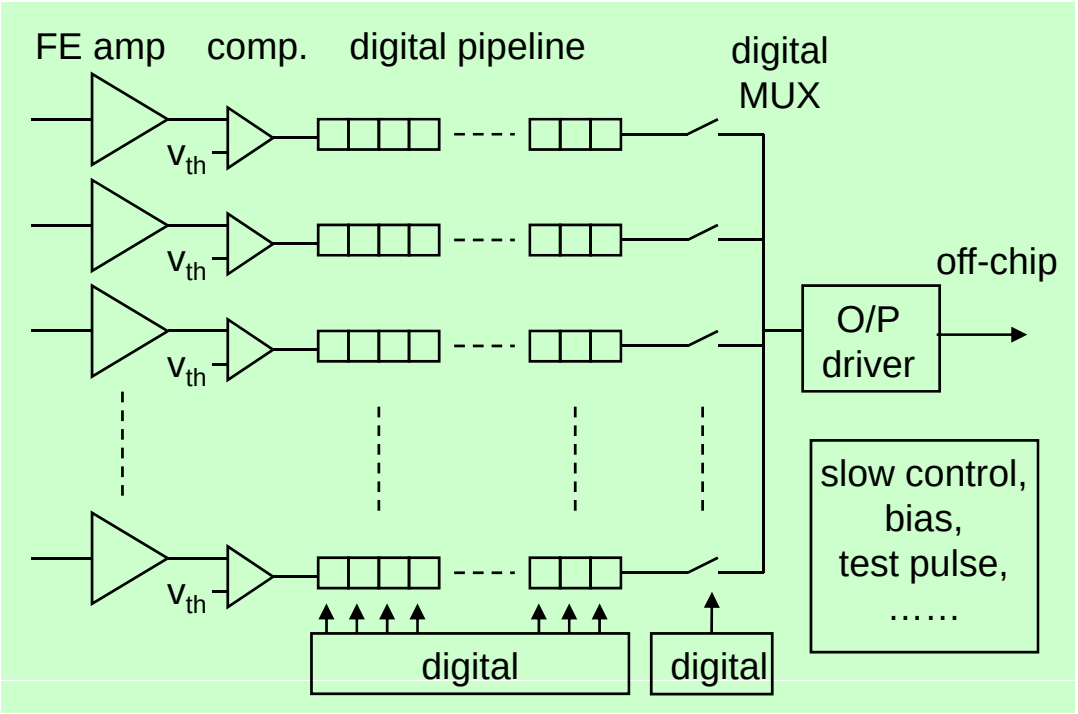
binary architecture – un-sparsified

much simpler (than digital APV)
particularly for pipeline and readout side

need fast front end and comparator
=> more power here

but no ADC power and much simpler digital functionality will consume less – this architecture **will** be lowest power

binary architecture also compatible with "two-in-one" & cluster-width discrimination approach to track triggering layers



can retain system features we like

simpler synchronous system
no FE timestamping
data volume known, occupancy independent (no trigger-to-trigger variation)

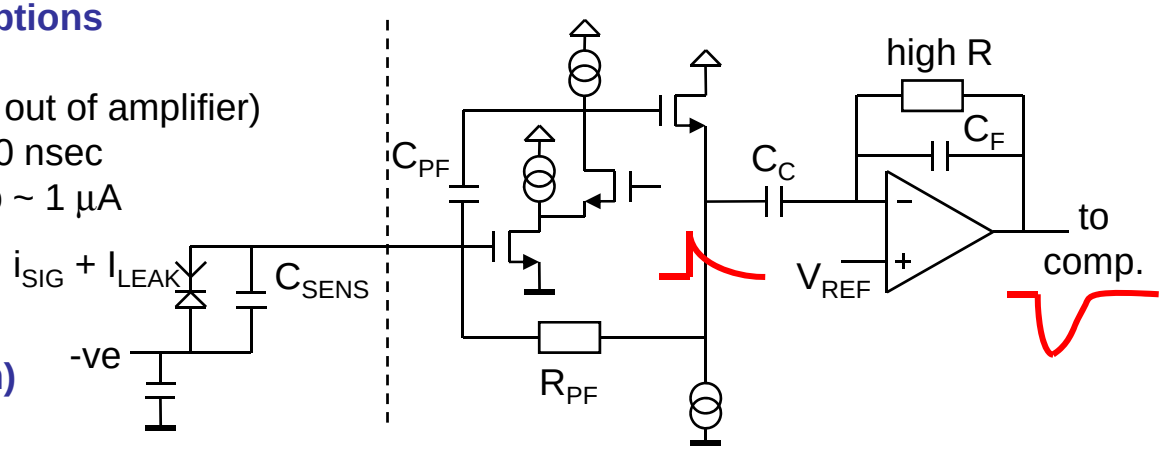
un-sparsified binary is the option we are currently planning to implement this year

but less diagnostics (can measure front end pulse shape on every channel in present system)
loss of position resolution
common mode immunity

binary front end amplifier

preliminary specifications and assumptions

n-on-p sensor (signal current flows out of amplifier)
needs to be fast, peaking time ~ 20 nsec
needs to sink leakage current up to ~ 1 μA



current preferred architecture (130 nm)

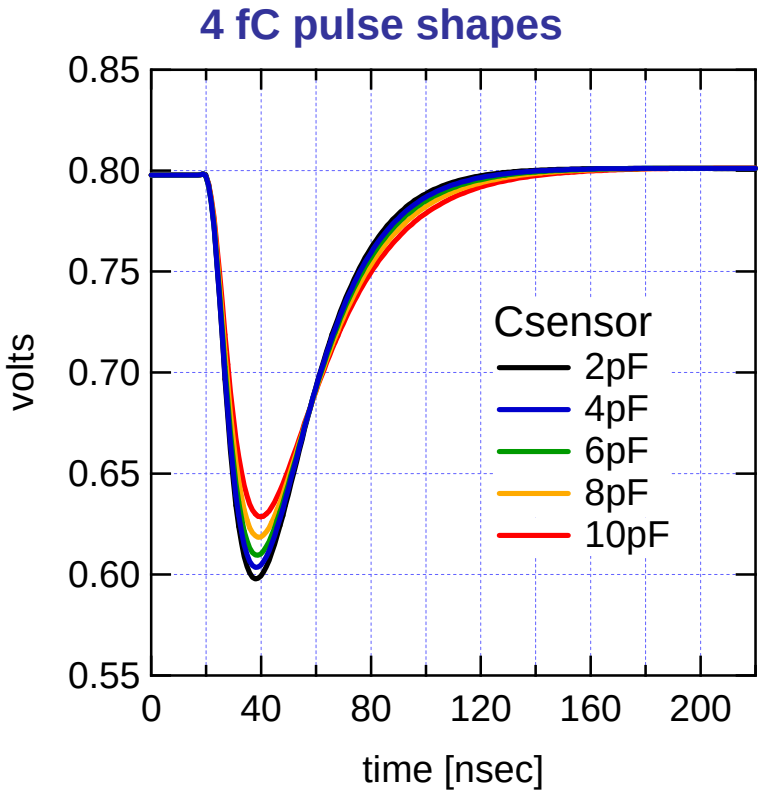
NMOS I/P device
- 1/f corner low enough (simulation) – apparently no noise penalty
- better connection to sensor for PSR (sensor bias decoupling and I/P FET source both at GND)

preamp feedback uses real resistor (not FET)
- low Rpf (200k) allows DC leakage to be accommodated (1 μA -> 200 mV)
- uses highest resistance technology in process (1k7/square poly, +/-20%)
- Rpf.Cpf = 200k.100fF = 20 ns decay time constant of preamp (no pile-up)
- 200k contributes ~ 220e (for this shaping)

postamp provides gain
- risetime provides integrating time constant
- AC coupled to preamp (DC shift due to leakage decoupled)
- O/P DC level set by Vref – defines DC level at following comparator input

will show some simulated performance pictures – all results at preliminary stage

binary FE pulse shape



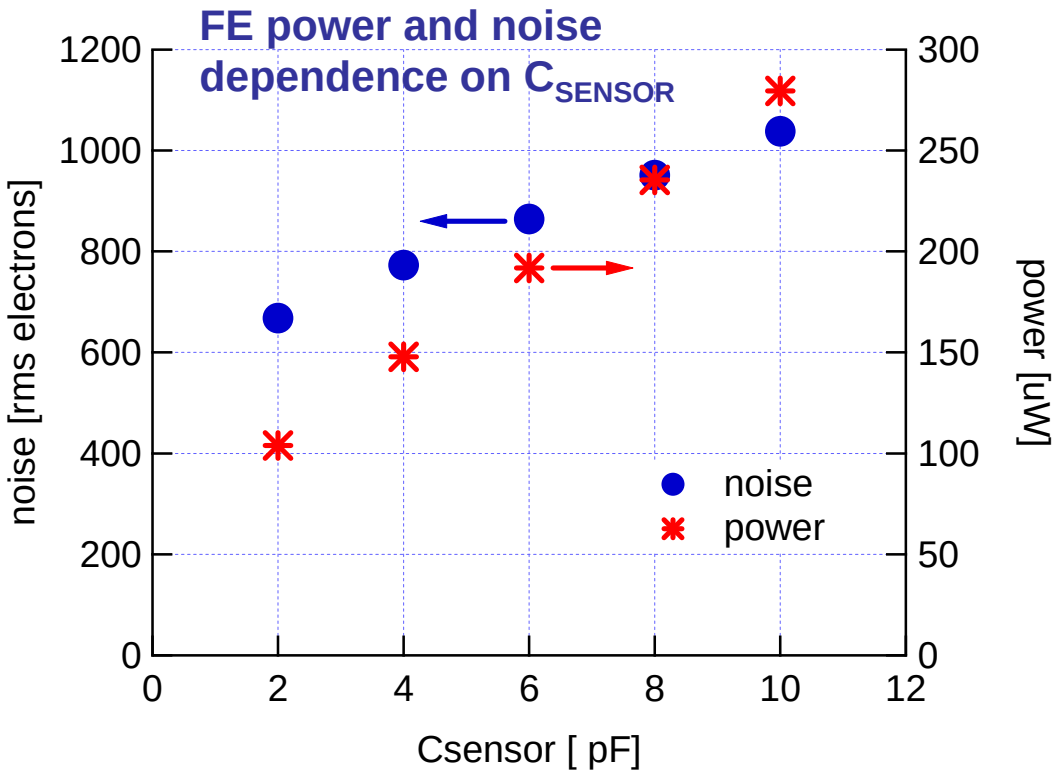
trade-off between power and noise
thin sensors, long strips will need more power to get less noise

pulse shape tuned to keep risetime ~ constant as C_{SENSOR} varies by increasing current in input FET

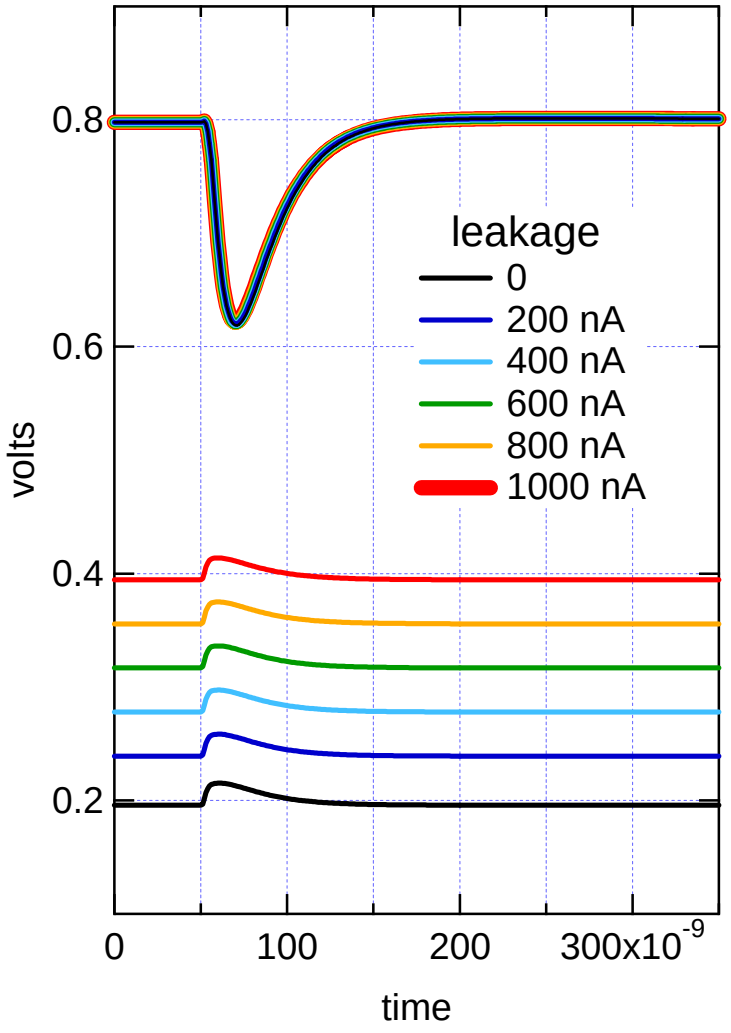
~ 170 – 200 mV pulse height for 4 fC (25,000 e)

=> power scales linearly with C_{SENSOR}

simulations show noise < ~1000e for power ~ 200 μW for C_{SENSOR} ~ 6 pF



Effects of leakage current

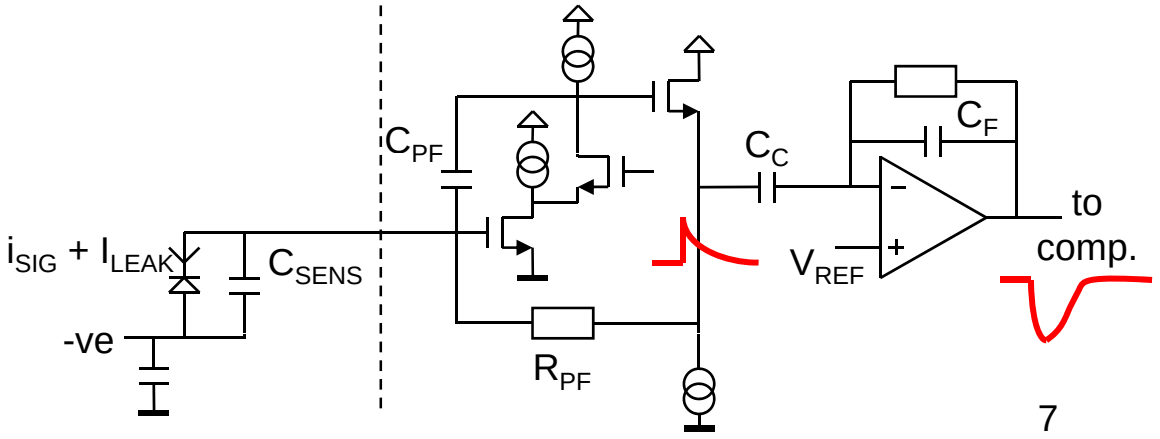


postamp output unaffected

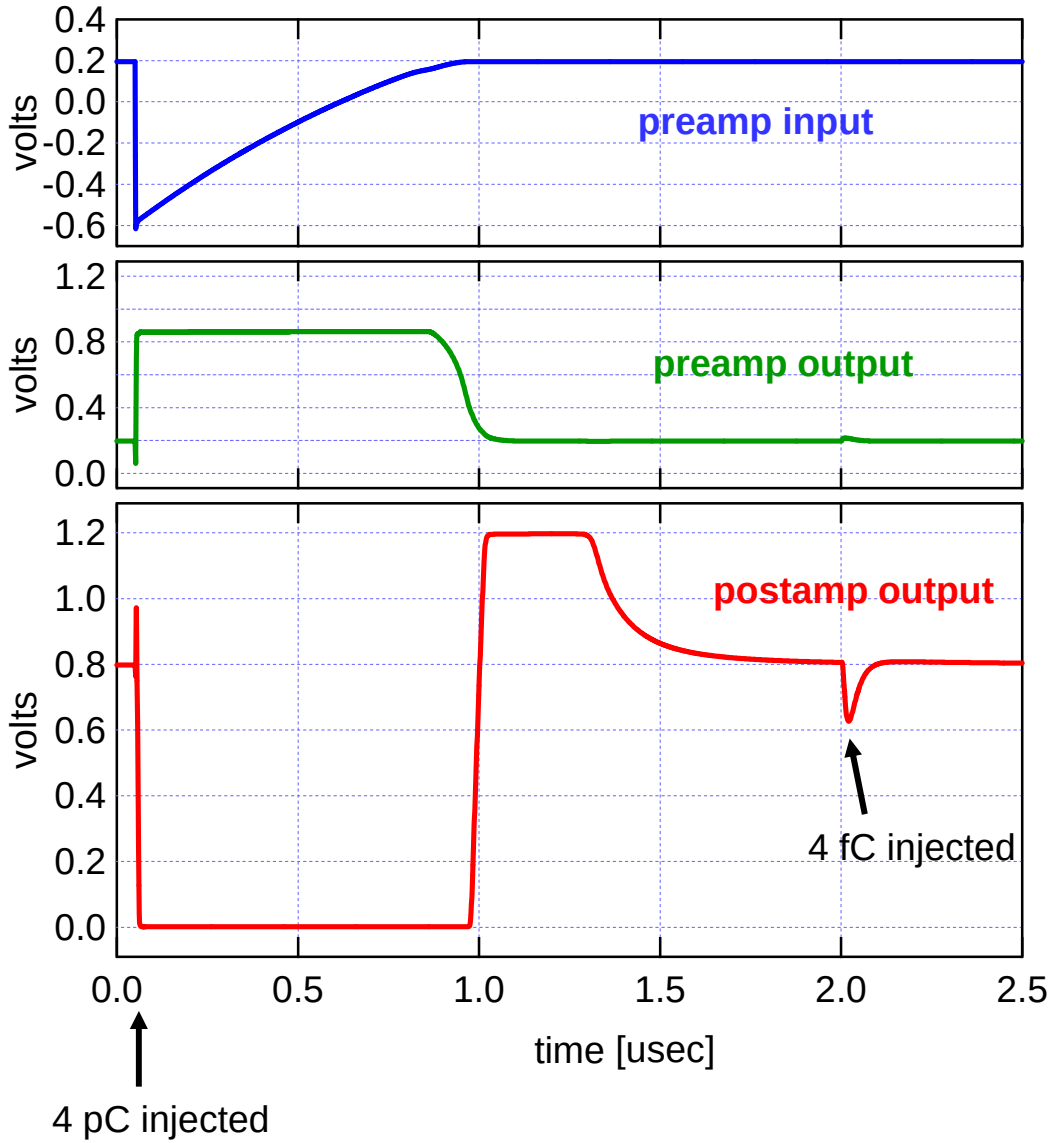
preamp output shows DC shift across R_{PF}

1 μA leakage contributes ~ 440e noise to be added in quadrature to amplifier noise
(short shaping time helps with parallel noise)

e.g. 900 (total amplifier for C_{SENSOR} ~ 6 pF)
+ 440 (leakage)
= ~1000e total



response to overload



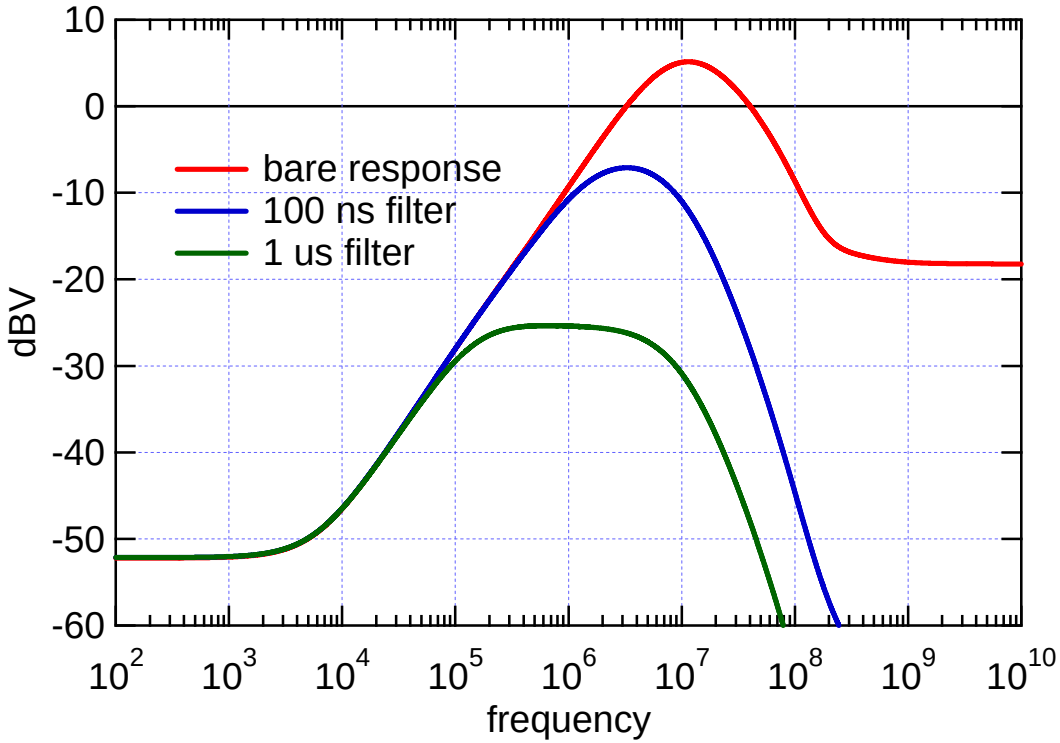
overload behaviour well-controlled

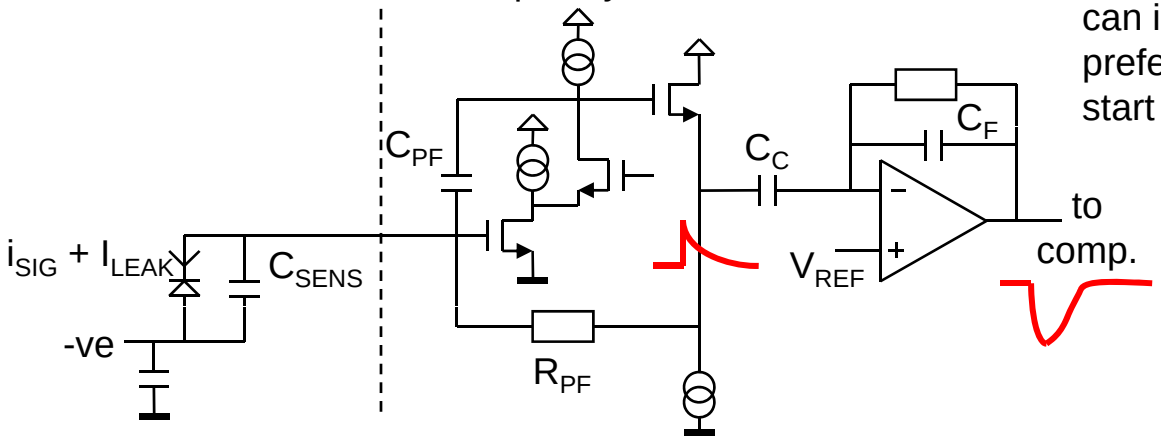
low R_{PF} beneficial

front end recovers from 4 pC signal and sensitive to normal signals within 2.5 μs

=> no “APV-like” hips effect

power supply rejection





power supply rejection at postamp output to swept frequency sinusoidal waveform on positive supply rail

0 dBV = unity gain
-20 dBV = factor 10 rejection

bare response shows good rejection at low frequency, peaking at ~10 MHz

AC preamp/postamp coupling together with opamp postamp gives good low f behaviour

peaking at ~10 MHz (gain) due to coupling through bias circuits

can improve with realistic filtering, but would prefer some rejection at all frequencies to start with

needs further study

effect of preamp feedback resistor tolerance

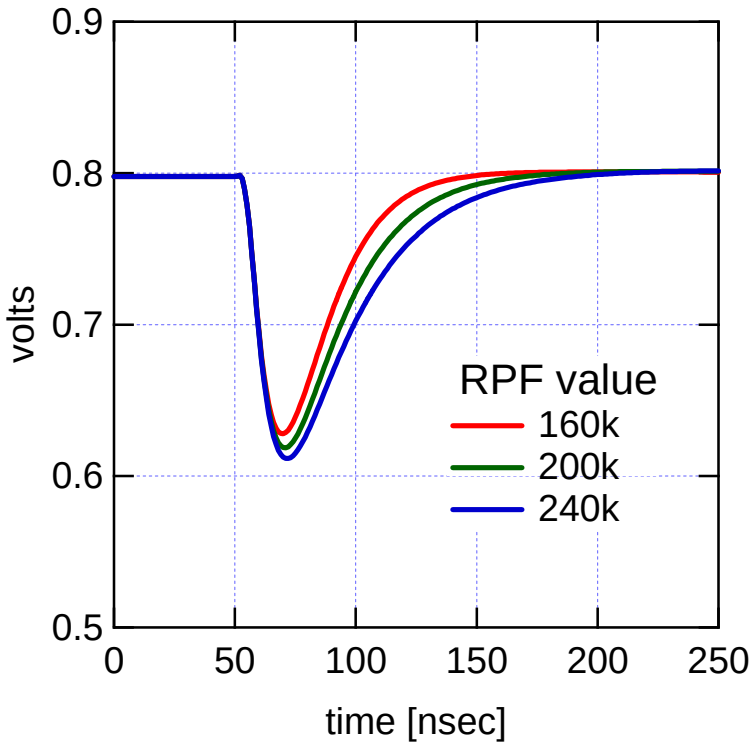
using process resistor with +/- 20% tolerance (+/- 3 σ) for R_{PF} gives some pulse shape variation

=> noise will be affected

e.g. for C_{SENSOR} = 5 pF get:

160k	911e
200k	880e
240k	857e

~ +/- 3% noise variation



power estimate

previously presented estimate for 130nm binary chip – non-sparsified readout

	power/chan. [μW]	
preamp/shaper	180	20 ns, C_{SENSOR} ~5pF
comparator	20	simulations
digital	60	guess – loosely based on APV
fast serial output	230	guess for LVDS readout
	490	

still valid?

230 μW probably excessive for readout power

low voltage differential current output should take less

still think 0.5 mW / channel is a good target, hopefully conservative and safe number to use for overall short strip chip power estimates

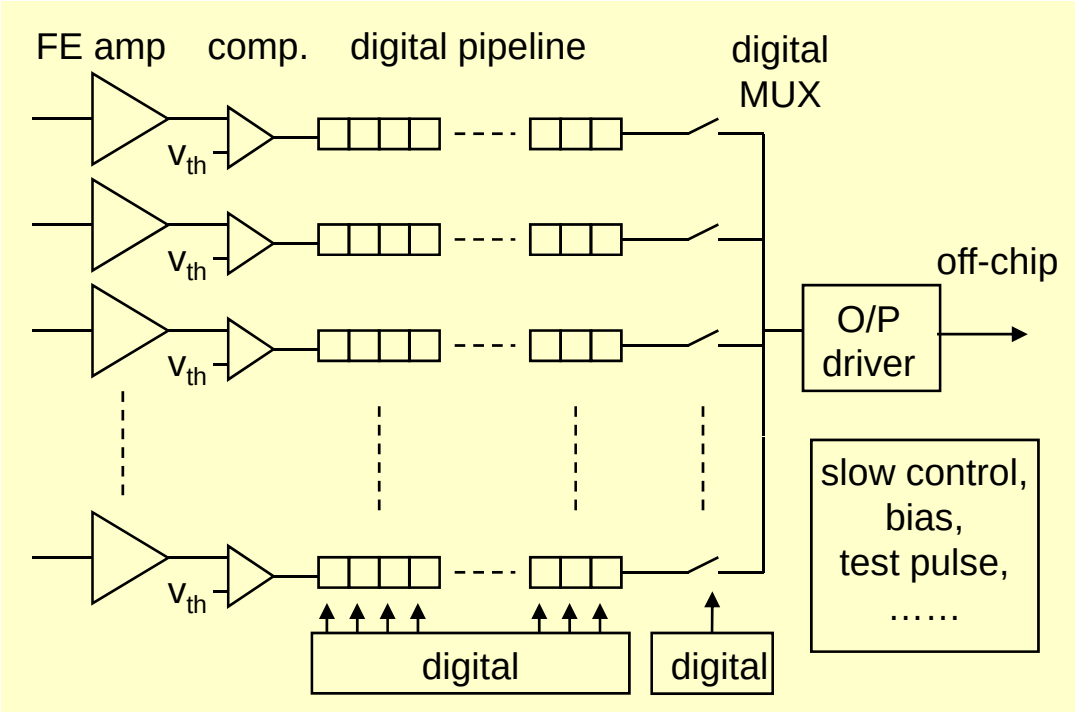
full prototype in 1st iteration

relative simplicity of binary option means could go for complete chip on timescale ~ 1year

could learn a lot sooner rather than later - would also provide collaborators with something to use
though chip numbers will be limited

choose front end most likely to suit SLHC (e.g. n-side readout)
(can still submit test structures for alternative front ends)

CBC (CMS Binary Chip)



could leave out some features
e.g. bias gen., test pulse, I^2C I/F

but should have main functionality:

pipeline, pipe control logic, and mux.
trimDAC for comparator thresholds
differential O/P

output would be APV-like (i.e. header with pipeline address) but digital (just hits)

20 Mbps => could combine 4 CBCs onto one 80 Mbps GBT lane (simple mux)
=> 128 CBCs / GBT link

binary chip specifications (preliminary)

parameter	target spec.	justification/comment
noise	<1000 e for C < ~5 pF	does not include leakage current contribution
timewalk	copy Atlas ABCD spec.?	
supply rejection	>20 dB at any frequency?	factor 10 – maybe implemented externally (passive RC)
overload recovery	hip signals up to 4 pC	sensitive to normal signals < 2.5 usec.
power	0.5 mW / ch. for C< ~5pF	
leakage current (DC sensor)	up to 1uA	should fail gracefully for higher current
signal polarity	-ve	conventional signal (&leakage) current flows out of amp.
bond pads	wire	cheap, easy to prototype, but labour intensive assembly
power supplies	1.2 V analogue, digital supplied separately	digital could be run at lower VDD to save power
pipeline	256	up to 6.4 usec
buffering (FIFO)	up to 32	triggered pipeline timeslices awaiting readout
+ …		
+ …		

summary

UK programme incorporates development of 130 nm readout chip for short strips

current plans are:

- binary un-sparsified architecture
- full-size chip on first iteration

front end amplifier architectures already under design

remainder of chip (digital) will begin soon

- some specifications clear – others will develop over coming months – input invited

hope to submit this year (Autumn) - chips available ~ end of year

binary architecture already compatible with some of the track-trigger approaches under consideration

relative simplicity (simpler chip, simpler system) should also allow to free-up resources to help with track-trigger solution (“two-in-one”, cluster-width, or stacked)